TPL9201
8-CHANNEL RELAY DRIVER WITH INTEGRATED 5-V LDO AND ZERO-VOLT DETECTION

SLIS123D–JUNE 2006–REVISED FEBRUARY 2008

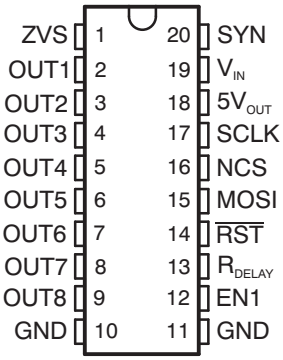
FEATURES

- **Eight Low-Side Drivers With Internal Clamp for Inductive Loads and Current Limiting for Self Protection**
  - **Seven Outputs Rated at 150 mA and Controlled Through Serial Interface**
  - **One Output Rated at 150 mA and Controlled Through Serial Interface and Dedicated Enable Pin**
- **5-V ± 5% Regulated Power Supply With 200-mA Load Capability at V_{IN} Max of 18 V**
- **Internal Voltage Supervisory for Regulated Output**
- **Serial Communications for Control of Eight Low-Side Drivers**
- **Enable/Disable Input for OUT1**
- **5-V or 3.3-V I/O Tolerant for Interface to Microcontroller**
- **Programmable Power-On Reset Delay Before $\overline{RST}$ Asserted High, Once 5 V Is Within Specified Range (6 ms Typ)**
- **Programmable Deglitch Timer Before $\overline{RST}$ Asserted Low (40 μs Typ)**
- **Zero-Voltage Detection Signal**
- **Thermal Shutdown for Self Protection**

APPLICATIONS

- **Electrical Appliances**
  - **Air Conditioning Units**
  - **Ranges**
  - **Dishwashers**
  - **Refrigerators**
  - **Microwaves**
  - **Washing Machines**
- **General-Purpose Interface Circuits, Allowing Microcontroller Interface to Relays, Electric Motors, LEDs, and Buzzers**

N OR PWP PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The power supply provides regulated 5-V output to power the system microcontroller and drive eight low-side switches. The ac zero-detect circuitry is monitoring the crossover voltage of the mains ac supply. The resultant signal is a low-frequency clock output on the ZVS terminal, based on the ac-line cycle. This information allows the microcontroller to reduce in-rush current by powering loads on the ac-line peak voltage.

A serial communications interface controls the eight low-side outputs; each output has an internal snubber circuit to absorb the energy in the inductor at turn OFF. Alternatively, the system can use a fly-back diode to V_{IN} to help recirculate the energy in an inductive load at turn OFF.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	PDIP – N	Tube of 20	TPL9201N	TPL9201N
	PowerPAD™ – PWP	Reel of 2000	TPL9201PWPR	PL201
		Tube of 70	TPL9201PWP	

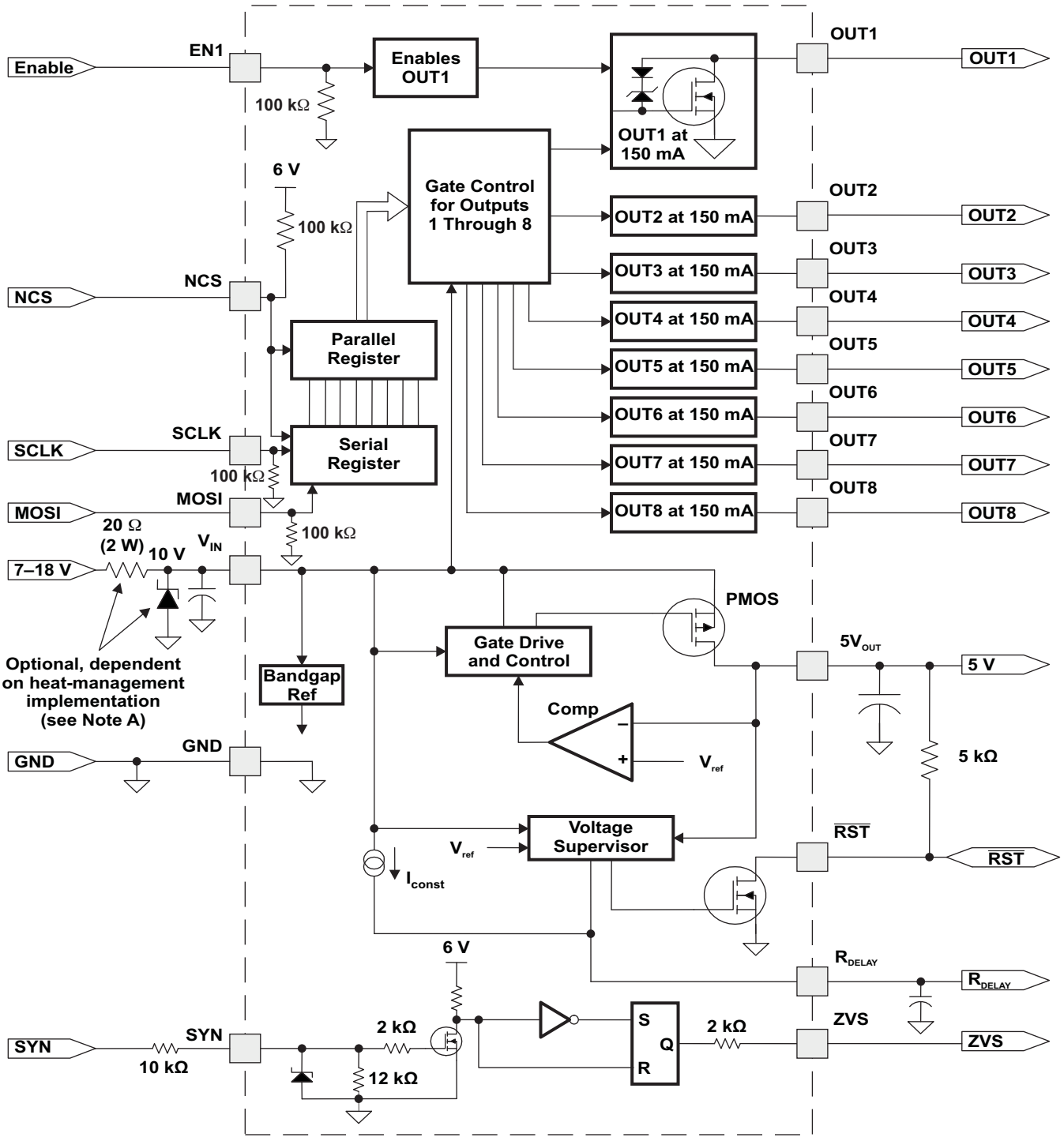
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PINOUT CONFIGURATION

NO.	NAME	I/O	DESCRIPTION
1	ZVS	O	Zero-voltage synchronization
2	OUT1	O	Low-side output 1
3	OUT2	O	Low-side output 2
4	OUT3	O	Low-side output 3
5	OUT4	O	Low-side output 4
6	OUT5	O	Low-side output 5
7	OUT6	O	Low-side output 6
8	OUT7	O	Low-side output 7
9	OUT8	O	Low-side output 8
10(1)	GND	I	Ground
11(1)	GND	I	Ground
12	EN1	I	Enable/disable for OUT1
13	R_{DELAY}	O	Power-up reset delay
14(2)	$\overline{RST}$	I/O	Power-on reset output (open drain, active low)
15	MOSI	I	Serial data input
16	NCS	I	Chip select
17	SCLK	I	Serial clock for data synchronization
18	$5V_{OUT}$	O	Regulated output
19	V_{IN}	I	Unregulated input voltage source
20	SYN	I	AC zero detect input

(1) Terminals 10 and 11 are fused internally in the lead frame for the 20-pin PDIP package.
(2) Terminal 14 can be used as an input or an output.

FUNCTIONAL BLOCK DIAGRAM



A. The resistor and Zener diode are required if there is insufficient thermal-management allocation.

DETAILED DESCRIPTION

The 5-V regulator is powered from V_{IN}, and the regulated output is within 5 V ± 5% over the operating conditions. The open-drain power-on reset ($\overline{RST}$) pin remains low until the regulator exceeds the set threshold, and the timer value set by the capacitor on the reset delay (R_{DELAY}) pin expires. If both of these conditions are satisfied, $\overline{RST}$ is asserted high. This signifies to the microcontroller that serial communications can be initiated to the TPL9201.

The serial communications is an 8-bit format, with data transfer synchronized using a serial clock from the microcontroller. A single register controls all the outputs (one bit per output). The default value is zero (OFF). If an output requires pulse width modulation (PWM) function, the register must be updated at a rate faster than the desired PWM frequency. OUT1 can be controlled by serial input from the microcontroller or with the dedicated enable (EN1) pin. If EN1 is pulled low or left open, the serial input through the shift register controls OUT1. If EN1 is pulled high, OUT1 always is turned on, and the serial input for OUT1 is ignored.

The SYN input translates the image of the mains voltage through the secondary of the transformer. The SYN input has a resistor to protect from high currents into the IC. The zero-voltage synchronization output translates the ac-line cycle frequency into a low-frequency clock, which can be used for a timing reference and to help power loads on the ac-line peak voltage (to reduce in-rush currents).

If $\overline{RST}$ is asserted, all outputs are turned OFF internally, and the input register is reset to all zeroes. The microcontroller must write to the register to turn the outputs ON again.

Absolute Maximum Ratings(1)

			MIN	MAX	UNIT
$V_{I(unreg)}$	Unregulated input voltage(2) (3)	V_{IN}		24	V
		SYN		24	
$V_{I(logic)}$	Logic input voltage(2) (3)	EN1, MOSI, SCLK, and NCS		7	V
		$\overline{RST}$ and R_{DELAY}		7	
V_O	Low-side output voltage	OUT1–OUT8		16.5	V
I_{LIMIT}	Output current limit(4)	OUTn = ON and shorted to V_{IN} with low impedance		350	mA
θ_{JA}	Thermal impedance, junction to ambient(5)	N package		69	°C/W
		PWP package		33	
θ_{JC}	Thermal impedance, junction to case(5)	N package		54	°C/W
		PWP package		20	
θ_{JP}	Thermal impedance, junction to thermal pad(5)	PWP package		1.4	°C/W
P_D	Continuous power dissipation(6)	N package		1.8	W
		PWP package		3.7	
ESD	Electrostatic discharge(7)			2	kV
T_A	Operating ambient temperature range		–40	125	°C
T_{stg}	Storage temperature range		–65	125	°C
T_{lead}	Lead temperature	Soldering, 10 s		260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Absolute negative voltage on these pins must not go below –0.5 V.
(4) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed 1 ms.
(5) The thermal data is based on using 1-oz copper trace with JEDEC 51-5 test board for PWP and JEDEC 51-7 test board for N.
(6) The data is based on ambient temperature of 25°C max.
(7) The Human-Body Model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

Dissipation Ratings

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 125°C$ POWER RATING
N	1812 mW	14.5 mW/°C	362 mW
PWP	3787 mW	30.3 mW/°C	757 mW

Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{I(unreg)}$	Unregulated input voltage	V_{IN}	7	18	V
		SYN	0	18	
$V_{I(logic)}$	Logic input voltage	EN1, MOSI, SCLK, NCS, $\overline{RST}$, and R_{DELAY}	0	5.25	V
T_A	Operating ambient temperature		–40	125	°C

Electrical Characteristics

T_A = –40°C to 125°C, V_{IN} = 7 V to 18 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
Supply Voltage and Current						
V_{IN}(2)	Input voltage		7		18	V
I_{VIN}	Input supply current	Enable = ON, OUT1–OUT8 = Off			3	mA
		Enable = ON, OUT1–OUT8 = On			5	
Logic Inputs (MOSI, NCS, SCLK, and EN1)						
V_{IL}	Logic input low level	I_{IL} = 100 µA			0.8	V
V_{IH}	Logic input high level	I_{IL} = 100 µA	2.4			
Reset ($\overline{RST}$)						
V_{OL}	Low-level logic output	I_{OL} = 1.6 mA			0.4	V
V_{OH}(3)	High-level logic output	5-kΩ pullup to V_{CC}	V_{CC} – 0.8			V
V_H	Disabling reset threshold	5-V regulator ramps up		4.25	4.5	V
V_L	Enabling reset threshold	5-V regulator ramps down	3.3	3.75		V
V_{HYS}	Threshold hysteresis		0.12	0.5		V
Reset Delay (R_{DELAY})						
I_{OUT}	Output current		18	28	48	µA
T_{DW}	Reset delay timer	C = 47 nF	3	6		ms
T_{UP}	Reset capacitor to low level	C = 47 nF		45		µs
Output (OUT1–OUT8)						
V_{OL}	Output ON	I_{OUTn} = 150 mA		0.4	0.7	V
I_{OH}	Output leakage	V_{OH} = Max of 16.5 V			2	µA
Regulator Output ($5V_{OUT}$)						
$5V_{OUT}$	Output supply	I_{5VOUT} = 5 mA to 200 mA, V_{IN} = 7 V to 18 V, C_{5VOUT} = 1 µF	4.75	5	5.25	V
I_{5VOUT} limit	Output short-circuit current	$5V_{OUT}$ = 0 V	200			mA
Thermal Shutdown						
T_{SD}	Thermal shutdown			150		°C
T_{HYS}	Hysteresis			20		°C
Zero Voltage Synchronization (ZVS)						
V_{SYNTH}	Transition threshold		0.4	0.75	1.1	V
I_{SYN}	Input activating current	R_{ZV} = 10 kΩ, V_{SYN} = 24 V			2	mA
t_D	Transition time	Rising and falling	10			µs

(1) All typical values are at T_A = 25°C.
(2) There are external high-frequency noise-suppression capacitors and filter capacitors on V_{IN}.
(3) V_{CC} is the pullup resistor voltage.

Output Control Register

MSB **LSB**

IN8	IN7	IN6	IN5	IN4	IN3	IN2	IN1
0	0	0	0	0	0	0	0

INn = 0: Output OFF
INn = 1: Output ON

To operate the output in PWM mode, the output control register must be updated at a rate twice the desired PWM frequency of the output. Maximum PWM frequency is 5 kHz. The register is updated every 100 μs.

ENABLE TRUTH TABLE

EN1	SERIAL INPUT FOR OUT1	OUT1
Open	H	On
Open	L	Off
L	H	On
L	L	Off
H	H	On
H	L	On

Serial Communications Interface

The serial communications is an 8-bit format, with data transfer synchronized using a serial clock from the microcontroller (see Figure 1). A single register controls all the outputs. The signal gives the instruction to control the output of TPL9201.

The NCS signal enables the SCLK and MOSI data when it is low. After NCS is set low for T_1, synchronization clock and data begin to transmit and, after the 8-bit data has been transmitted, NCS is set high again to disable SCLK and MOSI and transfer the serial data to the control register. SCLK must be held low when NCS is in the high state.

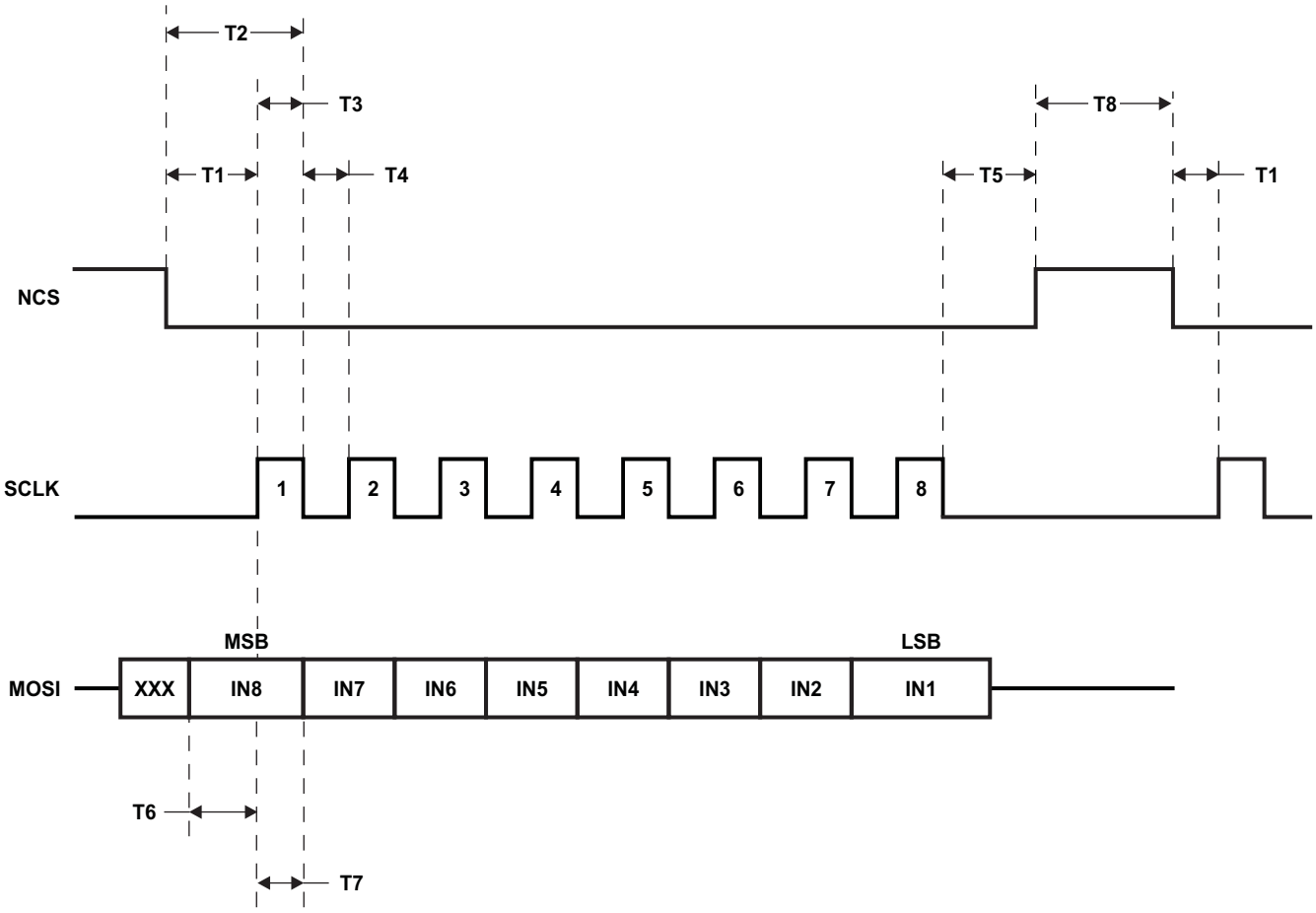


Figure 1. Serial Communications

Timing Requirements

T_A = –40°C to 125°C, V_{IN} = 7 V to 18 V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
f_{SPI}	SPI frequency		4		MHz
T1	Delay time, NCS falling edge to SCLK rising edge	10			ns
T2	Delay time, NCS falling edge to SCLK falling edge	80			ns
T3	Pulse duration, SCLK high	60			ns
T4	Pulse duration, SCLK low	60			ns
T5	Delay time, last SCLK falling edge to NCS rising edge	80			ns
T6	Setup time, MOSI valid before SCLK edge	10			ns
T7	Hold time, MOSI valid after SCLK edge	10			ns
T8	Time between two words for transmitting	170			ns

Reset Delay (R_{DELAY})

The R_{DELAY} output provides a constant current source to charge an external capacitor to approximately 6.5 V. The external capacitor is selected to provide a delay time, based on the current equation for a capacitor, $I = C(\Delta v/\Delta t)$ and a 28-μA typical output current.

Therefore, the user should select a 47-nF capacitor to provide a 6-ms delay at 3.55 V.

$I = C(\Delta v/\Delta t)$

$28\ \mu A = C \times (3.55\ V/6\ ms)$

$C = 47\ nF$

APPLICATION INFORMATION

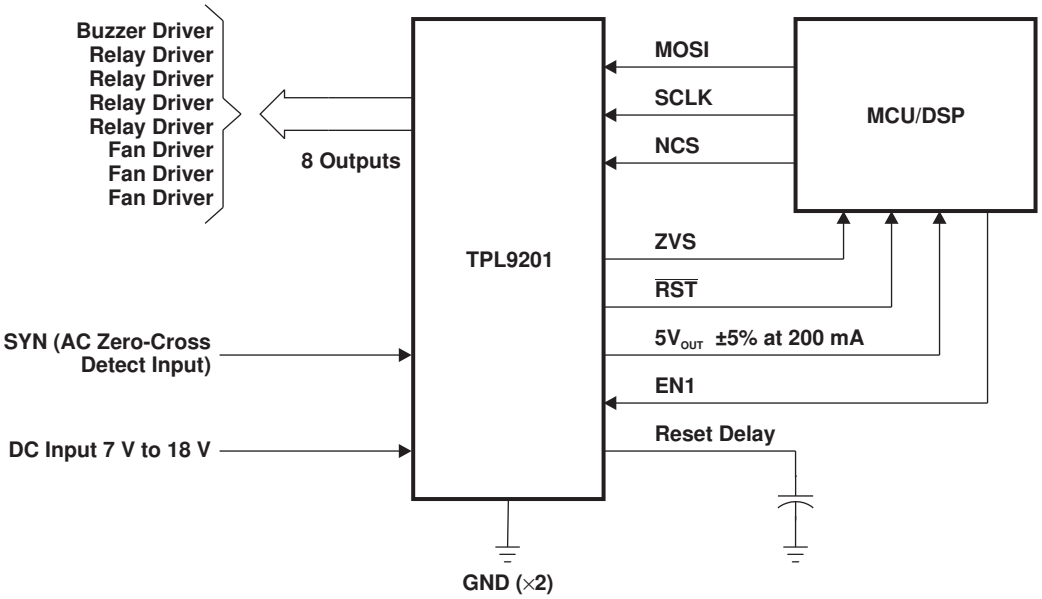


Figure 2. Typical Application

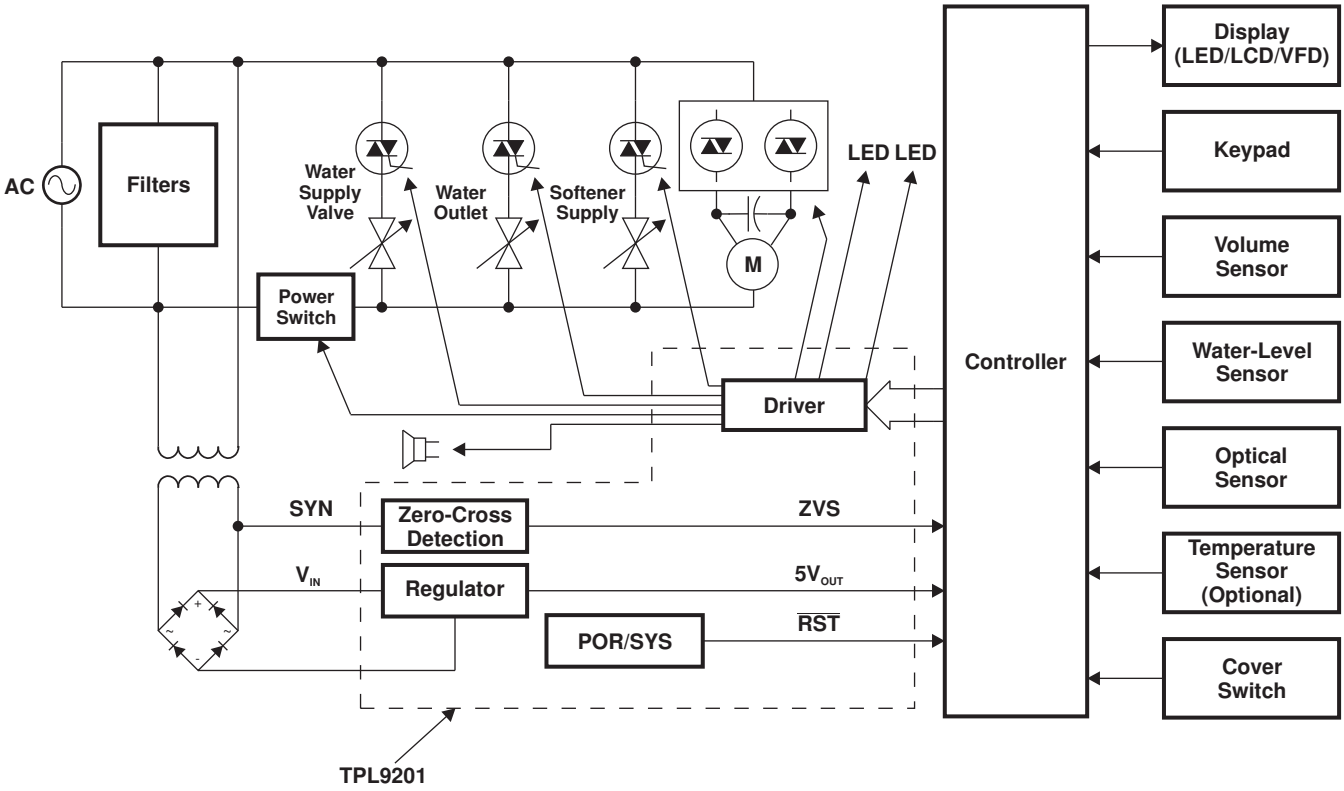


Figure 3. Washing-Machine Application

PCB Layout

To maximize the efficiency of this package for application on a single-layer or multilayer PCB, certain guidelines must be followed when laying out this part on the PCB.

The following information is to be used as a guideline only.

For further information, see the PowerPAD concept implementation document.

Application Using a Multilayer PCB

In a multilayer board application, the thermal vias are the primary method of heat transfer from the package thermal pad to the internal ground plane (see Figure 4 and Figure 5).

The efficiency of this method depends on several factors: die area, number of thermal vias, thickness of copper, etc. (see the *PowerPAD™ Thermally Enhanced Package Technical Brief*, literature number SLMA002).

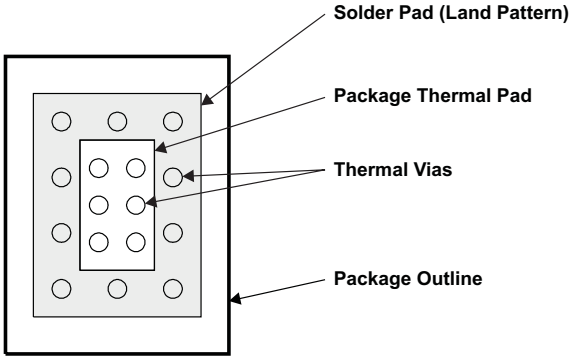


Figure 4. Package and PCB Land Configuration for a Multilayer PCB

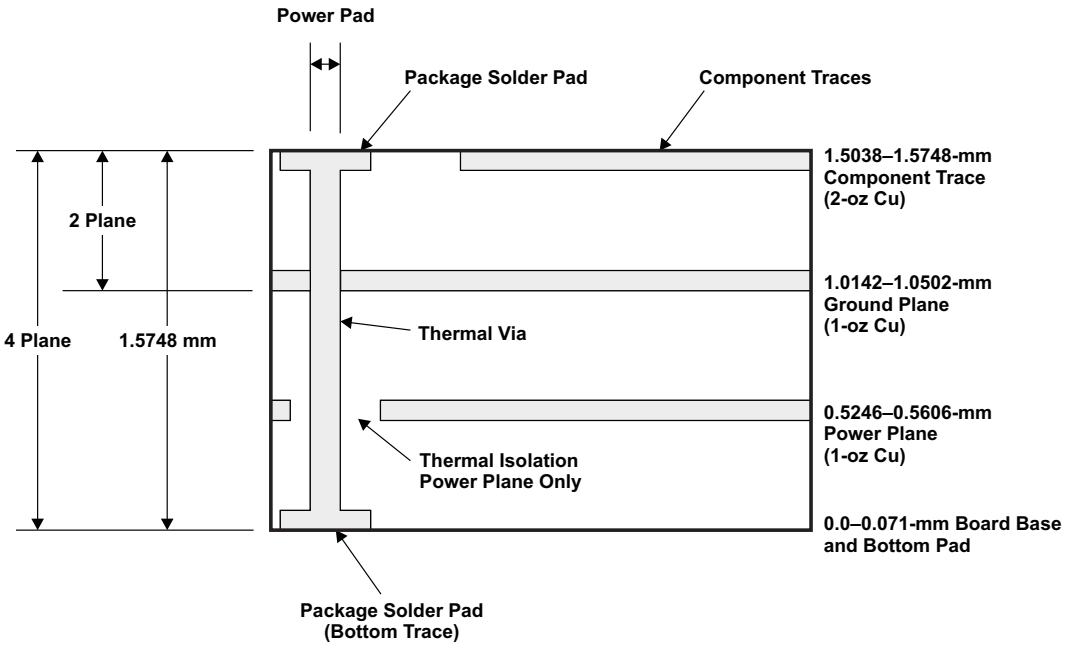


Figure 5. Multilayer Board (Side View)

Application Using a Single-Layer PCB

In a single-layer board application, the thermal pad is attached to a heat spreader (copper area) by using the low thermal-impedance attachment method (solder paste or thermal-conductive epoxy). With either method, it is advisable to use as much copper trace area as possible to dissipate the heat.

CAUTION:

If the attachment method is not implemented correctly, the functionality of the product cannot be ensured. Power-dissipation capability is adversely affected if the device is incorrectly mounted onto the circuit board.

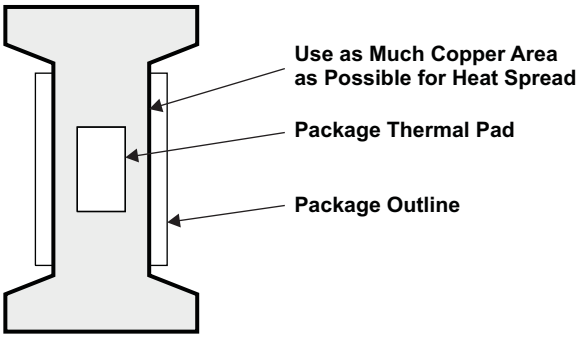


Figure 6. Layout Recommendations for a Single-Layer PCB

Recommended Board Layout

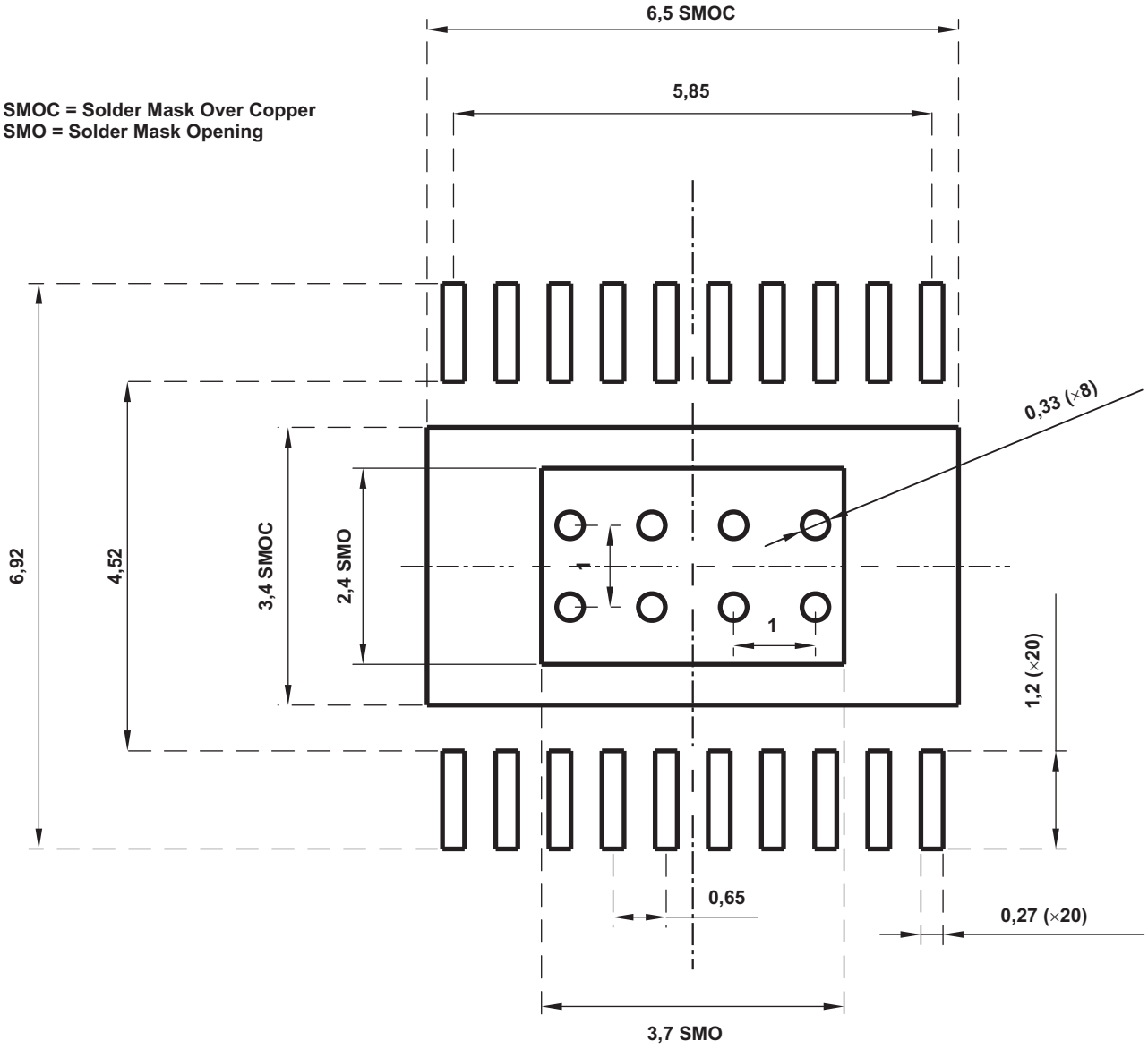


Figure 7. Recommended Board Layout for PWP

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPL9201PWP	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PL201
TPL9201PWP.A	Active	Production	HTSSOP (PWP) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PL201
TPL9201PWPR	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PL201
TPL9201PWPR.A	Active	Production	HTSSOP (PWP) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PL201

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

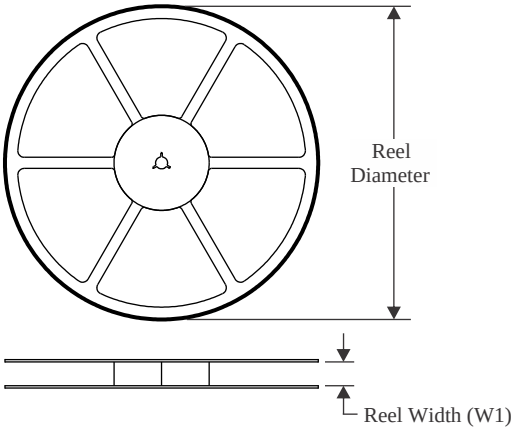
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

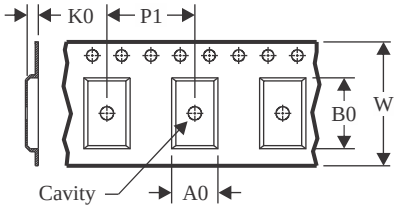
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

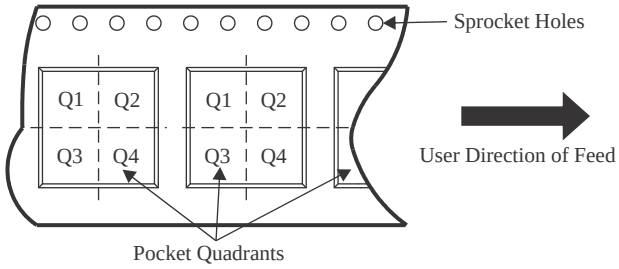


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

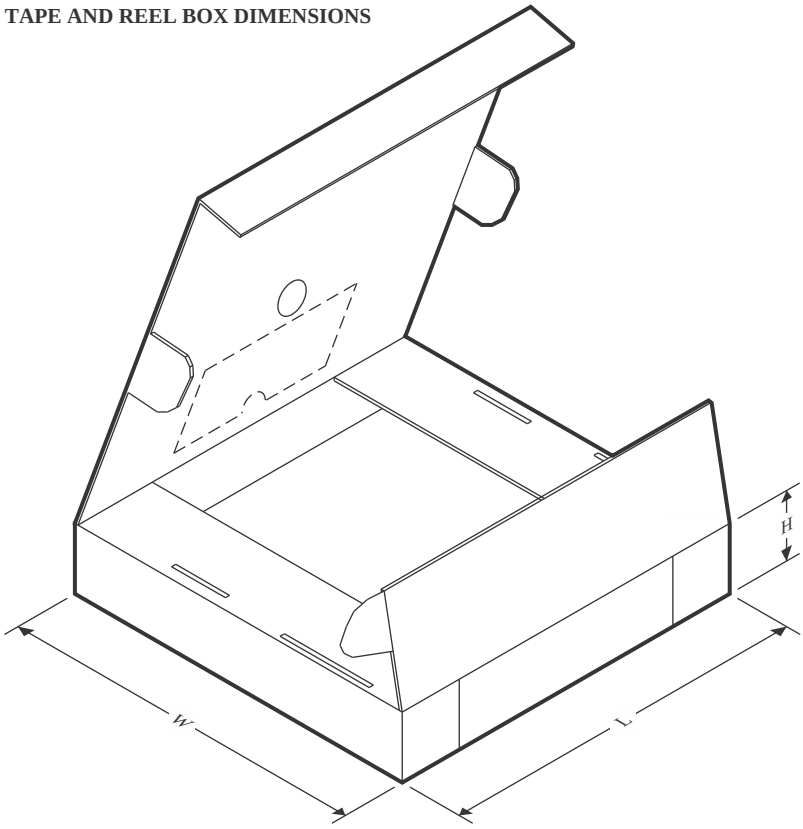
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL9201PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

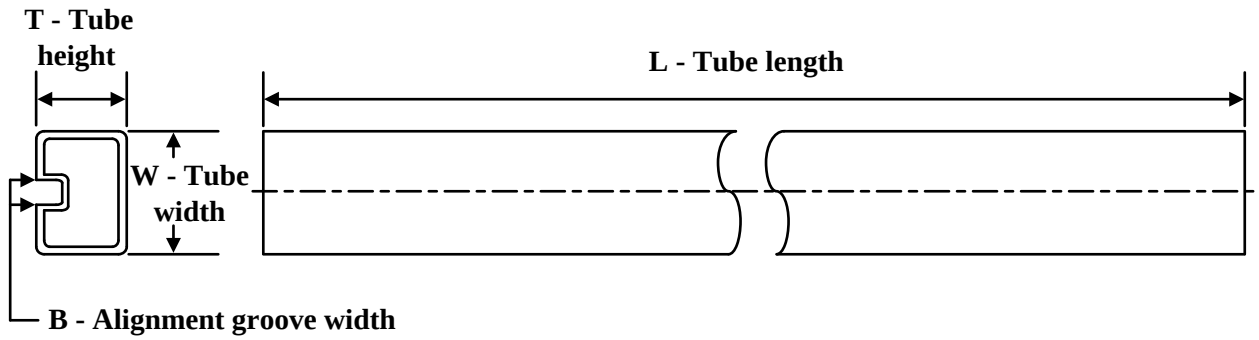
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL9201PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPL9201PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPL9201PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

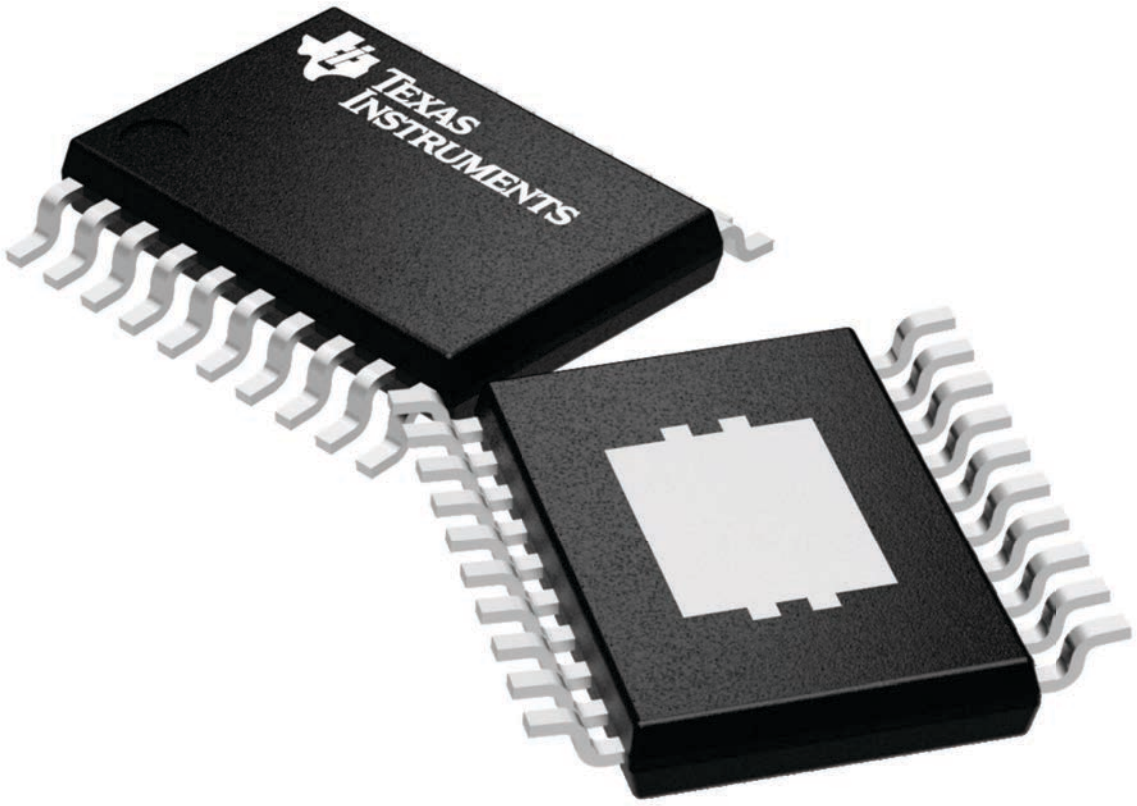
PWP 20

HTSSOP - 1.2 mm max height

6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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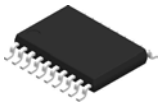
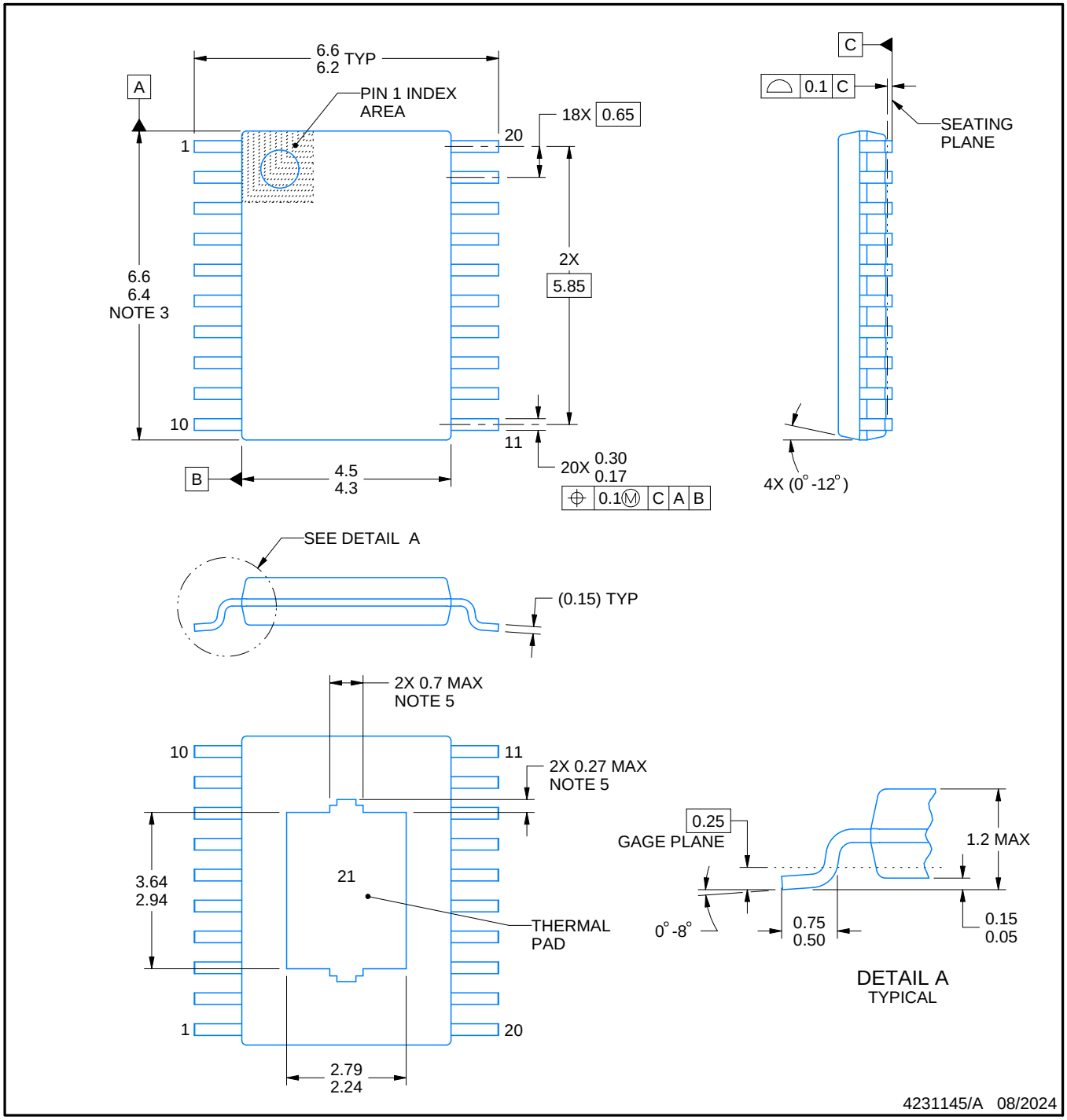


PACKAGE OUTLINE

PWP0020W

PowerPAD™ TSSOP - 1.2 mm max height

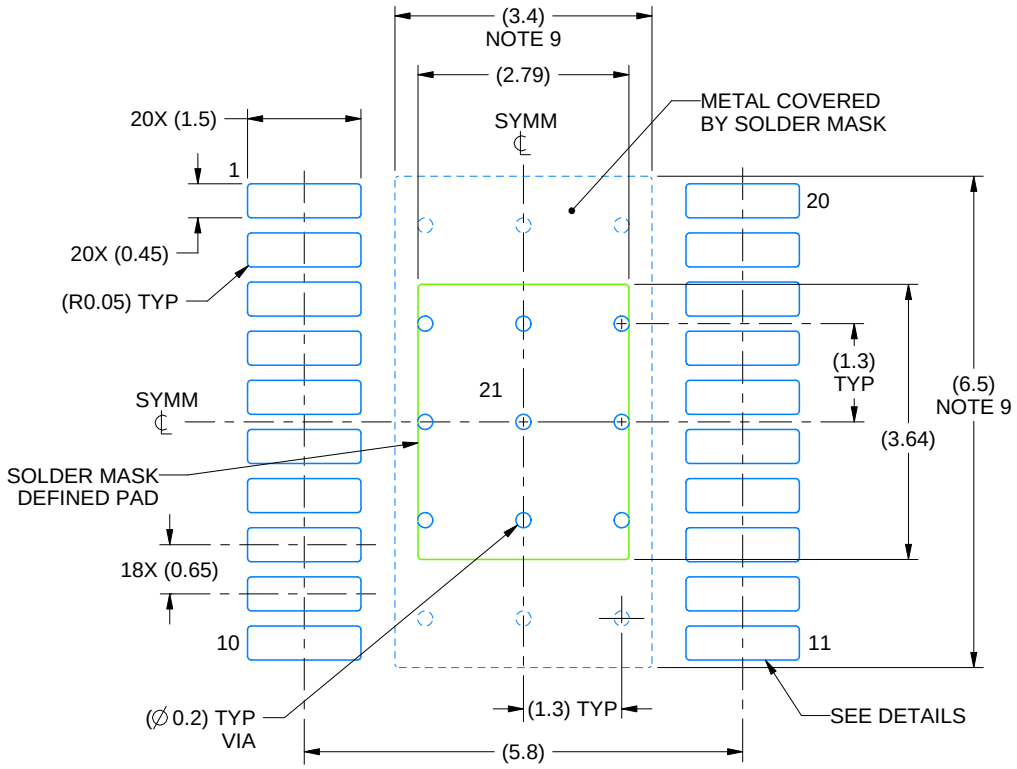
SMALL OUTLINE PACKAGE



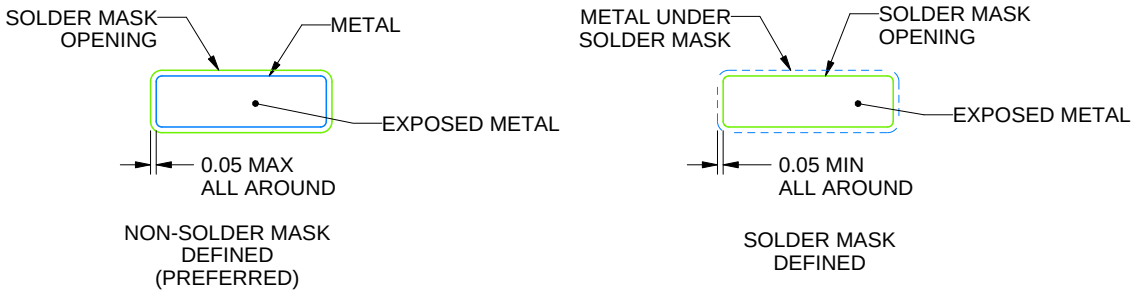
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

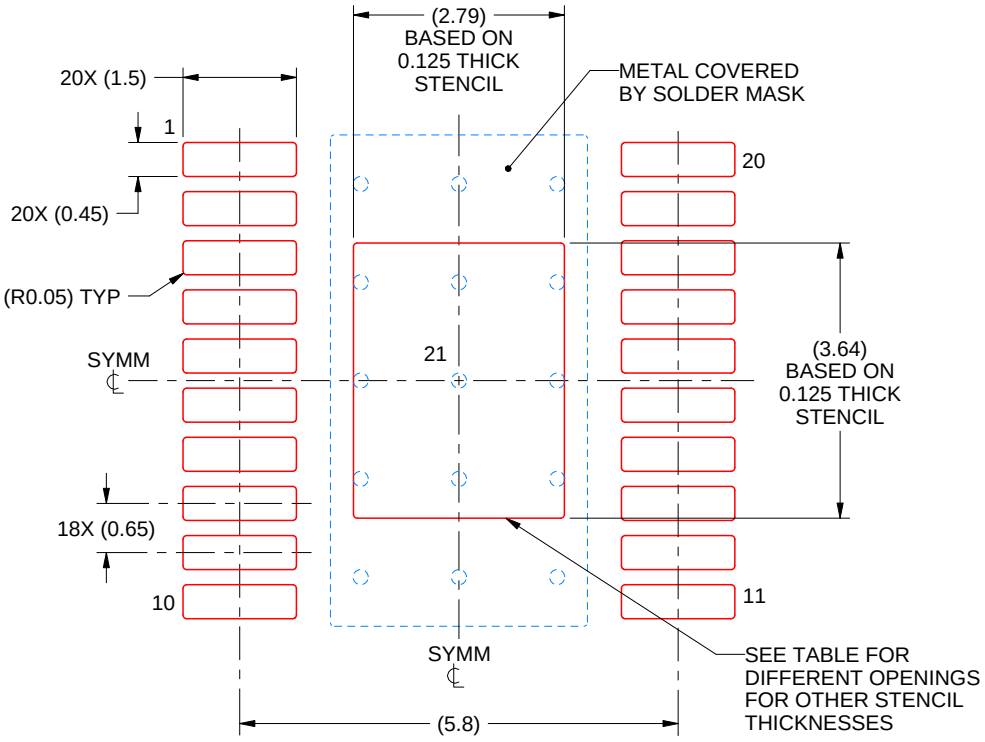


SOLDER MASK DETAILS

4231145/A 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.12 X 4.07
0.125	2.79 X 3.64 (SHOWN)
0.15	2.55 X 3.32
0.175	2.36 X 3.08

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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