



PSMN057-200B

N-channel TrenchMOS SiliconMAX standard level FET

27 March 2023

Product data sheet

1. General description

SiliconMAX standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

2. Features and benefits

- Higher operating power due to low thermal resistance
- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

3. Applications

- DC-to-DC converters
- Switched-mode power supplies

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	200	V
I_D	drain current	$T_{mb} = 100\text{ °C}$	-	-	27.5	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$	-	-	250	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 17\text{ A}; T_j = 175\text{ °C}$	-	-	165	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 39\text{ A}; V_{DS} = 160\text{ V}; V_{GS} = 10\text{ V}; T_j = 25\text{ °C}$	-	37	50	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	D2PAK (SOT404)	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN057-200B	D2PAK	plastic, single-ended surface-mounted package (D2PAK); 3 terminals (one lead cropped); 2.54 mm pitch; 11 mm x 10 mm x 4.3 mm body	SOT404

7. Marking

Table 4. Marking codes

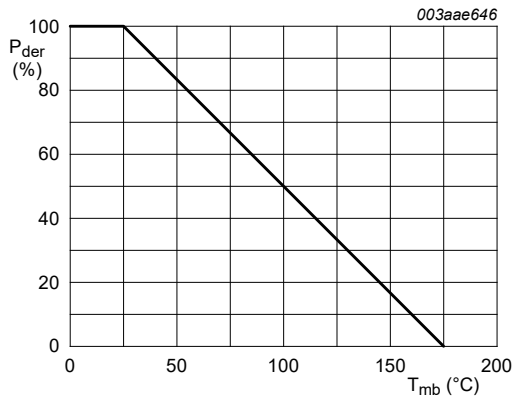
Type number	Marking code
PSMN057-200B	PSMN057 200B

8. Limiting values

Table 5. Limiting values

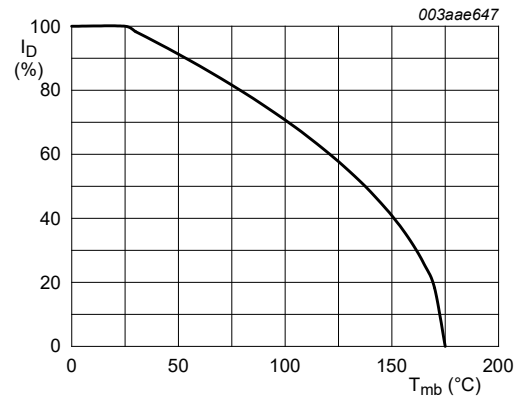
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	200	V
V _{DGR}	drain-gate voltage	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ		-	200	V
V _{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C		-	250	W
I _D	drain current	T _{mb} = 100 °C		-	27.5	A
		T _{mb} = 25 °C		-	39	A
I _{DM}	peak drain current	pulsed; T _{mb} = 25 °C		-	156	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	39	A
I _{SM}	peak source current	pulsed; T _{mb} = 25 °C		-	156	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 23 A; V _{sup} ≤ 50 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 240 μs		-	925	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 50 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω; unclamped		-	23	A



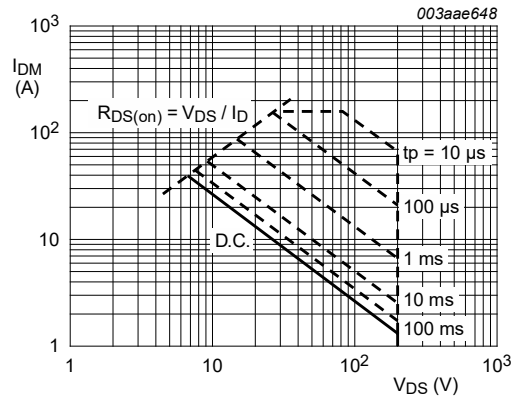
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



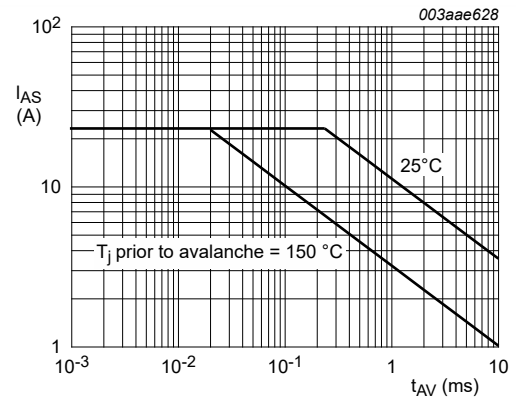
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig. 2. Normalized continuous drain current as a function of mounting base temperature



$T_{mb} = 25^{\circ}\text{C}$; I_{DM} is single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



unclamped inductive load

Fig. 4. Single-shot avalanche rating; avalanche current as a function of avalanche period

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	0.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	minimum footprint; FR4 board	-	50	-	K/W

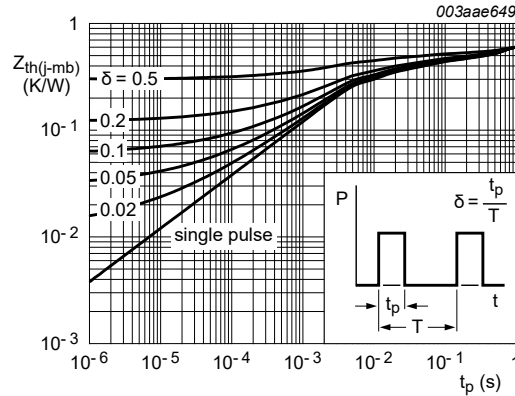


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25^\circ \text{C}$	200	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55^\circ \text{C}$	178	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175^\circ \text{C}$	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25^\circ \text{C}$	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55^\circ \text{C}$	-	-	4.4	V
I_{DSS}	drain leakage current	$V_{DS} = 200 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175^\circ \text{C}$	-	-	500	μA
		$V_{DS} = 200 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25^\circ \text{C}$	-	0.03	10	μA
I_{GSS}	gate leakage current	$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25^\circ \text{C}$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25^\circ \text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 17 \text{ A}; T_j = 175^\circ \text{C}$	-	-	165	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 17 \text{ A}; T_j = 25^\circ \text{C}$	-	41	57	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}$	-	2	4.1	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 39 \text{ A}; V_{DS} = 160 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25^\circ \text{C}$	-	96	135	nC
Q_{GS}	gate-source charge		-	13	-	nC
Q_{GD}	gate-drain charge		-	37	50	nC
C_{iss}	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25^\circ \text{C}$	-	3750	5036	pF
C_{oss}	output capacitance		-	385	520	pF
C_{rss}	reverse transfer capacitance		-	180	252	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 100 \text{ V}; R_L = 2.7 \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 5.6 \Omega; T_j = 25^\circ \text{C}$	-	18	-	ns
t_r	rise time		-	58	-	ns
$t_{d(off)}$	turn-off delay time		-	105	-	ns
t_f	fall time		-	78	-	ns
L_D	internal drain inductance	measured from tab to centre of die; $T_j = 25^\circ \text{C}$	-	3.5	-	nH
L_S	internal source inductance	measured from source lead to source bond pad; $T_j = 25^\circ \text{C}$	-	7.5	-	nH

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	133	173	ns
Q_r	recovered charge	$V_{DS} = 30\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	-	895	-	nC

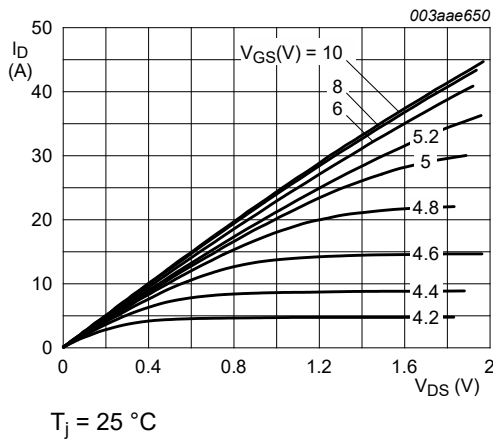


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

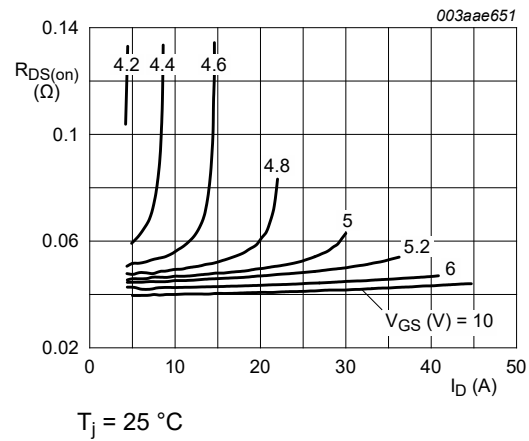


Fig. 7. Drain-source on-state resistance as a function of drain current; typical values

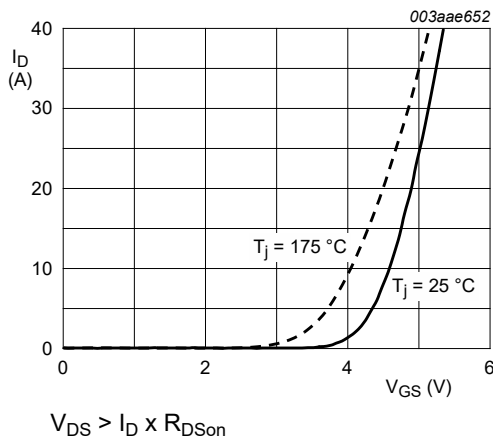


Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values

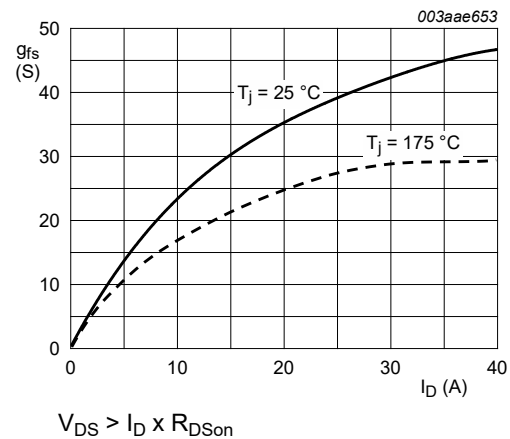


Fig. 9. Forward transconductance as a function of drain current; typical values

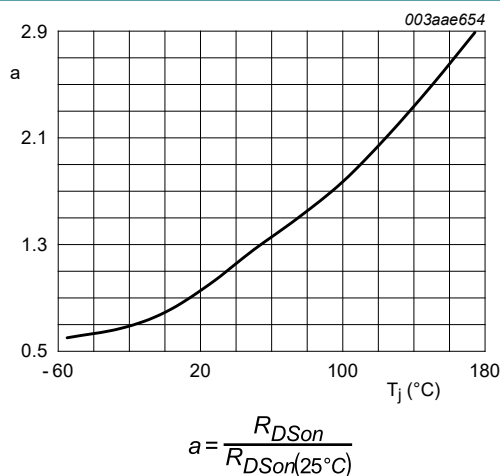


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

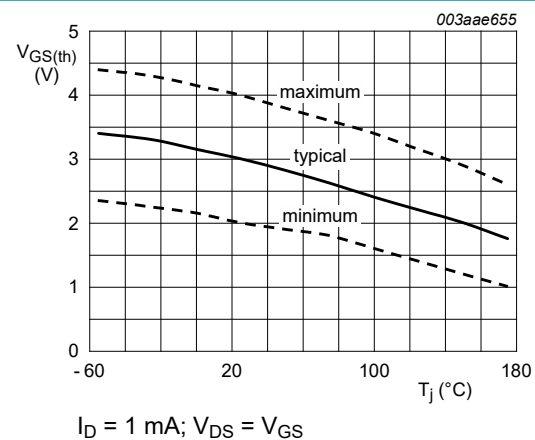


Fig. 11. Gate-source threshold voltage as a function of junction temperature

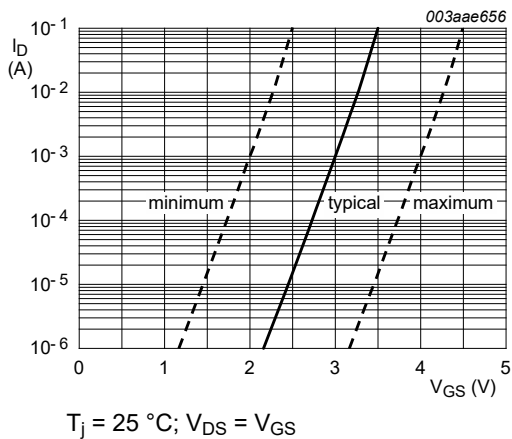


Fig. 12. Sub-threshold drain current as a function of gate-source voltage

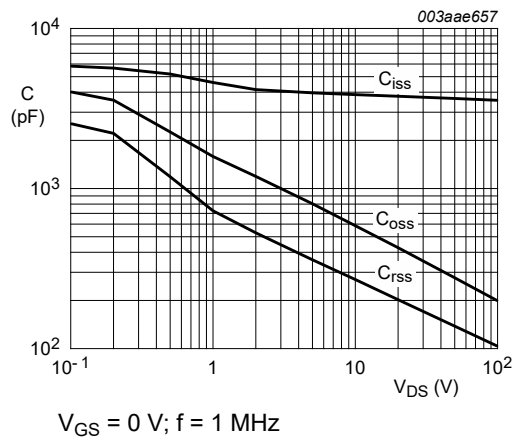


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

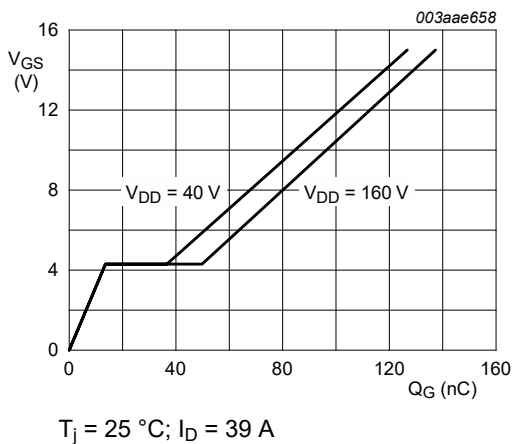


Fig. 14. Gate-source voltage as a function of gate charge; typical values

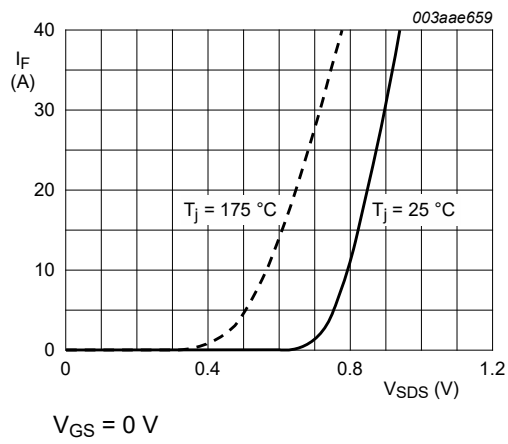


Fig. 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

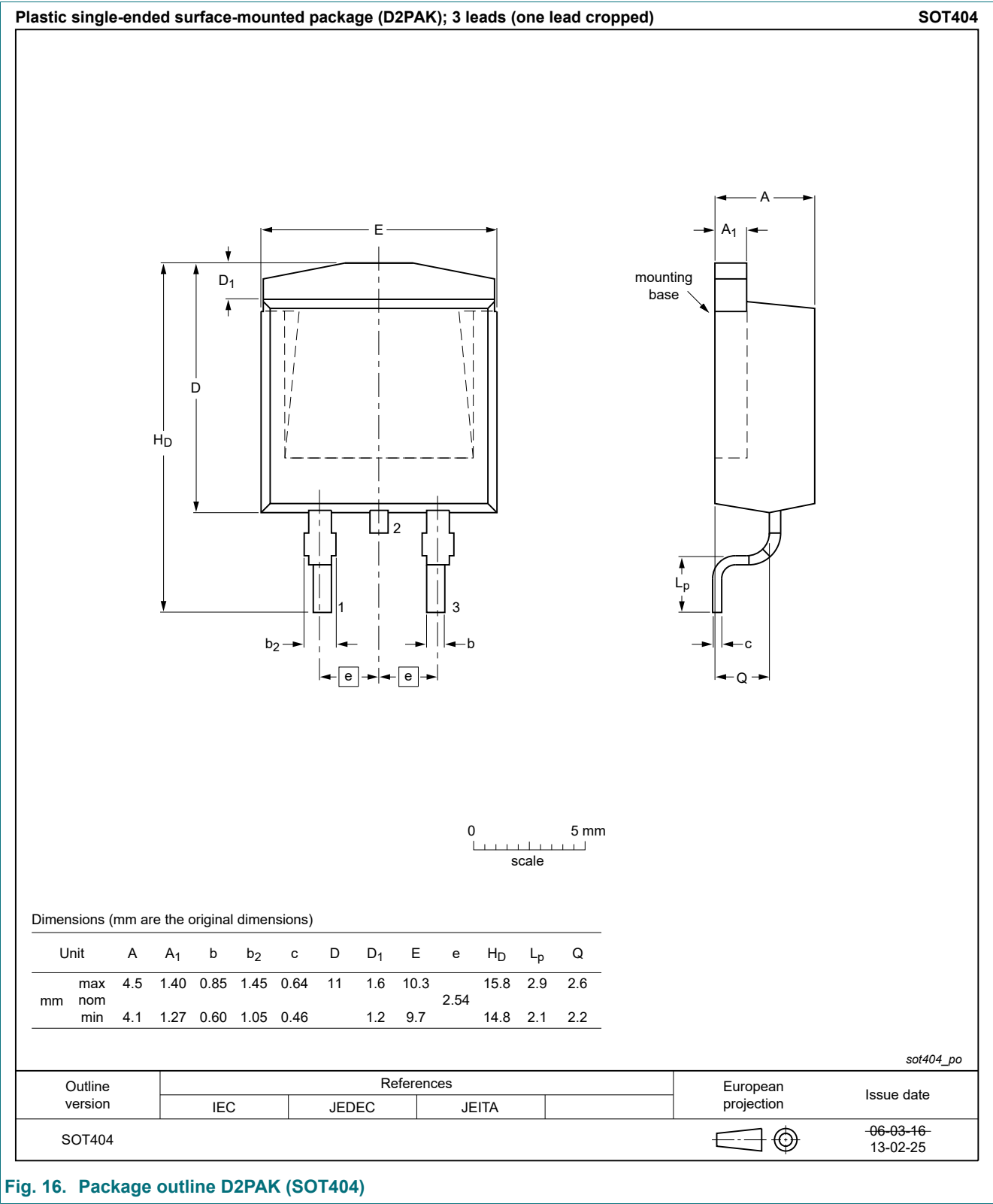


Fig. 16. Package outline D2PAK (SOT404)

12. Soldering

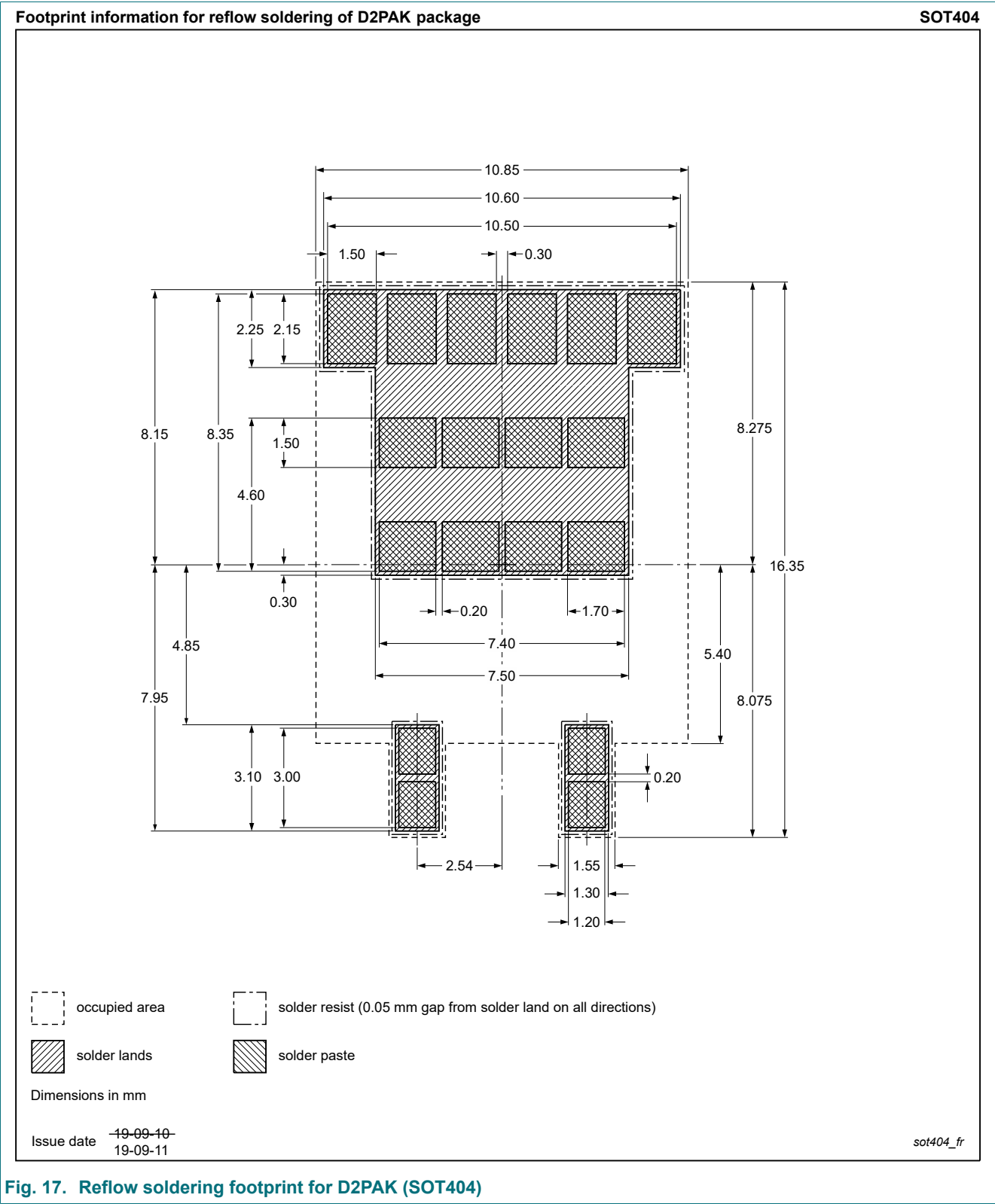


Fig. 17. Reflow soldering footprint for D2PAK (SOT404)

13. Legal information

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 1

4. Quick reference data..... 1

5. Pinning information..... 1

6. Ordering information..... 2

7. Marking..... 2

8. Limiting values..... 2

9. Thermal characteristics..... 3

10. Characteristics..... 4

11. Package outline..... 7

12. Soldering..... 8

13. Legal information..... 9

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Date of release: 27 March 2023