

# 74AHC3GU04

## Triple unbuffered inverter

Rev. 5 — 8 May 2013

Product data sheet

### 1. General description

The 74AHC3GU04 is a high-speed Si-gate CMOS device. This device provides three inverter gates with unbuffered outputs.

### 2. Features and benefits

- Symmetrical output impedance
- High noise immunity
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
  - ◆ CDM JESD22-C101D exceeds 1000 V
- Low power dissipation
- Balanced propagation delays
- Multiple package options
- Specified from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  and from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

### 3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74AHC3GU04DP	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm		SOT505-2
74AHC3GU04DC	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm		SOT765-1
74AHC3GU04GD	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body $3 \times 2 \times 0.5$ mm		SOT996-2



## 4. Marking

Table 2. Marking codes

Type number	Marking code <sup>[1]</sup>
74AHC3GU04DP	AU4
74AHC3GU04DC	AU4
74AHC3GU04GD	AU4

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

## 5. Functional diagram

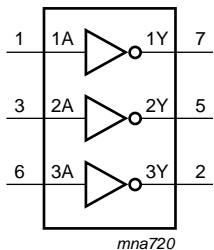


Fig 1. Logic symbol

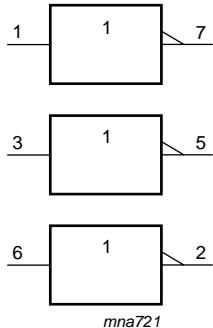


Fig 2. IEC logic symbol

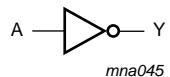


Fig 3. Logic diagram (one gate)

## 6. Pinning information

### 6.1 Pinning

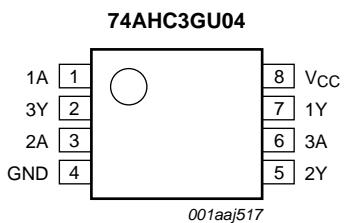


Fig 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

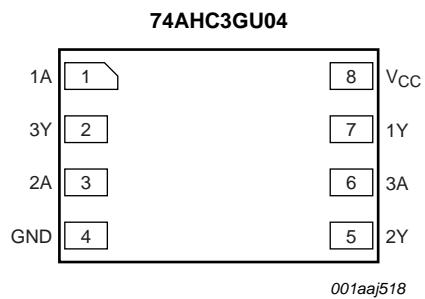


Fig 5. Pin configuration SOT996-2 (XSON8)

## 6.2 Pin description

**Table 3. Pin description**

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 6	data input
GND	4	ground (0 V)
1Y, 2Y, 3Y	7, 5, 2	data output
V <sub>CC</sub>	8	supply voltage

## 7. Functional description

**Table 4. Function table**

*H = HIGH voltage level; L = LOW voltage level*

Input	Output
A	Y
L	H
H	L

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V	[1] -20	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V	[1] -	±20	mA
I <sub>O</sub>	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	-	±25	mA
I <sub>CC</sub>	supply current		-	75	mA
I <sub>GND</sub>	ground current		-75	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[2] -	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP8 package: above 55 °C the value of P<sub>tot</sub> derates linearly with 2.5 mW/K.

For VSSOP8 package: above 110 °C the value of P<sub>tot</sub> derates linearly with 8 mW/K.

For XSON8 package: above 45 °C the value of P<sub>tot</sub> derates linearly with 2.4 mW/K.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.0	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	-	-	100	ns/V
		$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	-	-	20	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0 \text{ V}$	1.7	-	-	1.7	-	1.7	-	V
		$V_{CC} = 3.0 \text{ V}$	2.4	-	-	2.4	-	2.4	-	V
		$V_{CC} = 5.5 \text{ V}$	4.4	-	-	4.4	-	4.4	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0 \text{ V}$	-	-	0.3	-	0.3	-	0.3	V
		$V_{CC} = 3.0 \text{ V}$	-	-	0.6	-	0.6	-	0.6	V
		$V_{CC} = 5.5 \text{ V}$	-	-	1.1	-	1.1	-	1.1	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = -50 \mu\text{A}; V_{CC} = 2.0 \text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -50 \mu\text{A}; V_{CC} = 3.0 \text{ V}$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_O = -50 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.40	-	V
		$I_O = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.94	-	-	3.8	-	3.70	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$								
		$I_O = 50 \mu\text{A}; V_{CC} = 2.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu\text{A}; V_{CC} = 3.0 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
		$I_O = 8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
$I_I$	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to $5.5 \text{ V}$	-	-	0.1	-	1.0	-	2.0	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	1.0	-	10	-	40	$\mu\text{A}$
$C_I$	input capacitance		-	3.0	10	-	10	-	10	pF

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

*GND = 0 V; For test circuit see [Figure 7](#).*

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$t_{pd}$	propagation delay	nA to nY; see <a href="#">Figure 6</a>	[1]							
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[2]							
		$C_L = 15 \text{ pF}$	-	3.0	7.1	1.0	8.5	1.0	10.0	ns
		$C_L = 50 \text{ pF}$	-	4.3	10.6	1.0	12.0	1.0	13.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	[3]							
		$C_L = 15 \text{ pF}$	-	2.5	5.5	1.0	6.0	1.0	7.0	ns
		$C_L = 50 \text{ pF}$	-	3.5	7.0	1.0	8.0	1.0	9.0	ns
$C_{PD}$	power dissipation capacitance	per buffer; $V_I = \text{GND to } V_{CC}$	[4]	-	4	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[2] Typical values are measured at  $V_{CC} = 3.3 \text{ V}$ .

[3] Typical values are measured at  $V_{CC} = 5.0 \text{ V}$ .

[4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

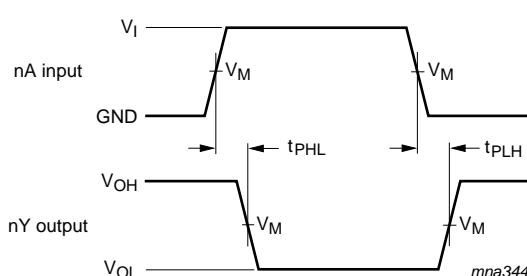
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

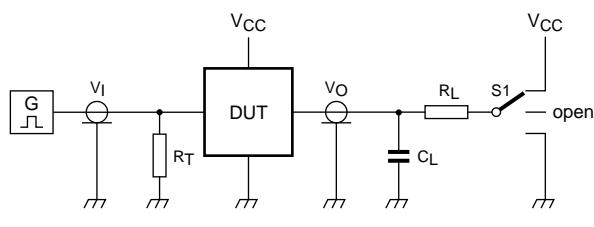
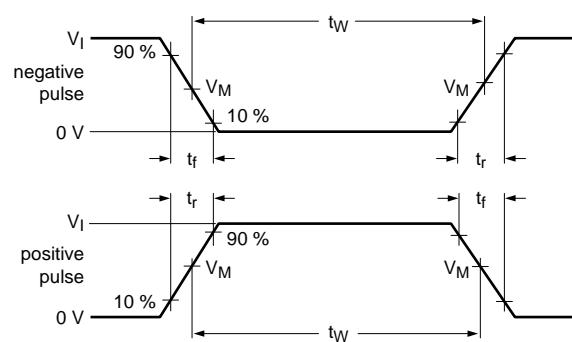
## 12. Waveforms



**Fig 6. The input (nA) to output (nY) propagation delays.**

**Table 9. Measurement points**

Type	Input	Output	
		$V_M$	$V_M$
74AHC3GU04	$0.5V_{CC}$		$0.5V_{CC}$



001aad983

Test data is given in [Table 10](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

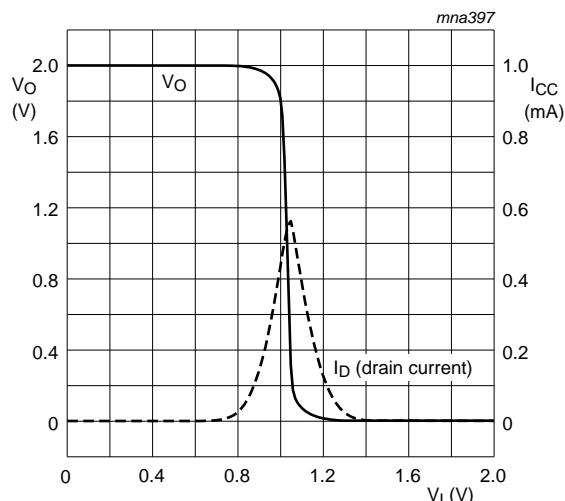
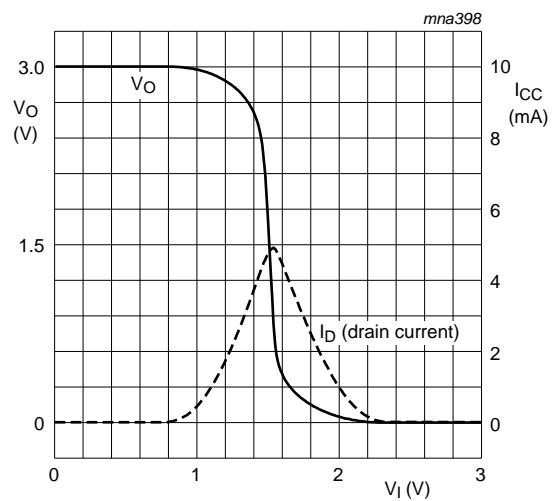
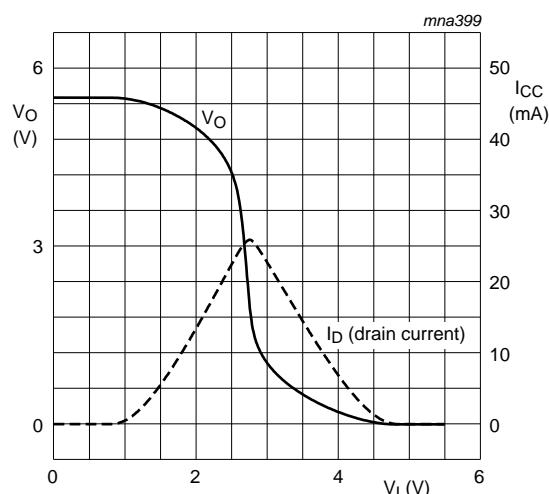
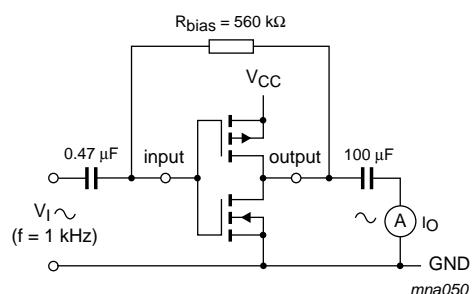
$S1$  = Test selection switch.

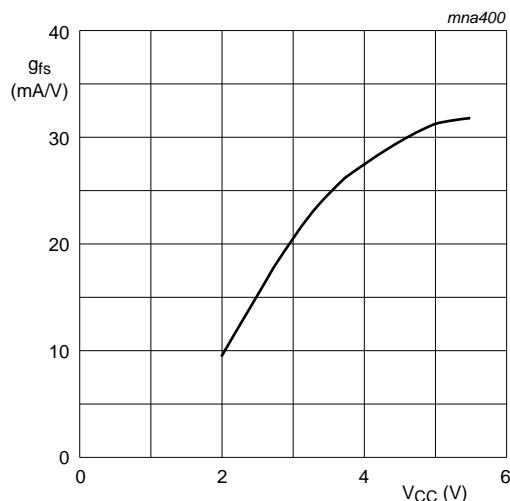
**Fig 7. Test circuit for measuring switching times**

**Table 10. Test data**

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74AHC3GU04	$V_{CC}$	$\leq 3$ ns	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

### 13. Typical transfer characteristics

Fig 8.  $V_{CC} = 2.0$  V;  $I_O = 0$  AFig 9.  $V_{CC} = 3.0$  V;  $I_O = 0$  AFig 10.  $V_{CC} = 5.5$  V;  $I_O = 0$  AFig 11. Test set-up for measuring forward transconductance  $g_{fs} = \Delta I_O / \Delta V_I$  at  $V_O$  is constant

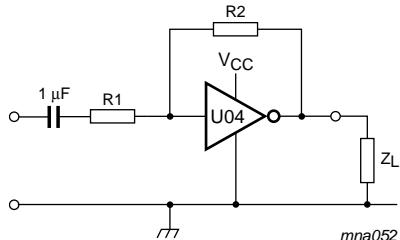
Fig 12. Typical forward transconductance  $g_{fs}$  as a function of the supply voltage at  $T_{amb} = 25^{\circ}\text{C}$ 

## 14. Application information

Some applications are:

- Linear amplifier (see [Figure 13](#))
- In crystal oscillator design (see [Figure 14](#))

**Remark:** All values given are typical unless otherwise specified.



Maximum  $V_{o(p-p)} = V_{CC} - 1.5$  V centered at  $0.5 \times V_{CC}$ .

$$G_v = -\frac{G_{ol}}{1 + \frac{R1}{R2}(1 + G_{ol})}$$

$G_{ol}$  = open loop gain

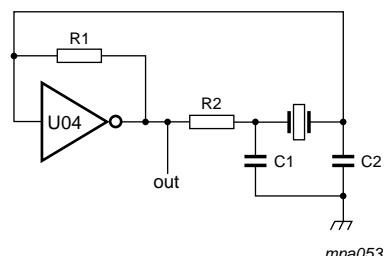
$G_v$  = voltage gain

$R1 \geq 3 \text{ k}\Omega$ ,  $R2 \leq 1 \text{ M}\Omega$

$Z_L > 10 \text{ k}\Omega$ ;  $G_{ol} = 20$  (typ.)

Typical unity gain bandwidth product is 5 MHz.

Fig 13. Used as a linear amplifier



$C1 = 47 \text{ pF}$  (typ.)

$C2 = 22 \text{ pF}$  (typ.)

$R1 = 1 \text{ M}\Omega$  to  $10 \text{ M}\Omega$  (typ.)

$R2$  optimum value depends on the frequency and required stability against changes in  $V_{CC}$  or average minimum  $I_{CC}$  ( $I_{CC}$  is typically 2 mA at  $V_{CC} = 3$  V and  $f = 1$  MHz).

Fig 14. Crystal oscillator configuration

**Table 11. External components for resonator ( $f < 1$  MHz)***All values given are typical and must be used as an initial set-up.*

Frequency	R1	R2	C1	C2
10 kHz to 15.9 kHz	22 MΩ	220 kΩ	56 pF	20 pF
16 kHz to 24.9 kHz	22 MΩ	220 kΩ	56 pF	10 pF
25 kHz to 54.9 kHz	22 MΩ	100 kΩ	56 pF	10 pF
55 kHz to 129.9 kHz	22 MΩ	100 kΩ	47 pF	5 pF
130 kHz to 199.9 kHz	22 MΩ	47 kΩ	47 pF	5 pF
200 kHz to 349.9 kHz	22 MΩ	47 kΩ	47 pF	5 pF
350 kHz to 600 kHz	22 MΩ	47 kΩ	47 pF	5 pF

**Table 12. Optimum value for R2**

Frequency	R2	Optimum for
3 kHz	2.0 kΩ	minimum required $I_{CC}$
	8.0 kΩ	minimum influence due to change in $V_{CC}$
6 kHz	1.0 kΩ	minimum required $I_{CC}$
	4.7 kΩ	minimum influence by $V_{CC}$
10 kHz	0.5 kΩ	minimum required $I_{CC}$
	2.0 kΩ	minimum influence by $V_{CC}$
14 kHz	0.5 kΩ	minimum required $I_{CC}$
	1.0 kΩ	minimum influence by $V_{CC}$
>14 kHz	-	replace R2 by C3 with a typical value of 35 pF

## 15. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

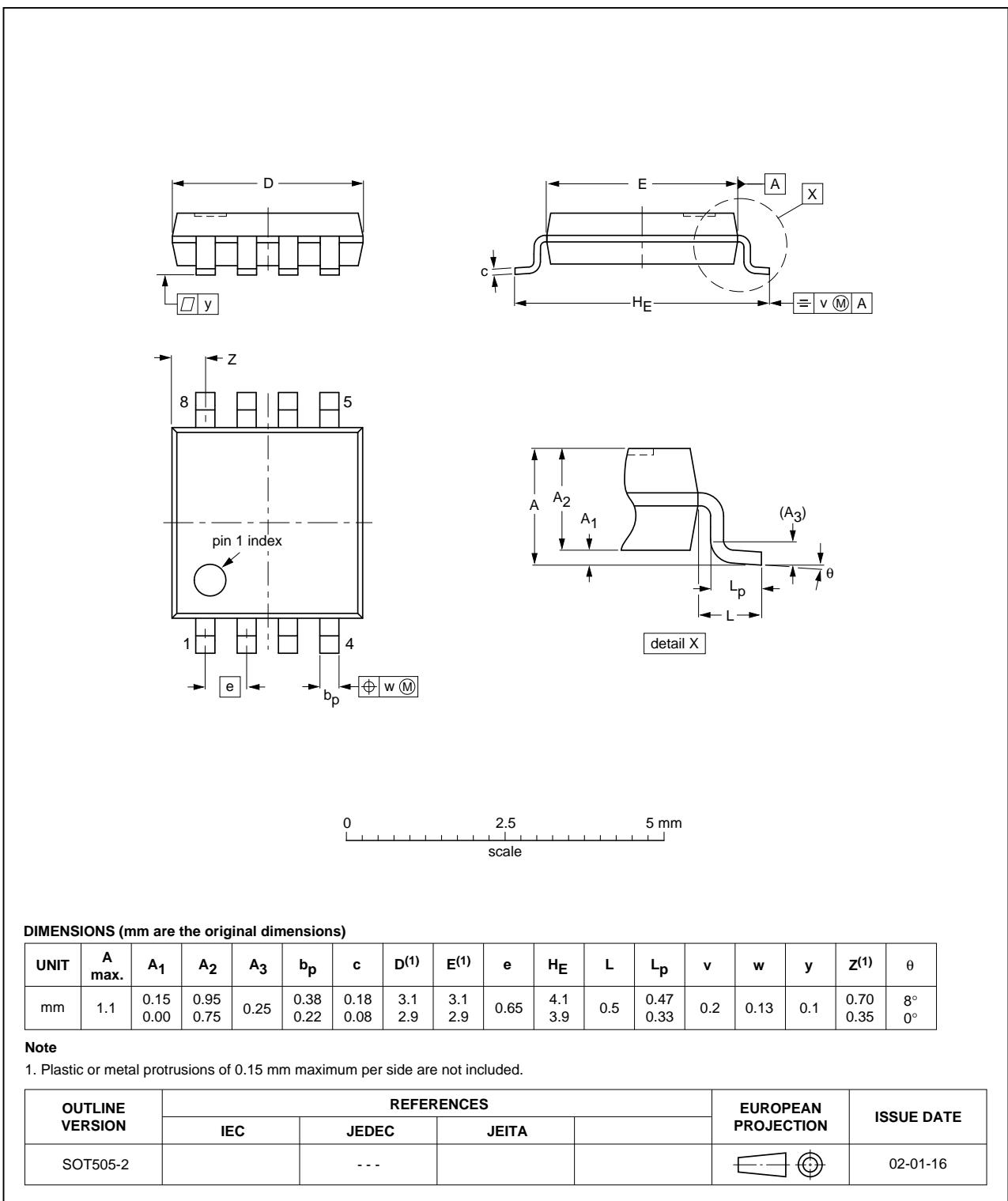


Fig 15. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

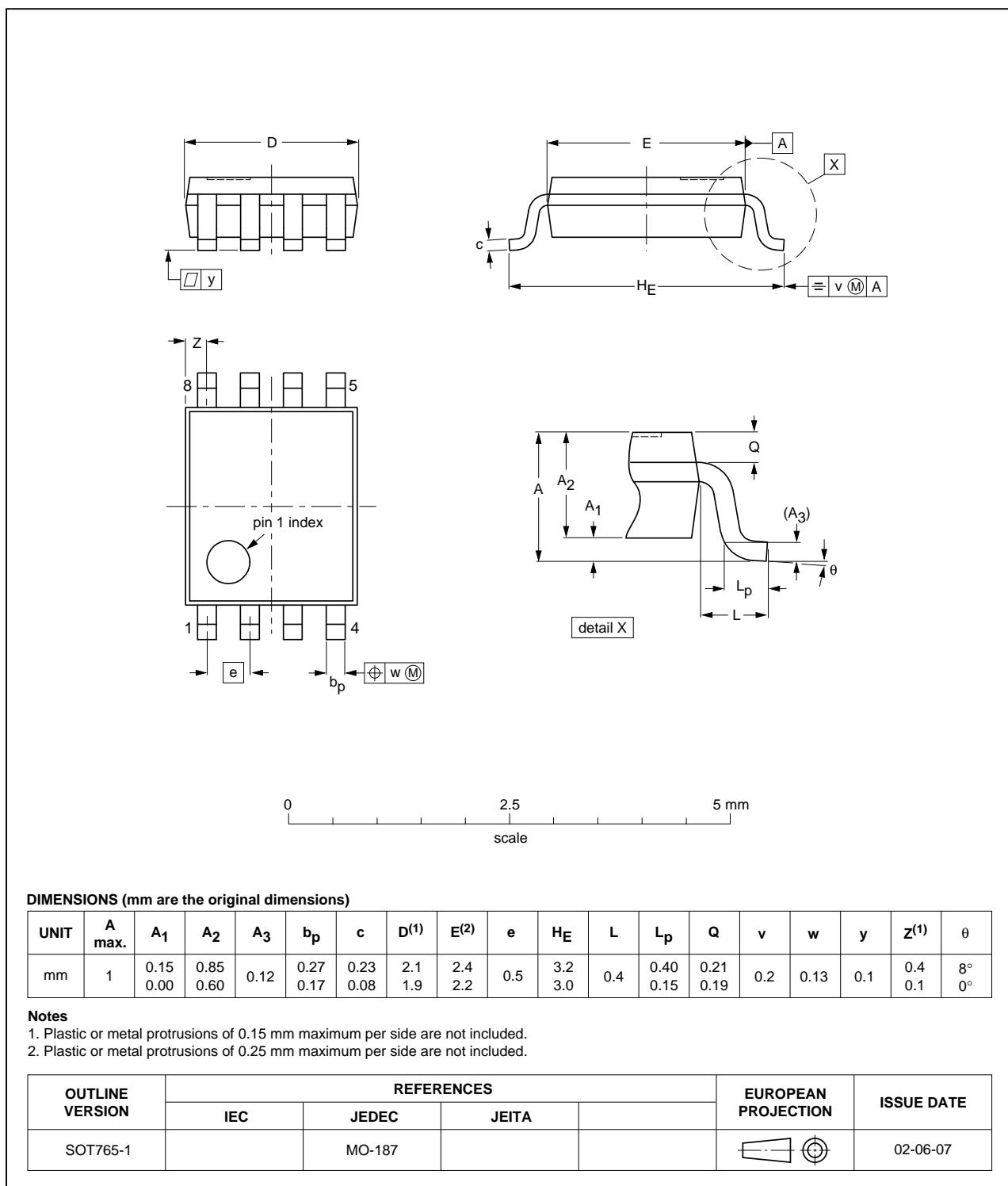


Fig 16. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads;  
8 terminals; body 3 x 2 x 0.5 mm

SOT996-2

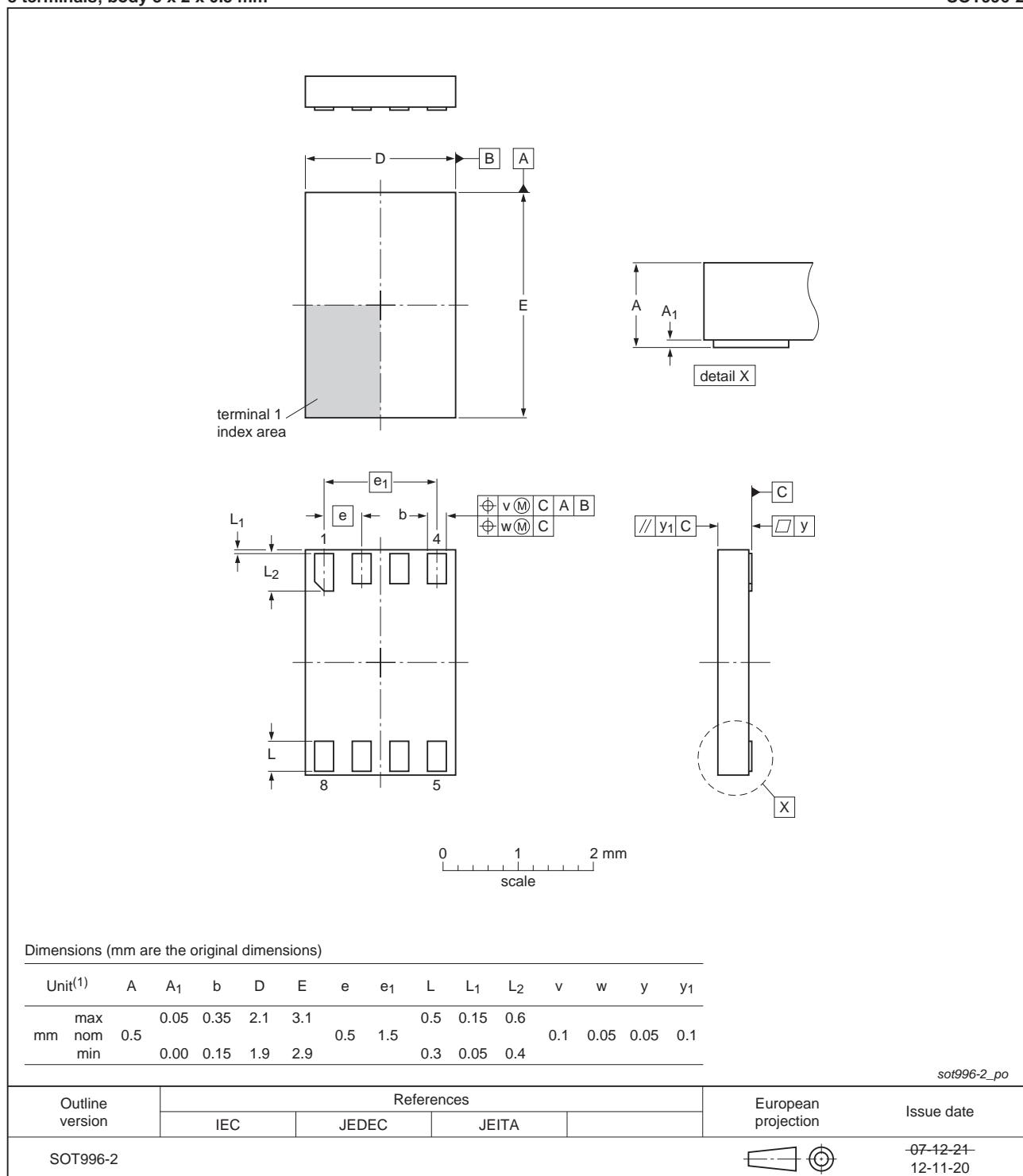


Fig 17. Package outline SOT996-2 (XSON8)

## 16. Abbreviations

**Table 13. Abbreviations**

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 17. Revision history

**Table 14. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC3GU04 v.5	20130508	Product data sheet	-	74AHC3GU04 v.4
Modifications:	<ul style="list-style-type: none"> <li>For type number 74AHC3GU04GD XSON8U has changed to XSON8.</li> </ul>			
74AHC3GU04 v.4	20100107	Product data sheet	-	74AHC3GU04 v.3
			<ul style="list-style-type: none"> <li>Marking code for 74AHC3GU04DP package changed from AU04 to AU4</li> </ul>	
74AHC3GU04 v.3	20090126	Product data sheet	-	74AHC3GU04 v.2
74AHC3GU04 v.2	20040923	Product specification	-	74AHC3GU04 v.1
74AHC3GU04 v.1	20040305	Product specification	-	-

## 18. Legal information

### 18.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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