FEATURES

- Generates six clock outputs from 20 MHz to 80 MHz (the S4403 generates ten outputs and HFOUT generates 10MHz to 40MHz)
- 21 selectable phase/frequency relationships for the clock outputs
- Compensates for clock skew by allowing output delay adjustment down to 3.125 ns increments
- TTL outputs have less than 400 ps maximum skew
- Lock Detect output indicates loop status
- Internal PLL with VCO operating at 160 to 320 MHz
- Test Enable input allows VCO bypass for open-loop operation in board test
- Maximum 1.0 ns of phase error (750 ps from part to part)
- Proven 1.0 micron BiCMOS technology
- Single +5V power supply operation
- 28/44 PLCC packages

APPLICATIONS

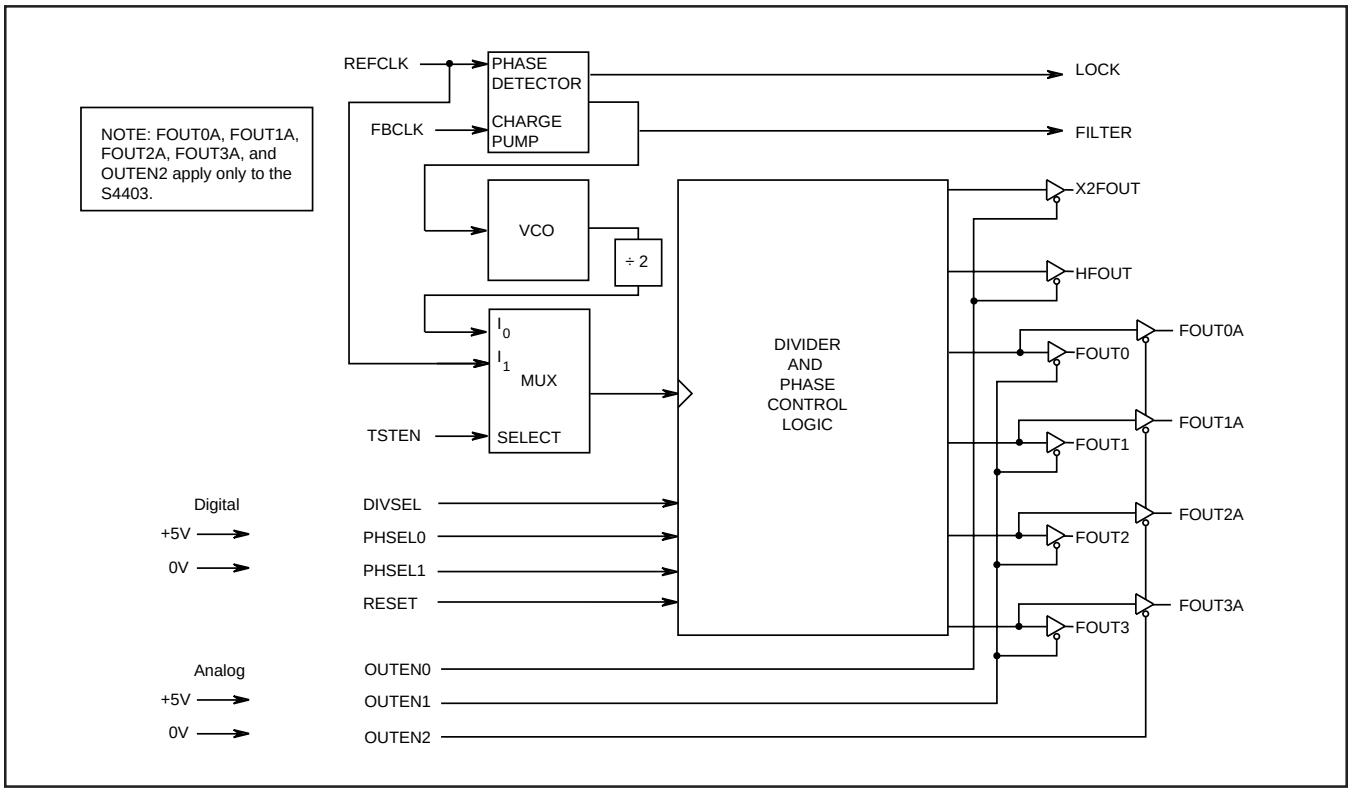
- CMOS ASIC Systems
- High-speed Microprocessor Systems
- Backplane Clock Deskew and Distribution

GENERAL DESCRIPTION

The S4402/S4403 BiCMOS clock generators allow the user to generate multiphase TTL clocks in the 10–80 MHz range with less than 400 ps of skew. Use of a single off-chip filter allows an entire 160–320 MHz phase-locked loop (PLL) to be implemented on-chip. Divide-by-two and times-two outputs allow the ability to generate output clocks at half, equal to, or twice the reference clock input frequency. By using the programmable divider and phase selector, the user can select from up to 21 different output relationships. The outputs can be phase-adjusted in increments as small as 3.125 ns to tailor the clocks to exact system requirements.

Implemented in AMCC's proven 1.0 micron BiCMOS technology, the S4402 generates six TTL outputs, while the S4403 provides those six plus four duplicates (FOUT0A–FOUT3A) for a total of ten. Output enables are provided for the various banks, allowing clock control for board and system tests.

Figure 1. Clock Generator Block Diagram



FUNCTIONAL DESCRIPTION

Frequency and Phase Controls

The S4402/S4403 clock generators provide multiple outputs that are synchronized in both frequency and phase to a periodic clock input. Two select pins and an external feedback path allow the user to phase-adjust the six outputs (FOUT0–FOUT3, HFOUT, and X2FOUT) relative to the input clock REFCLK, as well as control their frequency.

The DIVSEL input controls the programmable divider that follows the voltage controlled oscillator (VCO). This doubles the lock range of the PLL by allowing the user to select a VCO frequency divided by four (DIVSEL Low) or by eight (DIVSEL High).

The frequency of the four FOUT0–FOUT3 outputs (and the duplicate set of the four FOUT0A–FOUT3A outputs on the S4403) is determined by the REFCLK clock frequency and the output that is tied back to the FBCLK input. In addition, the X2FOUT TTL output provides a clock signal identical to the FOUT0 output in the divide-by-four mode, and twice the FOUT0 frequency (maximum frequency of 80 MHz) in the divide-by-eight mode. The HFOUT TTL output provides a clock signal that is in phase with the FOUT0 output, but at half the FOUT0 frequency in both the divide-by-four and divide-by-eight modes. Refer to the Output Select Matrix in Table 3 for the specific relationships.

Phase adjustments can be made in increments as small as 3.125 ns. The minimum phase delay between FOUT0–FOUT3 signals is a function of the VCO frequency. The VCO frequency can be determined by multiplying the output frequency by the divide-by ratio of four or eight, controlled by DIVSEL. The minimum phase delay t is equal to the period of the VCO frequency:

$$t = 1 / \text{VCO freq}$$

Since the VCO can operate in the 160 MHz to 320 MHz range, minimum phase delay values can range from 6.25 ns to 3.125 ns. Table 1 shows various FOUT/VCO frequencies and the associated phase resolution.

The PHSEL1 and PHSEL0 inputs allow the user to select several phase relationships among the four FOUT0–FOUT3 TTL clock outputs. These choices can be seen in Table 2, and the Output Select Matrix provided in Table 3 describes the 21 output configurations available to the user. The two “Select Pins” columns specify the signal levels on the pins PHSEL0 and PHSEL1. These are active High signals. The column entitled “Output Fed to FBCLK” indicates which output (FOUT0–FOUT3, HFOUT, or X2FOUT) is externally connected to the feedback input (FBCLK) to produce the resulting waveforms shown in the appropriate row in the table. The last seven columns specify the resulting phase and frequency relationships of each output to the user clock input (REFCLK). A negative value indicates the time by which the output rising edge precedes the input (REFCLK) rising edge. A positive value is the time by which the rising edge of the output follows the rising edge of the input clock.

Table 1. Example Phase Resolution

FOUT0–3 Freq	Divider Select	VCO Freq	Min Phase Resolution
80 MHz	4	320 MHz	3.125 ns
66 MHz	4	266 MHz	3.75 ns
50 MHz	4	200 MHz	5.0 ns
40 MHz	4	160 MHz	6.25 ns
40 MHz	8	320 MHz	3.125 ns
33 MHz	8	266 MHz	3.75 ns
25 MHz	8	200 MHz	5.0 ns
20 MHz	8	160 MHz	6.25 ns

Table 2. Phase Selections

PHSEL1	PHSEL0	Phase Relationship
0	0	All at same phase
0	1	FOUT0–FOUT3 outputs skewed by 90 degrees from each other
1	0	FOUT1 leads FOUT0 by minimum phase, FOUT2 lags FOUT0 by minimum phase, and FOUT3 lags FOUT0 by 90 degrees
1	1	FOUT1 lags FOUT0 by minimum phase, FOUT2 lags FOUT1 by minimum phase, and FOUT3 lags FOUT2 by minimum phase

Example:

In a typical system, designers may need several low-skew outputs, one early clock, one late clock, a clock at half the input clock frequency, and one at twice the input clock frequency. This system requirement can be met by setting PHSEL1 to 1, PHSEL0 to 0, and feeding back FOUT0 to the FBCLK input (Row 10 of Table 3). The result is that FOUT0 will be phase-aligned to REFCLK, FOUT1 will lead REFCLK by a minimum phase delay, FOUT2 will lag REFCLK by a minimum phase delay, FOUT3 will phase-lag REFCLK by 90°, HFOUT will be phase-aligned with REFCLK but at half the frequency, and X2FOUT will be either phase-aligned at the same frequency as the reference clock if DIVSEL = 0, or at twice the frequency if DIVSEL = 1.

Several other waveform examples and typical applications are provided on pages 7-8 and 7-9.

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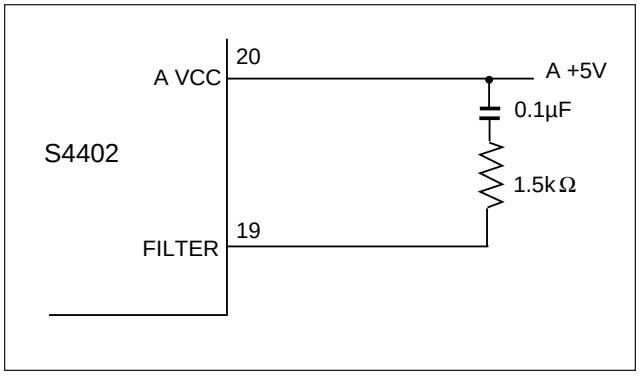
Enabling Outputs

The S4402 has two output-enable inputs that control which outputs toggle. (The S4403 has three output-enable inputs.) When held LOW, OUTEN0 controls the frequency doubler output X2FOUT and the half-frequency output HFOUT. OUTEN1 controls the FOUT0–FOUT3 outputs. The third input on the S4403, OUTEN2, controls the duplicate set of four outputs FOUT0A–FOUT3A. When an output enable pin is held High, its associated outputs are disabled and held in a High state.

Filter

The FILTER output is a tap between the analog output of the phase detector and the VCO input. This pin allows a simple external filter (Figure 2) to be included in the PLL. AMCC recommends the use of the filter component values shown. This filter was chosen for its ability to reduce the output jitter and filter out noise on the REFCLK input. The filter components should be in surface mounted packages with minimum lead inductance.

Figure 2. External PLL Filter



Reset

When the RESET pin is pulled low, all the internal states go to zero one clock cycle (from the VCO or REFCLK in the test mode) before the outputs go low. After the chip is reset, the PLL requires a resynchronization time of ≤5ms before lock is again achieved.

Lock Detect

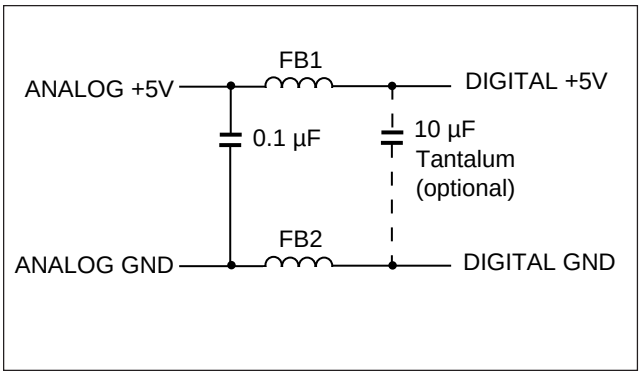
A lock detect function is provided by the LOCK output. When REFCLK and FBCLK are within 2–4 ns of each other, the PLL is in lock, and the LOCK output goes High.

Power Supply Considerations

Power for the analog portion of the S4402/S4403 chips must be isolated from the digital power supplies to minimize noise on the analog power supply pins. This isolation between the analog and digital power supplies can be accomplished with a simple external power supply filter (Figure 3). The analog power planes are connected to the digital power planes through single ferrite beads (FB1 and FB2) or inductors capable of handling 25 mA. The recommended value for the inductors is in the range from 5 to 100µH, and depends upon the frequency spectrum of the digital power supply noise. The ferrite beads should exhibit 75Ω impedance at 10 MHz.

Decoupling capacitors are also very important to minimize noise. The decoupling capacitors must have low lead inductance to be effective, so ceramic chip capacitors are recommended. Decoupling capacitors should be located as close to the power pins as physically possible. And the decoupling should be placed on the top surface of the board between the part and its connections to the power and ground planes.

Figure 3. External Power Supply Filter



Test Capabilities

The TSTEN input puts the S4402/S4403 into a test mode and allows users to bypass the VCO and provide their own clock through the REFCLK input. When TSTEN is High, the VCO is turned off and the REFCLK signal drives the divider/phase adjust circuitry, directly sequencing the outputs. The TSTEN and REFCLK inputs join the divider circuitry after the initial divide-by-two stage. Therefore, REFCLK is divided by two in the divide-by-four mode and divided by four in the divide-by-eight mode.

PIN DESCRIPTIONS

Input Signals

REFCLK. Frequency reference supplied by the user that, along with the output tied to the FBCLK input, determines the frequency of the FOUT0–FOUT3 outputs. Also replaces the VCO output when TSTEN is high (after first divide-by-two stage in divider phase control logic). See TSTEN.

FBCLK. Feedback clock that, along with the REFCLK input, determines the frequency of the FOUT0–FOUT3 outputs. One output is selected to feed back to this input. (See Table 3.)

DIVSEL. Controls the divider circuit that follows the VCO. When DIVSEL is low, the VCO frequency is divided by four. When DIVSEL is high, the VCO frequency is divided by eight. (See Tables 1 and 3.)

PHSEL0. This input, along with PHSEL1, allows selection of the phase relationship among the four FOUT0–FOUT3 outputs. See Tables 2 and 3 for the selection choices.

PHSEL1. Along with PHSEL0, allows selection of the phase relationship among the four FOUT0–FOUT3 outputs. See Tables 2 and 3 for the selection choices.

OUTEN0. Active Low. Output enable signal that controls which outputs toggle. Controls the frequency doubler output (X2FOUT) and the half-frequency output (HFOUT).

OUTEN1. Active Low. Output enable signal that controls which outputs toggle. Controls the FOUT0–FOUT3 outputs.

OUTEN2. (S4403 only.) Active Low. Controls the duplicate set of outputs to FOUT0–FOUT3 (FOUT0A, FOUT1A, FOUT2A, AND FOUT3A).

RESET. Active Low. Initializes internal states for test purposes.

TSTEN. Active High. Allows REFCLK to drive the divider phase adjust circuitry, after the first divide-by-two stage. Therefore, REFCLK is divided by two in the divide-by-four mode, and divided by four in the divide-by-eight mode, and used to directly sequence the outputs.

Output Signals

FILTER. A tap between the analog output of the phase detector and the VCO input. Allows a simple external filter (a single resistor and one capacitor) to be included in the PLL.

X2FOUT. Provides a clock signal identical to the FOUT0 output in the divide-by-four mode and twice the FOUT0 frequency (maximum of 80 MHz) in the divide-by-eight mode.

FOUT0. Clock output.

FOUT1. Clock output.

FOUT2. Clock output.

FOUT3. Clock output.

HFOUT. Provides a clock signal in phase with the FOUT0 output, but at half the FOUT0 frequency in both the divide-by-four and divide-by-eight modes.

LOCK. Goes high when REFCLK and FBCLK are within 2–4 ns of each other, demonstrating that the PLL is in lock.

FOUT0A. (S4403 only.) Clock output—duplicates FOUT0.

FOUT1A. (S4403 only.) Clock output—duplicates FOUT1.

FOUT2A. (S4403 only.) Clock output—duplicates FOUT2.

FOUT3A. (S4403 only.) Clock output—duplicates FOUT3.

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Table 3. Output Select Matrix

Configuration Number	Select Pins		Output Fed to FBCLK	Output Phase Relationships					÷4	÷8
	PHSEL1	PHSEL0		FOUT0	FOUT1	FOUT2	FOUT3	HFOUT	X2FOUT	
1	0	0	FOUT0–FOUT3	0	0	0	0	0/2	0	2(0)
2	0	0	HFOUT	2(0)	2(0)	2(0)	2(0)	0	2(0)	4(0)
3	0	0	X2FOUT (÷8)	0/2	0/2	0/2	0/2	0/4		0
4	0	1	FOUT0	0	Q	2Q	3Q	0/2	0	2(0)
5	0	1	FOUT1	–Q	0	Q	2Q	–Q/2	–Q	2(–Q)
6	0	1	FOUT2	–2Q	–Q	0	Q	–2Q/2	–2Q	2(–2Q)
7	0	1	FOUT3	–3Q	–2Q	–Q	0	–3Q/2	–3Q	2(–3Q)
8	0	1	HFOUT	2(0)	2(Q)	2(2Q)	2(3Q)	0	2(0)	4(0)
9	0	1	X2FOUT (÷8)	0/2	Q/2	2Q/2	3Q/2	0/4		0
10	1	0	FOUT0	0	–t	t	Q	0/2	0	2(0)
11	1	0	FOUT1	t	0	2t	Q+t	t/2	t	2(t)
12	1	0	FOUT2	–t	–2t	0	Q–t	–t/2	–t	2(–t)
13	1	0	FOUT3	–Q	–Q–t	–Q+t	0	–Q/2	–Q	2(–Q)
14	1	0	HFOUT	2(0)	2(–t)	2(t)	2(Q)	0	2(0)	4(0)
15	1	0	X2FOUT (÷8)	0/2	–t/2	t/2	Q/2	0/4		0
16	1	1	FOUT0	0	t	2t	3t	0/2	0	2(0)
17	1	1	FOUT1	–t	0	t	2t	–t/2	–t	2(–t)
18	1	1	FOUT2	–2t	–t	0	t	–2t/2	–2t	2(–2t)
19	1	1	FOUT3	–3t	–2t	–t	0	–3t/2	–3t	2(–3t)
20	1	1	HFOUT	2(0)	2(t)	2(2t)	2(3t)	0	2(0)	4(0)
21	1	1	X2FOUT (÷8)	0/2	t/2	2t/2	3t/2	0/4		0

Notes:
1. “0” implies the output is aligned with REFCLK.
2. “t” implies the output lags REFCLK by a minimum phase delay.
3. “Q” implies the output lags REFCLK by 90° of phase
4. “–t” implies the output leads REFCLK by a minimum phase delay.
5. “–Q” implies the output leads REFCLK by 90° of phase.
6. “2( )” implies the output is at twice the frequency of REFCLK.

Legend

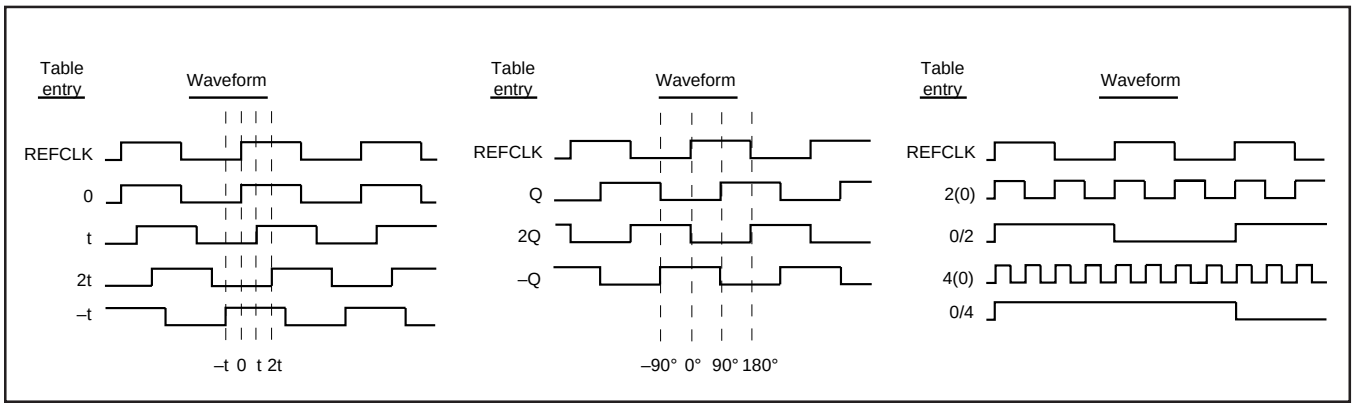
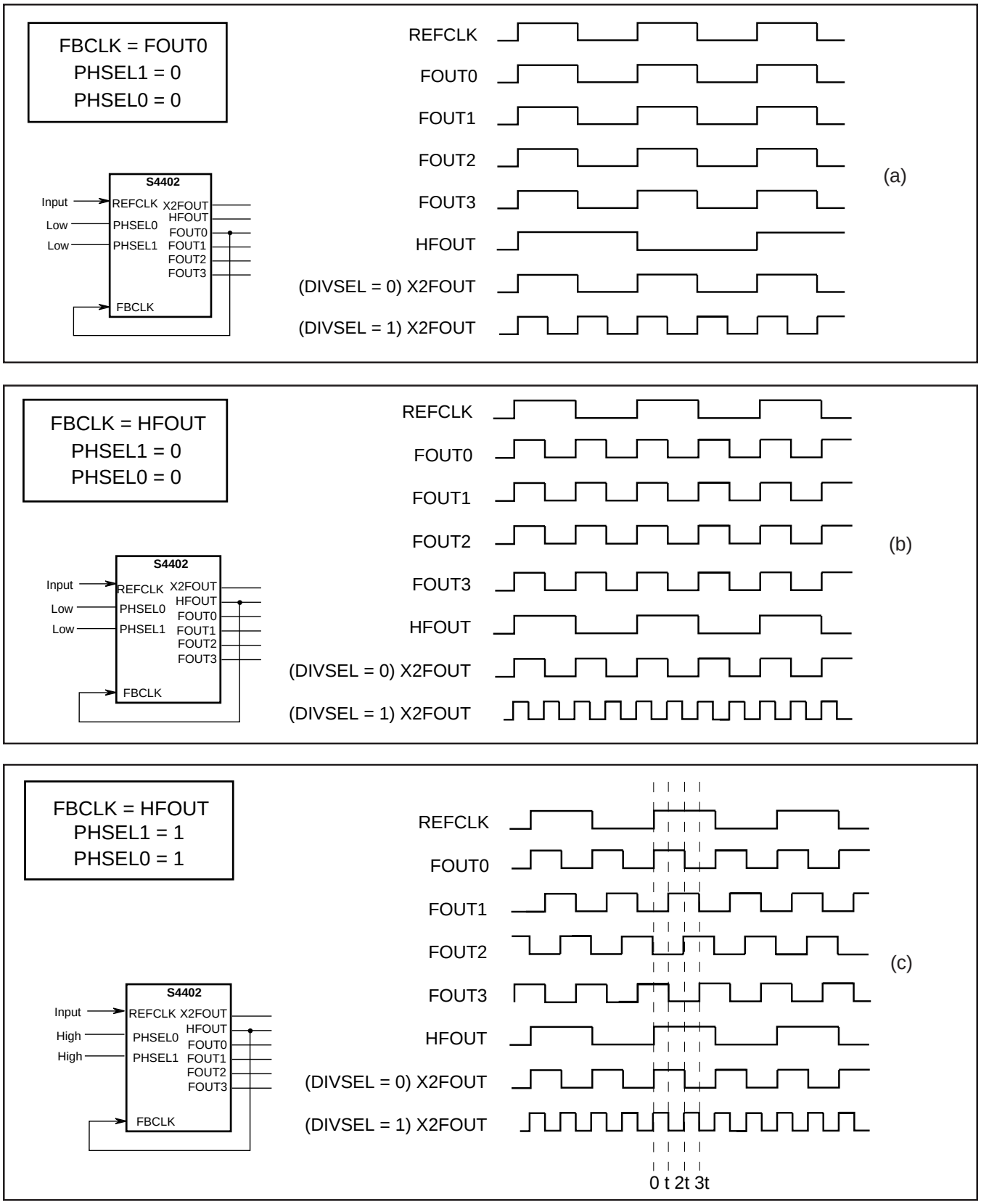


Figure 4. Configuration Examples



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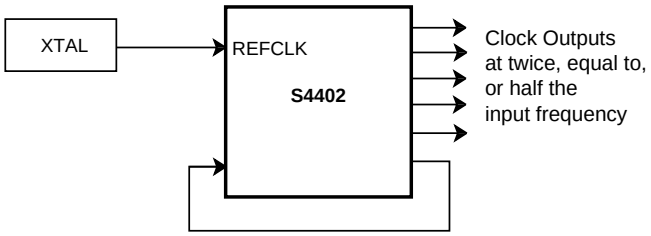
TYPICAL APPLICATIONS

The S4402/S4403 chips are designed to meet a large variety of system clocking requirements. Several typical applications are provided below.

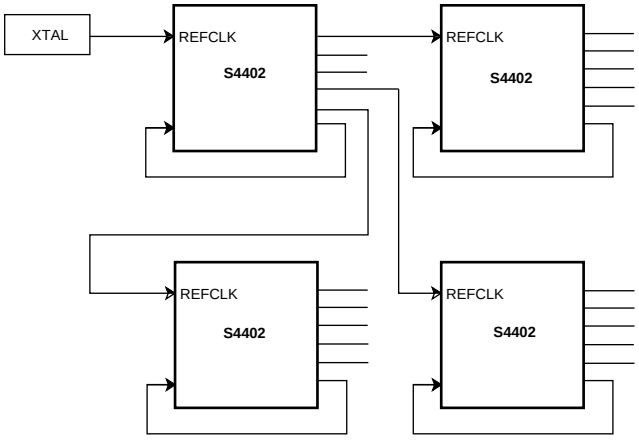
Application 1. High-Frequency, Low-Skew Clock Generation

One of the most basic capabilities of the S4402/S4403 devices is generating multiple phase-aligned low-skew clocks at various multiples of the input clock frequency. For example, in a multiple-board system a half-frequency clock can be generated for use across the backplane, where it is simpler to route a low-speed signal. This signal can then be doubled on the boards, and synchronization will be maintained.



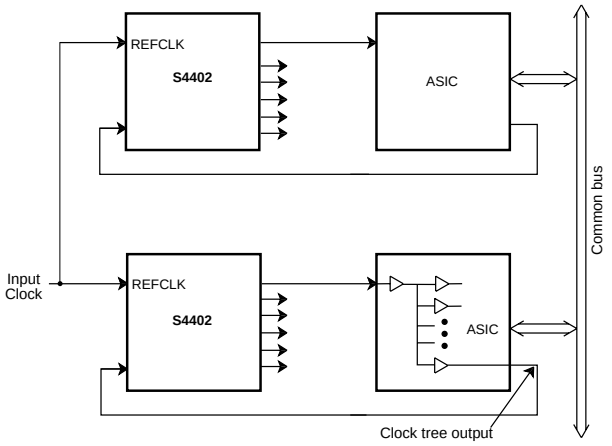
Application 2. Low-Skew Clock Distribution

One common problem in clocking high-speed systems is that of distributing several copies of a system clock while maintaining low skew throughout the system. The S4402/S4403 devices guarantee low skew among all the clocks in the system, as they have effectively zero delay between their input and output signals, with an output skew of less than 400 ps. The user can also adjust the phases of the outputs in increments as small as 3.125 ns, for load and trace length matching.



Application 3. Delay Compensation

Since the relative edges of the S4402/S4403 outputs can be precisely controlled, these chips can be used to compensate for different delays due to trace lengths or to internal chip delays, simplifying board layout and bus timing. In the example shown, the two ASICs have a difference of several nanoseconds in their propagation delays. The S4402s ensure that the output signals are aligned, so that the data valid uncertainty on the common bus is minimized.



ABSOLUTE MAXIMUM RATINGS

	Commercial
TTL Supply Voltage VCC (VEE = 0)	7.0 V
TTL Input Voltage (VEE = 0)	5.5 V
Operating Temperature	0°C to 70°C ambient
Operating Junction Temperature TJ	+ 130°C
Storage Temperature	–65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Commercial			Units
	Min	Nom	Max	
TTL Supply Voltage (VCC)	4.75	5.0	5.25	V
Operating Temperature	0 (ambient)	—	70 (ambient)	°C
Junction Temperature	—	—	130	°C

DC CHARACTERISTICS

Symbol	Parameter	DC Test Conditions		Min	Typ[1]	Max	Units
V_{IH}[2]	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs		2.0			V
V_{IL}[2]	Input LOW voltage	Guaranteed input LOW voltage for all inputs				0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = -18mA			-0.8	-1.2	V
V_{OH}	Output HIGH voltage	V_{CC} = Min	I_{OH} = -12mA[3] (COM)	2.4			V
			I_{OH} = -24mA[3] (COM)	2.0			V
V_{OL}	Output LOW voltage	V_{CC} = Min	I_{OL} = 24mA[3] (COM)			0.5	V
I_{IH}	Input HIGH current	V_{CC} = Min, V_{IN} = 2.4V	OUTEN2			-200	µA
			Other			50	µA
I_I	Input HIGH current at max	V_{CC} = Max, V_{IN} = V_{CC}				1.0	mA
I_{IL}	Input LOW current	V_{CC} = Min, V_{IN} = 0.5V	OUTEN2			-500	µA
			Other			-50	µA
I_{OS}[4]	Output short circuit current	V_{CC} = Max, V_{OUT} = 0V		-25		-100	mA
I_{CC}	Static	V_{CC} = Max	COM			70	mA
I_{CC}	Total I_{CC} (Dynamic and Static)	V_{LOAD} = 25pF at 50 MHz	COM			190	mA

1. Typical limits are at 25°C, V_{CC} = 5.0V.
2. These input levels should only be tested in a static, noise-free environment.
3. I_{OH}/I_{OL} values indicated are for DC test correlation. Actual dynamic currents are significantly higher and are optimized to balance rise and fall times.
4. Maximum test duration is one second.

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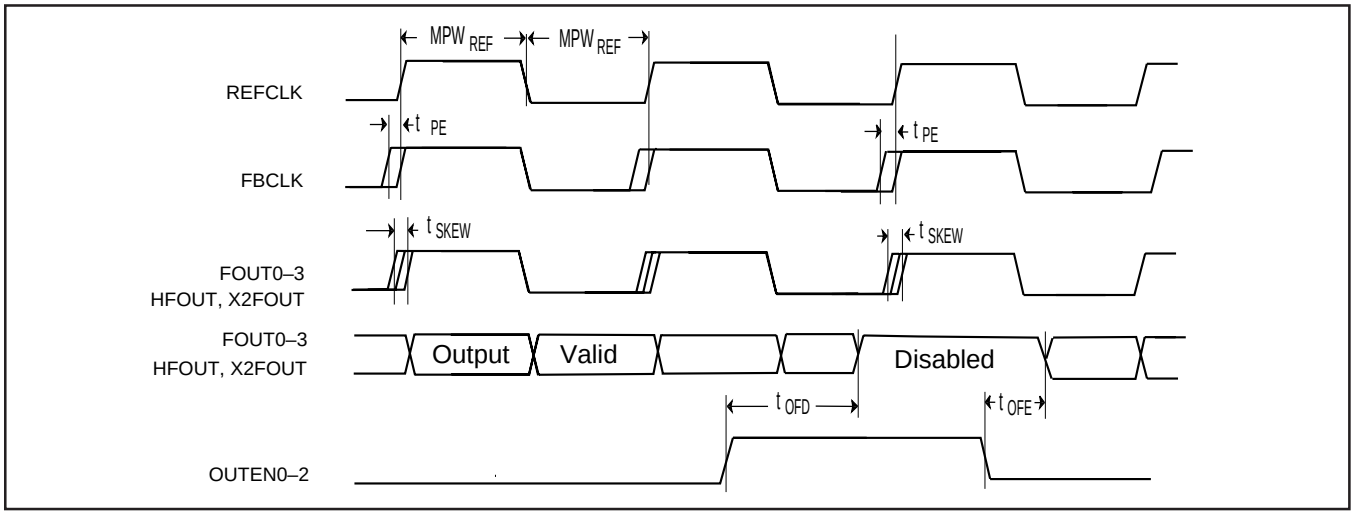
Table 4. AC Specifications

Symbol	Description	S4402/3-66		S4402/3-80		Units
		Min	Max	Min	Max	
f_{VCO}	VCO Frequency	160	266	160	320	MHz
f_{REF}	REFCLK Frequency	10	66	10	80	MHz
MPW_{REF}	REFCLK Minimum Pulse Width	7.0		6.0		ns
t_{PE}	Phase Error between REFCLK and FBCLK	-1.0	0	-1.0	0	ns
t_{PED}	Phase Error Difference from Part to Part[1]	0	750	0	750	ps
t_{SKEW}	Output Skew[2]	0	400	0	400	ps
t_{DC}	Output Duty Cycle[3]	45	55	45	55	%
f_{FOUT}	FOUT Frequency[4]	20	66	20	80	MHz
f_{HFOUT}	HFOUT Frequency[4]	10	33	10	40	MHz
f_{2XFOUT}	2XFOUT Frequency[4]	40	66	40	80	MHz
t_{PS}	Nominal Phase Shift Increment	3.75	6.25	3.125	6.25	ns
t_{PSJ}	Phase Shift Variation[5]	-250	+250	-250	+250	ps
t_{OFD}	Tpd OUTEN0–2 to FOUTs, Disable	2	7	2	7	ns
t_{OFE}	Tpd OUTEN0–2 to FOUTs, Enable	2	7	2	7	ns
t_{IRF}	Input Rise/Fall Time	1	3	1	3	ns
t_{ORF}	FOUT Rise/Fall Time[6]	0.5	1.5	0.5	1.5	ns
t_{LOCK}	Loop Acquisition Time[7]		5		5	ms
t_j	Clock Stability[8]		500		500	ps

1. Difference in phase error between two parts at the same voltage, temperature and frequency.
2. Output skew guaranteed for equal loading at each output.
3. Outputs loaded with 35pF, measured at 1.5V.
4. C_{LOAD} = 35 pF.
5. All phase shift increments and variation are measured relative to FOUT0 at 1.5V.
6. With 35 pF output loading (0.8 V to 2.0 V transition).
7. Depends on loop filter chosen. (Number given is for example filter.)
8. Clock period jitter with all FOUT outputs operating at 66 MHz and loaded with 25pF using loop filter shown. Parameter guaranteed, but not tested.

Figure 5. Timing Waveforms



BOARD LAYOUT CONSIDERATIONS

• The S4402/S4403 chips are sensitive to noise on the Analog +5 V and Filter pins. Care should be taken during board layout for optimum results.

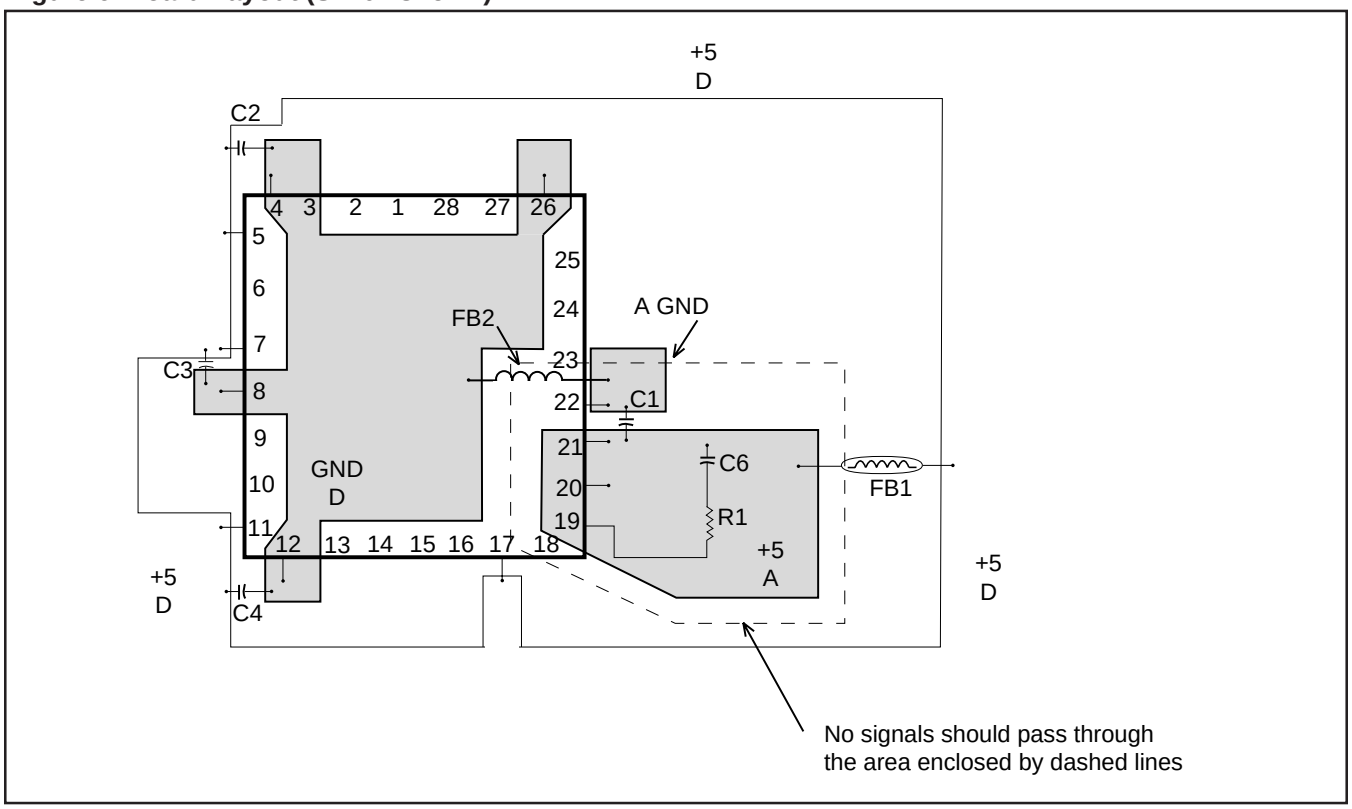
• All decoupling capacitors (C1–C4 = 0.1 µF) should be bypassed between VCC and GND, and placed as close to the chip as possible (preferably using ceramic chip caps) and placed on top of board between S4402/S4403 and the power and ground plane connections.

• No dynamic signal lines should pass through or beneath the filter circuitry area (enclosed by dashed lines in Figure 6) to avoid the possibility of noise due to crosstalk.

• The analog VCC supply can be a filtered digital VCC supply as shown below. The ferrite beads or inductors, FB1 and FB2, should be placed within three inches of the chip.

• The analog VCC plane should be separated from the digital VCC and ground planes by at least 1/8 inch.

Figure 6. Board Layout (S4402 shown)



Component	Description
C1–C4	0.1 µF ceramic capacitor
C6	0.1 µF ceramic capacitor
R1	1.5 K 10% resistor
FB1,FB2	Ferrite bead or inductor

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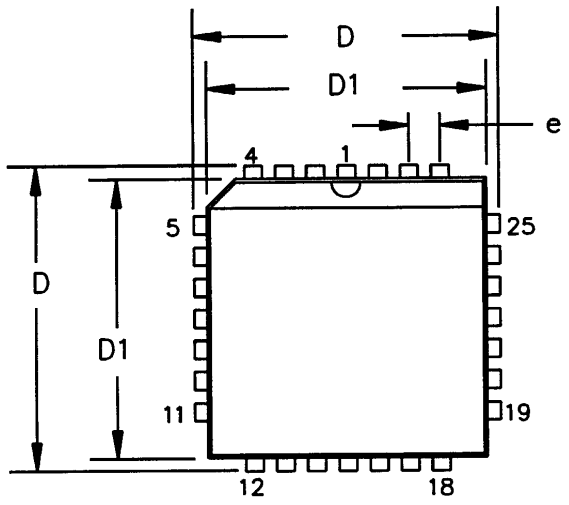
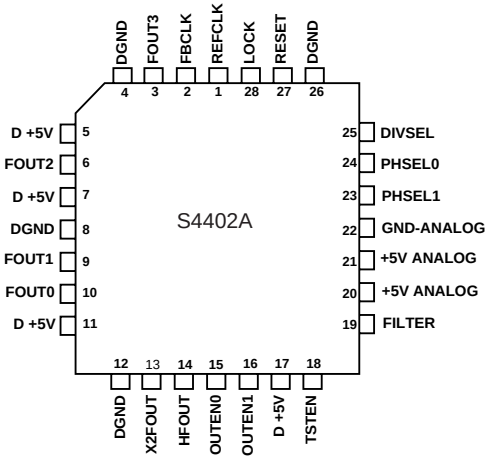
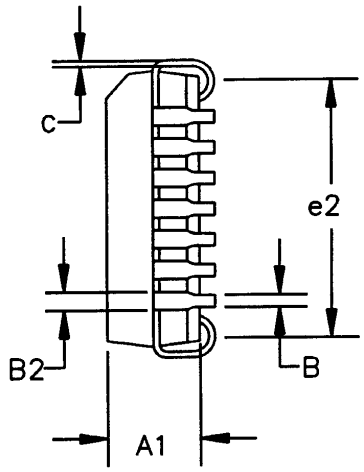
Figure 7. S4402 28 PLCC Package and Pinout







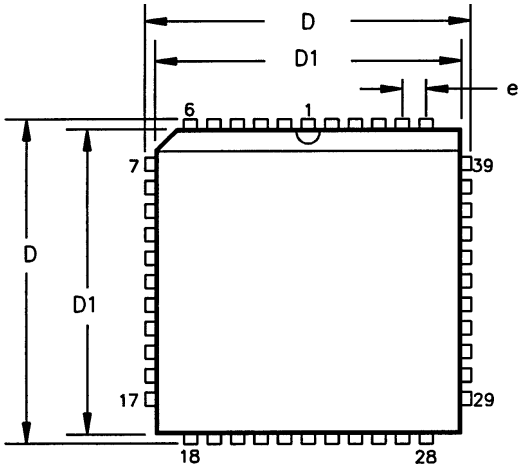
SYM	MIN	MAX
A1	.147	.157
B	.013	.021
B2	.026	.032
C	.007	.013
D	.487	.497
D1	.444	.459
e	.048	.052
e2	.410	.430

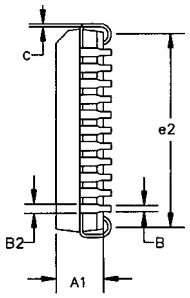
All dimensions nominal in inches.

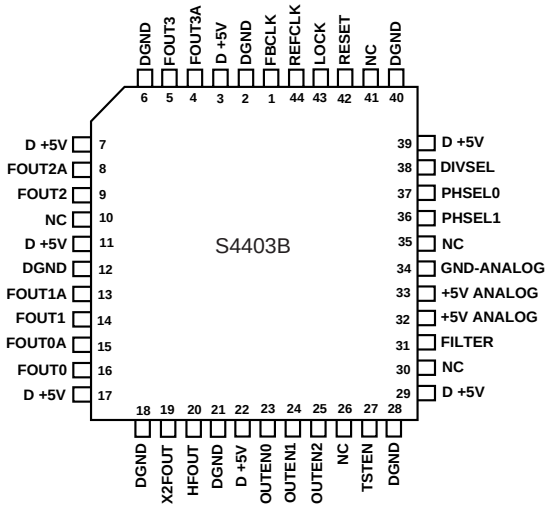
28 PLCC Thermal Resistance

Still Air	100 Linear Ft./Min	200 Linear Ft./Min
60˚C/Watt	50˚C/Watt	45˚C/Watt

Figure 8. S4403 44 PLCC Package and Pinout







SYM	MIN	MAX
A1	.147	.157
B	.013	.021
B2	.026	.032
C	.007	.013
D	.687	.697
D1	.644	.659
e	.048	.052
e2	.610	.630

All dimensions nominal in inches.

Ordering Information

AMCC clock driver products are available in several output skew and shipping configurations. The order number is formed by a combination of:

- **Device Number**
- **Package Type**
- **Speed Option**
- **Optional Shipping Configuration**

S4402/03 **A** **– 66** **/TD**

Optional Shipping Configuration
Blank = tube
/D = dry pack
/TD = tape, reel and dry pack

Speed Option
– 66 = 66 MHz
– 80 = 80 MHz

Package Option
A = 28-pin PLCC (S4402)
B = 44-pin PLCC (S4403)

Device Number
S4402
S4403

Example: S4402A-66/D
28-pin PLCC package, shipped dry packed in the standard tube.

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