

SN54ALS03B, SN74ALS03B
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS
WITH OPEN-COLLECTOR OUTPUTS

SDAS013B – MARCH 1984 – REVISED DECEMBER 1994

- **Package Options Include Plastic Small-Outline (D) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

description

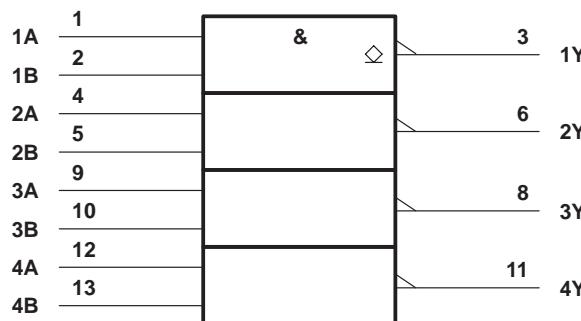
These devices contain four independent 2-input positive-NAND buffers. They perform the Boolean functions $Y = A \bullet \bar{B}$ or $Y = \bar{A} + \bar{B}$ in positive logic. The open-collector outputs require pullup resistors to perform correctly. These outputs may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate high V_{OH} levels.

The SN54ALS03B is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS03B is characterized for operation from 0°C to 70°C .

FUNCTION TABLE
 (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

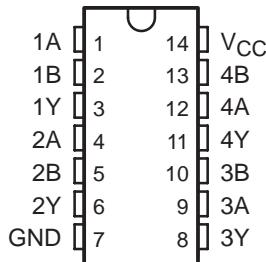
logic symbol†



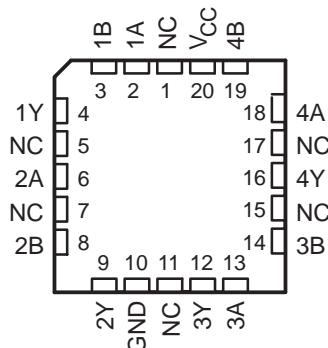
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, and N packages.

SN54ALS03B . . . J PACKAGE
SN74ALS03B . . . D OR N PACKAGE
 (TOP VIEW)

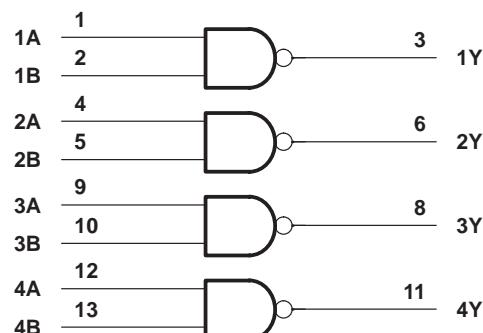


SN54ALS03B . . . FK PACKAGE
 (TOP VIEW)



NC – No internal connection

logic diagram (positive logic)



SN54ALS03B, SN74ALS03B QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Off-state output voltage	7 V
Operating free-air temperature range, T_A :	
SN54ALS03B	-55°C to 125°C
SN74ALS03B	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS03B			SN74ALS03B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2		2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
V _{OH}	High-level output voltage			5.5			5.5	V
I _{OL}	Low-level output current			4			8	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS03B			SN74ALS03B			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OL}	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4
		$I_{OL} = 8 \text{ mA}$					0.35	0.5
I_I	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$			-0.1			-0.1	mA
I_{OH}	$V_{CC} = 4.5 \text{ V}$, $V_{OH} = 5.5 \text{ V}$			0.1			0.1	mA
I_{CCH}	$V_{CC} = 5.5 \text{ V}$, $V_I = 0$		0.43	0.85		0.43	0.85	mA
I_{CCI}	$V_{CC} = 5.5 \text{ V}$, $V_I = 4.5 \text{ V}$		1.62	3		1.62	4	mA

[‡]All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

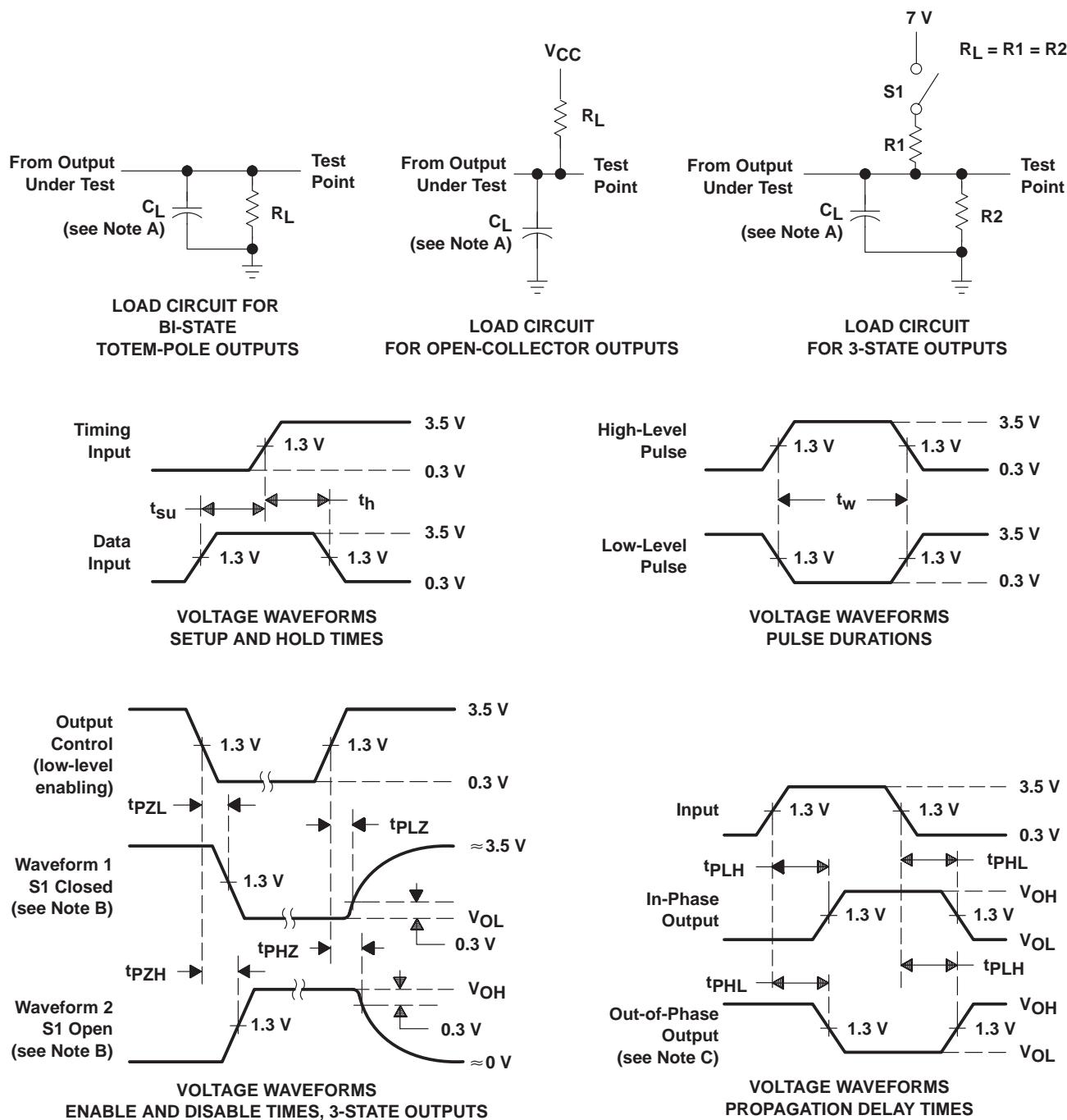
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 2 kΩ, T _A = MIN to MAX§				UNIT	
			SN54ALS03B		SN74ALS03B			
			MIN	MAX	MIN	MAX		
t _{PLH}	A or B	Y	20	59	20	50	ns	
t _{PHI}			3	23	3	13		

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALS03BD	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	0 to 70	ALS03B
SN74ALS03BDR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS03B
SN74ALS03BDR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS03B
SN74ALS03BN	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS03BN
SN74ALS03BN.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS03BN

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

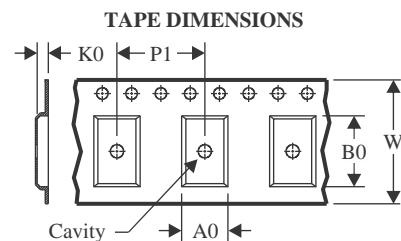
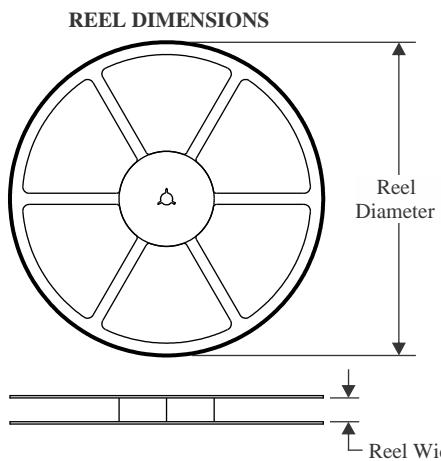
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

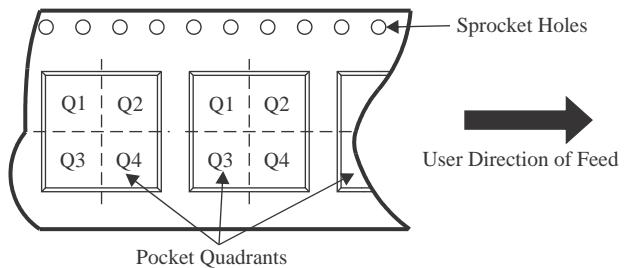
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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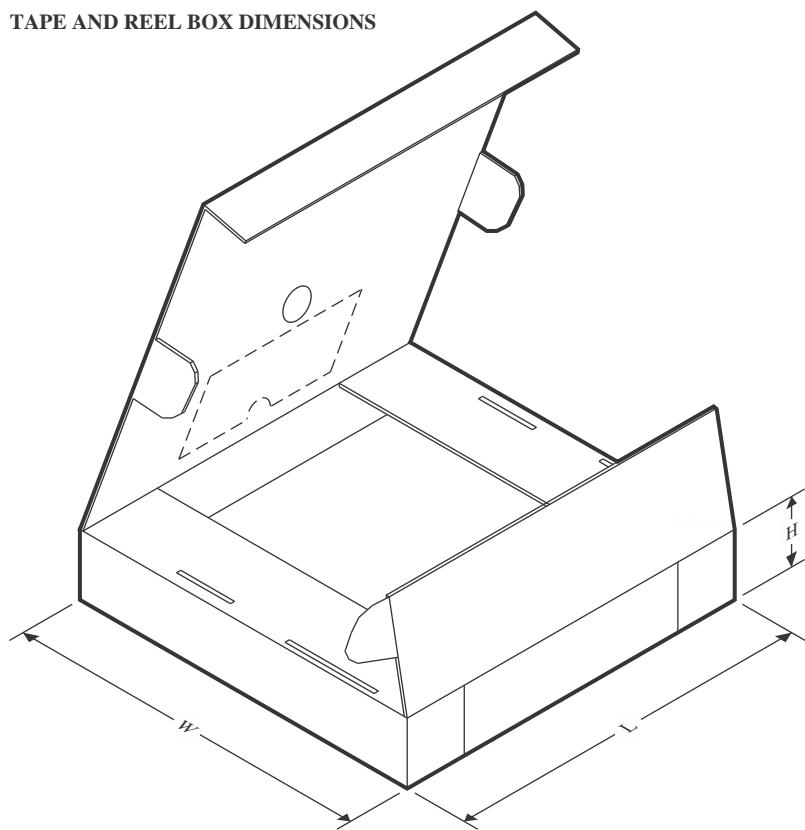
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


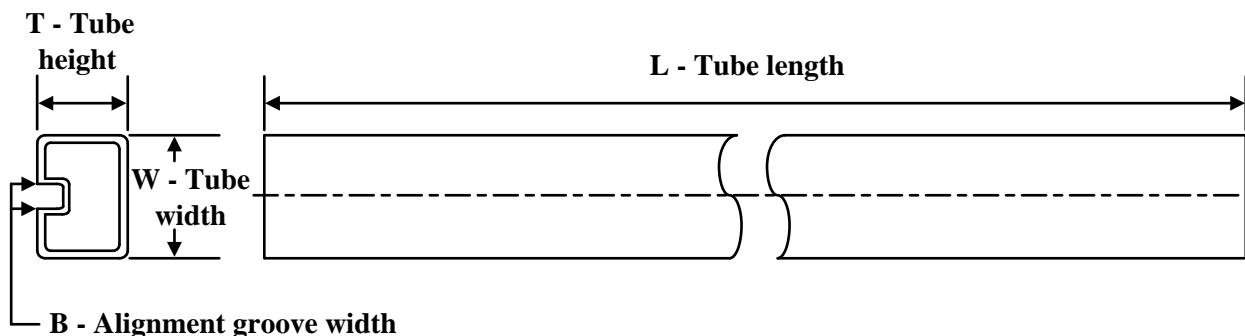
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS03BDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS03BDR	SOIC	D	14	2500	353.0	353.0	32.0

TUBE


*All dimensions are nominal

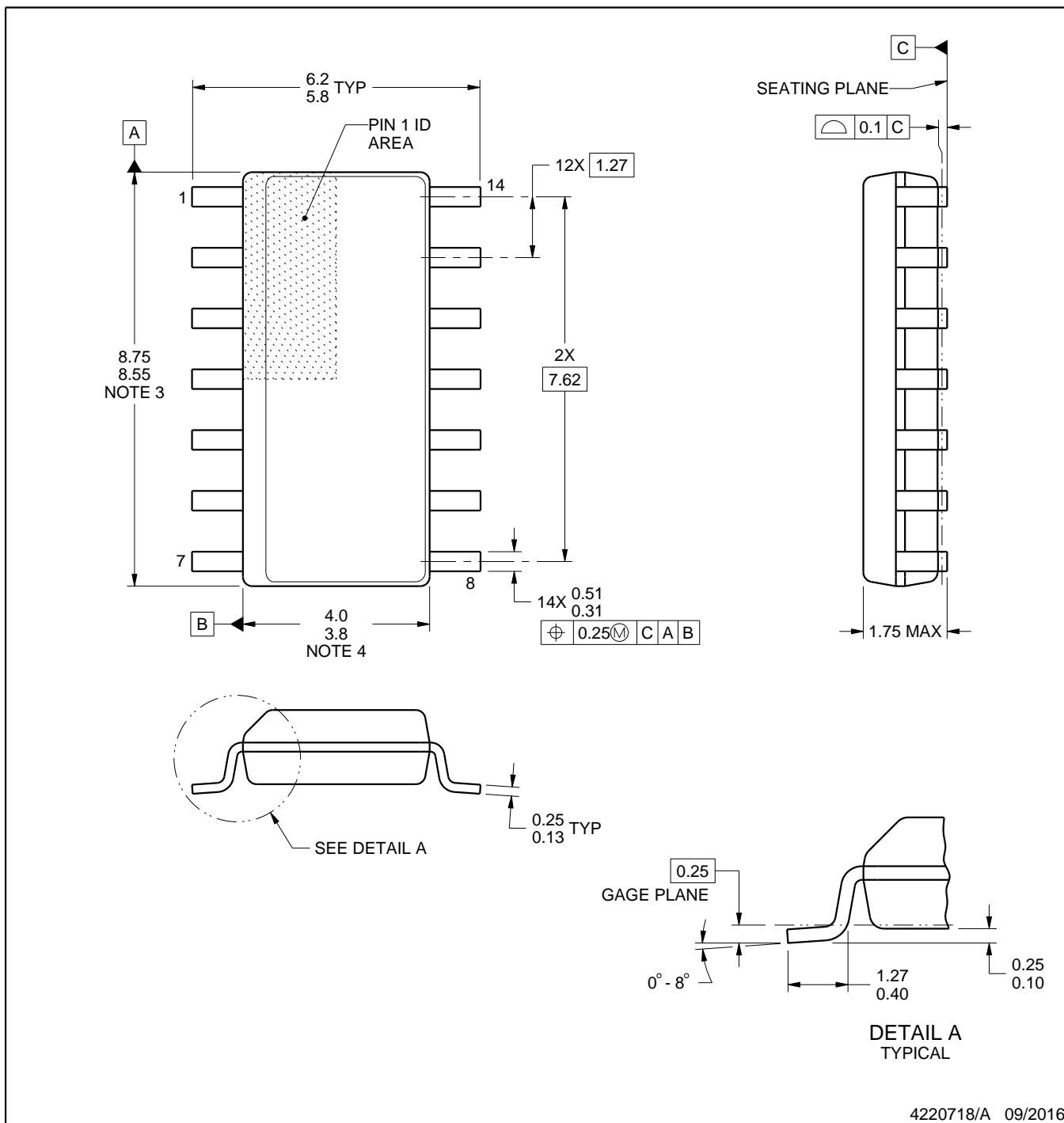
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
SN74ALS03BN	N	PDIP	14	25	506	13.97	11230	4.32
SN74ALS03BN	N	PDIP	14	25	506	13.97	11230	4.32
SN74ALS03BN.A	N	PDIP	14	25	506	13.97	11230	4.32
SN74ALS03BN.A	N	PDIP	14	25	506	13.97	11230	4.32

PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

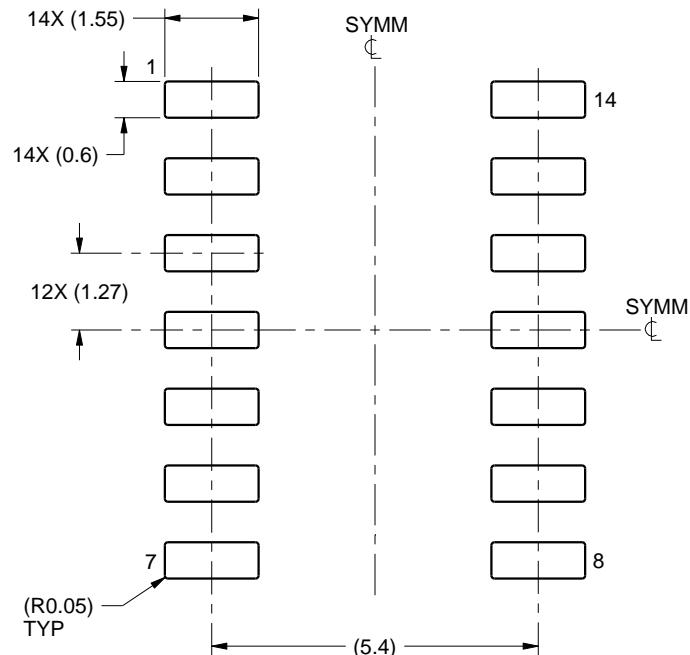
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

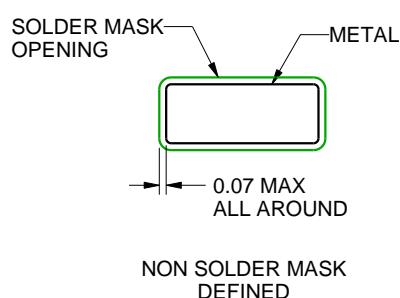
D0014A

SOIC - 1.75 mm max height

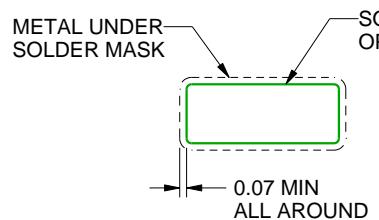
SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

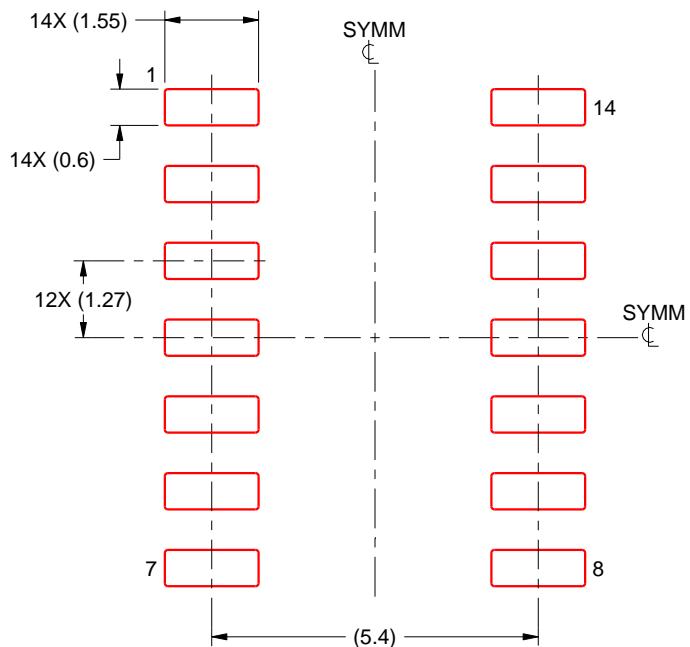
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



**SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X**

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



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