

LM161/LM361 High Speed Differential Comparators

Check for Samples: LM161, LM361

FEATURES

- Independent strobes
- Ensured high speed: 20 ns max
- · Tight delay matching on both outputs
- Complementary TTL outputs
- Operates from op amp supplies: ±15V
- Low speed variation with overdrive variation
- Low input offset voltage
- Versatile supply voltage range

DESCRIPTION

The LM161/LM361 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the SE529/NE529 for which it is a pin-for-pin replacement. The device has been optimized for greater speed performance and lower input offset voltage. Typically delay varies only 3 ns for over-drive variations of 5 mV to 500 mV. It may be operated from op amp supplies (±15V).

Complementary outputs having maximum skew are provided. Applications involve high speed analog to digital converters and zero-crossing detectors in disk file systems.

CONNECTION DIAGRAMS

SOIC or PDIP Package

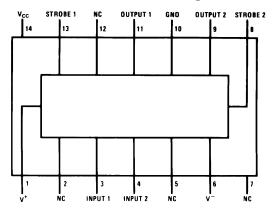


Figure 1. Top View Package Numbers D0014A, NFF0014A

TO-100 Package

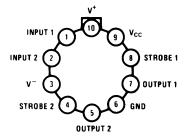


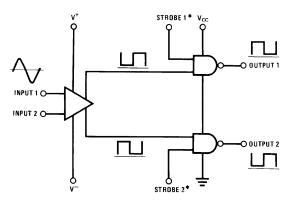
Figure 2. Package Number LME0010C

ATA.

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LOGIC DIAGRAM



*Output is low when current is drawn from strobe pin.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

+16V
-16V
+7V
+7V
±5V
±6V
600 mW
−65°C to +150°C
T _{MIN} T _{MAX}
−55°C to +125°C
−25°C to +85°C
0°C to +70°C
260°C
0.3V

⁽¹⁾ The device may be damaged by use beyond the maximum ratings.

Operating Conditions

			Min	Тур	Max
Complex Valtage V/+	LM161		5V		15V
Supply Voltage V ⁺	LM361		5V		15V
Cupply Valtage V	LM161		-6V		-15V
Supply Voltage V ⁻	LM361		-6V		-15V
Complex Valtages V	LM161		4.5V	5V	5.5V
Supply Voltage V _{CC}	LM361		4.75V	5V	5.25V
ESD Tolerance (1)	·				1600V
	PDIP Package	Soldering (10 seconds) ⁽²⁾			260°C
Soldering Information (2)	SOIC Package	Vapor Phase (60 seconds)			215°C
		Infrared (15 seconds)			220°C

⁽¹⁾ Human body model, 1.5 k Ω in series with 100 pF.

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⁽²⁾ See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.



Electrical Characteristics (1)(2)(1)

 $(V^{+} = +10V, V_{CC} = +5V, V^{-} = -10V, T_{MIN} \le T_{A} \le T_{MAX}, \text{ unless noted})$

Parameter	Conditions	Limits								
			LM161			LM361				
		Min	Min Typ		Min	Тур	Max			
Input Offset Voltage			1	3		1	5	mV		
Input Bias Current	T _25°C		5			10		μΑ		
input bias Current	T _A =25°C			20			30	μΑ		
Input Offset Current	T _A =25°C		2			2		μΑ		
input Onset Current	1 _A =25 C			3			5	μΑ		
Voltage Gain	T _A =25°C		3			3		V/mV		
Input Resistance	T _A =25°C, f=1 kHz		20			20		kΩ		
Logical "1" Output Voltage	V_{CC} =4.75V, I_{SOURCE} =-0.5 mA	2.4	3.3		2.4	3.3		V		
Logical "0" Output Voltage	V_{CC} =4.75V, I_{SINK} =6.4 mA			0.4			0.4	V		
Strobe Input "1" Current (Output Enabled)	V _{CC} =5.25V, V _{STROBE} =2.4V			200			200	μA		
trobe Input "0" Current V _{CC} =5.25V, Dutput Disabled) V _{STROBE} =0.4V				-1.6			-1.6	mA		
Strobe Input "0" Voltage	V _{CC} =4.75V			8.0			0.8	V		
Strobe Input "1" Voltage	V _{CC} =4.75V	2			2			V		
Output Short Circuit Current	V _{CC} =5.25V, V _{OUT} =0V	-18		-55	-18		-55	mA		
Supply Current I ⁺	V ⁺ =10V, V ⁻ =−10V, V _{CC} =5.25V, -55°C≤T _A ≤125°C			4.5				mA		
Supply Current I ⁺	V ⁺ =10V, V ⁻ =−10V, V _{CC} =5.25V, 0°C≤T _A ≤70°C						5	mA		
Supply Current I ⁻	V ⁺ =10V, V ⁻ =−10V, V _{CC} =5.25V, -55°C≤T _A ≤125°C			10				mA		
Supply Current I ⁻	V ⁺ =10V, V ⁻ =−10V,V _{CC} =5.25V, 0°C≤T _A ≤70°C						10	mA		
Supply Current I _{CC}	$V^{+}=10V, V^{-}=-10V, V_{CC}=5.25V, -55^{\circ}C \le T_{A} \le 125^{\circ}C$			18				mA		
upply Current I_{CC} $V^{+}=10V, V^{-}=-10V, V_{CC}=5.25V, 0^{\circ}C \leq T_{A} \leq 70^{\circ}C$							20	mA		
Transient Response	V _{IN} = 50 mV overdrive ⁽³⁾									
Propagation Delay Time $(t_{pd(0)})$	T _A =25°C		14	20		14	20	ns		
Propagation Delay Time (t _{pd(1)})	T _A =25°C		14	20		14	20	ns		
Delay Between Output A and B	T _A =25°C		2	5		2	5	ns		
Strobe Delay Time (t _{pd(0)})	T _A =25°C		8			8		ns		
Strobe Delay Time (t _{pd(1)})	T _A =25°C		8			8		ns		

(1) Typical thermal impedances are as follows:

H Package J Package N Package 165°C/W (Still Air) 112°C/W 105°C/W 67°C/W (400 LF/Min Air Flow) $\theta_{\rm jC}$

Refer to RETS161X for LM161H and LM161J military specifications.

Measurements using AC Test circuit, Fanout = 1. The devices are faster at low supply voltages.

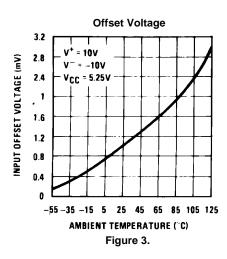
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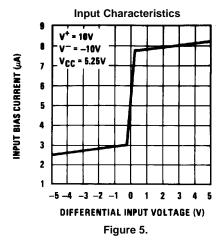
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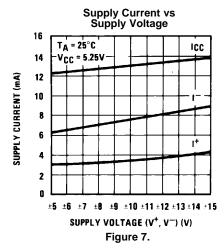


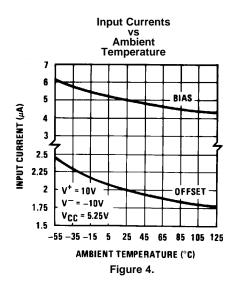
Typical Performance Characteristics

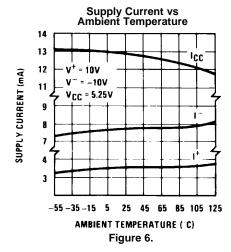
Product Folder Links: LM161 LM361

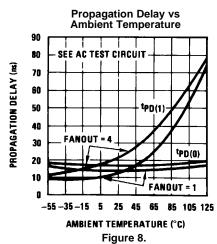






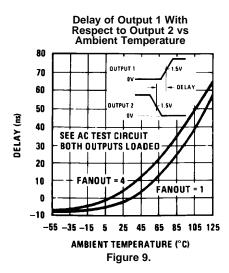


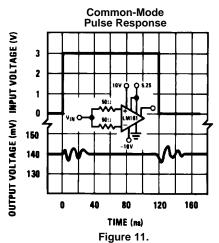


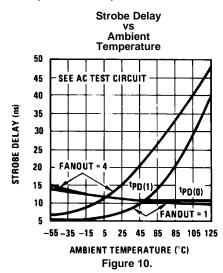


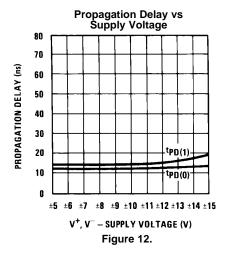


Typical Performance Characteristics (continued)



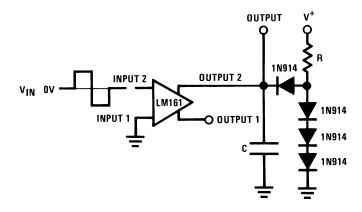








AC TEST CIRCUIT

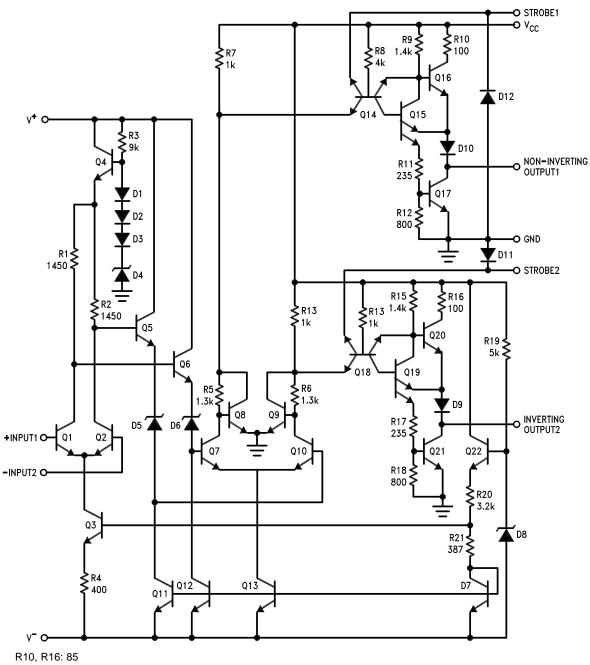


$V_{IN} = \pm 50 \text{ mV}$	FANOUT = 1	FANOUT = 4	V ⁻ = −10V	C=15 pF	C = 30 pF
$V^{+} = +10V$	R = 2.4k	$R = 680\Omega$	$V_{CC} = 5.25V$		



SCHEMATIC DIAGRAM

LM161



R11, R17: 205

SNOSBJ5C-MAY 1999-REVISED MARCH 2013



REVISION HISTORY

Cł	hanges from Revision B (March 2013) to Revision C	Page
•	Changed layout of National Data Sheet to TI format	7





7-Oct-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type	_	Pins	_		Lead/Ball Finish		Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)		(3)		(4/5)	
LM361H	ACTIVE	TO-100	LME	10	500	TBD	Call TI	Call TI	0 to 70	LM361H	Samples
LM361H/NOPB	ACTIVE	TO-100	LME	10	500	Green (RoHS & no Sb/Br)	POST-PLATE	Level-1-NA-UNLIM	0 to 70	LM361H	Samples
LM361M	ACTIVE	SOIC	D	14	55	TBD	Call TI	Call TI	0 to 70	LM361M	Samples
LM361M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM361M	Samples
LM361MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM361M	Samples
LM361N	ACTIVE	PDIP	NFF	14	25	TBD	Call TI	Call TI	0 to 70	LM361N	Samples
LM361N/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LM361N	Samples
LM529CH	ACTIVE	TO-100	LME	10	500	TBD	Call TI	Call TI	0 to 70	LM361H	Samples
LM529CN	ACTIVE	PDIP	NFF	14	25	TBD	Call TI	Call TI	0 to 70	LM361N	Samples
NE529A	ACTIVE	PDIP	NFF	14	25	TBD	Call TI	Call TI	0 to 70	LM361N	Samples
NE529K	ACTIVE	TO-100	LME	10	500	TBD	Call TI	Call TI	0 to 70	LM361H	Samples
SE529K	ACTIVE	TO-100	LME	10	500	TBD	Call TI	Call TI	0 to 70	LM361H	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

7-Oct-2013

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

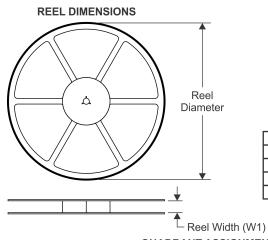
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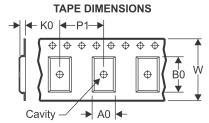
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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

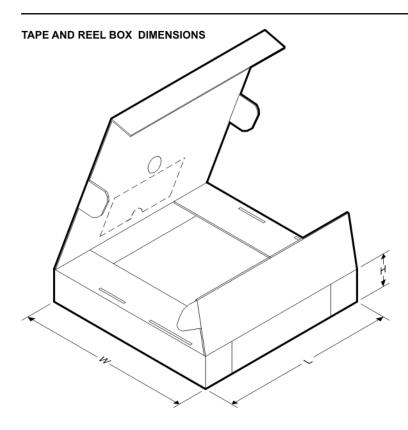
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM361MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

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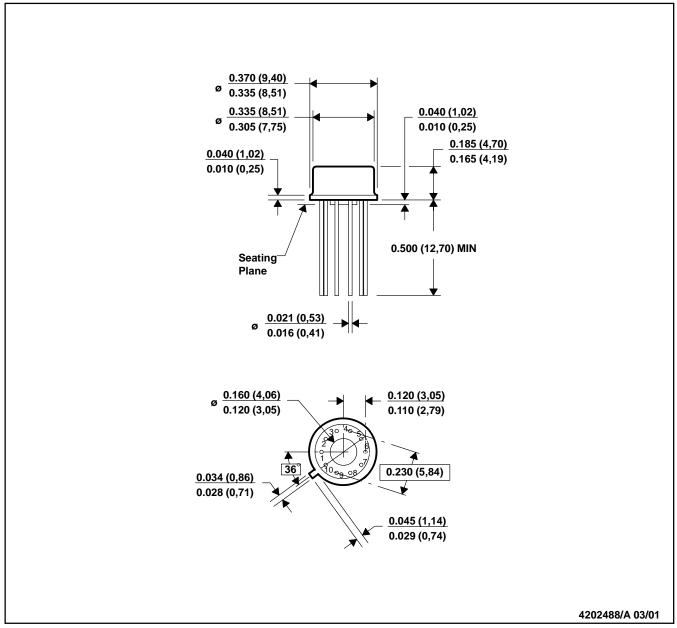


*All dimensions are nominal

ĺ	Device	Device Package Type		Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
	LM361MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0	

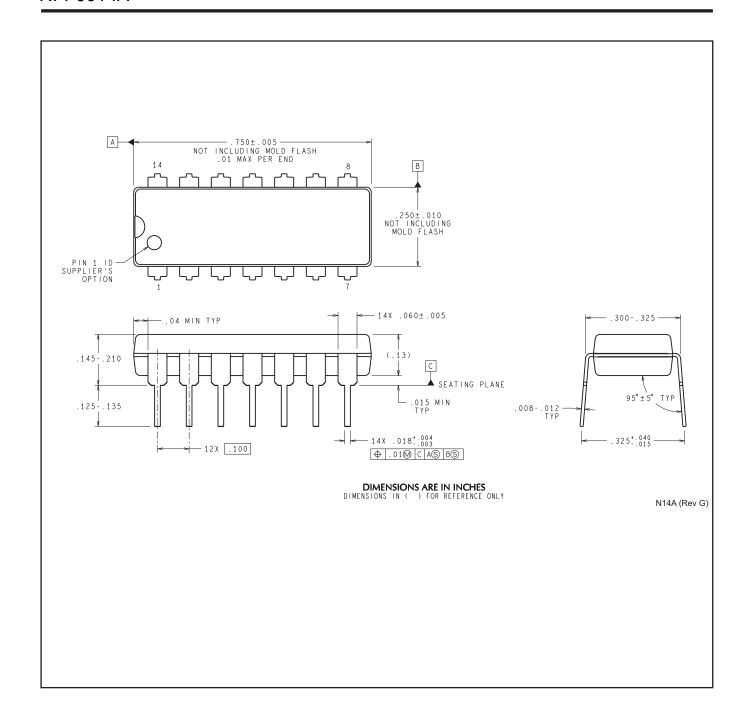
LME (O-MBCY-W10)

METAL CYLINDRICAL PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
 - D. Pin numbers shown for reference only. Numbers may not be marked on package.
 - E. Falls within JEDEC MO-006/TO-100.







D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



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