CY2DP814

1:4 Clock Fanout Buffer

Features

- Low-voltage operation
- V_{DD} = 3.3 V
- 1:4 fanout
- Single input configurable for LVDS, LVPECL, or LVTTL
- Four differential pairs of LVPECL outputs
- Drives 50-ohm load
- Low input capacitance
- Less than 4 ns typical propagation delay
- 85 ps typical output-to-output skew
- Commercial temperature range
- Available in TSSOP package

Description

The Cypress CY2 series of network circuits are produced using advanced 0.35-micron CMOS technology, achieving the industry's fastest logic.

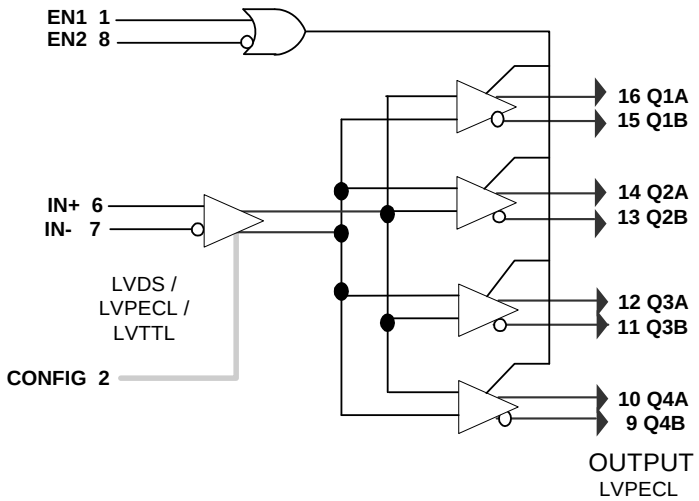
The Cypress CY2DP814 fanout buffer features a single LVDS- or a single LVPECL-compatible input and four LVPECL output pairs.

Designed for data communications clock management applications, the fanout from a single input reduces loading on the input clock.

The CY2DP814 is ideal for both level translations from single-ended to LVPECL, and/or for the distribution of LVDS-based clock signals. The Cypress CY2DP814 has configurable input between logic families. The input can be selectable for an LVPECL, LVTTL or LVDS signal, while the output drivers support LVPECL capable of driving 50-ohm lines.

For a complete list of related documentation, click here.

Logic Block Diagram



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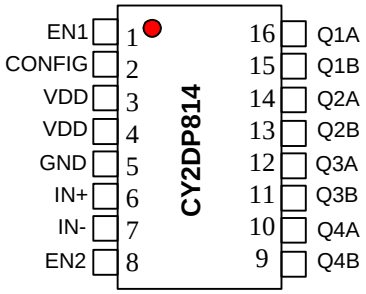
Pin Configuration

Figure 1. 16-pin TSSOP/SOIC pinout



16 pin TSSOP / SOIC

Pin Description

Pin Number	Pin Name	Pin Standard Interface	Description
6, 7	IN+, IN	Configurable	Differential input pair or single line. LVPECL default. See CONFIG below.
2	CONFIG	LVTTL/LVCMOS	Converts inputs from the default LVPECL/LVDS (logic = 0) to LVTTL/LVCMOS (logic = 1). See Figure 2 on page 4 and Figure 3 on page 4 for additional information.
1, 8	EN1, EN2	LVTTL/LVCMOS	Enable/disable logic. See Function Table below for details.
16, 15, 14, 13, 12, 11, 10, 9	Q1A, Q1B, Q2A, Q2B, Q3A, Q3B, Q4A, Q4B	LVPECL	Differential outputs.
3, 4	V_{DD}	POWER	Positive supply voltage.
5	GND	POWER	Ground.

Figure 2. LVTTL/LVCMOS

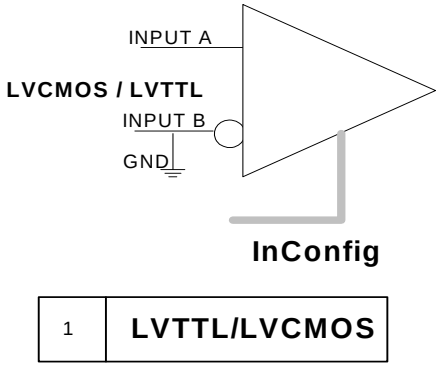
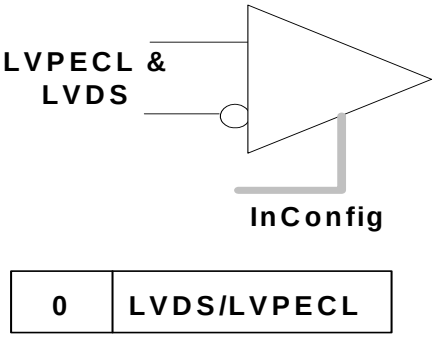


Figure 3. LVDS/LVPECL



EN1 EN2 Function Table

Enable Logic		Input		Outputs	
EN1	**EN2**	**IN+**	**IN–**	**QnA**	**QnB**
H	H	H	L	H	L
H	L	H	L	H	L
L	L	H	L	H	L
L	H	X	X	Z	Z

Input Receiver Configuration

For Differential or LVTTL/LVCMOS

CONFIG Pin 2 Binary Value	Input Receiver Family	Input Receiver Type
1	LVTTL in LVCMOS	Single ended, non-inverting, inverting, void of bias resistors.
0	LVDS	Low voltage differential signaling
	LVPECL	Low voltage pseudo (positive) emitter coupled logic

Function Control of the TTL Input Logic

Used to Accept or Invert the Input Signal

LVTTL/LVCMOS INPUT LOGIC			
Input Condition		**Input Logic**	**Output Logic Q pins**
Ground	IN– Pin 7	–	–
	IN+ Pin 6	Input	True
V_{CC}	IN– Pin 7	–	–
	IN+ Pin 6	Input	Invert
Ground	IN+ Pin 6	–	–
	IN– Pin 7	Input	Invert
V_{CC}	IN+ Pin 6	–	–
	IN– Pin 7	Input	True

Power Supply Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
I_{CCD}	Dynamic power supply current	V_{DD} = Max Input toggling 50% duty cycle, outputs loaded	–	1.5	2.0	mA/ MHz
I_C	Total power supply current	V_{DD} = Max input toggling 50% duty cycle, outputs loaded, fL= 100 MHz	–	90	100	mA

Figure 4. Differential Receiver to Driver Propagation Delay and Driver Transition Time [1, 2, 3, 4, 5]

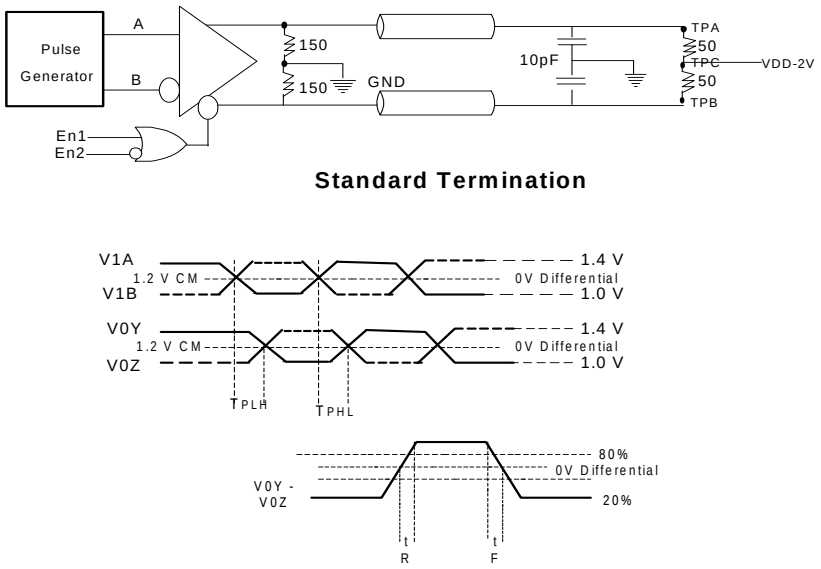
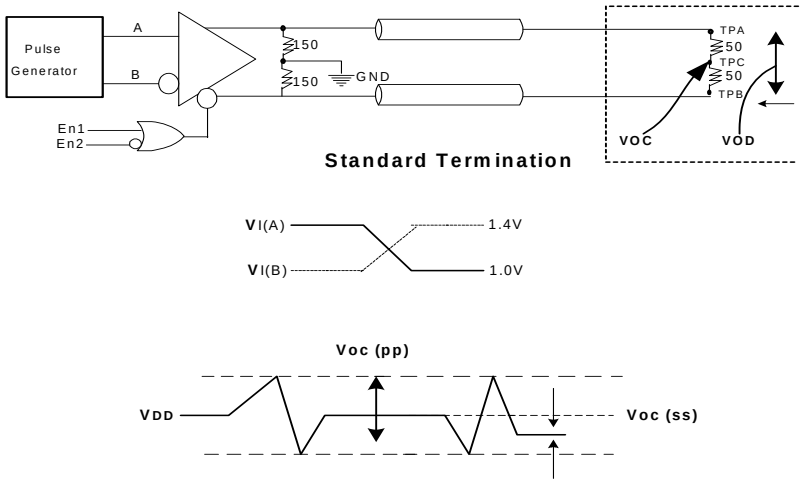


Figure 5. Test Circuit and Voltage Definitions for the Driver Common-mode Output Voltage [1, 2, 3, 5, 6]



Notes
1. RL = 50 ohm ± 1%; Zline = 50 ohm 6 = Ó.
2. CL includes instrumentation and fixture capacitance within 6 mm of the UT.
3. TPA and B are used for prop delay and rise/fall measurements. TPC is used for VOC measurements only and otherwise connected to V_{DD} – 2.
4. When measuring Tr/Tf, tpd, V_{OD} point TPC is held at V_{DD} – 2.0 V.
5. LVCMOS/LVTTL single-ended input value. Ground either input: when on the B side, non-inversion takes place. If A side is grounded, the signal becomes the complement of the input on B side. See Function Control of the TTL Input Logic on page 5.
6. V_{OC} measurement requires equipment with a 3-dB bandwidth of at least 300 MHz.

Figure 6. Test Circuit and Voltage Definitions for the Differential Output Signal [7, 8, 9, 10, 11]

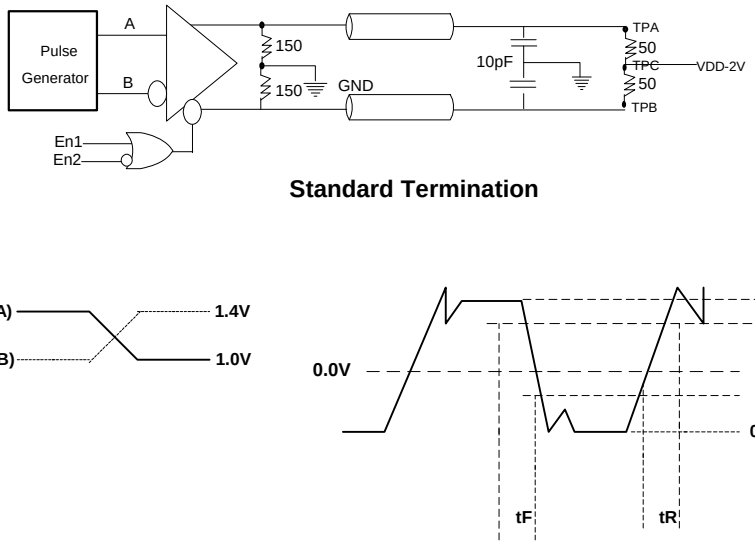
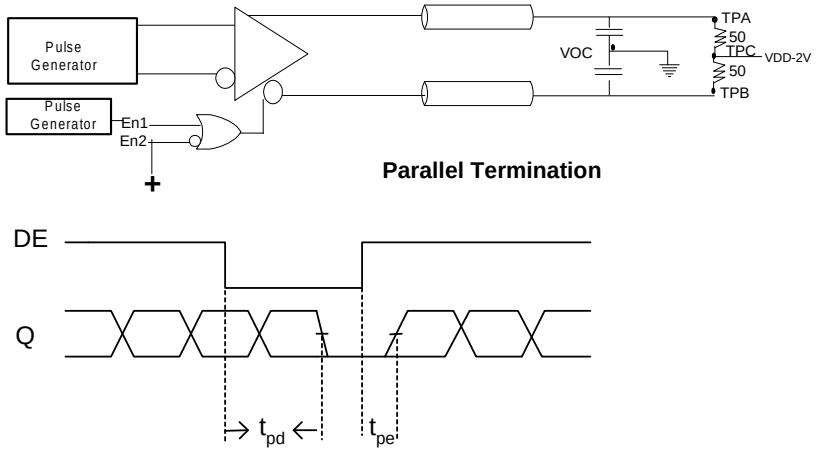


Figure 7. Test Circuit and Voltage Definitions for the Driver Common-Mode Output Voltage [7, 8, 9, 12, 13]



Notes

7. RL = 50 ohm ± 1%; Zline = 50 ohm 6 = Ó.
8. CL includes instrumentation and fixture capacitance within 6 mm of the UT.
9. TPA and B are used for prop delay and rise/fall measurements. TPC is used for VOC measurements only and otherwise connected to VDD – 2.
10. When measuring Tr/Tf, tpd, VOD point TPC is held at VDD – 2.0 V.
11. LVCMOS/LVTTL single-ended input value. Ground either input: when on the B side, non-inversion takes place. If A side is grounded, the signal becomes the complement of the input on B side. See Function Control of the TTL Input Logic on page 5.
12. V_{OC} measurement requires equipment with a 3-dB bandwidth of at least 300 MHz.
13. All input pulses are supplied by a frequency generator with the following characteristics: t_R and $t_F \leq 1$ ns; pulse re-rate = 50 Mpps; pulse width = 10 ± 0.2 ns.

Maximum Ratings

Exceeding maximum ratings [14, 15] may shorten the useful life of the device. User guidelines are not tested.

Storage temperature: ..... –65 °C to +150 °C

Ambient temperature: ..... 0 °C to 70 °C

Supply voltage to ground potential (Inputs and V_{CC} only) .....–0.3 V to 4.6 V

Supply voltage to ground potential (Outputs only) ..... –0.3 V to V_{DD} + 0.3 V

DC input voltage ..... –0.3 V to V_{DD} + 0.3 V

DC output voltage ..... –0.3 V to V_{DD} + 0.9 V

Power dissipation ..... 0.75 W

DC Electrical Characteristics

3.3 V LVDS Input

Parameter	Description	Conditions		Min	Typ	Max	Unit
V_{ID}	Magnitude of differential input voltage			100		600	mV
V_{IC}	Common-mode of differential input voltage $IV_{ID}I$ (min. and max.)			$IV_{ID}I$ /2	2.4–($IV_{ID}I$ /2)		V
I_{IH}	Input high current	V_{DD} = Max	$V_{IN} = V_{DD}$	–	±10	±20	µA
I_{IL}	Input low current	V_{DD} = Max	$V_{IN} = V_{SS}$	–	±0	±20	µA
I_I	Input high current	V_{DD} = Max, $V_{IN} = V_{DD}$(max)	–	–	–	±20	µA

DC Electrical Characteristics

3.3 V LVPECL Input

Parameter	Description	Condition		Min	Typ	Max	Unit
I V_{ID} I	Differential input voltage p-p	Guaranteed logic high level	–	400	–	2600	mV
VCM	Common-mode voltage		–	1650	–	2250	mV
I_{IH}	Input high current	V_{DD} = Max	$V_{IN} = V_{DD}$	–	±10	±20	µA
I_{IL}	Input low current	V_{DD} = Max	$V_{IN} = V_{SS}$	–	±10	±20	µA
I_I	Input high current	V_{DD} = Max, $V_{IN} = V_{DD}$(max.)	–	–	–	±20	µA

Notes

14. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
15. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Characteristics

3.3 V LVTTL/LVCMOS Input

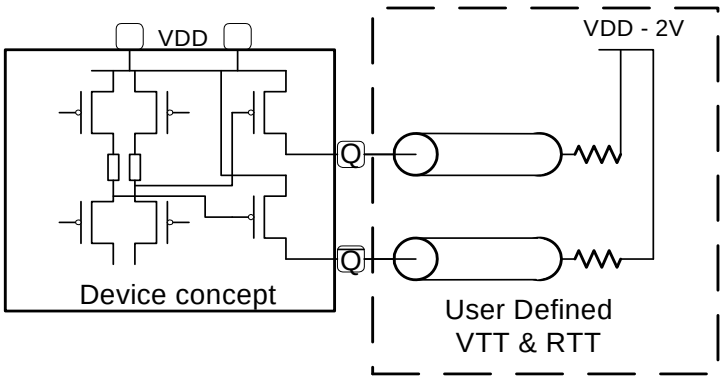
Parameter	Description	Condition		Min	Typ	Max	Unit
V_{IH}	Input high voltage	Guaranteed logic high level	–	2	–		V
V_{IL}	Input low voltage	Guaranteed logic low level	–	–	–	0.8	V
I_{IH}	Input high current	V_{DD} = Max	V_{IN} = 2.7 V	–	–	1	µA
I_{IL}	Input low current	V_{DD} = Max	V_{IN} = 0.5 V	–	–	–1	µA
I_I	Input high current	V_{DD} = Max, V_{IN} = V_{DD}(max)	–	–	–	20	µA
V_{IK}	Clamp diode voltage	V_{DD} = Min, I_{IN} = –18 mA	–	–	–0.7	–1.2	V
V_H	Input hysteresis	–	–	–	80	–	mV

DC Electrical Characteristics

3.3 V LVPECL Output

Parameter	Description	Condition		Min	Typ	Max	Unit
I V_{OD} I	Driver differential output voltage p-p	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	RL = 50 ohm	1000	–	3600	mV
I V_{OC} I	Driver common-mode p-p	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	RL = 50 ohm	–	–	226	mV
Rise Time	Differential 20% to 80%	CL–10 pF RL and CL to GND	RL = 50 ohm	300	–	800	ps
Fall Time							
V_{OH}	Output high voltage	V_{DD} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12 mA	2.1	–	3.0	V
V_{OL}	Output low voltage	User-defined (see Figure 8)		–	–		V
I_{OS}	Short circuit current	V_{DD} = Max, V_{OUT} = G_{ND}		–125	–	–150	mA

Figure 8. Differential PECL Output



AC Switching Characteristics

At 3.3 V V_{DD} = 3.3 V ± 5%, Temperature = 0 °C to 70 °C

Parameter	Description	Conditions	Min	Typ	Max	Unit
IN [+,–] to Q[A,B] Data & Clock Speed						
t_{PLH}	Propagation delay – low to high	V_{OD} = 100 mV	3	4	5	ns
t_{PHL}	Propagation delay – High to low		3	4	5	ns
t_{PD}	Propagation delay	–	3	4	5	ns
EN [1,2] to Q[A,B] Control Speed						
t_{PE}	Enable (EN) to functional operation	–	–	–	6	ns
t_{pd}	Functional operation to disable	–	–	–	5	ns
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase)	–	–	0.085	0.2	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output (t_{PHL}–t_{PLH})	–	–	0.2	–	ns
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type. Same input signal level and output load.	V_{ID} = 100 mV	–	–	1	ns

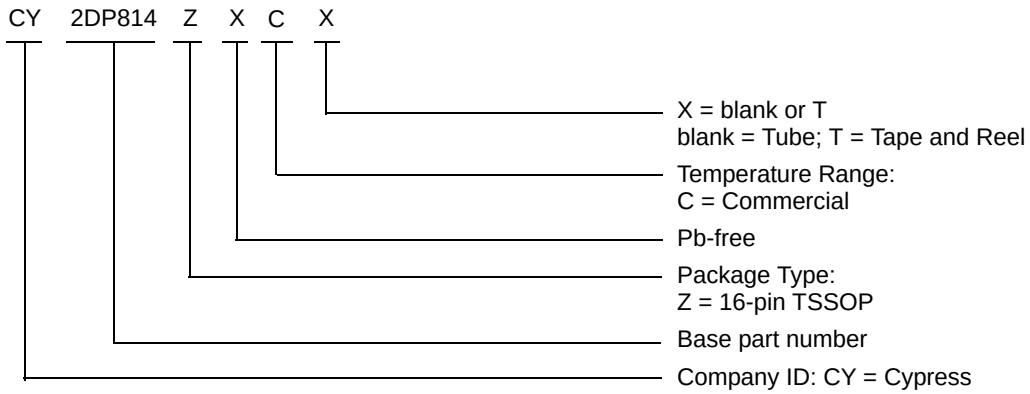
High-frequency Parametrics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Fmax	Maximum frequency V_{DD} = 3.3 V	50% duty cycle tW(50–50) Standard Load Circuit	–	–	450	MHz
Fmax(20)	Maximum frequency V_{DD} = 3.3 V	20% duty cycle tW(20–80) LVPECL Input Vin = V_{IH}(Max)/V_{IL}(Min) Vout = V_{OH}(Min)/V_{OL} (Max) (Limit)	–	–	175	MHz
TW	Minimum pulse V_{DD} = 3.3 V	LVPECL Input Vin = V_{IH}(Max)/V_{IL}(Min) F = 100 MHz Vout = V_{OH}(Min)/V_{OL}(Max) (Limit)	900	–	–	ps

Ordering Information

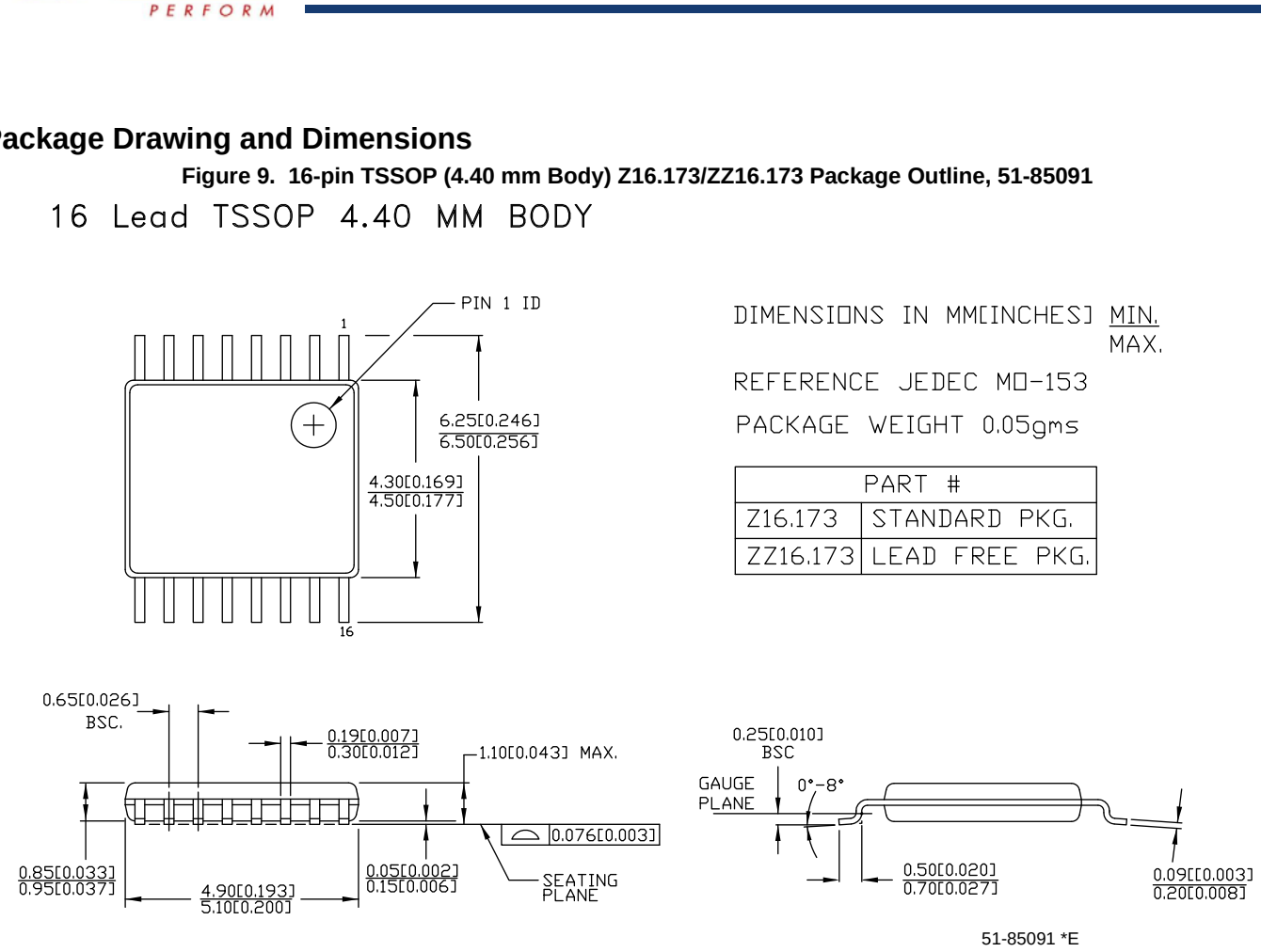
Part Number	Package Type	Product Flow
Pb free		
CY2DP814ZXC	16-pin TSSOP	Commercial, 0 °C to 70 °C
CY2DP814ZXCT	16-pin TSSOP – Tape and Reel	Commercial, 0 °C to 70 °C

Ordering Code Definitions



Package Drawing and Dimensions

Figure 9. 16-pin TSSOP (4.40 mm Body) Z16.173/ZZ16.173 Package Outline, 51-85091



Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVPECL	Low-Voltage Pseudo (Positive) Emitter-Coupled Logic
LVTTL	Low-Voltage Transistor-Transistor Logic
TSSOP	Thin Shrink Small Outline Package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

Document History Page

Document Title: CY2DP814, 1:4 Clock Fanout Buffer Document Number: 38-07060				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	10785	06/07/01	IKA	Convert from IMI to Cypress
*A	115610	07/02/02	CTK	Range of VCM
*B	122746	12/15/02	RBI	Added power-up requirements to maximum ratings information.
*C	382376	See ECN	RGL	Added typical values Added Lead-free device for TSSOP commercial Removed pruned parts
*D	403374	See ECN	RGL	Added Lead-free for TSSOP Industrial
*E	2595534	10/23/08	CXQ	Removed CY2DP814ZC from the Ordering Information. Updated template
*F	2904795	04/05/2010	TSV	Removed inactive part number CY2DP814ZCT from the Ordering Information table. Updated package diagram.
*G	3052284	10/08/2010	CXQ	Updated Features (To mention commercial temperature range). Updated Maximum Ratings: Changed ambient temperature to 0 °C to 70 °C. Changed temperature range to 0 °C to 70 °C in AC Switching Characteristics. Removed CY2DP814ZXI and CY2DP814ZXIT from Ordering Information. Updated Package Drawing and Dimensions. Updated Sales, Solutions, and Legal Information.
*H	3342673	08/12/2011	PURU	Added Contents. Updated footnotes. Added Ordering Code Definitions. Added Acronyms and Units of Measure.
*I	4506605	09/18/2014	TAVA	Updated Package Drawing and Dimensions: spec 51-85091 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*J	4587303	12/04/2014	TAVA	Added related documentation hyperlink in page 1. Updated Figure 9 in Package Drawing and Dimensions (spec 51-85091 *D to *E).

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