

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74HC273AP,TC74HC273AF

## Octal D-Type Flip Flop with Clear

The TC74HC273A is a high speed CMOS OCTAL D-TYPE FLIP FLOP fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

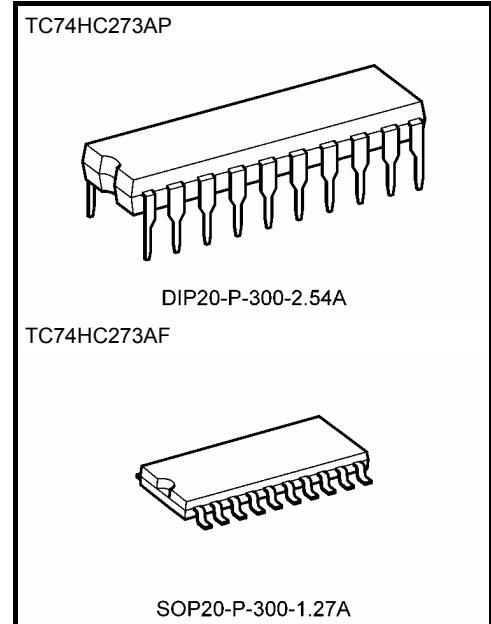
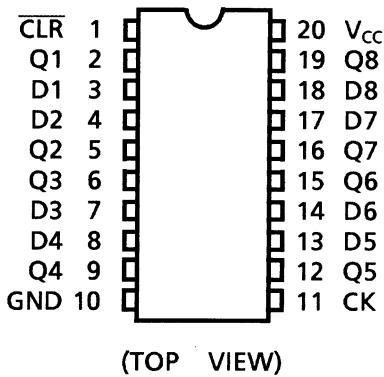
When the  $\overline{\text{CLR}}$  input is held "L", the Q outputs are at a low logic level independent of the other inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

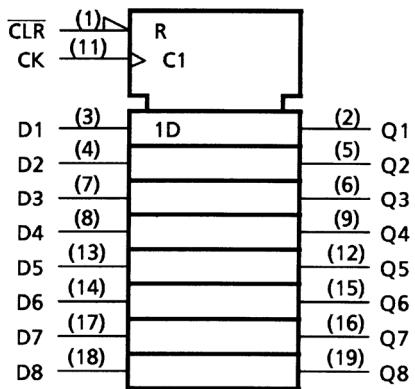
- High speed:  $f_{\text{max}} = 67 \text{ MHz}$  (typ.) at  $V_{\text{CC}} = 5 \text{ V}$
- Low power dissipation:  $I_{\text{CC}} = 4 \mu\text{A}$  (max) at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$  (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance:  $|I_{\text{OH}}| = I_{\text{OL}} = 4 \text{ mA}$  (min)
- Balanced propagation delays:  $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Wide operating voltage range:  $V_{\text{CC}}$  (opr) = 2~6 V
- Pin and function compatible with 74LS273

### Pin Assignment



Weight  
 DIP20-P-300-2.54A : 1.30 g (typ.)  
 SOP20-P-300-1.27A : 0.22 g (typ.)

## IEC Logic Symbol

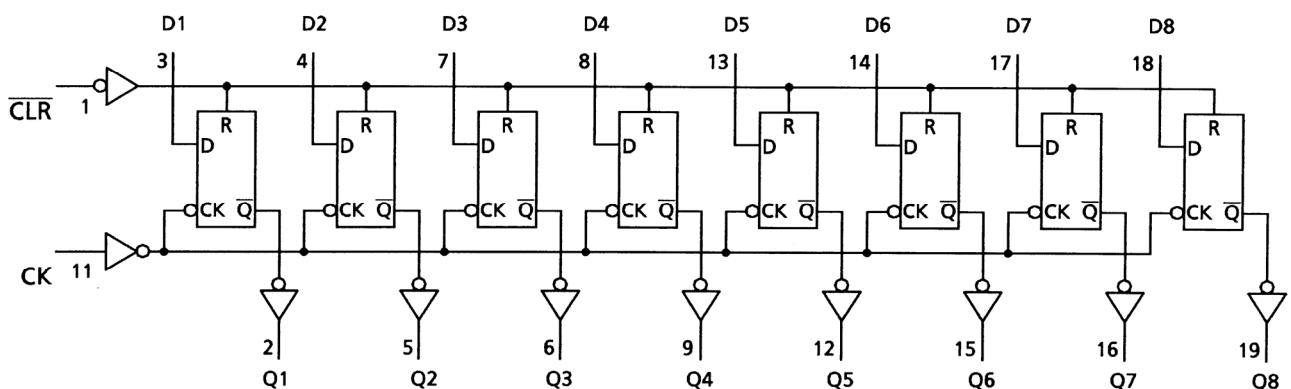


## Truth Table

Inputs			Output	Function
CLR	D	CK	Q	
L	X	X	L	Clear
H	L	↑	L	—
H	H	↑	H	—
H	X	↓	Q <sub>n</sub>	No change

X: Don't care

## System Diagram



**Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	V <sub>CC</sub>	−0.5~7	V
DC input voltage	V <sub>IN</sub>	−0.5~V <sub>CC</sub> + 0.5	V
DC output voltage	V <sub>OUT</sub>	−0.5~V <sub>CC</sub> + 0.5	V
Input diode current	I <sub>IK</sub>	±20	mA
Output diode current	I <sub>OK</sub>	±20	mA
DC output current	I <sub>OUT</sub>	±25	mA
DC V <sub>CC</sub> /ground current	I <sub>CC</sub>	±50	mA
Power dissipation	P <sub>D</sub>	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T <sub>STG</sub>	−65~150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: 500 mW in the range of Ta = −40~65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C shall be applied until 300 mW.

**Operating Ranges (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	2~6	V
Input voltage	V <sub>IN</sub>	0~V <sub>CC</sub>	V
Output voltage	V <sub>OUT</sub>	0~V <sub>CC</sub>	V
Operating temperature	T <sub>OPR</sub>	−40~85	°C
Input rise and fall time	t <sub>r</sub> , t <sub>f</sub>	0~1000 (V <sub>CC</sub> = 2.0 V) 0~500 (V <sub>CC</sub> = 4.5 V) 0~400 (V <sub>CC</sub> = 6.0 V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either V<sub>CC</sub> or GND.

## Electrical Characteristics

## DC Characteristics

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		Unit
				Min	Typ.	Max	Min	Max	
High-level input voltage	V <sub>IH</sub>	—	2.0	1.50	—	—	1.50	—	V
			4.5	3.15	—	—	3.15	—	
			6.0	4.20	—	—	4.20	—	
Low-level input voltage	V <sub>IL</sub>	—	2.0	—	—	0.50	—	0.50	V
			4.5	—	—	1.35	—	1.35	
			6.0	—	—	1.80	—	1.80	
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2.0	1.9	2.0	—	1.9	V
				4.5	4.4	4.5	—	4.4	
				6.0	5.9	6.0	—	5.9	
			I <sub>OH</sub> = -4 mA I <sub>OH</sub> = -5.2 mA	4.5	4.18	4.31	—	4.13	
				6.0	5.68	5.80	—	5.63	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2.0	—	0.0	0.1	—	V
				4.5	—	0.0	0.1	—	
				6.0	—	0.0	0.1	—	
			I <sub>OL</sub> = 4 mA I <sub>OL</sub> = 5.2 mA	4.5	—	0.17	0.26	—	
				6.0	—	0.18	0.26	—	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input: t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40~85°C	Unit
			V <sub>CC</sub> (V)	Typ.	Limit		
Minimum pulse width (CK)	t <sub>W</sub> (L) t <sub>W</sub> (H)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width (CLR)	t <sub>W</sub> (L)	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time	t <sub>s</sub>	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum hold time	t <sub>h</sub>	—	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time (CLR)	t <sub>rem</sub>	—	2.0	—	50	65	ns
			4.5	—	10	13	
			6.0	—	9	11	
Clock frequency	f	—	2.0	—	6	5	MHz
			4.5	—	30	24	
			6.0	—	35	28	

AC Characteristics ( $C_L = 15 \text{ pF}$ ,  $V_{CC} = 5 \text{ V}$ ,  $T_a = 25^\circ\text{C}$ , input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}$ $t_{THL}$	—	—	4	8	ns
Propagation delay time (CK-Q)	$t_{pLH}$ $t_{pHL}$	—	—	15	25	ns
Propagation delay time ( $\overline{CLR}$ -Q)	$t_{pLH}$ $t_{pHL}$	—	—	16	27	ns
Maximum clock frequency	$f_{max}$	—	40	67	—	MHz

AC Characteristics ( $C_L = 50 \text{ pF}$ , input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40~85°C		Unit
			V <sub>CC</sub> (V)	Min	Typ.	Max	Min	
Output transition time	$t_{TLH}$ $t_{THL}$	—	2.0	—	25	75	—	95
			4.5	—	7	15	—	19
			6.0	—	6	13	—	16
Propagation delay time (CK-Q)	$t_{pLH}$ $t_{pHL}$	—	2.0	—	54	145	—	180
			4.5	—	18	29	—	36
			6.0	—	15	25	—	31
Propagation delay time ( $\overline{CLR}$ -Q)	$t_{pLH}$ $t_{pHL}$	—	2.0	—	60	160	—	200
			4.5	—	20	32	—	40
			6.0	—	17	27	—	34
Maximum clock frequency	$f_{max}$	—	2.0	6	18	—	5	—
			4.5	30	56	—	24	—
			6.0	35	66	—	28	—
Input capacitance	$C_{IN}$	—	—	5	10	—	10	pF
Power dissipation capacitance	$C_{PD}$ (Note)	—	—	43	—	—	—	pF

Note:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC} (\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per flip flop)}$$

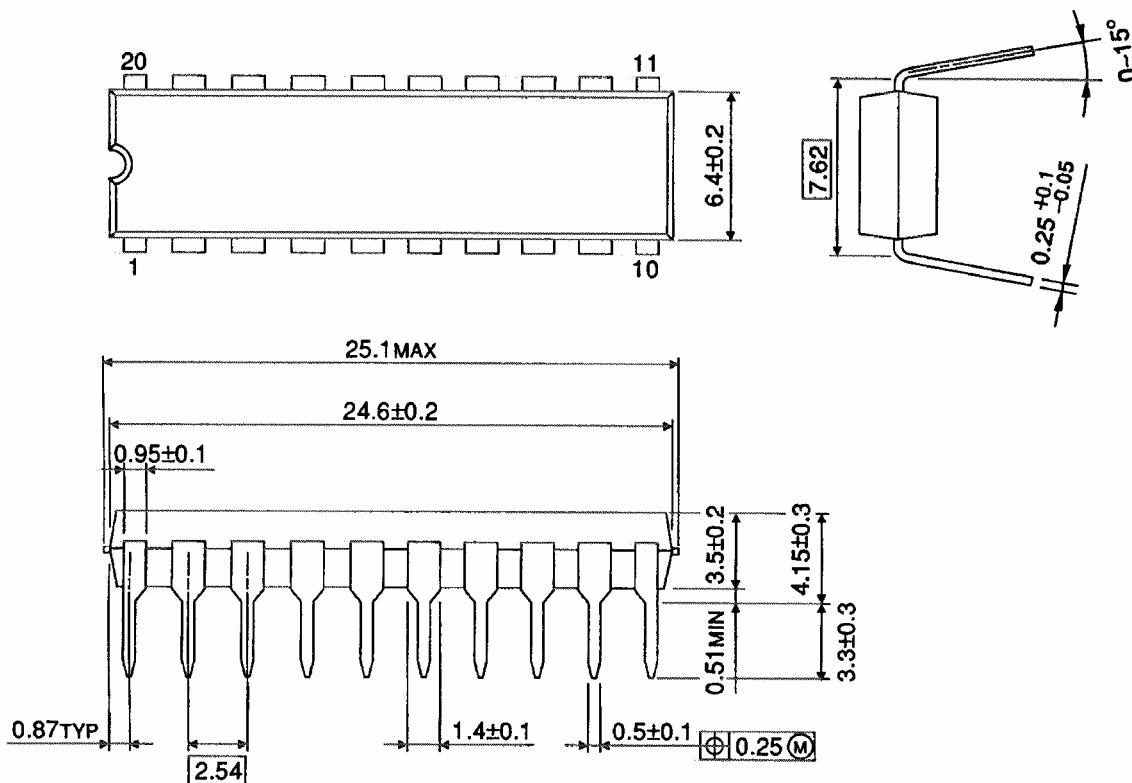
And the total  $C_{PD}$  when  $n$  pcs. of flip flop operate can be gained by the following equation:

$$C_{PD} (\text{total}) = 32 + 11 \cdot n$$

**Package Dimensions**

DIP20-P-300-2.54A

Unit : mm

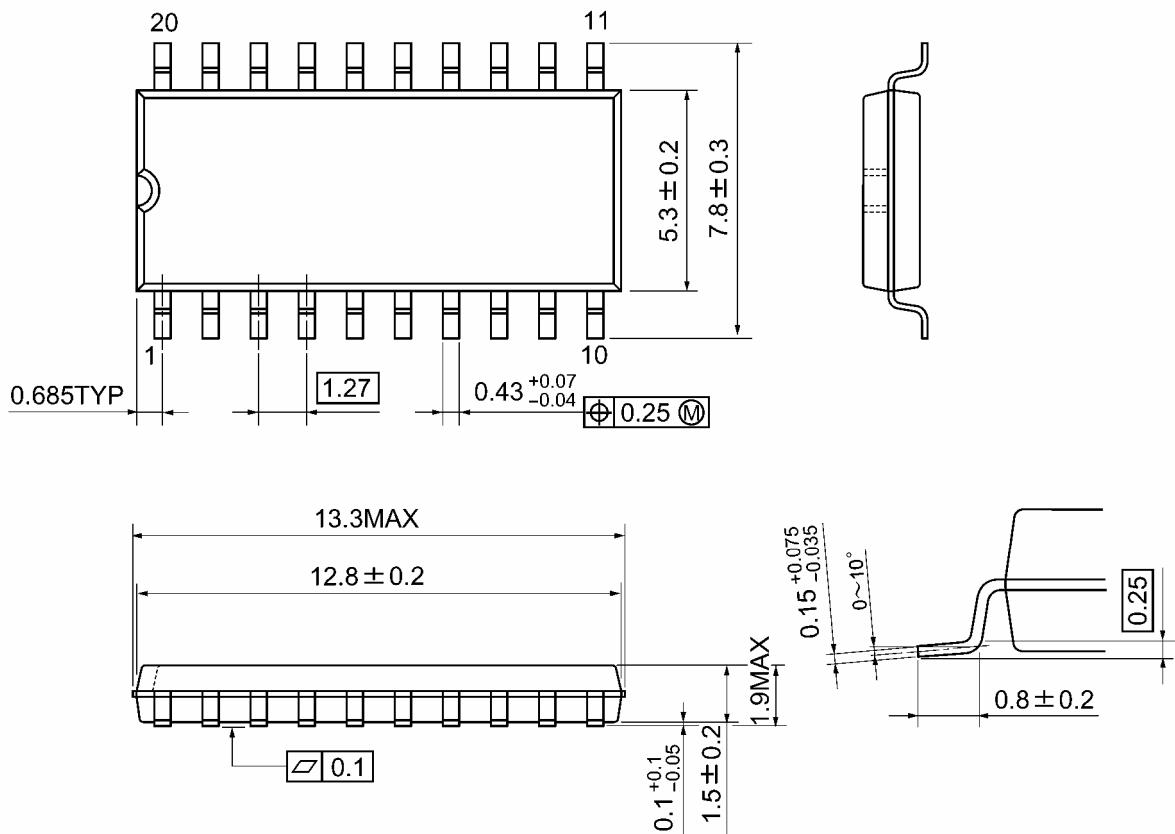


Weight: 1.30 g (typ.)

**Package Dimensions**

SOP20-P-300-1.27A

Unit: mm



Weight: 0.22 g (typ.)

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20070701-EN GENERAL

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