



High-Speed, Digitally Adjusted Step-Down Controllers for Notebook CPUs

ABSOLUTE MAXIMUM RATINGS

V+ to GND-0.3V to +30V
V_{CC}, V_{DD} to GND-0.3V to +6V
PGND to GND±0.3V
SHDN, PGOOD to GND-0.3V to +6V
OVP, ILIM, FB, FBS, CC, REF, D0-D4,
GNDS, TON to GND-0.3V to (V_{CC} + 0.3V)
SKIP to GND (Note 1).....-0.3V to (V_{CC} + 0.3V)
DL to PGND.....-0.3V to (V_{DD} + 0.3V)
BST to GND-0.3V to +36V

DH to LX-0.3V to (BST + 0.3V)
LX to BST-6V to +0.3V
REF Short Circuit to GNDContinuous
Continuous Power Dissipation (T_A = +70°C)
24-Pin QSOP (derate 9.5mW/°C above +70°C).....762mW
Operating Temperature Range-40°C to +85°C
Junction Temperature+150°C
Storage Temperature Range-65°C to +165°C
Lead Temperature (soldering, 10s)+300°C

Note 1: SKIP may be forced below -0.3V, temporarily exceeding the absolute maximum rating, for the purpose of debugging prototype breadboards using the no-fault test mode. Limit the current drawn to -5mA maximum.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{BATT} = 15V, V_{CC} = V_{DD} = 5V, SKIP = GND, T_A = 0°C to +85°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Input Voltage Range	Battery voltage, V+		2		28	V
	V _{CC} , V _{DD}		4.5		5.5	
DC Output Voltage Accuracy	V _{BATT} = 4.5V to 28V, includes load regulation error	DAC codes from 1.3V to 2V	-1		1	%
		DAC codes from 0.925V to 1.275V	-1.2		1.2	
Load Regulation Error	I _{LOAD} = 0 to 7A			9		mV
Remote-Sense Voltage Error	FB - FBS or GNDS - GND = 0 to 25mV			3		mV
Line Regulation Error	V _{CC} = 4.5V to 5.5V, V _{BATT} = 4.5V to 28V			5		mV
FB Input Bias Current	FB (MAX1710 only) or FBS		-0.2		0.2	µA
FB Input Resistance (MAX1711/MAX1712)			130	180	240	kΩ
GNDS Input Bias Current			-1		1	µA
Soft-Start Ramp Time	Rising edge of SHDN to full I _{LIM}			1.7		ms
On-Time	V _{BATT} = 24V, FB = 2V (Note 2)	TON = GND (550kHz)	140	160	180	ns
		TON = REF (400kHz)	175	200	225	
		TON = open (300kHz)	260	290	320	
		TON = V _{CC} (200kHz)	380	425	470	
Minimum Off-Time	(Note 2)			400	500	ns
Quiescent Supply Current (V _{CC})	Measured at V _{CC} , FB forced above the regulation point			600	950	µA
Quiescent Supply Current (V _{DD})	Measured at V _{DD} , FB forced above the regulation point			<1	5	µA
Quiescent Battery Supply Current	Measured at V+			25	40	µA
Shutdown Supply Current (V _{CC})	SHDN = 0			<1	5	µA
Shutdown Supply Current (V _{DD})	SHDN = 0			<1	5	µA
Shutdown Battery Supply Current	SHDN = 0, measured at V+ = 28V, V _{CC} = V _{DD} = 0 or 5V			<1	5	µA
Reference Voltage	V _{CC} = 4.5V to 5.5V, no external REF load		1.98	2	2.02	V
Reference Load Regulation	I _{REF} = 0 to 50µA				0.01	V
REF Sink Current	REF in regulation		10			µA
REF Fault Lockout Voltage	Falling edge, hysteresis = 40mV			1.6		V

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{BATT} = 15V$, $V_{CC} = V_{DD} = 5V$, $\overline{SKIP} = GND$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Overvoltage Trip Threshold	With respect to unloaded output voltage (MAX1710)		10.5	12.5	14.5	%
	(MAX1711/MAX1712)		2.21	2.25	2.29	V
Overvoltage Fault Propagation Delay	FB forced 2% above trip threshold		1.5			μs
Output Undervoltage Protection Threshold	With respect to unloaded output voltage (MAX1710)		65	70	75	%
	(MAX1711/MAX1712)		0.76	0.8	0.84	V
Output Undervoltage Protection Time	From $\overline{SHDN}$ signal going high		10		30	ms
Current-Limit Threshold (Positive Direction, Fixed)	LX to PGND, ILIM tied to VCC		90	100	110	mV
Current-Limit Threshold (Positive Direction, Adjustable)	LX to PGND	R _{LIM} = 100kΩ	40	50	60	mV
		R _{LIM} = 400kΩ	170	200	230	
Current-Limit Threshold (Negative Direction)	LX to PGND, T _A = +25°C		-150	-120	-80	mV
Current-Limit Threshold (Zero Crossing)	LX to PGND		3			mV
PGOOD Propagation Delay	FB forced 2% below PGOOD trip threshold, falling edge		1.5			μs
PGOOD Output Low Voltage	I _{SINK} = 1mA		0.4			V
PGOOD Leakage Current	High state, forced to 5.5V		1			μA
Thermal Shutdown Threshold	Hysteresis = 10°C		150			°C
VCC Undervoltage Lockout Threshold	Rising edge, hysteresis = 20mV, PWM disabled below this level		4.1		4.4	V
DH Gate-Driver On-Resistance	BST-LX forced to 5V		5			Ω
DL Gate-Driver On-Resistance (Pullup)	DL, high state		5			Ω
DL Gate-Driver On-Resistance (Pulldown)	DL, low state		0.5	1.7		Ω
DH Gate-Driver Source/Sink Current	DH forced to 2.5V, BST-LX forced to 5V		1			A
DL Gate-Driver Sink Current	DL forced to 2.5V		3			A
DL Gate-Driver Source Current	DL forced to 2.5V		1			A
Dead Time	DL rising		35			ns
	DH rising		26			
$\overline{SKIP}$ Input Current Logic Threshold	To enable no-fault mode, T _A = +25°C		-1.5		-0.1	mA
PGOOD Trip Threshold	Measured at FB with respect to unloaded output voltage, falling edge, hysteresis = 1%		-8	-5	-3	%
Logic Input High Voltage	D0–D4, $\overline{SHDN}$, $\overline{SKIP}$, $\overline{OVP}$		2.4			V
Logic Input Low Voltage	D0–D4, $\overline{SHDN}$, $\overline{SKIP}$, $\overline{OVP}$				0.8	V
Logic Input Current	$\overline{SHDN}$, $\overline{SKIP}$, $\overline{OVP}$		-1		1	μA
Logic Input Pullup Current	D0–D4, each forced to GND		3	5	10	μA

MAX1710/MAX1711/MAX1712

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{BATT} = 15V$, $V_{CC} = V_{DD} = 5V$, $\overline{SKIP} = GND$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
TON V_{CC} Level	TON logic input high level	$V_{CC} - 0.4$			V
TON Float Voltage	TON logic input upper-midrange level	3.15		3.85	V
TON Reference Level	TON logic input lower-midrange level	1.65		2.35	V
TON GND Level	TON logic input low level			0.5	V
TON Logic Input Current	TON only, forced to GND or V_{CC}	-3		3	μA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, $V_{BATT} = 15V$, $V_{CC} = V_{DD} = 5V$, $\overline{SKIP} = GND$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Input Voltage Range	Battery voltage, V_+		2		28	V
	V_{CC} , V_{DD}		4.5		5.5	
DC Output Voltage Accuracy	$V_{BATT} = 4.5V$ to $28V$, for all D/A codes, includes load regulation error	DAC codes from 1.32V to 2V	-1.5		1.5	%
		DAC codes from 0.925V to 1.275V	-1.7		1.7	%
On-Time	$V_{BATT} = 24V$, FB = 2V (Note 2)	TON = GND (550kHz)	140		180	ns
		TON = REF (400kHz)	175		225	
		TON = open (300kHz)	260		320	
		TON = V_{CC} (200kHz)	380		470	
Minimum Off-Time	(Note 2)				500	ns
Quiescent Supply Current (V_{CC})	Measured at V_{CC} , FB forced above the regulation point				950	μA
Reference Voltage	$V_{CC} = 4.5V$ to $5.5V$, no external REF load		1.98		2.02	V
Overvoltage Trip Threshold	With respect to unloaded output voltage (MAX1710)		10		15	%
	(MAX1711/MAX1712)		2.20		2.30	V
Output Undervoltage Protection Threshold	With respect to unloaded output voltage (MAX1710)		65		75	%
	(MAX1711/MAX1712)		0.75		0.85	V
Current-Limit Threshold (Positive Direction, Fixed)	LX to PGND, ILIM tied to V_{CC}		85		115	mV
Current-Limit Threshold (Positive Direction, Adjustable)	LX to PGND	$R_{LIM} = 100k\Omega$	35		65	mV
		$R_{LIM} = 400k\Omega$	160		240	
V_{CC} Undervoltage Lockout Threshold	Rising edge, hysteresis = 20mV, PWM disabled below this level		4.1		4.4	V
Logic Input High Voltage	D0–D4, $\overline{SHDN}$, $\overline{SKIP}$, $\overline{OVP}$		2.4			V
Logic Input Low Voltage	D0–D4, $\overline{SHDN}$, $\overline{SKIP}$, $\overline{OVP}$				0.8	V
Logic Input Current	$\overline{SHDN}$, $\overline{SKIP}$, $\overline{OVP}$		-1		1	μA
Logic Input Pullup Current	D0–D4, each forced to GND		3		10	μA

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{BATT} = 15V$, $V_{CC} = V_{DD} = 5V$, $\overline{SKIP} = GND$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted.) (Note 3)

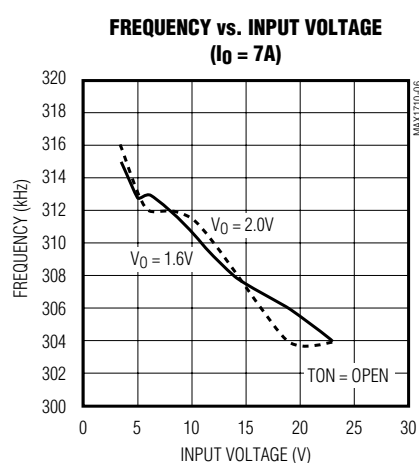
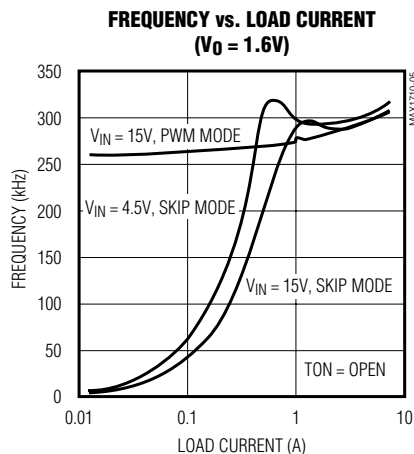
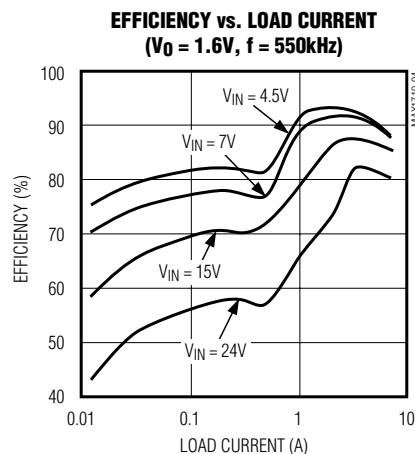
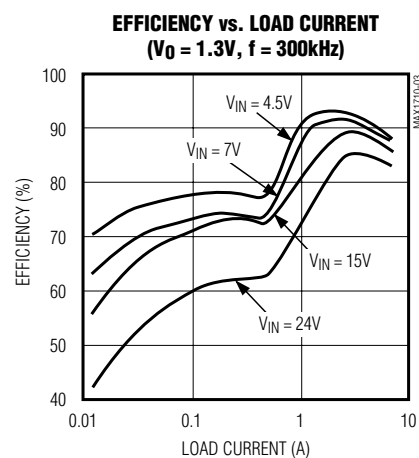
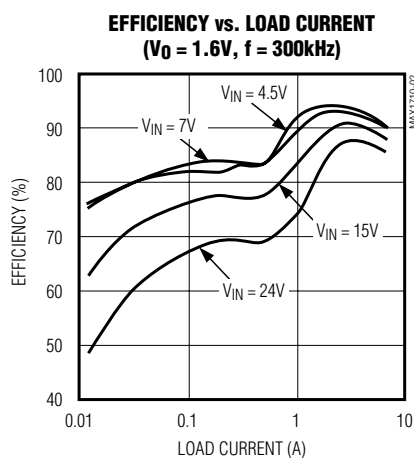
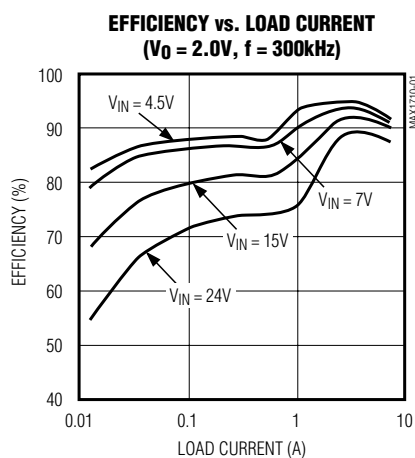
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
PGOOD Trip Threshold	Measured at FB with respect to unloaded output voltage, falling edge, hysteresis = 1%	-8.5		-2.5	%
PGOOD Output Low Voltage	$I_{SINK} = 1mA$			0.4	V
PGOOD Leakage Current	High state, forced to 5.5V			1	μA

Note 2: On-Time and Off-Time specifications are measured from 50% point to 50% point at the DH pin with LX forced to 0V, BST forced to 5V, and a 250pF capacitor connected from DH to LX. Actual in-circuit times may differ due to MOSFET switching speeds.

Note 3: Specifications from $-40^{\circ}C$ to $0^{\circ}C$ are guaranteed but not production tested.

Typical Operating Characteristics

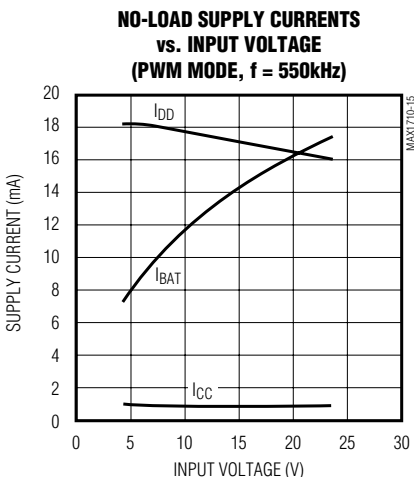
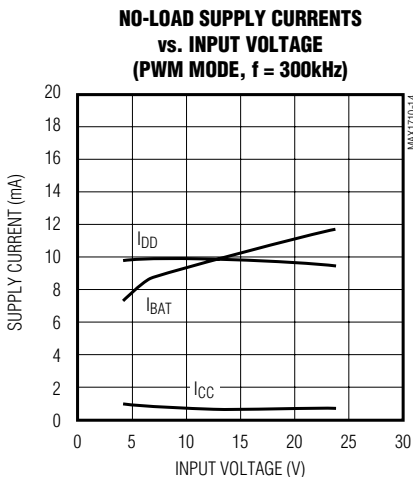
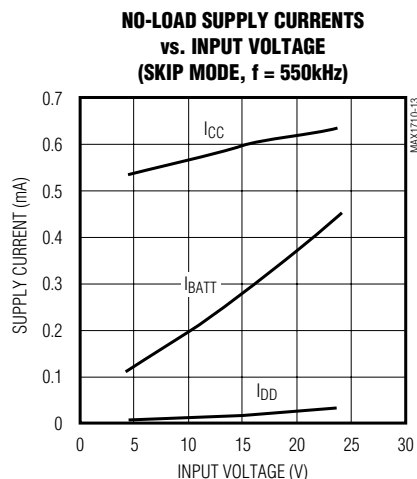
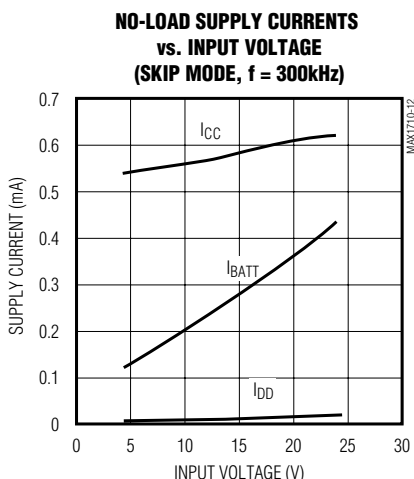
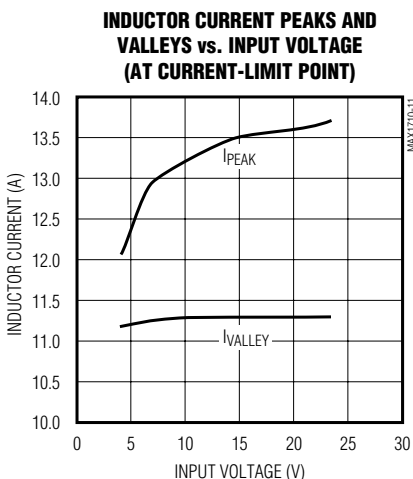
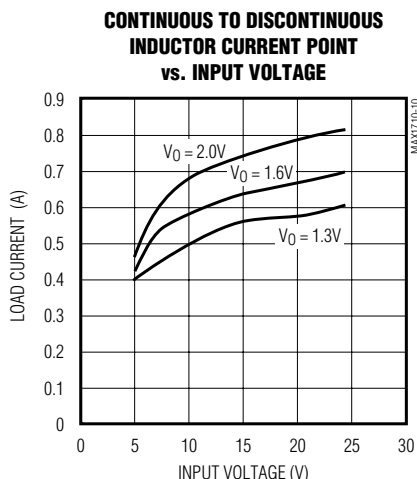
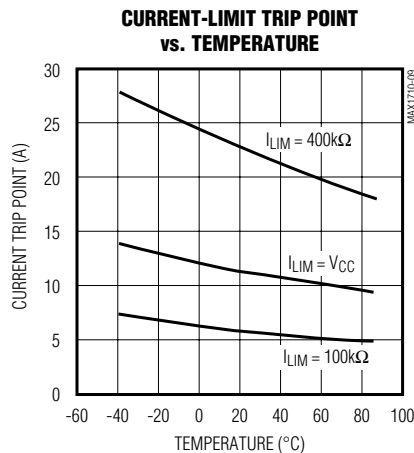
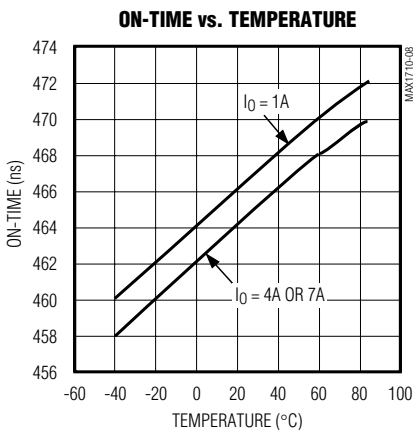
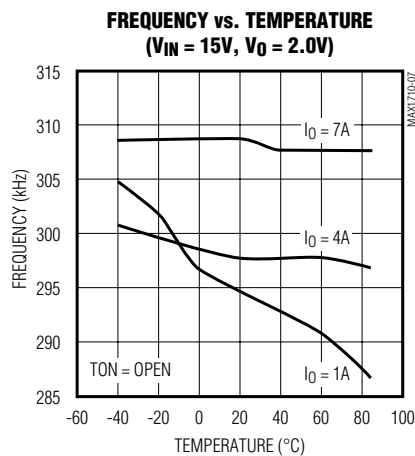
(7A CPU supply circuit of Figure 1, $T_A = +25^{\circ}C$, unless otherwise noted.)



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Typical Operating Characteristics (continued)

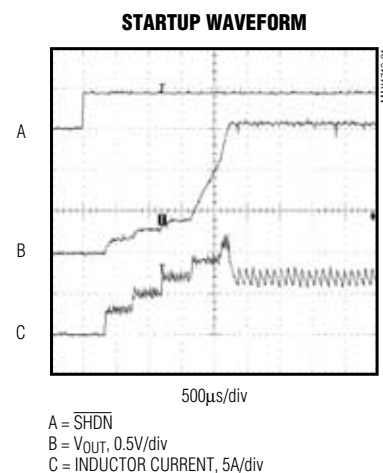
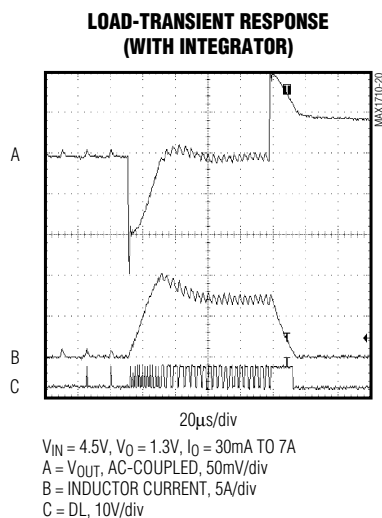
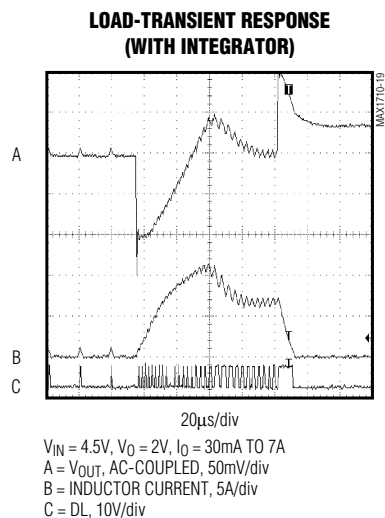
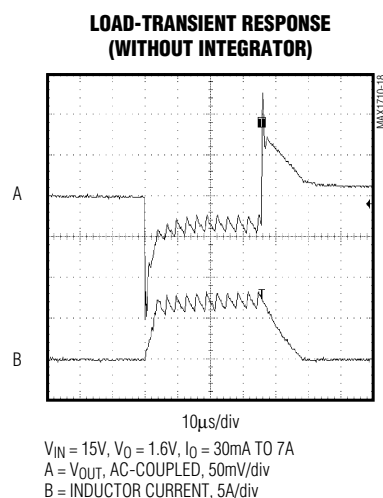
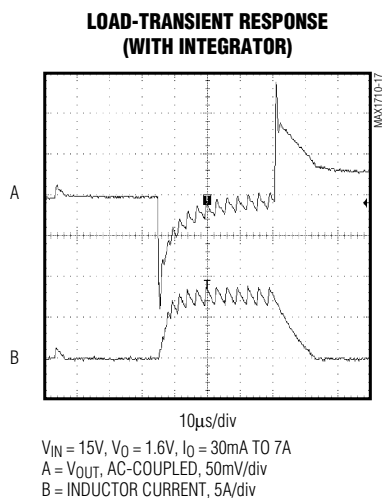
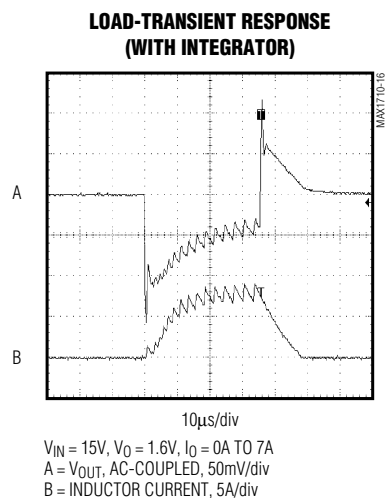
(7A CPU supply circuit of Figure 1, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



High-Speed, Digitally Adjusted Step-Down Controllers for Notebook CPUs

Typical Operating Characteristics (continued)

(7A CPU supply circuit of Figure 1, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

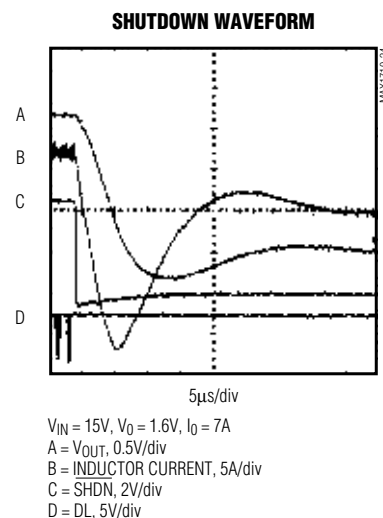
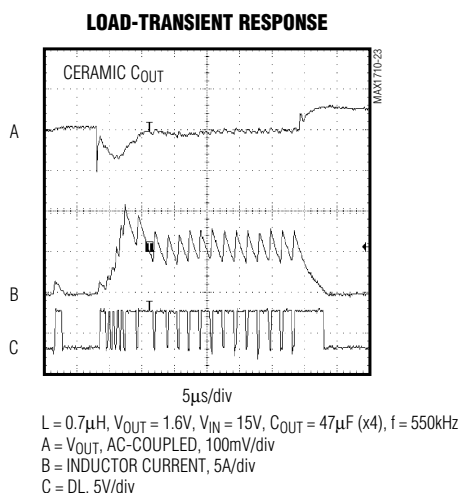
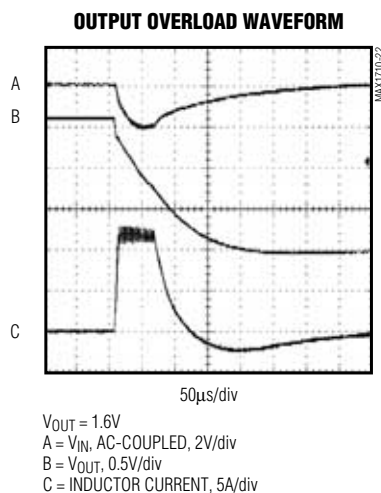


MAX1710/MAX1711/MAX1712

High-Speed, Digitally Adjusted Step-Down Controllers for Notebook CPUs

Typical Operating Characteristics (continued)

(7A CPU supply circuit of Figure 1, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1	V+	Battery Voltage Sense Connection. V+ is used only for PWM one-shot timing. DH on-time is inversely proportional to V+ input voltage over a range of 2V to 28V.
2	$\overline{\text{SHDN}}$	Shutdown Control Input, active low. $\overline{\text{SHDN}}$ cannot withstand the battery voltage. In shutdown mode, DL is forced to V_{DD} in order to enforce overvoltage protection, even when powered down (unless OVP is high).
3	FB	Fast Feedback Input, normally connected to V_{OUT} . FB is connected to the bulk output filter capacitors locally at the power supply. An external resistor-divider can optionally set the output voltage.
4	FBS	Feedback Remote-Sense Input, normally connected to V_{OUT} directly at the load. FBS internally connects to the integrator that fine tunes the DC output voltage. Tie FBS to V_{CC} to disable all three integrator amplifiers. Tie FBS to FB (or disable the integrators) when externally adjusting the output voltage with a resistor-divider.
5	CC	Integrator Capacitor Connection. Connect a 100pF to 1000pF (470pF typical) capacitor to GND to set the integration time constant.
6	ILIM	Current-Limit Threshold Adjustment. Connects to an external resistor to GND. The LX-PGND current-limit threshold defaults to +100mV if ILIM is tied to V_{CC} . The current-limit threshold is 1/10 of the voltage forced at ILIM. In adjustable mode, the threshold is $V_{TH} = R_{LIM} \times 5\mu\text{A}/10$.
7	VCC	Analog Supply Voltage Input for PWM Core, 4.5V to 5.5V. Bypass V_{CC} to GND with a 0.1µF minimum capacitor.
8	TON	On-Time Selection Control Input. This is a four-level input that sets the K factor to determine DH on-time. GND = 550kHz, REF = 400kHz, open = 300kHz, VCC = 200kHz.
9	REF	2.0V Reference Output. Bypass REF to GND with a 0.22µF minimum capacitor. REF can source 50µA for external loads. Loading REF degrades FB accuracy according to the REF load-regulation error (see <i>Electrical Characteristics</i>).

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Pin Description (continued)

PIN	NAME	FUNCTION
10	GND	Analog Ground
11	GNDS	Ground Remote-Sense Input, normally connected to ground directly at the load. GNDS internally connects to the integrator that fine tunes the ground offset voltage.
12	PGOOD	Open-Drain Power-Good Output
13	DL	Low-Side Gate-Driver Output, swings 0 to V _{DD}
14	PGND	Power Ground. Also used as the inverting input for the current-limit comparator.
15	V _{DD}	Supply Voltage Input for the DL Gate Driver, 4.5V to 5.5V
16 (MAX1710)	$\overline{\text{OVP}}$	Overvoltage-Protection Disable Control Input (Table 4). GND = normal operation and overvoltage protection active, V _{CC} = overvoltage protection disabled.
16 (MAX1711/ MAX1712)	D4	DAC Code Input, MSB. 5μA internal pullup to V _{CC} (Tables 1, 2, and 3).
17	D3	DAC Code Input. 5μA internal pullup to V _{CC} .
18	D2	DAC Code Input. 5μA internal pullup.
19	D1	DAC Code Input. 5μA internal pullup.
20	D0	DAC Code Input LSB. 5μA internal pullup.
21	$\overline{\text{SKIP}}$	Low-Noise-Mode Selection Control Input. Low-noise forced-PWM mode causes inductor current recirculation at light loads and suppresses pulse-skipping operation. Normal operation prevents current recirculation. $\overline{\text{SKIP}}$ can also be used to disable both overvoltage and undervoltage protection circuits and clear the fault latch (Figure 6). GND = normal operation, V _{CC} = low-noise mode. Do not leave $\overline{\text{SKIP}}$ floating.
22	BST	Boost Flying-Capacitor Connection. An optional resistor in series with BST allows the DH pullup current to be adjusted (Figure 5). This technique of slowing the LX rise time can be used to prevent accidental turn-on of the low-side MOSFET due to excessive gate-drain capacitance.
23	LX	Inductor Connection. LX serves as the lower supply rail for the DH high-side gate driver. Also used for the noninverting input to the current-limit comparator, as well as the skip-mode zero-crossing comparator.
24	DH	High-Side Gate-Driver Output. Swings LX to BST.

Standard Application Circuit

The standard application circuit (Figure 1) generates a low-voltage, high-power rail for supplying up to 7A to the core CPU V_{CC} in a notebook computer. This DC-DC converter steps down a battery or AC adapter voltage to sub-2V levels with high efficiency and accuracy, and represents a good compromise between size, efficiency, and cost.

See the MAX1710 EV kit manual for a list of components and suppliers.

Detailed Description

The MAX1710/MAX1711/MAX1712 buck controllers are targeted for low-voltage, high-current CPU power supplies for notebook computers. CPU cores typically exhibit 0A to 10A or greater load steps when the clock is throttled. The proprietary Quick-PWM pulse-width modulator in the MAX1710/MAX1711/MAX1712 is specifically designed for handling these fast load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency cur-

MAX1710/MAX1711/MAX1712

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MAX1710/MAX1711/MAX1712

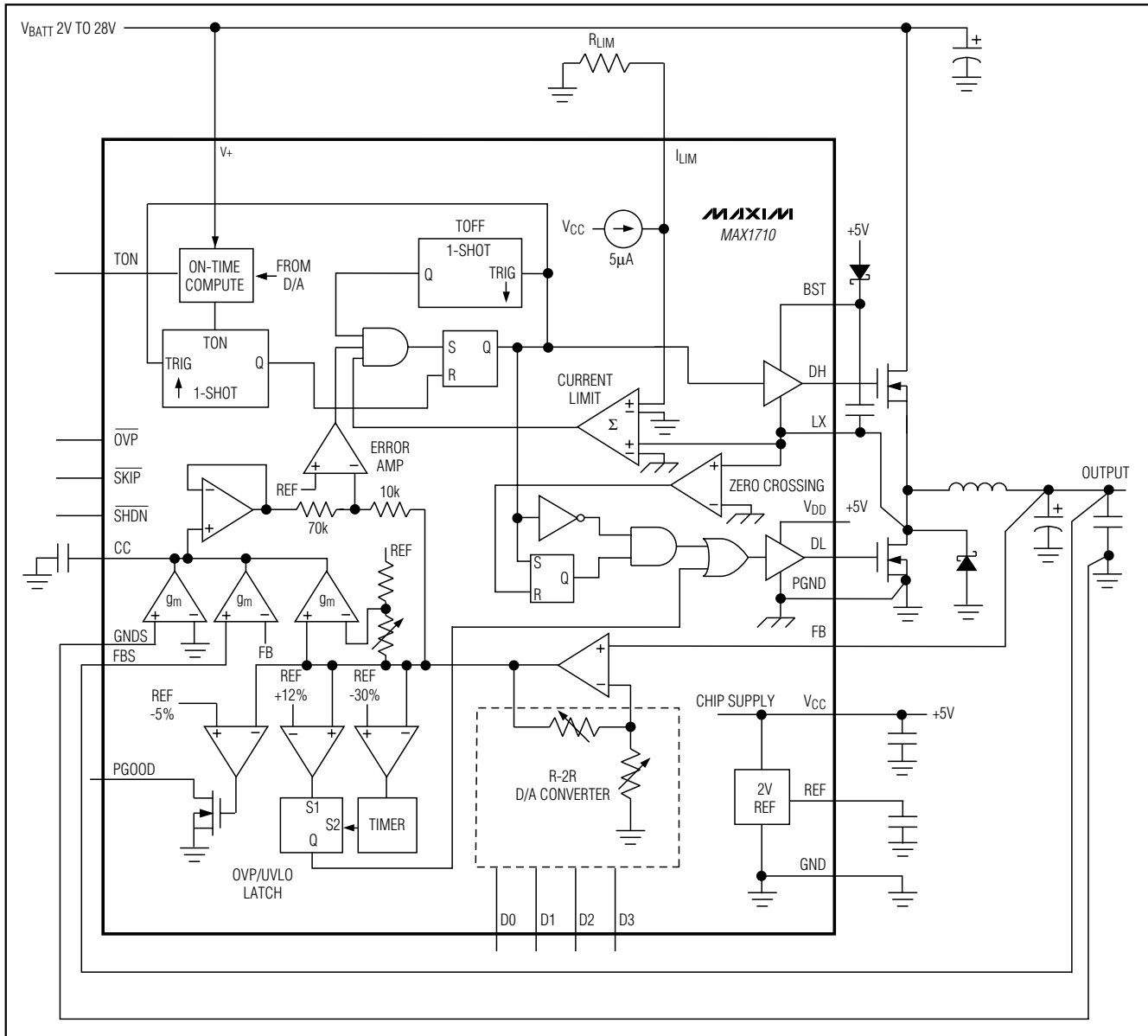


Figure 2. MAX1710 Functional Diagram

$$I_{BIAS} = I_{CC} + f \times (Q_{G1} + Q_{G2}) = 15\text{mA to } 30\text{mA (typ)}$$

where I_{CC} is $600\mu\text{A}$ (typ), f is the switching frequency, and Q_{G1} and Q_{G2} are the MOSFET data sheet total gate-charge specification limits at $V_{GS} = 5\text{V}$.

Free-Running, Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is an almost fixed-frequency, constant-on-time current-mode type with volt-

age feed-forward (Figure 2). This architecture relies on the filter capacitor's ESR to act as the current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (400ns typ). The on-time one-shot is triggered if the error comparator is low, the

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Table 1. MAX1710 FB Output Voltage DAC Codes

D3	D2	D1	D0	OUTPUT VOLTAGE (V)
0	0	0	0	2.00
0	0	0	1	1.95
0	0	1	0	1.90
0	0	1	1	1.85
0	1	0	0	1.80
0	1	0	1	1.75
0	1	1	0	1.70
0	1	1	1	1.65
1	0	0	0	1.60
1	0	0	1	1.55
1	0	1	0	1.50
1	0	1	1	1.45
1	1	0	0	1.40
1	1	0	1	1.35
1	1	1	0	1.30
1	1	1	1	1.25

low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time One-Shot (TON)

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltage. The high-side switch on-time is inversely proportional to the battery voltage as measured by the V₊ input, and directly proportional to the output voltage as set by the DAC code. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: first, the frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band; second, the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple:

$$\text{On-Time} = K (V_{\text{OUT}} + 0.075\text{V}) / V_{\text{IN}}$$

where K is set by the TON pin-strap connection and 0.075V is an approximation to accommodate for the expected drop across the low-side MOSFET switch. One-shot timing error increases for the shorter on-time

Table 2. MAX1711 FB Output Voltage DAC Codes

D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
0	0	0	0	0	2.00
0	0	0	0	1	1.95
0	0	0	1	0	1.90
0	0	0	1	1	1.85
0	0	1	0	0	1.80
0	0	1	0	1	1.75
0	0	1	1	0	1.70
0	0	1	1	1	1.65
0	1	0	0	0	1.60
0	1	0	0	1	1.55
0	1	0	1	0	1.50
0	1	0	1	1	1.45
0	1	1	0	0	1.40
0	1	1	0	1	1.35
0	1	1	1	0	1.30
0	1	1	1	1	Shutdown3*
1	0	0	0	0	1.275
1	0	0	0	1	1.250
1	0	0	1	0	1.225
1	0	0	1	1	1.200
1	0	1	0	0	1.175
1	0	1	0	1	1.150
1	0	1	1	0	1.125
1	0	1	1	1	1.100
1	1	0	0	0	1.075
1	1	0	0	1	1.050
1	1	0	1	0	1.025
1	1	0	1	1	1.000
1	1	1	0	0	0.975
1	1	1	0	1	0.950
1	1	1	1	0	0.925
1	1	1	1	1	Shutdown3*

*See Table 4.

settings due to fixed propagation delays and is approximately $\pm 12.5\%$ at 550kHz and 400kHz, and $\pm 10\%$ at the two slower settings. This translates to reduced switching-frequency accuracy at higher frequencies (Table 5). Switching frequency increases as a function of load current due to the increasing drop across the low-side

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Table 3. MAX1712 FB Output Voltage DAC Codes (VRM 9.0)

D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
0	0	0	0	0	1.850
0	0	0	0	1	1.825
0	0	0	1	0	1.800
0	0	0	1	1	1.775
0	0	1	0	0	1.750
0	0	1	0	1	1.725
0	0	1	1	0	1.700
0	0	1	1	1	1.675
0	1	0	0	0	1.650
0	1	0	0	1	1.625
0	1	0	1	0	1.600
0	1	0	1	1	1.575
0	1	1	0	0	1.550
0	1	1	0	1	1.525
0	1	1	1	0	1.500
0	1	1	1	1	1.475
1	0	0	0	0	1.450
1	0	0	0	1	1.425
1	0	0	1	0	1.400
1	0	0	1	1	1.375
1	0	1	0	0	1.350
1	0	1	0	1	1.325
1	0	1	1	0	1.300
1	0	1	1	1	1.275
1	1	0	0	0	1.250
1	1	0	0	1	1.225
1	1	0	1	0	1.200
1	1	0	1	1	1.175
1	1	1	0	0	1.150
1	1	1	0	1	1.125
1	1	1	1	0	1.100
1	1	1	1	1	Shutdown3*

*See Table 4.

MOSFET, which causes a faster inductor-current discharge ramp. The on-times guaranteed in the *Electrical Characteristics* are influenced by switching delays in the external high-side power MOSFET. The exact switching frequency will depend on gate charge, internal gate

resistance, source inductance, and DH output drive characteristics.

Two external factors that can influence switching-frequency accuracy are resistive drops in the two conduction loops (including inductor and PC board resistance) and the dead-time effect. These effects are the largest contributors to the change of frequency with changing load current. The dead-time effect is a notable discontinuity in the switching frequency as the load current is varied (see *Typical Operating Characteristics*). It occurs whenever the inductor current reverses, most commonly at light loads with SKIP high. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the low-to-high dead time. For loads above the critical conduction point, the actual switching frequency is:

$$f = \frac{V_{OUT} + V_{DROP1}}{t_{ON}(V_{IN} + V_{DROP2})}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the resistances in the charging path, and t_{ON} is the on-time calculated by the MAX1710/MAX1711/MAX1712.

Integrator Amplifiers (CC)

There are three integrator amplifiers that provide a fine adjustment to the output regulation point. One amplifier monitors the difference between GNDS and GND, while another monitors the difference between FBS and FB. The third amplifier integrates the difference between REF and the DAC output. These three transconductance amplifiers' outputs are directly summed inside the chip, so the integration time constant can be set easily with a capacitor. The g_m of each amplifier is 160 μ mho (typ). The integrator block has an ability to move and correct the output voltage by about -2%, +4%. For each amplifier, the differential input voltage range is about ± 50 mV total, including DC offset and AC ripple. The voltage gain of each integrator is about 80V/V.

The FBS amplifier corrects for DC voltage drops in PC board traces and connectors in the output bus path between the DC-DC converter and the load. The GNDS amplifier performs a similar DC correction task for the output ground bus. The third amplifier provides an averaging function that forces V_{OUT} to be regulated at the average value of the output ripple waveform. If the integrator amplifiers are disabled, V_{OUT} is regulated at the valleys of the output ripple waveform. This creates a slight load-regulation characteristic in which the output

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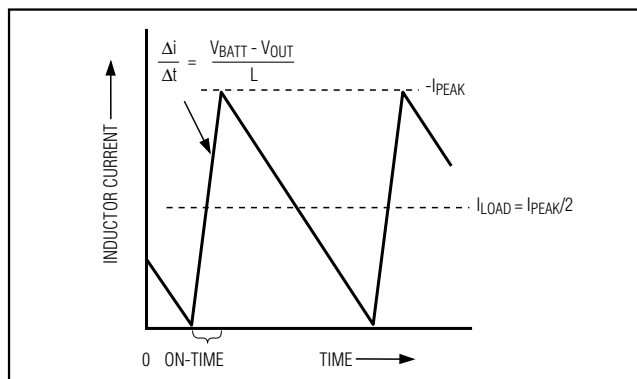


Figure 3. Pulse-Skipping/Discontinuous Crossover Point

voltage rises approximately 1% (up to 1/2 the peak amplitude of the ripple waveform as a limit) when under light loads.

Integrators have both beneficial and detrimental characteristics. While they do correct for drops due to DC bus resistance and tighten the DC output voltage tolerance limits by averaging the peak-to-peak output ripple, they can interfere with achieving the fastest possible load-transient response. The fastest transient response is achieved when all three integrators are disabled. This works very well when the MAX1710/MAX1711/MAX1712 circuit can be placed very close to the CPU.

There is often a connector, or at least many milliohms of PC board trace resistance, between the DC-DC converter and the CPU. In these cases, the best strategy is to place most of the bulk bypass capacitors close to the CPU, with just one capacitor on the other side of the connector near the MAX1710/MAX1711/MAX1712 to control ripple if the CPU card is unplugged. In this situation, the remote-sense lines and integrators provide a real benefit.

When FBS is connected to VCC so that all three integrators are disabled, CC can be left unconnected, which eliminates a component.

Automatic Pulse-Skipping Switchover

At light loads, an inherent automatic switchover to PFM takes place. This switchover is effected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the "critical conduction" point; see Continuous to Discontinuous Inductor Current Point vs. Input Voltage graph in the *Typical Operating Characteristics*). For a battery range of 7V to 24V, this

threshold is relatively constant, with only a minor dependence on battery voltage.

$$I_{\text{LOAD(SKIP)}} \approx \frac{K}{2L}$$

where K is the On-Time Scale factor (Table 6). The load-current level at which PFM/PWM crossover occurs, $I_{\text{LOAD(SKIP)}}$, is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value (Figure 3). For example, in the standard application circuit with $t_{\text{ON}} = 300\text{ns}$ at 24V, $V_{\text{OUT}} = 2\text{V}$, and $L = 2\mu\text{H}$, switchover to pulse-skipping operation occurs at $I_{\text{LOAD}} = 1.65\text{A}$ or about 1/4 full load. The crossover point occurs at an even lower value if a swinging (soft-saturation) inductor is used.

The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency can be made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input voltage levels).

Forced-PWM Mode ($\overline{\text{SKIP}} = \text{High}$)

The low-noise, forced-PWM mode ($\overline{\text{SKIP}}$ driven high) disables the zero-crossing comparator, which controls the low-side switch on-time. This causes the low-side gate-drive waveform to become the complement of the high-side gate-drive waveform. This in turn causes the inductor current to reverse at light loads, as the PWM loop strives to maintain a duty ratio of $V_{\text{OUT}}/V_{\text{IN}}$. The benefit of forced-PWM mode is to keep the switching frequency fairly constant, but it comes at a cost: the no-load battery current can be as high as 40mA or more.

Forced-PWM mode is most useful for reducing audio-frequency noise, improving load-transient response, providing sink-current capability for dynamic output voltage adjustment, and improving the cross-regulation of multiple-output applications that use a flyback transformer or coupled inductor.

Current-Limit Circuit (ILIM)

The current-limit circuit employs a unique "valley" current-sensing algorithm that uses the on-state resistance of the low-side MOSFET as a current-sensing element. If the current-sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle (Figure 4). The actual peak current is greater than the current-limit threshold by an amount equal to the induc-

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tor ripple current. Therefore the exact current-limit characteristic and maximum load capability are a function of the MOSFET on-resistance, inductor value, and battery voltage. The reward for this uncertainty is robust, loss-less overcurrent sensing. When combined with the UVP protection circuit, this current-limit method is effective in almost every circumstance.

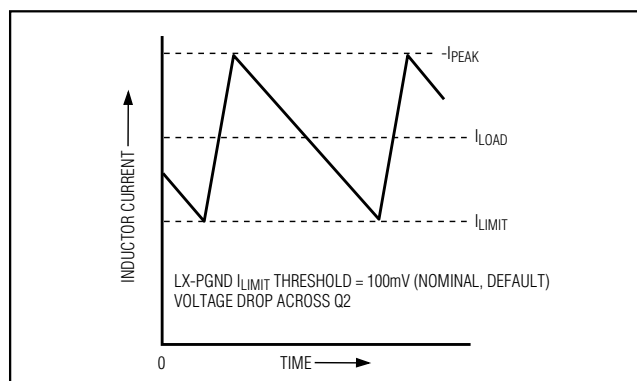


Figure 4. "Valley" Current-Limit Threshold Point

There is also a negative current limit that prevents excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit, and therefore tracks the positive current limit when I_{LIM} is adjusted.

The current-limit threshold can be adjusted with an external resistor (R_{LIM}) at I_{LIM} . A precision $5\mu A$ pullup current source at I_{LIM} sets a voltage drop on this resistor, adjusting the current-limit threshold from 50mV to 200mV. In the adjustable mode, the current-limit threshold voltage is precisely 1/10th the voltage seen at I_{LIM} . Therefore, choose R_{LIM} equal to $2k\Omega/mV$ of the current-limit threshold. The threshold defaults to 100mV when I_{LIM} is tied to V_{CC} . The logic threshold for switchover to the 100mV default value is approximately $V_{CC} - 1V$.

The adjustable current limit can accommodate MOSFETs with atypical on-resistance characteristics (see *Design Procedure*).

A capacitor in parallel with R_{LIM} can provide a variable soft-start function.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors don't corrupt the current-sense signals seen by LX and PGND. The IC must be mounted close to the low-side MOSFET with short, direct traces making a Kelvin-sense connection to the source and drain terminals.

MOSFET Gate Drivers (DH, DL)

The DH and DL drivers are optimized for driving moderate-size, high-side and larger, low-side power MOSFETs. This is consistent with the low duty factor seen in the notebook CPU environment, where a large $V_{BATT} - V_{OUT}$ differential exists. An adaptive dead-time circuit monitors the DL output and prevents the high-side FET from turning on until DL is fully off. There must be a low-resistance, low-inductance path from the DL driver to the MOSFET gate in order for the adaptive dead-time circuit to work properly. Otherwise, the sense circuitry in the MAX1710/MAX1711/MAX1712 will interpret the MOSFET gate as "off" while there is actually still charge left on the gate. Use very short, wide traces measuring 10 to 20 squares (50 to 100 mils wide if the MOSFET is 1 inch from the MAX1710/MAX1711/MAX1712).

The dead time at the other edge (DH turning off) is determined by a fixed 35ns (typ) internal delay.

The internal pulldown transistor that drives DL low is robust, with a 0.5Ω (typ) on-resistance. This helps prevent DL from being pulled up during the fast rise time of the inductor node, due to capacitive coupling from the drain to the gate of the massive low-side synchronous-rectifier MOSFET. However, you might still encounter some combinations of high- and low-side FETs that will cause excessive gate-drain coupling, which can lead to efficiency-killing, EMI-producing shoot-through currents. This can often be remedied by adding a resistor in series with BST, which increases the turn-on time of the high-side FET without degrading the turn-off time (Figure 5).

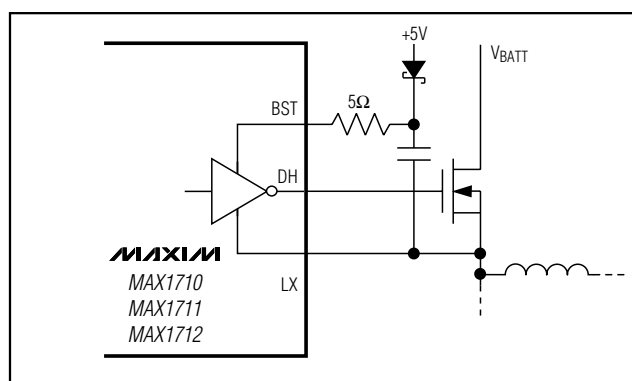


Figure 5. Reducing the Switching-Node Rise Time

DAC Converter (D0-D4)

The DAC programs the output voltage. It receives a digital code from pins on the CPU module that are either hard-wired to GND or left open-circuit. The MAX1710/MAX1711/MAX1712 contain weak internal

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Table 4. Operating Mode Truth Table

SHDN	SKIP	OVP	DL	MODE	COMMENTS
0	X	0	High	Shutdown1	Low-power shutdown state. DL is forced to V _{DD} , enforcing OVP. I _{CC} < 1μA typ.
0	X	1	Low	Shutdown2	Low-power shutdown state. DL is forced to GND, disabling OVP. I _{CC} < 1μA typ. Exiting shutdown triggers a soft-start cycle.
1	X	X	Low	Shutdown3 (MAX1711/ MAX1712)	DAC code = X1111 (MAX1711), DAC code = 11111 (MAX1712) (Table 2). DL is forced to PGND, DH is forced to LX. The MAX1711/MAX1712 eventually goes into UVP fault mode as the load current discharges the output.
1	Below GND	X	Switching	No fault	Test mode with OVP, UVP, and thermal faults disabled and latches cleared. Otherwise normal operation, with automatic PWM/PFM switchover for pulse skipping at light loads (Figure 6).
1	X	1	Switching	No OVP	OVP faults disabled and OVP latch cleared. Otherwise normal operation, with SKIP controlling PWM/PFM switchover.
1	V _{CC}	X	Switching	Run (PWM), Low Noise	Low-noise operation with no automatic switchover. Fixed-frequency PWM action is forced regardless of load. Inductor current reverses at light load levels. I _{CC} draw = 750μA typ. I _{DD} draw = 15mA typ.
1	GND	X	Switching	Run (PFM/PWM)	Normal operation with automatic PWM/PFM switchover for pulse skipping at light loads. I _{CC} = 600μA typ. I _{DD} draw = load dependent.
1	X	X	High	Fault	Fault latch has been set by OVP, output UVLO, or thermal shutdown. Device will remain in FAULT mode until V _{CC} power is cycled, SKIP is forced below ground, or SHDN is toggled.

Table 5. Frequency Selection Guidelines

FREQUENCY (kHz)	TYPICAL APPLICATION	COMMENT
200	4-cell Li+ notebook CPU core	Use for absolute best efficiency.
300	4-cell Li+ notebook CPU core	Considered mainstream by current standards.
400	3-cell Li+ notebook CPU core	Useful in 4-cell systems for lighter loads than the CPU or where size is key.
550	+5V-input notebook CPU core	Good operating point for compound buck designs or desktop circuits.

pullups on each input in order to eliminate external resistors.

When changing MAX1710 DAC codes while powered up, the over/undervoltage protection features can be activated if the code is changed more than 1LSB at a time. For applications needing the capability of changing DAC codes “on-the-fly,” use the MAX1711/MAX1712.

POR, UVLO, and Soft-Start

Power-on reset (POR) occurs when V_{CC} rises above approximately 2V, resetting the fault latch and soft-start counter, and preparing the PWM for operation. V_{CC} undervoltage lockout (UVLO) circuitry inhibits switching and forces the DL gate driver high (in order to enforce output overvoltage protection) until V_{CC} rises above 4.2V, whereupon an internal digital soft-start timer begins to ramp up the maximum allowed current limit. The ramp occurs in five steps: 20%, 40%, 60%, 80%, and 100%, with 100% current available after 1.7ms ±50%.

A continuously adjustable, analog soft-start function can be realized by adding a capacitor in parallel with R_{LIM} at ILIM. This soft-start method requires a minimum interval between power-down and power-up to allow R_{LIM} to discharge the capacitor.

Power-Good Output (PGOOD)

The output (FB) is continuously monitored for undervoltage by the PGOOD comparator, except in shutdown or standby mode. The -5% undervoltage trip threshold is measured with respect to the nominal unloaded output voltage, as set by the DAC. If the DAC code increases in steps greater than 1LSB, it is likely that PGOOD will momentarily go low. In shutdown and standby modes, PGOOD is actively held low. The PGOOD output is a true

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open-drain type with no parasitic ESD diodes. Note that the PGOOD undervoltage detector is completely independent of the output UVP fault detector.

Output Overvoltage Protection (OVP)

The OVP circuit is designed to protect against a shorted high-side MOSFET by drawing high current and blowing the battery fuse. The FB node is continuously monitored for overvoltage. The overvoltage trip threshold tracks the DAC code setting. If the output is more than 12.5% above the nominal regulation point for the MAX1710 (2.25V absolute for the MAX1711/MAX1712), overvoltage protection OVP is triggered and the circuit shuts down. The DL low-side gate-driver output is then latched high until $\overline{\text{SHDN}}$ is toggled or V_{CC} power is cycled below 1V. This action turns on the synchronous-rectifier MOSFET with 100% duty and, in turn, rapidly discharges the output filter capacitor and forces the output to ground.

If the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery fuse will blow. Note that DL going high can have the effect of causing output polarity reversal, due to energy stored in the output LC at the instant OVP activates. If the load can't tolerate being forced to a negative voltage, it may be desirable to place a power Schottky diode across the output to act as a reverse-polarity clamp (Figure 1). The MAX1710/MAX1711/MAX1712 themselves can be affected by the FB pin going below ground, with the negative voltage coupling into SHDN. It may be necessary to add 1k Ω resistors in series with FB and FBS (Figure 7).

DL is also kept high continuously when V_{CC} UVLO is active as well as in Shutdown1 mode (Table 4). Overvoltage protection can be defeated via the $\overline{\text{OVP}}$ input (MAX1710 only) or via a $\overline{\text{SKIP}}$ test mode (see *Pin Description*).

Output Undervoltage Protection (UVP)

The output UVP function is similar to foldback current limiting, but employs a timer rather than a variable current limit. If the MAX1710 output (FB) is under 70% of the nominal value 20ms after coming out of shutdown, the PWM is latched off and won't restart until V_{CC} power is cycled or $\overline{\text{SHDN}}$ is toggled. For the MAX1711/MAX1712, the nominal UVP trip threshold is fixed at 0.8V.

No-Fault Test Mode

The over/undervoltage protection features can complicate the process of debugging prototype breadboards since there are (at most) a few milliseconds in which to determine what went wrong. Therefore, a test mode is provided to totally disable the OVP, UVP, and thermal shutdown features, and clear to the fault latch if it has

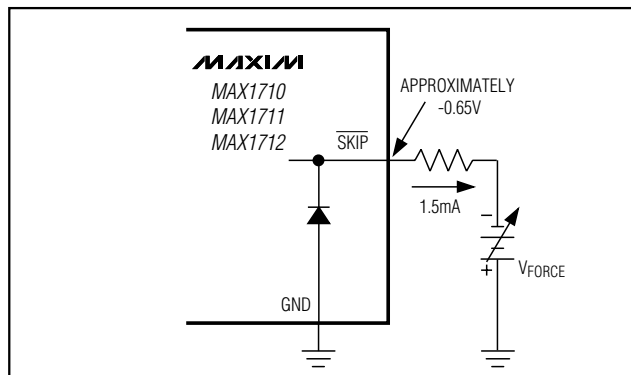


Figure 6. Disabling Over/Undervoltage Protection (Test Mode)

been previously set. The PWM operates as if $\overline{\text{SKIP}}$ were grounded (PFM/PWM mode).

The no-fault test mode is entered by sinking 1.5mA from $\overline{\text{SKIP}}$ via an external negative voltage source in series with a resistor (Figure 6). $\overline{\text{SKIP}}$ is clamped to GND with a silicon diode, so choose the resistor value equal to $(V_{\text{FORCE}} - 0.65V) / 1.5\text{mA}$.

Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- 1) **Input voltage range.** The maximum value ($V_{\text{BATT}}(\text{MAX})$) must accommodate the worst-case high AC adapter voltage. The minimum value ($V_{\text{BATT}}(\text{MIN})$) must account for the lowest battery voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- 2) **Maximum load current.** There are two values to consider. The *peak load current* ($I_{\text{LOAD}}(\text{MAX})$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The *continuous load current* (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Modern notebook CPUs generally exhibit $I_{\text{LOAD}} = I_{\text{LOAD}}(\text{MAX}) \times 80\%$.
- 3) **Switching frequency.** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input

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voltage, due to MOSFET switching losses that are proportional to frequency and V_{BATT}^2 . The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical (Table 5).

- 4) **Inductor operating point.** This choice provides trade-offs between size vs. efficiency. Low inductor values cause large ripple currents, resulting in the smallest size, but poor efficiency and high output noise. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit.

The MAX1710/MAX1711/MAX1712s' pulse-skipping algorithm initiates skip mode at the critical-conduction point. So, the inductor operating point also determines the load-current value at which PFM/PWM switchover occurs. The optimum point is usually found between 20% and 50% ripple current.

The inductor ripple current also impacts transient-response performance, especially at low $V_{BATT} - V_{OUT}$ differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time:

$$V_{SAG} = \frac{(\Delta I_{LOAD(MAX)})^2 \times L}{2 \times C_F \times DUTY (V_{BATT(MIN)} - V_{OUT})}$$

Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as follows:

$$L = \frac{V_{OUT}}{f \times LIR \times I_{LOAD(MAX)}}$$

Example: $I_{LOAD(MAX)} = 7A$, $V_{OUT} = 2V$, $f = 300kHz$, 50% ripple current or LIR = 0.5:

$$L = \frac{2V}{300kHz \times 0.5 \times 7A} = 1.9\mu H (2\mu H)$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is cheap and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (IPEAK):

$$I_{PEAK} = I_{LOAD(MAX)} + (LIR / 2) \times I_{LOAD(MAX)}$$

Setting the Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half of the ripple current, therefore:

$$I_{LIMIT(LOW)} > I_{LOAD(MAX)} - (LIR / 2) \times I_{LOAD(MAX)}$$

where $I_{LIMIT(LOW)}$ = minimum current-limit threshold voltage divided by the $R_{DS(ON)}$ of Q2. For the MAX1710, the minimum current-limit threshold (100mV default setting) is 90mV. Use the worst-case maximum value for $R_{DS(ON)}$ from the MOSFET Q2 data sheet, and add some margin for the rise in $R_{DS(ON)}$ with temperature. A good general rule is to allow 0.5% additional resistance for each °C of temperature rise.

Examining the 7A notebook CPU circuit example with a maximum $R_{DS(ON)} = 15m\Omega$ at high temperature reveals the following:

$$I_{LIMIT(LOW)} = 90mV / 15m\Omega = 6A$$

6A is greater than the valley current of 5.25A, so the circuit can easily deliver the full rated 7A using the default 100mV nominal ILIM threshold.

When adjusting the current limit, use a 1% tolerance R_{LIM} resistor to prevent a significant increase of errors in the current-limit tolerance.

Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance value must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the OVP circuit.

In CPU V_{CORE} converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \leq \frac{V_{DIP}}{I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple:

$$R_{ESR} \leq \frac{V_{p-p}}{LIR \times I_{LOAD(MAX)}}$$

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The actual microfarad capacitance value required relates to the physical size needed to achieve low ESR, as well as to the chemistry of the capacitor technology. Thus, the capacitor is usually selected by ESR and voltage rating rather than by capacitance value (this is true of tantalums, OS-CONs, and other electrolytics).

When using low-capacity filter capacitors such as ceramic or polymer types, capacitor size is usually determined by the capacity needed to prevent the overvoltage protection circuit from being tripped when transitioning from a full-load to a no-load condition. The capacitor must be large enough to prevent the inductor's stored energy from launching the output above the overvoltage protection threshold. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see also VSAG equation under *Design Procedure*).

With integrators disabled, the amount of overshoot due to stored inductor energy can be calculated as:

$$\Delta V = \sqrt{\left(\frac{C_{OUT} \times V_{OUT}^2 + L \times I_{PEAK}^2}{C_{OUT}} \right)} - V_{OUT}$$

where I_{PEAK} is the peak inductor current. To absolutely minimize the overshoot, disable the integrator first, since the inherent delay of the integrator can cause extra "run-on" switching cycles to occur after the load change.

Output Capacitor Stability Considerations

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation:

$$f_{ESR} = \frac{f}{\pi}$$

$$\text{where } f_{ESR} = \frac{1}{2 \times \pi \times R_{ESR} \times C_F}$$

For a typical 300kHz application, the ESR zero frequency must be well below 95kHz, preferably below 50kHz. Tantalum and OS-CON capacitors in widespread use at the time of publication have typical ESR zero frequencies of 15kHz. In the design example used for inductor selection, the ESR needed to support 50mVp-p ripple is $50\text{mV}/3.5\text{A} = 14.2\text{m}\Omega$. Three 470 $\mu\text{F}/4\text{V}$ Kemet T510 low-ESR tantalum capacitors in parallel provide 15m Ω max ESR. Their typical combined ESR results in a zero at 14.1kHz, well within the bounds of stability.

Don't put high-value ceramic capacitors directly across the fast feedback inputs (FB to GND) without taking precautions to ensure stability. Large ceramic capacitors can have a high ESR zero frequency and cause erratic,

unstable operation. However, it's easy to add enough series resistance by placing the capacitors a couple of inches downstream from the junction of the inductor and FB pin (see the *All-Ceramic-Capacitor Application* section).

Unstable operation manifests itself in two related but distinctly different ways: double-pulsing and fast-feedback loop instability.

Double-pulsing occurs due to noise on FB or because the ESR is so low that there isn't enough voltage ramp in the output voltage (FB) signal. This "fools" the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability, which is caused by insufficient ESR.

Loop instability can result in oscillations at the output after line or load perturbations that can trip the overvoltage protection latch or cause the output voltage to fall below the tolerance limit.

The easiest method for checking stability is to apply a very fast zero-to-max load transient (see MAX1710 Evaluation Kit manual) and carefully observe the output voltage ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Don't allow more than one cycle of ringing after the initial step-response under- or overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to power-up surge currents:

$$I_{RMS} = I_{LOAD} \left(\frac{\sqrt{V_{OUT}(V_{BATT} - V_{OUT})}}{V_{BATT}} \right)$$

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability (>5A) when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

For maximum efficiency, choose a high-side MOSFET (Q1) that has conduction losses equal to the switching losses at the optimum battery voltage (15V). Check to ensure that the conduction losses at minimum input voltage don't exceed the package thermal limits or violate the overall thermal budget. Check to ensure that conduction losses plus switching losses at the maximum

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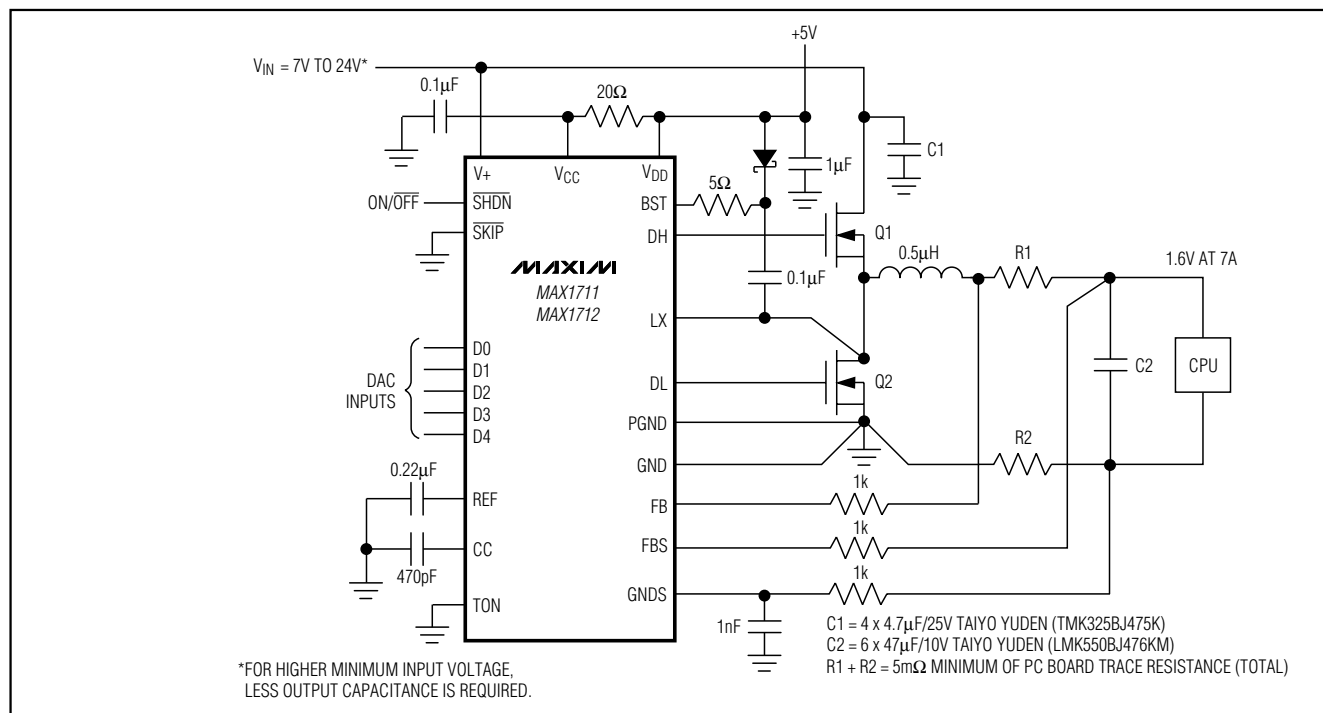


Figure 7. All-Ceramic-Capacitor Application

Table 6. Approximate K-Factors Errors

TON SETTING (kHz)	K FACTOR (µs-V)	APPROXIMATE K-FACTOR ERROR (%)	MIN VBATT AT VOUT = 2V (V)
200	5	±10	2.6
300	3.3	±10	2.9
400	2.5	±12.5	3.2
550	1.8	±12.5	3.6

input voltage don't exceed the package ratings or violate the overall thermal budget.

Choose a low-side MOSFET (Q2) that has the lowest possible $R_{DS(ON)}$, comes in a moderate to small package (i.e., SO-8), and is reasonably priced. Ensure that the MAX1710/MAX1711/MAX1712 DL gate driver can drive Q2; in other words, check that the gate isn't pulled up by the high-side switch turning on due to parasitic drain-to-gate capacitance, causing cross-conduction problems. Switching losses aren't an issue for the low-side MOSFET since it's a zero-voltage switched device when used in the buck topology.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET, the worst-case power dissipation due to resistance occurs at minimum battery voltage:

$$PD(Q1) = (V_{OUT} / V_{BATT(MIN)}) \times I_{LOAD}^2 \times R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired in order to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. Again, the optimum occurs when the switching (AC) losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses don't usually become an issue until the input is greater than approximately 15V.

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the CV^2F switching loss equation. If the high-side MOSFET you've chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when subjected to $V_{BATT(MAX)}$, you must reconsider your choice of MOSFET.

Calculating the power dissipation in Q1 due to switching losses is difficult, since it must allow for difficult-to-quantify

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fy factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including a sanity check using a thermocouple mounted on Q1:

$$PD(\text{switching}) = \frac{C_{RSS} \times V_{BATT(\text{MAX})}^2 \times f \times I_{LOAD}}{I_{GATE}}$$

where C_{RSS} is the reverse transfer capacitance of Q1 and I_{GATE} is the peak gate-drive source/sink current (1A typ).

For the low-side MOSFET, Q2, the worst-case power dissipation always occurs at maximum battery voltage:

$$PD(Q2) = (1 - V_{OUT} / V_{BATT(\text{MAX})}) \times I_{LOAD}^2 \times R_{DS(ON)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(\text{MAX})}$ but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, you must “overdesign” the circuit to tolerate $I_{LOAD} = I_{LIMIT(\text{HIGH})} + (LIR / 2) \times I_{LOAD(\text{MAX})}$, where $I_{LIMIT(\text{HIGH})}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. This means that the MOSFETs must be very well heatsinked. If short-circuit protection without overload protection is enough, a normal I_{LOAD} value can be used for calculating component stresses.

Choose a Schottky diode D1 having a forward voltage low enough to prevent the Q2 MOSFET body diode from turning on during the dead time. As a general rule, a diode having a DC current rating equal to 1/3 of the load current is sufficient. This diode is optional, and if efficiency isn't critical it can be removed.

Application Issues

Dropout Performance

The output voltage adjust range for continuous-conduction operation is restricted by the nonadjustable 500ns (max) minimum off-time one-shot. For best dropout performance, use the slowest (200kHz) on-time setting. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the T_{ON} K-factor. This error is higher at higher frequencies (Table 6). Also, keep in mind that transient response performance of buck regulators operated close to dropout is poor,

and bulk output capacitance must often be added (see V_{SAG} equation in the *Design Procedure*).

Dropout Design Example: $V_{BATT} = 3V$ min, $V_{OUT} = 2V$, $f = 300kHz$. The required duty is $(V_{OUT} + V_{SW}) / (V_{BATT} - V_{SW}) = (2V + 0.1V) / (3.0V - 0.1V) = 72.4\%$. The worst-case on-time is $(V_{OUT} + 0.075) / V_{BATT} \times K = 2.075V / 3V \times 3.35\mu s \times 90\% = 2.08\mu s$. The IC duty-factor limitation is:

$$DUTY = \frac{t_{ON(\text{MIN})}}{t_{ON(\text{MIN})} + t_{OFF(\text{MAX})}} = 2.08\mu s + 500ns = 80.6\%$$

which meets the required duty.

Remember to include inductor resistance and MOSFET on-state voltage drops (V_{SW}) when doing worst-case dropout duty-factor calculations.

All-Ceramic-Capacitor Application

Ceramic capacitors have advantages and disadvantages. They have ultra-low ESR, are noncombustible, are relatively small, and are nonpolarized. On the other hand, they're expensive and brittle, and their ultra-low ESR characteristic can result in excessively high ESR zero frequencies (affecting stability). In addition, they can cause output overshoot when going abruptly from full-load to no-load conditions, unless there are some bulk tantalum or electrolytic capacitors in parallel to absorb the stored energy in the inductor. In some cases, there may be no room for electrolytics, creating a need for a DC-DC design that uses nothing but ceramics.

The all-ceramic-capacitor application of Figure 7 has the same basic performance as the 7A Standard Application Circuit, but replaces the tantalum output capacitors with ceramics. This design relies on having a minimum of 5mΩ parasitic PC board trace resistance in series with the capacitor in order to reduce the ESR zero frequency. This small amount of resistance is easily obtained by locating the MAX1710/MAX1711/MAX1712 circuit 2 or 3 inches away from the CPU, and placing all the ceramic capacitors close to the CPU. Resistance values higher than 5mΩ just improve the stability (which can be observed by examining the load-transient response characteristic as shown in the *Typical Operating Characteristics*). Avoid adding excess PC board trace resistance because there's an efficiency penalty; 5mΩ is sufficient for the 7A circuit.

Output overshoot determines the minimum output capacitance requirement. In this example, the switching frequency has been increased to 550kHz and the inductor value has been reduced to 0.5μH (compared to 300kHz and 2μH for the standard 7A circuit) in order to

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minimize the energy transferred from inductor to capacitor during load-step recovery. Even so, the amount of overshoot is high enough (80mV) that for the MAX1710, it's wise to disable OVP or use the MAX1711/MAX1712 with their fixed 2.25V overvoltage protection threshold to avoid tripping the fault latch (see the overshoot equation in the *Output Capacitor Selection* section). The efficiency penalty for operating at 550kHz is about 2% to 3%, depending on the input voltage.

Two optional 1kΩ resistors are placed in series with FB and FBS. These resistors prevent the negative output voltage spike (that results from tripping OVP) from pulling SHDN low via its internal ESD diode, which tends to clear the fault latch, causing "hiccup" restarts.

Setting V_{OUT} with a Resistor-Divider

The output voltage can be adjusted with a resistor-divider rather than the DAC if desired (Figure 8). The drawback of this practice is that the on-time doesn't automatically receive correct compensation for changing output voltage levels. This can result in variable switching frequency as the resistor ratio is changed and/or excessive switching frequency. The equation for adjusting the output voltage is:

$$V_{OUT} = (V_{FB} - 1\%) \left(1 + \frac{R1}{R2} \right)$$

where V_{FB} is the currently selected DAC value. When using external resistors, FBS remote sensing is not recommended, but GNDS remote sensing is still possible. Connect FBS to FB and GNDS to remote ground location. In resistor-adjusted circuits, the DAC code should be set as close as possible to the actual output voltage so that the switching frequency doesn't become exces-

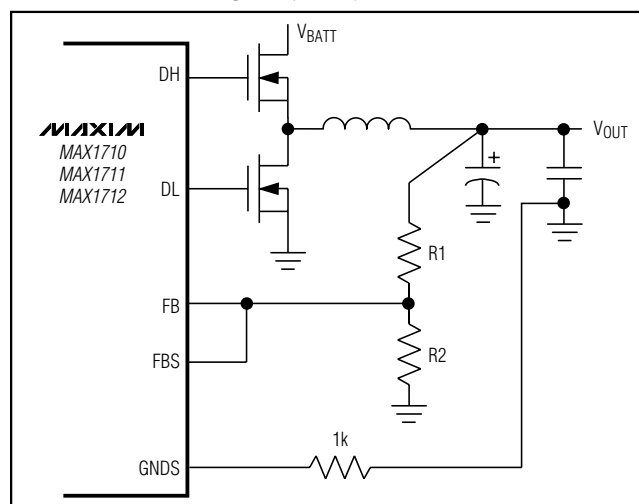


Figure 8. Setting V_{OUT} with a Resistor-Divider

sive. For highest accuracy, use the MAX1710 when adjusting V_{OUT} with external resistors. The MAX1710 FB node has very high impedance, while the MAX1711/MAX1712 have a 180kΩ ±35% FB impedance, which degrades V_{OUT} accuracy.

Adjusting V_{OUT} Above 2V

The feed-forward circuit that makes the on-time dependent on battery voltage maintains a nearly constant switching frequency as V_{IN} , I_{LOAD} , and the DAC code are changed. This works extremely well as long as FB is connected directly to the output.

When the output is adjusted higher than 2V with a resistor-divider, the switching frequency can be increased to relatively unreasonable levels as the actual off-time decreases and isn't compensated for by a change in on-time; 3.3V is about the maximum limit to the practical adjustment range. Even at the slowest TON setting and with the DAC set to 2V, the switching rate will exceed 600kHz.

The trip threshold for output overvoltage protection scales with the nominal output voltage setting.

2-Stage (5V-Powered) Notebook CPU Buck Regulator

The most efficient and overall cost-effective solution for stepping down a high-voltage battery to very low output voltage is to use a single-stage buck regulator that's powered directly from the battery. However, there may be situations where the battery bus can't be routed near the CPU, or where space constraints dictate the smallest possible local DC-DC converter. In such cases, the 5V-powered circuit of Figure 9 may be appropriate. The reduced input voltage allows a higher switching frequency and a much smaller inductor value.

Dynamic DAC Code Changes (MAX1711/MAX1712)

Changing the output voltage dynamically by switching DAC codes "on-the-fly" can be used to help make power-savings/performance trade-offs in the host system. Several important design issues arise from this practice.

First, know that attempting to slew the output upward quickly causes large current surges at the battery as the IC goes into output current limiting during the transition. Surge currents can be controlled either by counting the DAC code slowly (50kHz or slower rate suggested), or by modulating the I_{LIM} current-limit threshold.

The DAC inputs must be driven quickly to the new value so the device doesn't wrongly interpret a disallowed

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MAX1710/MAX1711/MAX1712

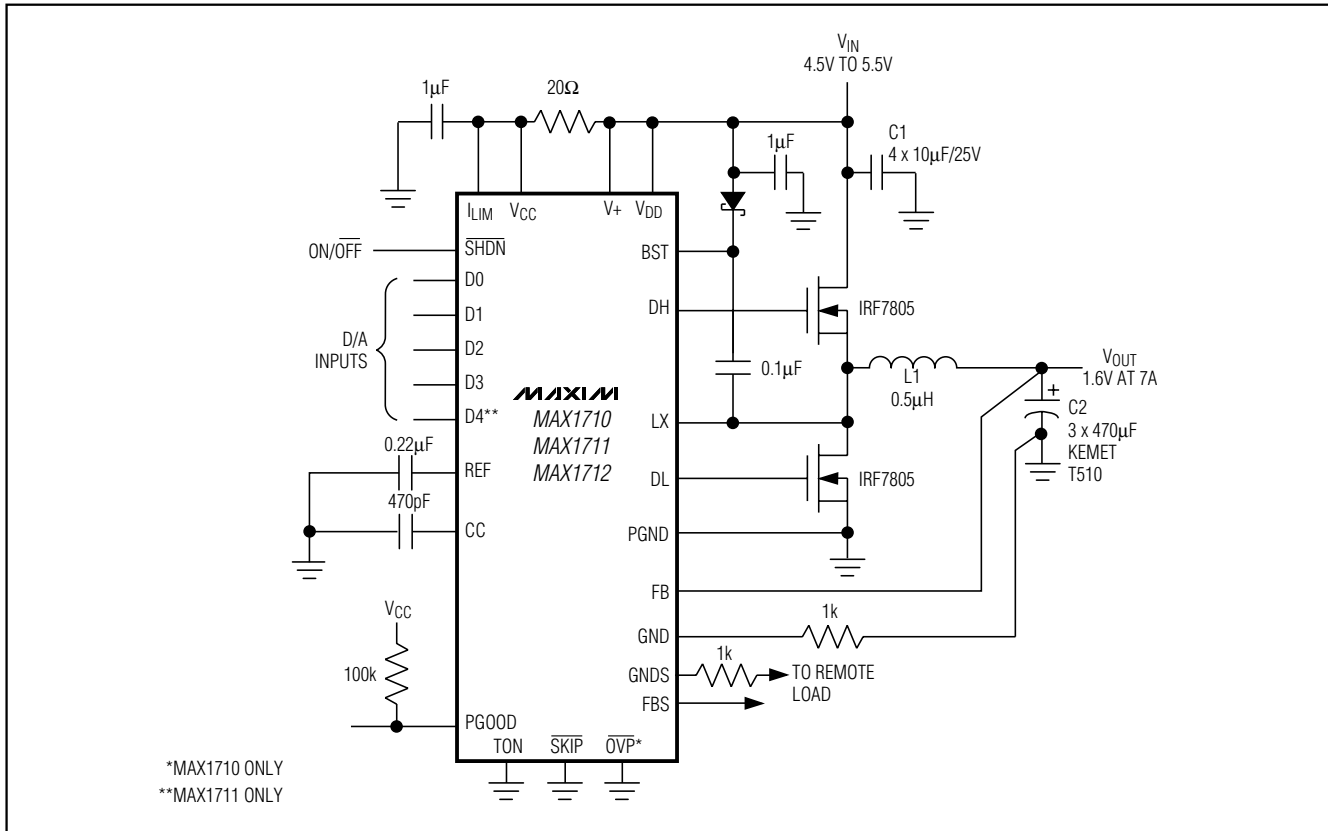


Figure 9. 5V-Powered, 7A CPU Buck Regulator

DAC code from the transitory value. Use 100ns maximum rise and fall times.

Selecting the output capacitors in dynamically adjusted V_{CORE} applications can be tricky due to trade-offs between capacitor capacity and ESR. In other words, if the capacitor has sufficiently low ESR to meet the load-transient response specification, its large capacity may cause excessive input surge currents. On the other hand, a purely ceramic capacitor may not have enough capacity to prevent overvoltage during the transition from full- to no-load condition (see the overshoot equation under *Output Capacitor Selection*). It may be necessary to mix capacitor types or use specialized capacitors such as those shown in Figure 7 in order to achieve the required ESR while staying within the min/max capacitance value window.

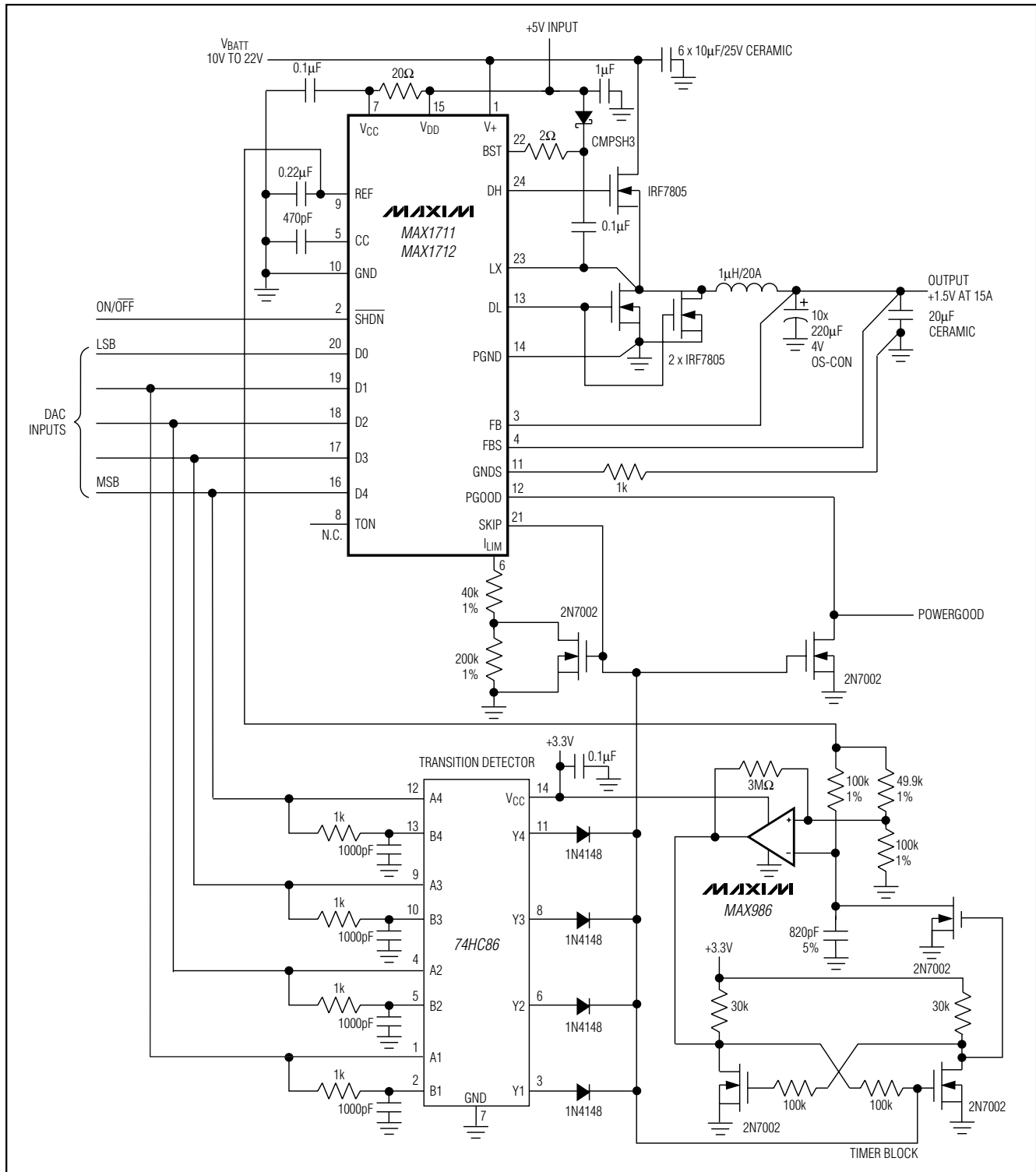
If the minimum load is very light, it may be necessary to assert forced PWM mode (via *SKIP*) during the transition period to guarantee some output sink current capability. Otherwise, the output voltage won't ramp downwards until pulled down by external load current.

Using forced PWM mode repeatedly to ensure sink current capability can have side effects, however. The energy taken from the output by the synchronous rectifier isn't lost, but is instead returned to the input. If the frequency of the high-to-low output voltage transition is high enough, efficiency will be degraded by the resistive "friction" losses associated with shuttling energy between input and output capacitors. Also, if the output is being overdriven by an external source (such as an external docking-station power supply), forced PWM mode may cause the battery voltage to become pumped up, possibly overvoltage the battery.

High-Power, Dynamically Adjustable CPU Application

The MAX1711/MAX1712 V_{CORE} regulator of Figure 10 is designed to have its output voltage switched between 1.3V and 1.45V in less than 100μs, while causing a minimum level of input surge current. To this end, the output capacitors were selected for having the correct value to a) support the needed ESR, b) prevent excess load-

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MAX1710/MAX1711/MAX1712

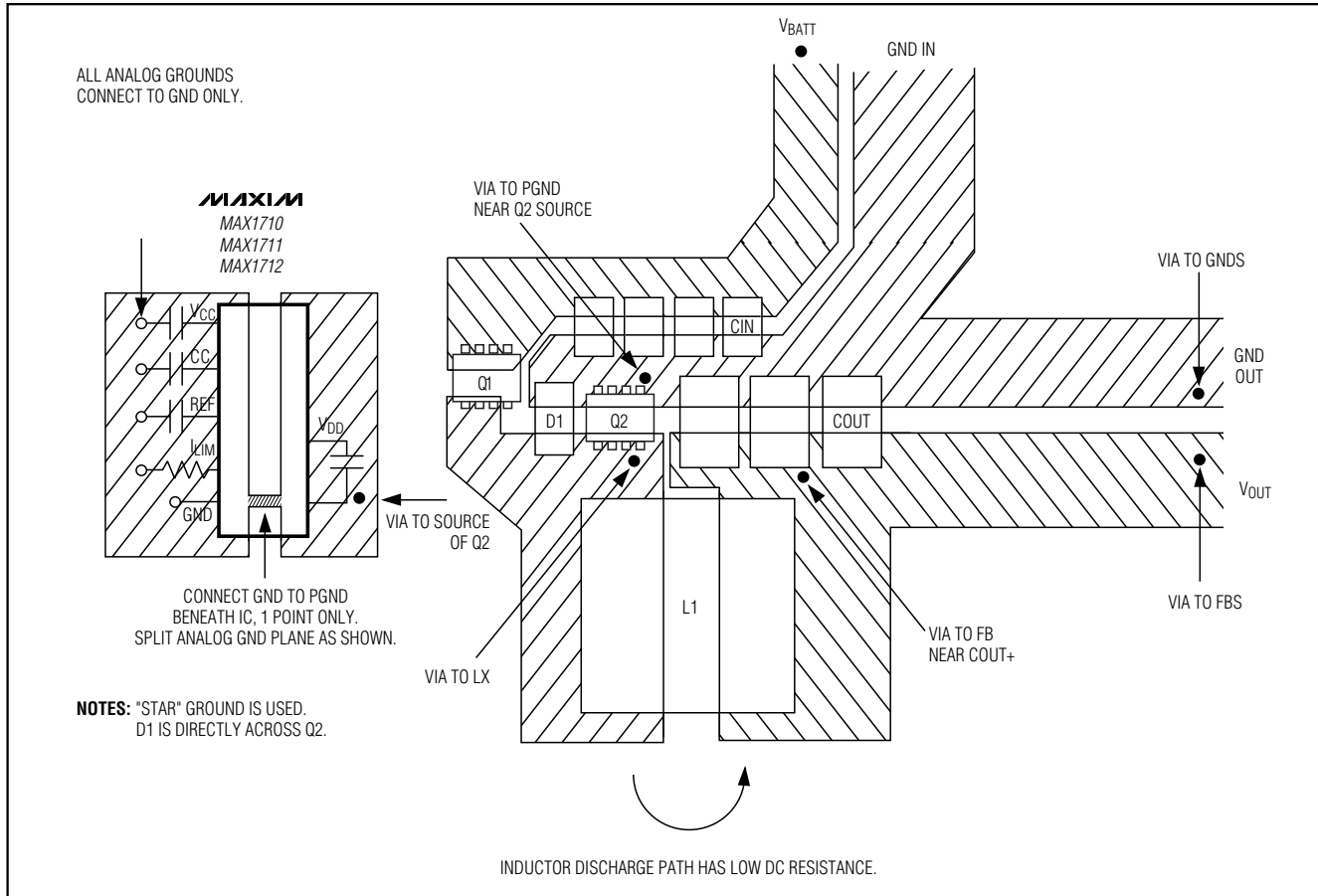


Figure 11. Power-Stage PC Board Layout Example

recovery overshoot, and c) minimize input surge currents.

The optional 74HC86 exclusive-OR gate detects code transitions on each of the four most-significant DAC inputs. The transition detector output goes to a precision pulse stretcher, a timer that extends the pulse for 75 μ s (nominal). This signal then feeds three circuits: the power-good detector, the $\overline{\text{SKIP}}$ input, and the ILIM current-limit control input, thus reducing the current-limit threshold during the transition interval (in order to reduce battery current surges). Likewise, $\overline{\text{SKIP}}$ going high asserts forced PWM mode in order to drag the output voltage down to the new value. Forced PWM mode is incompatible with good light-load efficiency due to inductor-current recirculation losses and gate-drive losses. Therefore, $\overline{\text{SKIP}}$ is driven high only during the 100 μ s max transition interval.

The power-good output signal is the logical OR of the 75 μ s timer signal and the MAX1711/MAX1712 PGOOD

signal. The internal PGOOD detector circuit monitors only output undervoltage; PGOOD will probably go low during upward transitions, but not downward. The final power-good output will always go low for at least 75 μ s due to the timer signal.

Load current capability is 15A peak and 12A continuous over a 10V to 22V input range. All three MOSFETs require good heatsinking. See the MAX1711 EV kit manual for a complete bill of materials.

PC Board Layout Guidelines

Careful PC board layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention (Figure 11). If possible, mount all of the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for good PC board layout:

High-Speed, Digitally Adjusted Step-Down Controllers for Notebook CPUs

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Connect GND and PGND together close to the IC. Carefully follow the grounding instructions under step 4 of the *Layout Procedure*.
- Keep the power traces and load connections short. This practice is essential for high efficiency. The use of thick copper PC boards (2 oz vs. 1 oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces is a difficult task that must be approached in terms of fractions of centimeters, where a single milliohm of excess trace resistance causes a measurable efficiency penalty.
- LX and PGND connections to Q2 for current limiting must be made using Kelvin sense connections in order to guarantee the current-limit accuracy. With SO-8 MOSFETs, this is best done by routing power to the MOSFETs from outside using the top copper layer, while tying in PGND and LX *inside* (underneath) the SO-8 package.
- When trade-offs in trace lengths must be made, it's preferable to allow the inductor charging path to be made longer than the discharge path. For example, it's better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Ensure that the FB connection to C_{OUT} is short and direct. However, in some cases it may be desirable to deliberately introduce some trace length between the FB inductor node and the output filter capacitor (see the *All-Ceramic-Capacitor Application* section).
- Route high-speed switching nodes away from sensitive analog areas (CC, REF, ILIM).
- Make all pin-strap control input connections ($\overline{\text{SKIP}}$, ILIM, etc.) to GND or V_{CC} rather than PGND or V_{DD}.

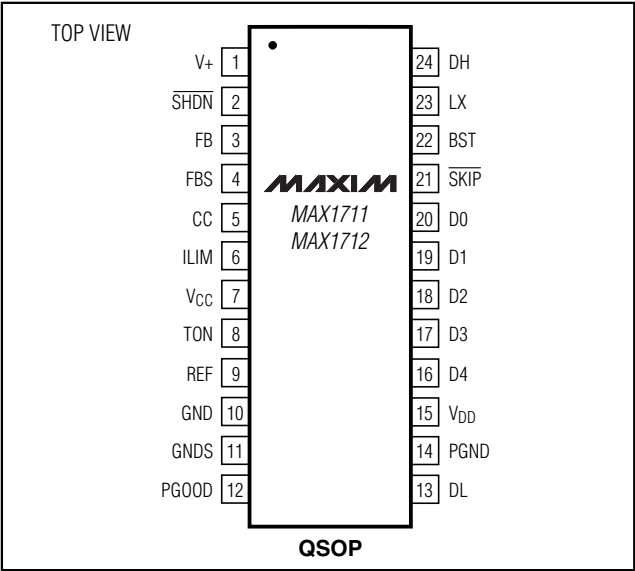
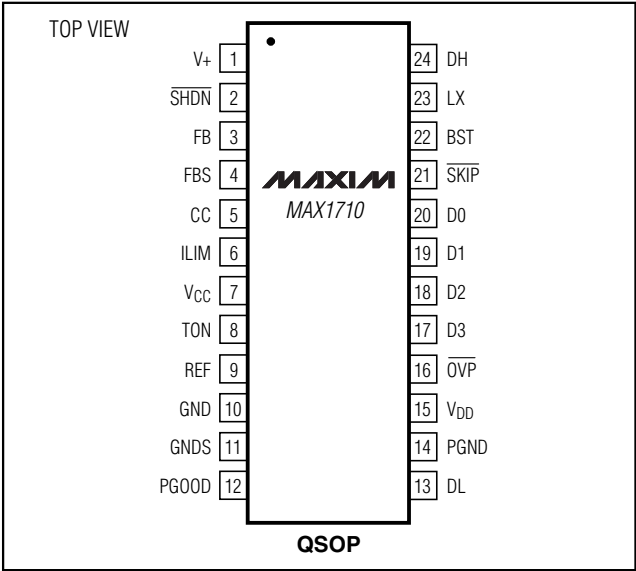
Layout Procedure

- 1) Place the power components first, with ground terminals adjacent (Q2 source, C_{IN}-, C_{OUT}-, D1 anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
- 2) Mount the controller IC adjacent to MOSFET Q2, preferably on the back side opposite Q2 to keep LX-PGND current-sense lines and the DL gate-drive line short and wide. The DL gate trace must be short and wide, measuring 10 to 20 squares (50 to 100 mils wide if the MOSFET is 1 inch from the controller IC).
- 3) Group the gate-drive components (BST diode and capacitor, V_{DD} bypass capacitor) together near the controller IC.
- 4) Make the DC-DC controller ground connections as shown in Figure 11. This diagram can be viewed as having three separate ground planes: output ground, where all the high-power components go; the PGND plane, where the PGND pin and V_{DD} bypass capacitor go; and an analog GND plane, where sensitive analog components go. The analog ground plane and PGND plane must meet only at a single point directly beneath the IC. These two planes are then connected to the high-power output ground with a short connection from V_{DD} cap/PGND to the source of the low-side MOSFET, Q2 (the middle of the star ground). This point must also be very close to the output capacitor ground terminal.
- 5) Connect the output power planes (V_{CORE} and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the CPU as is practical.

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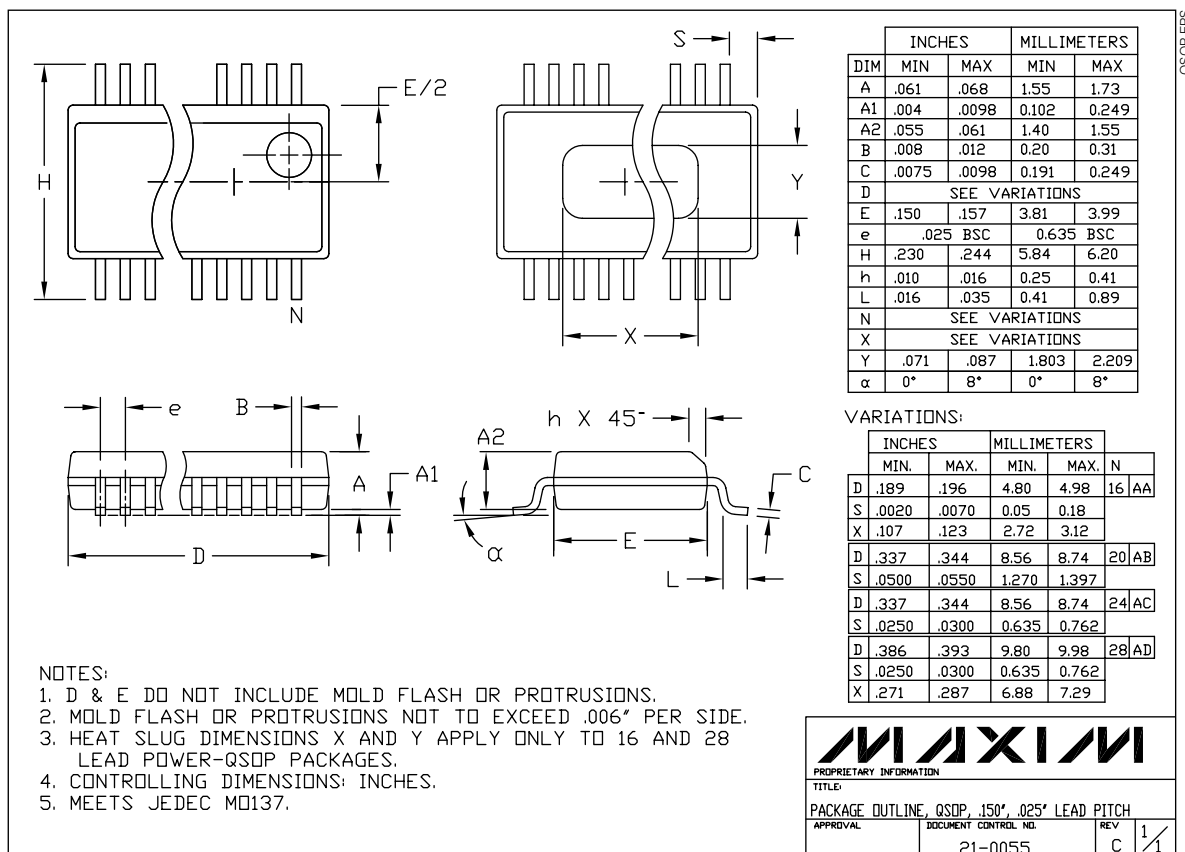
Pin Configurations

MAX1710/MAX1711/MAX1712



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Package Information



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