

SN54ALS576B, SN54AS576
 SN74ALS576B, SN74ALS577A, SN74AS576
 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS065B – DECEMBER 1982 – REVISED JANUARY 1995

- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Buffered Control Inputs
- SN74ALS577A Has Synchronous Clear
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N, NT) and Ceramic (J) 300-mil DIPs, and Ceramic Flat (W) Packages

description

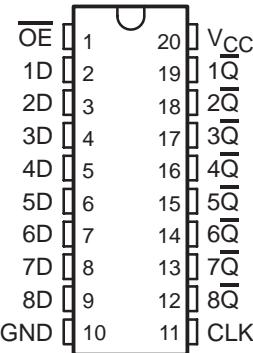
These octal D-type edge-triggered flip-flops feature 3-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These flip-flops enter data on the low-to-high transition of the clock (CLK) input.

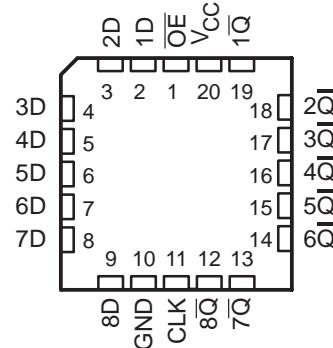
The output-enable (\overline{OE}) input does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are disabled.

The SN54ALS576B and SN54AS576 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS576B, SN74ALS577A, and SN74AS576 are characterized for operation from 0°C to 70°C .

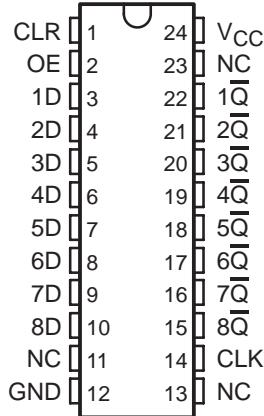
SN54ALS576B, SN54AS576 . . . J OR W PACKAGE
 SN74ALS576B, SN74AS576 . . . DW OR N PACKAGE
 (TOP VIEW)



SN54ALS576B, SN54AS576 . . . FK PACKAGE
 (TOP VIEW)



SN74ALS577A . . . DW OR NT PACKAGE
 (TOP VIEW)



NC – No internal connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN54ALS576B, SN54AS576

SN74ALS576B, SN74ALS577A, SN74AS576

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

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Function Tables

**'ALS576B, 'AS576
(each flip-flop)**

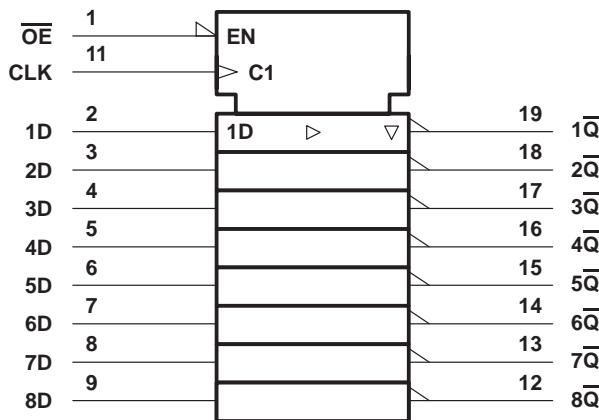
INPUTS			OUTPUT \bar{Q}
\bar{OE}	CLK	D	
L	↑	H	L
L	↑	L	H
L	L	X	\bar{Q}_0
H	X	X	Z

**SN74ALS577A
(each flip-flop)**

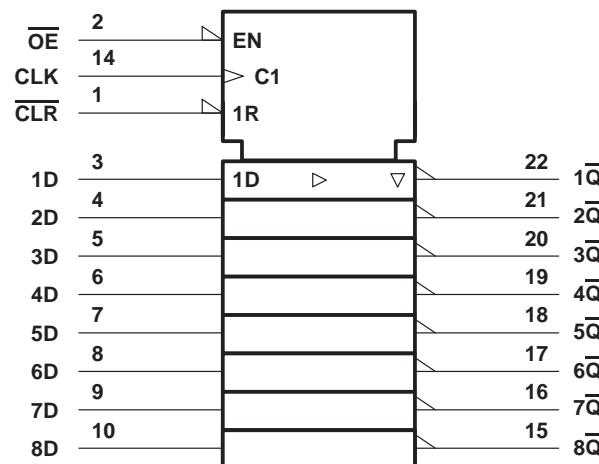
INPUTS				OUTPUT \bar{Q}
\bar{OE}	\bar{CLR}	CLK	D	
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	\bar{Q}_0
H	X	X	X	Z

logic symbols[†]

'ALS576B, 'AS576



SN74ALS577A

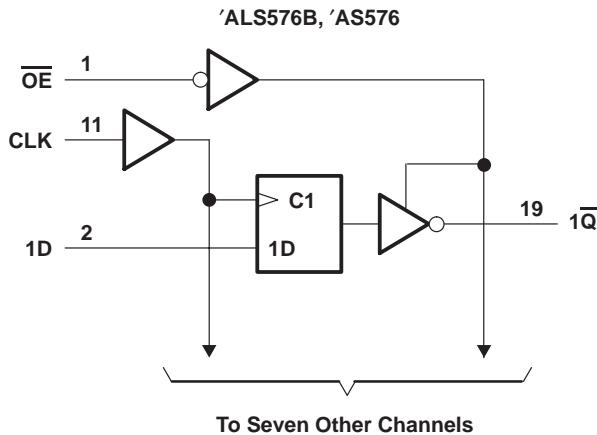


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

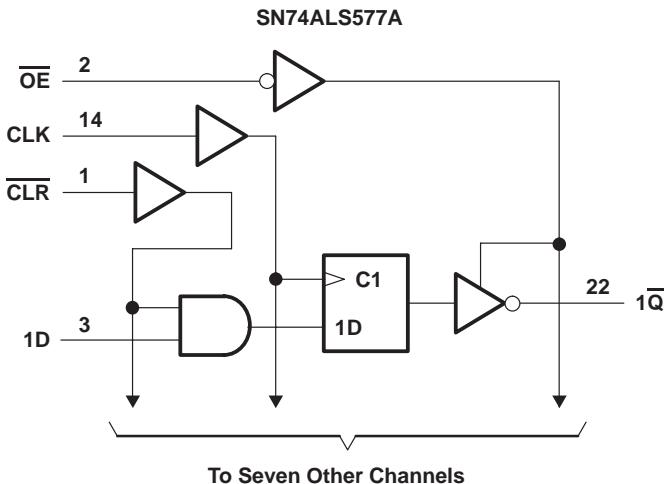
Pin numbers shown for the 'ALS576B and 'AS576 are for the DW, J, N, and W packages.

Pin numbers shown for the SN74ALS577A are for the DW and NT packages.

logic diagrams (positive logic)



Pin numbers shown are for the DW, J, N, and W packages.



Pin numbers shown are for the DW and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS576B			SN74ALS576B SN74ALS577A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-1			-2.6	mA
I _{OL}	Low-level output current			12			24	mA
f _{clock}	Clock frequency	'ALS576B		0	22	0	30	MHz
		SN74ALS577A				0	30	
t _w	Pulse duration	'ALS576B, CLK high or low		25		16.5		ns
		SN74ALS577A, CLK high or low				16.5		
t _{su}	Setup time before CLK↑	Data		15		15		ns
		SN74ALS577A CLR				15		
t _h	Hold time after CLK↑	Data		4		0		ns
		SN74ALS577A CLR				0		
T _A	Operating free-air temperature	-55		125	0		70	°C

SN54ALS576B, SN54AS576**SN74ALS576B, SN74ALS577A, SN74AS576****OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS576B			SN74ALS576B SN74ALS577A			UNIT
		MIN	TYPT†	MAX	MIN	TYPT†	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -1 \text{ mA}$	2.4	3.3				
		$I_{OH} = -2.6 \text{ mA}$			2.4	3.2		
V_{OL}	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 12 \text{ mA}$	0.25	0.4	0.25	0.4		V
		$I_{OL} = 24 \text{ mA}$			0.35	0.5		
I_{OZH}	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.7 \text{ V}$			20			20	μA
I_{OZL}	$V_{CC} = 5.5 \text{ V}$, $V_O = 0.4 \text{ V}$			-20			-20	μA
I_I	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$			-0.2			-0.2	mA
I_O^{\ddagger}	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-20	-112	-30	-112			mA
I_{CC}	$V_{CC} = 5.5 \text{ V}$	Outputs high	10	18	10	18		mA
		Outputs low	15	24	15	24		
		Outputs disabled	16	30	16	30		

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R1 = 500 \Omega$, $R2 = 500 \Omega$, $T_A = \text{MIN to MAX}^{\$}$						UNIT		
			SN54ALS576B		SN74ALS576B		SN74ALS577A				
			MIN	MAX	MIN	MAX	MIN	MAX			
f_{max}			22		30		30		MHz		
t_{PLH}	CLK	Any \bar{Q}	4	24	3	14	4	14	ns		
t_{PHL}			4	20	4	14	4	14			
t_{PZH}	\overline{OE}	Any \bar{Q}	4	24	3	18	4	18	ns		
t_{PZL}			3	23	4	18	4	18			
t_{PHZ}	\overline{OE}	Any \bar{Q}	2	14	1	10	2	10	ns		
t_{PLZ}			3	29	2	15	3	15			

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS576			SN74AS576			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-12			-15	mA
I _{OL}	Low-level output current			32			48	mA
f _{clock} *	Clock frequency	0	100	100	0	125	125	MHz
t _w *	Pulse duration	CLK high	5	5	4	4	4	ns
		CLK low	4	4	2	2	2	
t _{su} *	Setup time, data before CLK↑	3	3	3	2	2	2	ns
t _h *	Hold time, data after CLK↑	3	3	3	2	2	2	ns
T _A	Operating free-air temperature	-55	125	125	0	70	70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

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SDAS065B - DECEMBER 1982 - REVISED JANUARY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS576			SN74AS576			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -2 \text{ mA}$	$V_{CC} - 2$		$V_{CC} - 2$				V
	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -12 \text{ mA}$	2.4	3.2				
		$I_{OH} = -15 \text{ mA}$			2.4	3.3		
V_{OL}	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 32 \text{ mA}$	0.29	0.5				V
		$I_{OL} = 48 \text{ mA}$			0.33	0.5		
I_{OZH}	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.7 \text{ V}$			50			50	μA
I_{OZL}	$V_{CC} = 5.5 \text{ V}$, $V_O = 0.4 \text{ V}$			-50			-50	μA
I_I	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	D All others	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$		-3			-2	mA
				-0.5			-0.5	
I_O^\ddagger	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-30	-112	-30	-112			mA
I_{CC}	$V_{CC} = 5.5 \text{ V}$	Outputs high	77	125	77	125		mA
		Outputs low	84	135	84	135		
		Outputs disabled	84	135	84	135		

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

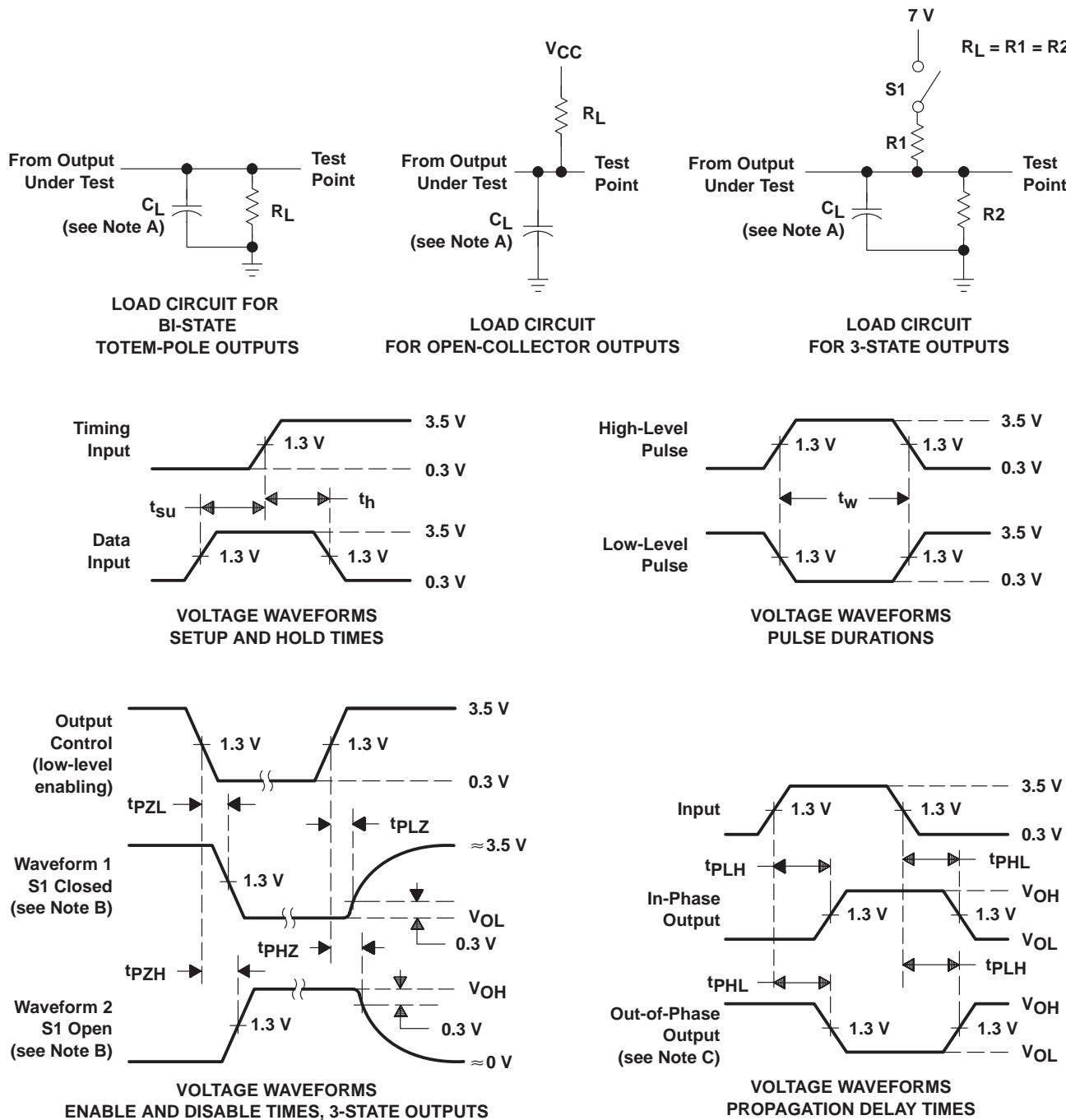
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $C_L = 50 \text{ pF}$, $R1 = 500 \Omega$, $R2 = 500 \Omega$, $T_A = \text{MIN to MAX}^\S$				UNIT	
			SN54AS576		SN74AS576			
			MIN	MAX	MIN	MAX		
f_{max}^*			100		125		MHz	
t_{PLH}	CLK	Any \bar{Q}	3	11	3	8	ns	
t_{PHL}			4	11	4	9		
t_{PZH}	\bar{OE}	Any \bar{Q}	2	7	2	6	ns	
t_{PZL}			3	11	3	10		
t_{PHZ}	\bar{OE}	Any \bar{Q}	2	7	2	6	ns	
t_{PLZ}			2	7	2	6		

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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**PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



NOTES:

- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
- D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
- E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
84001022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84001022A SNJ54ALS 576BFK	Samples
8400102RA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8400102RA SNJ54ALS576BJ	Samples
8400102SA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8400102SA SNJ54ALS576BW	Samples
SN54ALS576BJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54ALS576BJ	Samples
SN74ALS576BDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS576B	Samples
SN74ALS576BDWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS576B	Samples
SN74ALS576BDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS576B	Samples
SN74ALS576BDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS576B	Samples
SN74ALS576BDWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS576B	Samples
SN74ALS576BDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS576B	Samples
SN74ALS576BN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS576BN	Samples
SN74ALS576BN3	OBsolete	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74ALS576BNE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS576BN	Samples
SN74ALS576BNSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS576B	Samples
SN74ALS576BNSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS576B	Samples
SN74ALS576BNSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS576B	Samples
SN74ALS577ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS577A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALS577ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS577A	Samples
SN74ALS577ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS577A	Samples
SN74ALS577ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS577A	Samples
SN74ALS577ADWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS577A	Samples
SN74ALS577ADWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS577A	Samples
SN74ALS577ANT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS577ANT	Samples
SN74ALS577ANT3	OBsolete	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
SN74ALS577ANTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS577ANT	Samples
SN74AS576DWE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70	AS576	Samples
SN74AS576DWG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70	AS576	Samples
SN74AS576N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS576N	Samples
SN74AS576NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS576N	Samples
SNJ54ALS576BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	84001022A SNJ54ALS576BFK	Samples
SNJ54ALS576BJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	8400102RA SNJ54ALS576BJ	Samples
SNJ54ALS576BW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	8400102SA SNJ54ALS576BW	Samples
SNJ54AS576FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54AS576FK	Samples
SNJ54AS576J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54AS576J	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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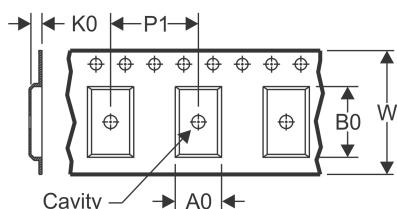
OTHER QUALIFIED VERSIONS OF SN54ALS576B, SN54AS576, SN74ALS576B, SN74AS576 :

- Catalog: [SN74ALS576B](#), [SN74AS576](#)
- Military: [SN54ALS576B](#), [SN54AS576](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS576BDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ALS576BNSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74ALS577ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

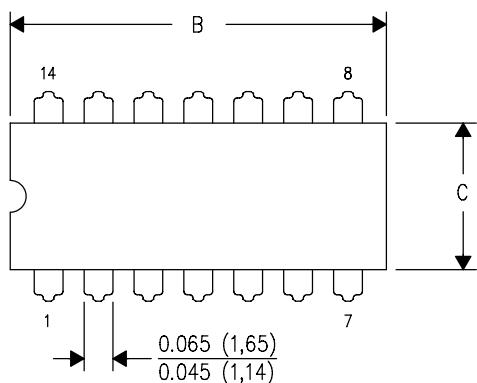

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS576BDWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ALS576BNSR	SO	NS	20	2000	367.0	367.0	45.0
SN74ALS577ADWR	SOIC	DW	24	2000	367.0	367.0	45.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

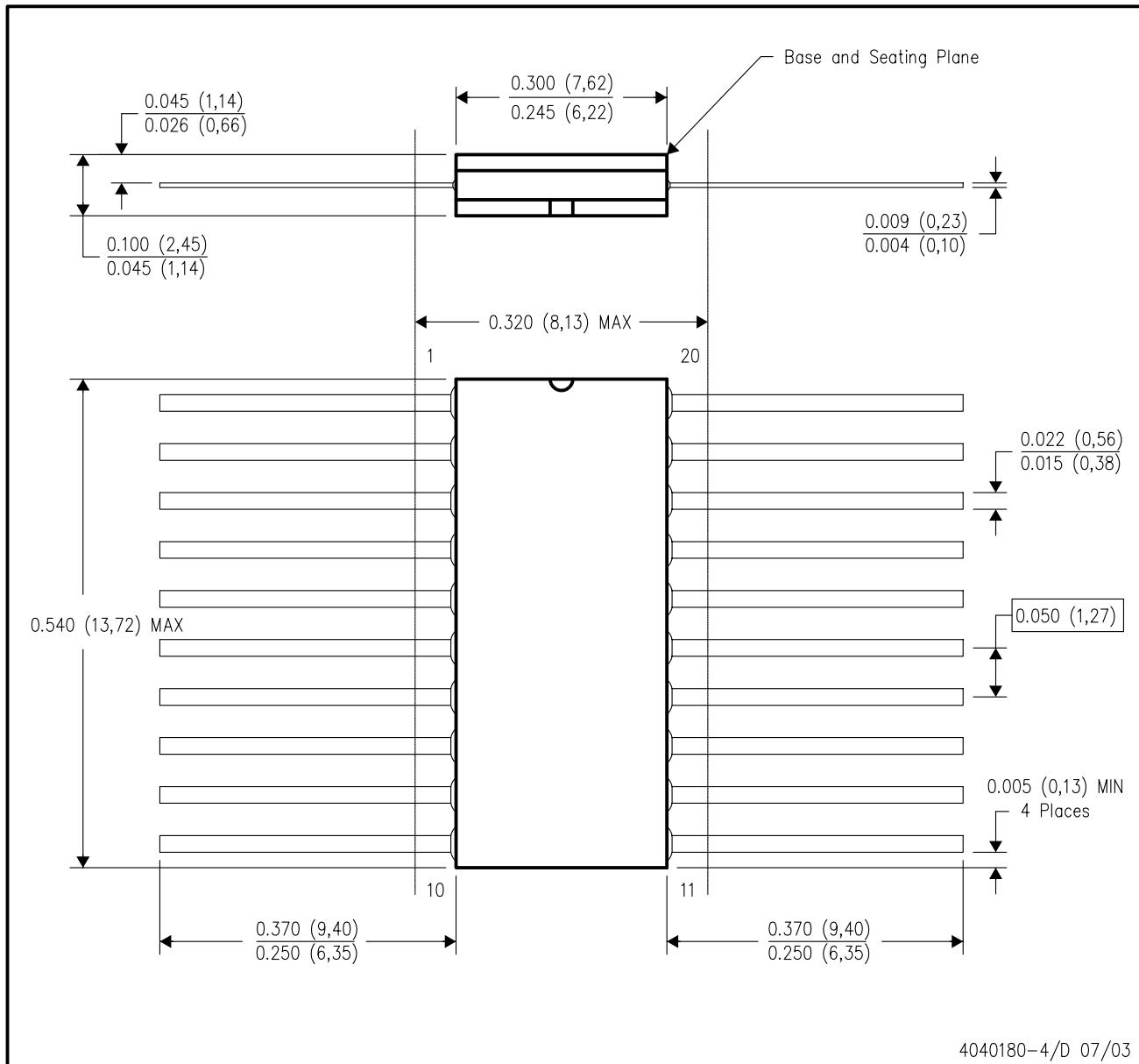


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



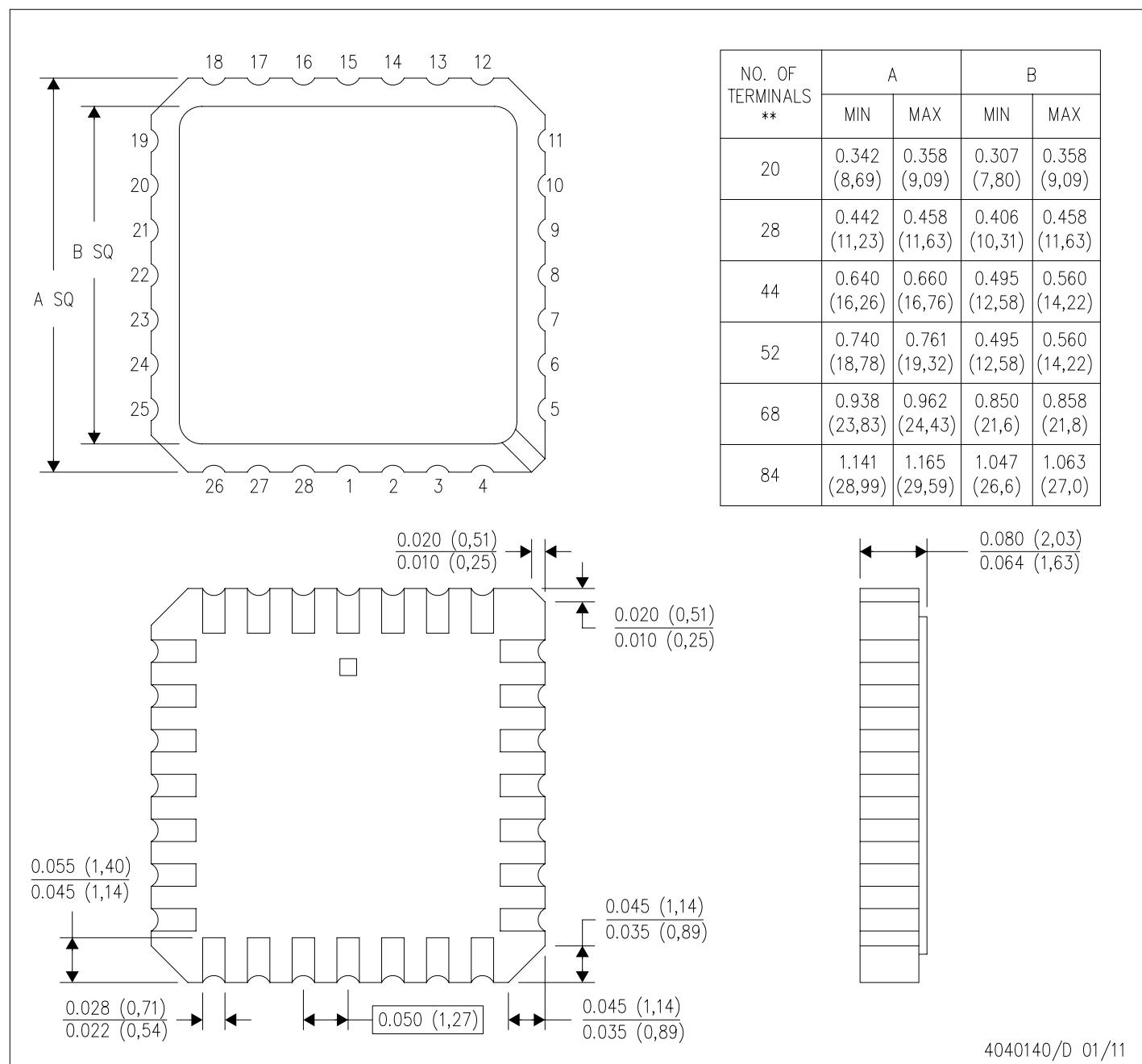
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

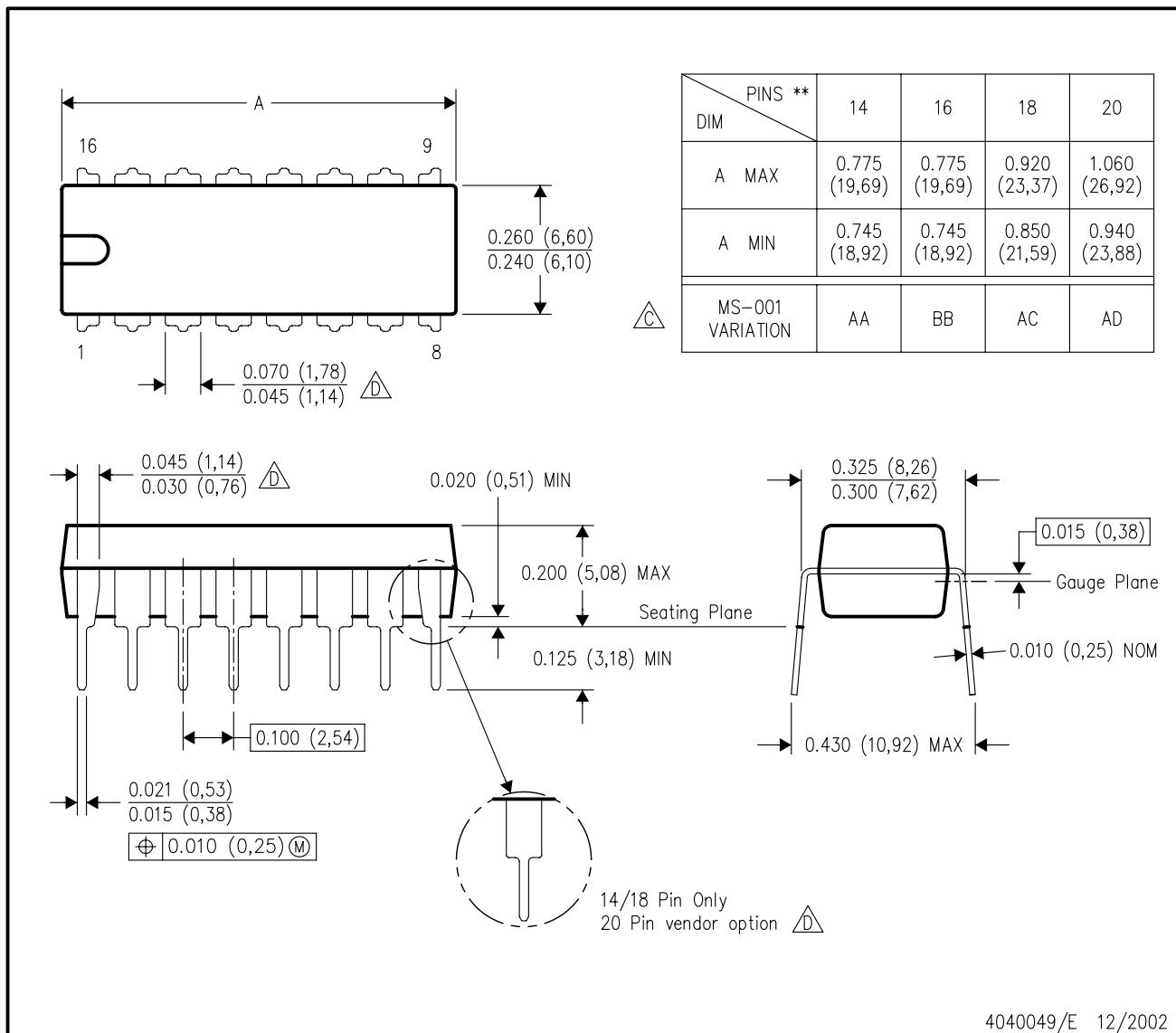
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

4040140/D 01/11

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

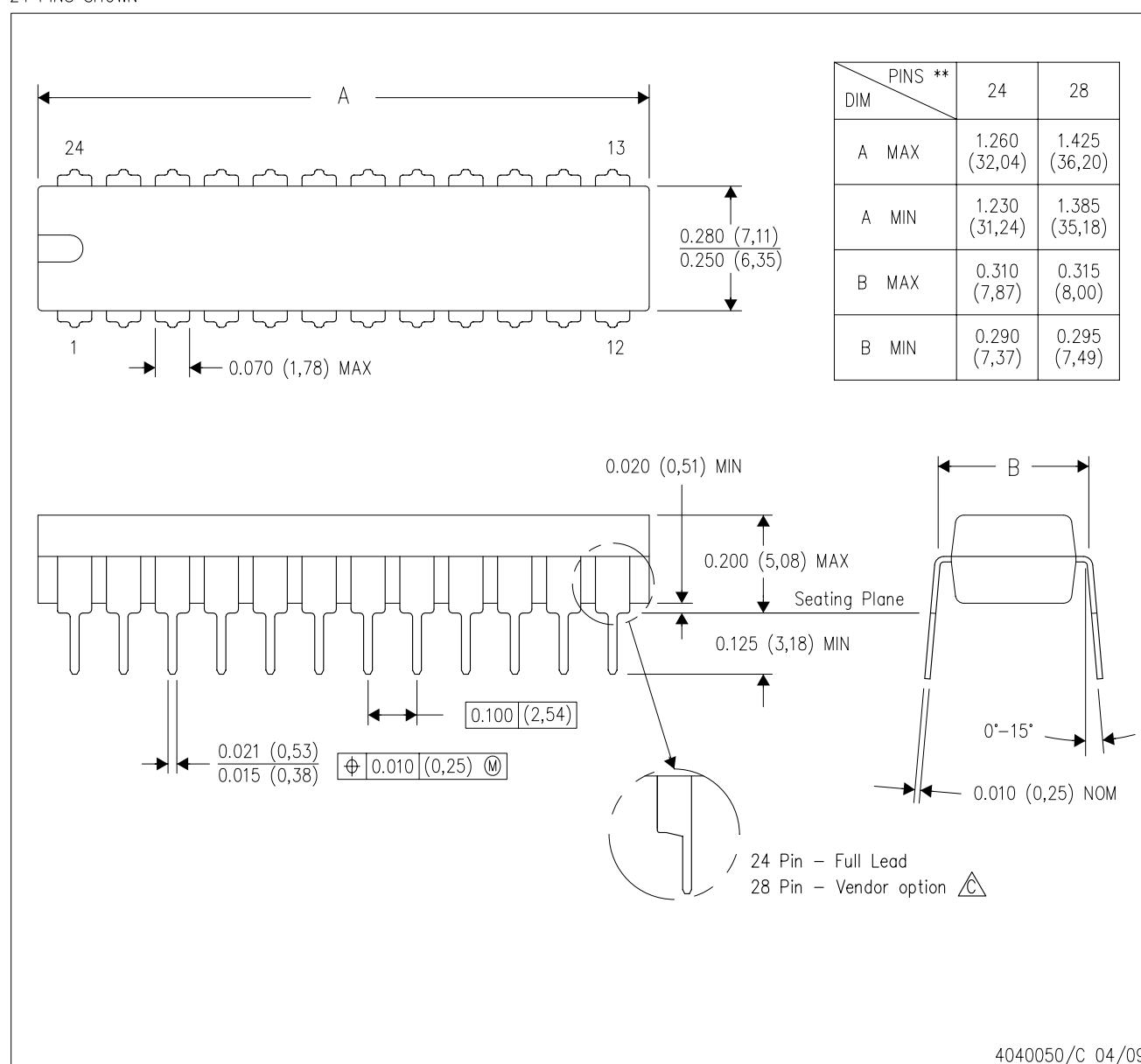
△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

NT (R-PDIP-T**)

24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



4040050/C 04/09

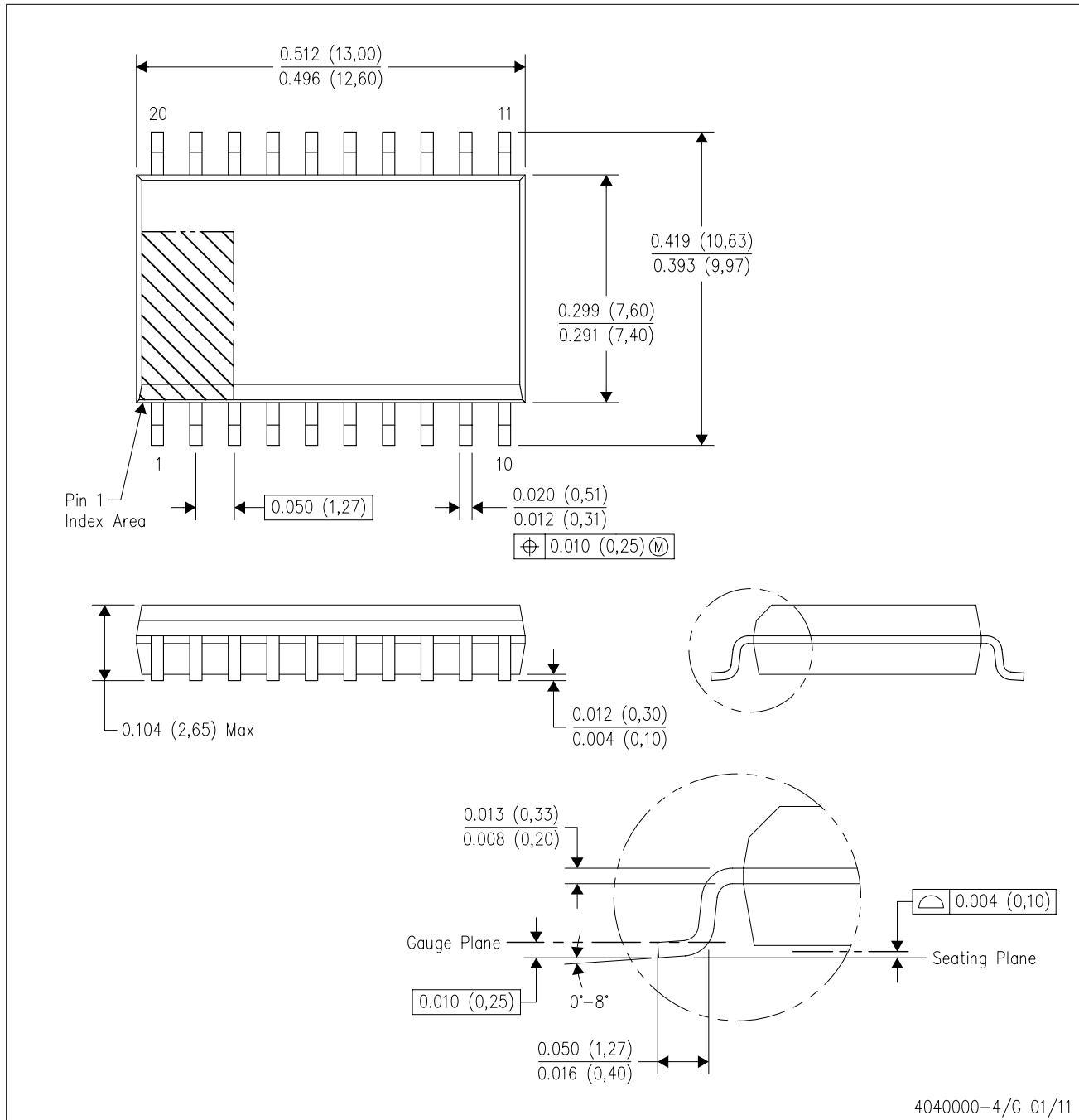
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

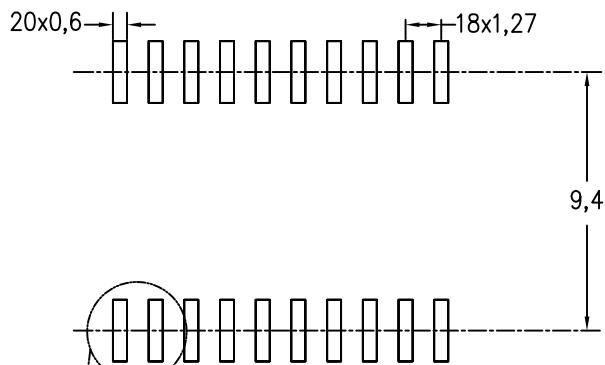
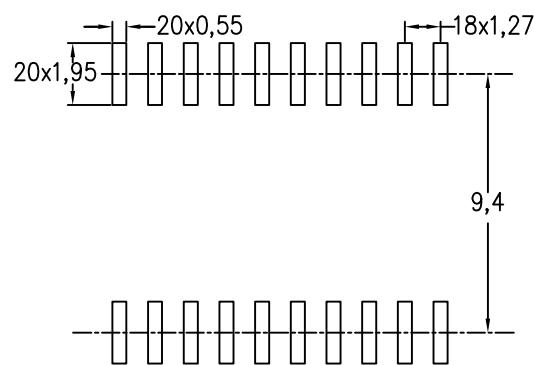


NOTES:

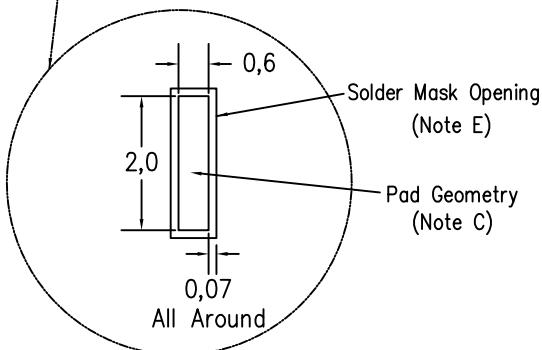
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)

Non Solder Mask Define Pad



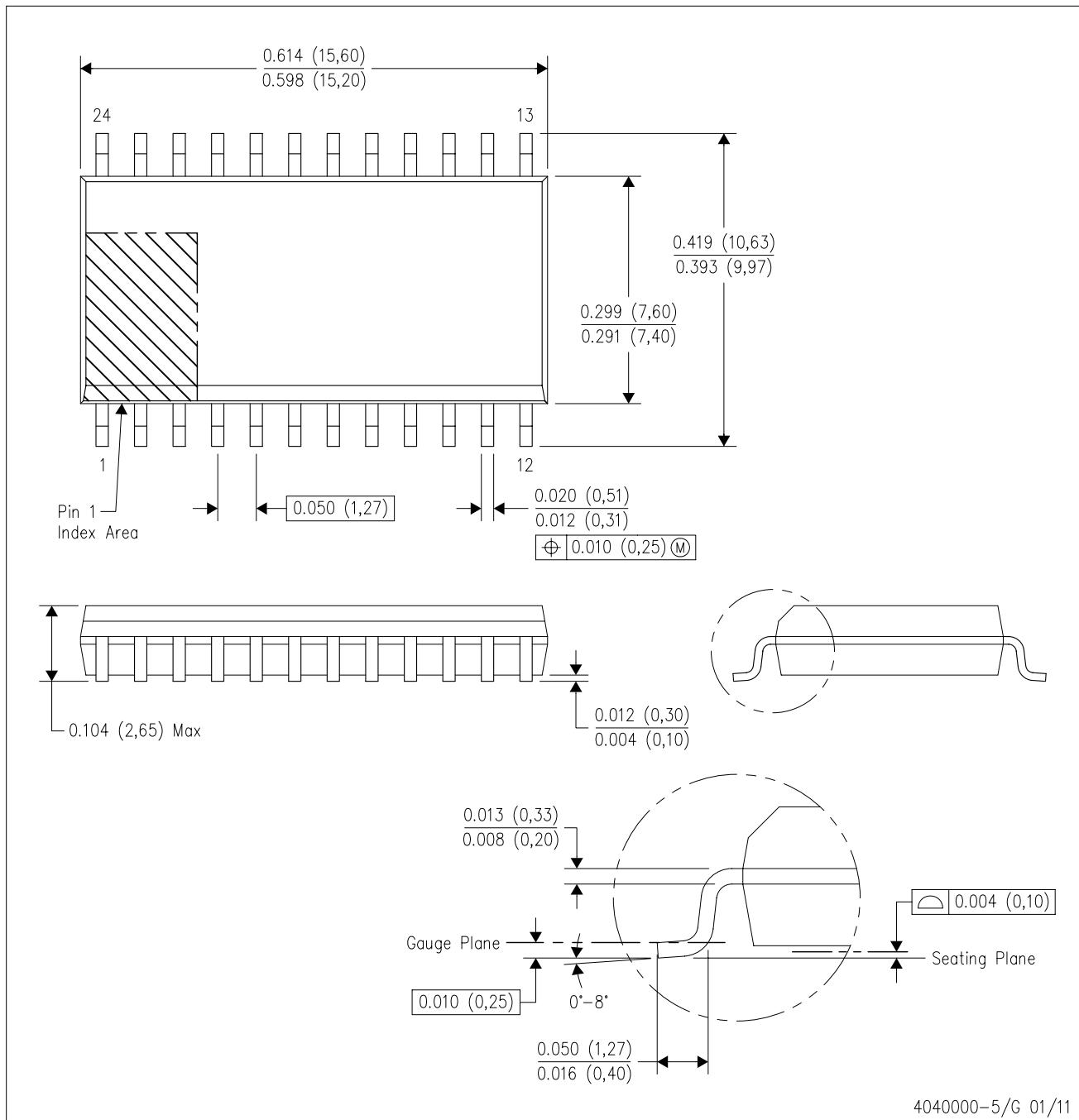
4209202-4/F 08/13

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES:

- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AD.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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