

Features:

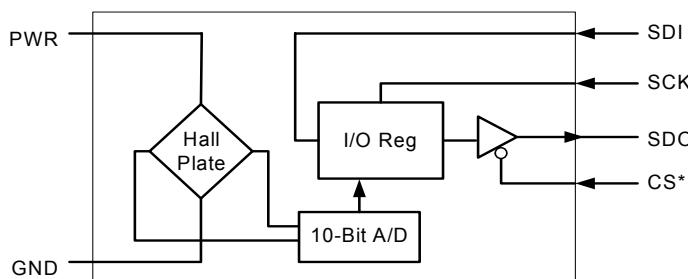
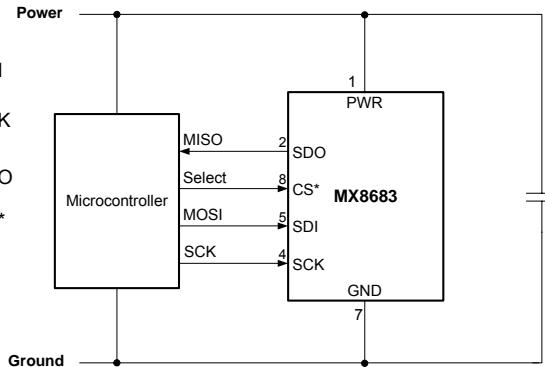
- Single 5 Volt Power Supply
- Externally Configurable ±20A Bi-Direction Current Sense per Turn
- 12-bit Serial Digital Output / 10-bit ADC
- Full Scale Magnetic Flux Intensity of ±200 Gauss
- 20K Conversions/Second
- Microcontroller Compatible
- Standard 3 Wire Serial Interface plus Chip Select
- In System Calibration: OTP Full Scale Trim via the Serial I/O Port
- Programmable Digital Filter Time Constant
- 4mm x 4mm 8 Lead DFN package RoHS Compliant

Applications:

- Load Detection and Management
- Motor Control
- Power Supplies

Ordering Information

Part No.	Description	Qty
MX8683R	DFN-8 Tube	91
MX8683RTR	DFN-8 Tape & Reel	2500

Functional Block Diagram Typical

Application Circuit


Absolute Maximum Ratings $T_A = +25^\circ\text{C}$ unless otherwise noted

Parameter	Min	Max	Unit
Voltage (Any Pin to GND)		+7	V
θ_{JA} , DFN-8 Package		30	°C/W
Operating Temperature Range	-40	+85	°C
Storage Temperature Range	-65	150	°C

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for an extended period may degrade the device and affect its reliability.

ESD Warning

ESD (electrostatic discharge) sensitive device. Although the MX8683 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Electrical CharacteristicsPWR= 5V, $T = +25^\circ\text{C}$

Parameter	Condition	Min	Typ	Max	Unit
Operating Voltage Range (PWR)		4.5		5.5	V
Supply Current (I_{PWR})			3		mA
Average A/D Reading	Zero Magnetic Flux	2040	2048	2056	LSB
Average A/D Reading	100 Gauss, North Pole		3072		LSB
Output Noise	Digital Filter Off		5.5		RMS LSB
SCK pulse period		200			nS
SCK pulse width	high or low	80			nS
CS* pulse period		50			µS
CS* falling to first SCK rising		100			nS
Last SCK falling to CS* rising		50			nS
SCK falling to SDO valid				60	nS
Digital output high		PWR-0.5			V
Digital output low				0.5	V
Digital input low		GND		0.8	V
Digital input high		2		PWR	V
Digital input current				1	µA

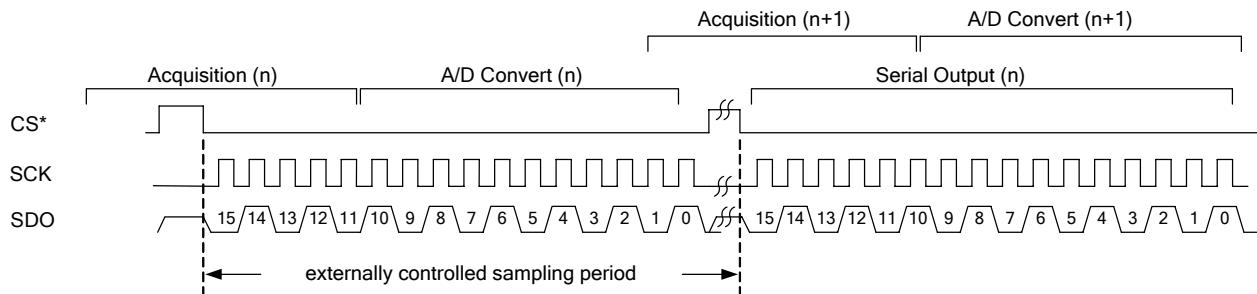
Pin Description

Pin No.	Name	Description
1	PWR	Input Voltage Supply
2	SDO	Serial Data Output
3	NC	No Connect
4	SCK	Serial Clock Input
5	SDI	Serial Data Input
6	NC	No Connect
7	GND	Connect to Ground
8	CS*	Active low chip select for the serial interface. When a logic "high" is on this pin, the MX8683 is tracking the hall input signal.

Detailed Circuit Description

The hall plate senses the magnetic field that is applied normal (perpendicular) to the package surface. The signal from the hall plate is offset-corrected by detecting the difference between a pair of analog samples during the acquisition time. During idle time (CS* high) the MX8683 tracks the first analog sample. Immediately (~10 nS) after the falling edge of CS* the first sample is held. The track mode for the second sample starts nominally 4 μ S after the falling edge of CS*. Typically 12 μ S after the falling edge of CS* the second sample is held and the resulting analog value is then converted by the A/D. The result of the A/D conversion is loaded into the I/O register at the next falling edge of CS*, in preparation for output on SDO.

The internal acquisition and A/D timing is asynchronous to the SCK serial interface clock. The magnetic field sampling period is controlled externally by the time between consecutive CS* falling edges. For zero magnetic field input the nominal A/D output is 2048 decimal. North pole towards the top surface of the MX8683 increases the A/D output count. Applications that require non-continuous one measurement at a time operation should pulse CS* low twice, reading the data when CS* is low for the second time.



POWER-ON RESET

The MX8683 contains a power-on reset circuit that resets all the internal flip-flops and initializes the internal registers to zero. The MX8683 will reset if the voltage at terminal PWR drops below 3.2V to 3.8V.

SYNCHRONOUS SERIAL I/O

The MX8683 (slave) can communicate with a microcomputer (master) via a three wire plus chip select serial interface. Chip select CS*, serial clock SCK, and serial data input SDI are output from the master controller to the MX8683.

Serial data output SDO is driven by the MX8683 when selected by CS* = 0.

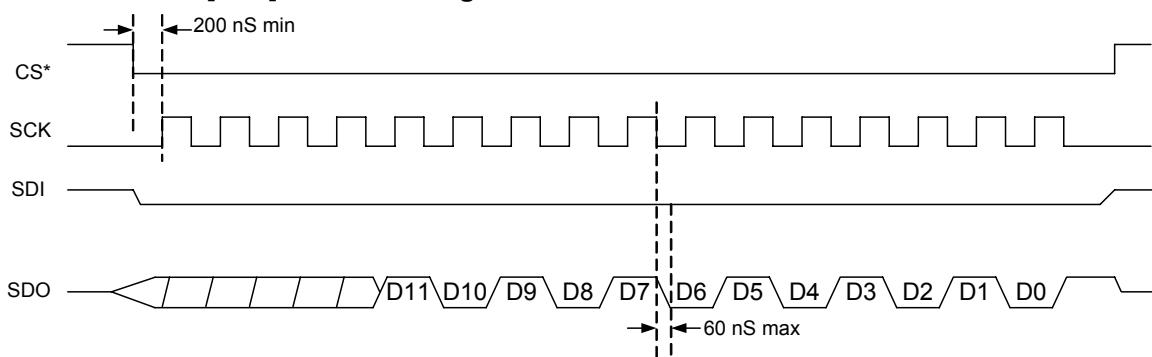
SDO is high impedance when CS* = 1.

SCK and SDI are don't care when CS* = 1.

SDI is captured by the rising edge of SCK.

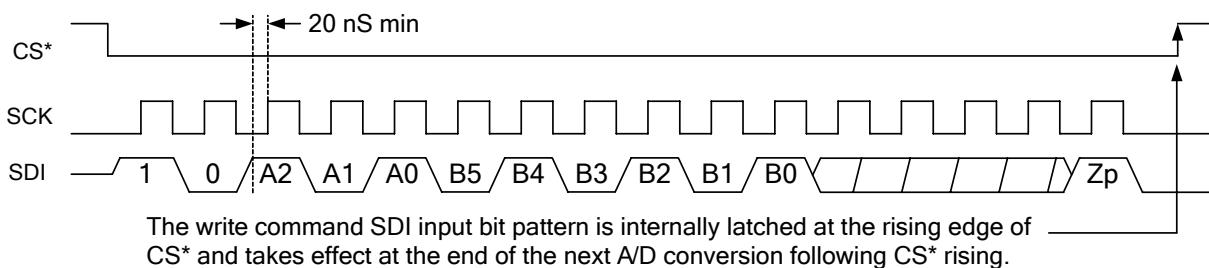
SDO changes in response to the falling edge of SCK.

Read 12-bit data D[11:0] when SDI = logic 0



Note: When the filter is off, D1=D0=0, D2=LSB of the 10-bit ADC.

Write command timing: (Bit Field A[2:0], B[5:0], OTP Bit Zp)



The exponentially weighted moving average digital filter has a transfer function equivalent to a first order low pass filter.

The I/O timing remains exactly the same when the filter is used. No decimation is performed.

Let T = Sample interval (the time from CS* falling edge to CS* falling edge). Then bandwidth = $1/(2\pi T)$.

Also if W = Sample weighting, then the digital output = $W * (\text{current sample}) + (1-W) * (\text{previous value})$.

At power-on the previous value is initialized to zero. A programmed change in A[2:0] does not reset the previous value. Therefore when using the filter, multiple samples must be taken at power-on or after changing A[2:0] before the filtered output will be correct.

Bit field A[2:0] controls the digital filter operation:

A[2:0]	Time Constant	Sample Weighting
000	No Filter	1
001	T	1/2
010	3T	1/4
011	7T	1/8
100	15T	1/16
101	31T	1/32
110	63T	1/64
111	127T	1/128

Bit field B[5:0] is the full scale adjust:

Characteristics are 0.8% step size, $\pm 25\%$ total range.

B[5:0] = 000000 is the lowest sensitivity (highest full scale)

B[5:0] = 111111 is the highest sensitivity

One-Time Programming:

Bit Zp, when logic 1 along with A[2:0] and B[5:0] values, programs those values into the internal non-volatile memory.

Programming a bit to logic 1 is permanent. A bit programmed to logic 1 cannot be made to go back to logic 0.

Always send a write command with Zp = 0 and SDI = 0 immediately after the programming command. The actual programming pulse occurs internally at the falling edge of CS* in the command following the command in which Zp = logic 1.

The write command can be used to preview the trim bits as long as Zp is logic 0.

Examples:

The bit field B[5:0] can be programmed while the A[2:0] bit field is "000", or vice versa. For example the total SDI bit pattern could be 10 000 001100 0000 1. This would permanently set the B[5:0] bit field to 001100 but the filter setting could still be subsequently changed by a different write command, either in preview or programming.

The SDI bit pattern 10 010 010000 0000 0 would set the filter time constant to 3T and the full scale field to 010000 as a preview, without making it permanent (because bit Zp = 0).

If the sample interval T = 1 mS and A[2:0] = 001 then the effective bandwidth would be $1/(2*3.14*1e-3) = 159$ Hz. For this condition, if the steady state output was 2000 counts and a step input was applied that would drive the output to 3000 counts then the digital output response would be 2000, 2500, 2750, 2875, 2937, 2968, 2984, 2992, 2996, 2998, 2999, 3000.

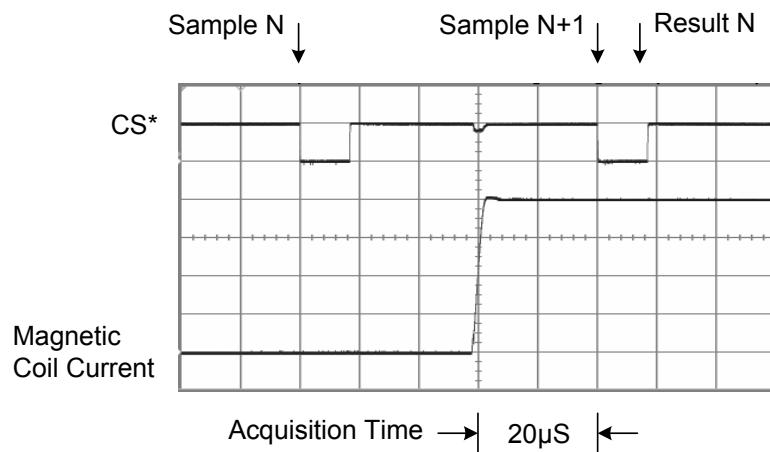


Figure 1

**Input Stimulus for
Transient Response**

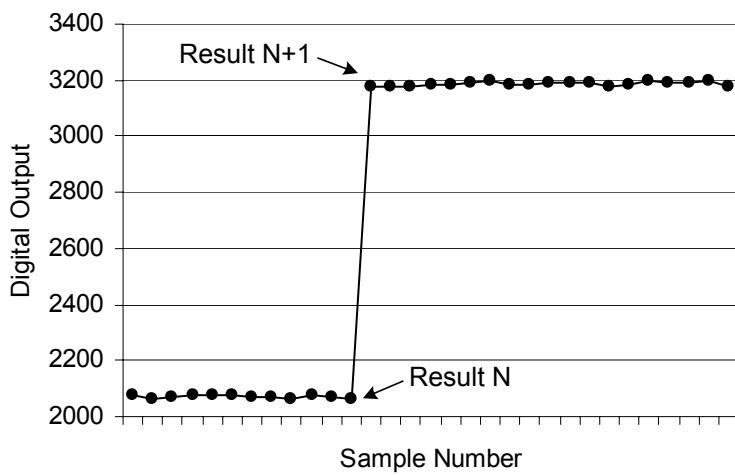


Figure 2

**Transient Response
No Filter
20µ Acquisition Time**

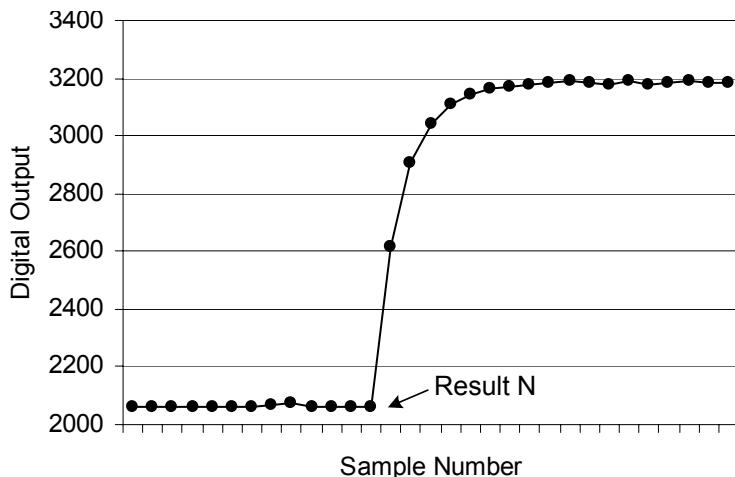
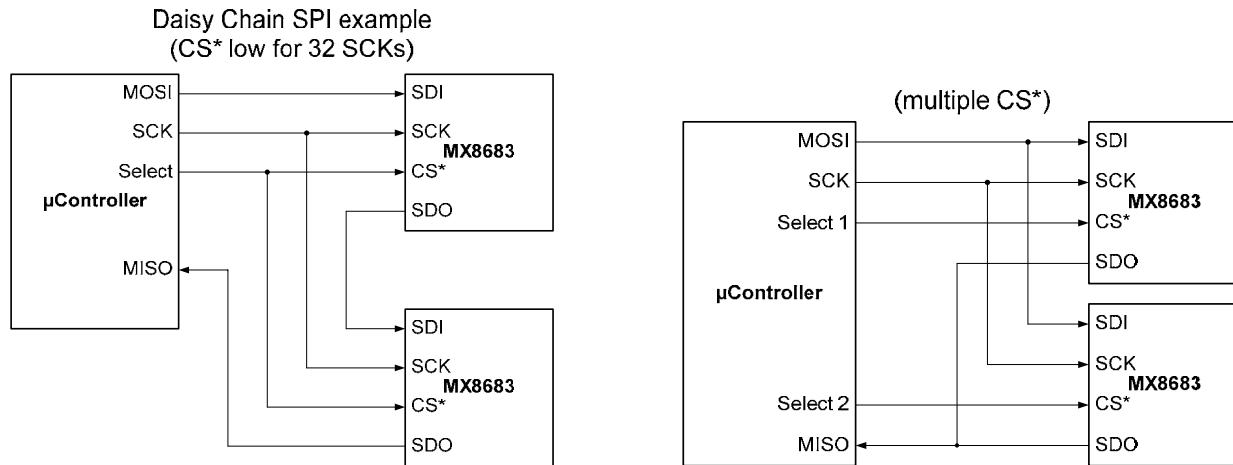


Figure 3

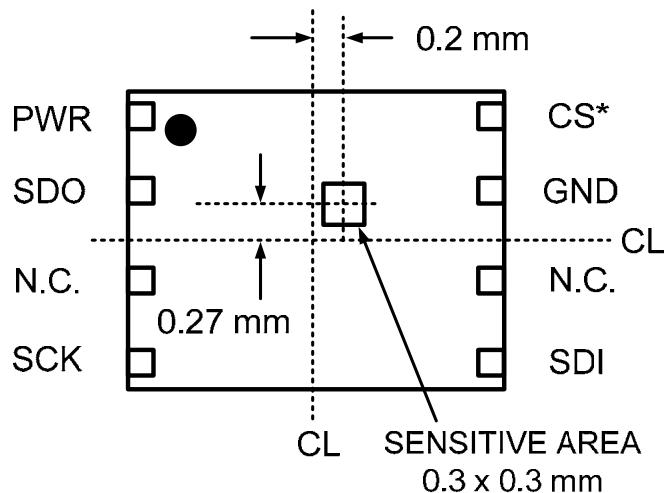
**Transient Response
Filter Bit Field A[2:0] = 001
20µ Acquisition Time**

Cascade Configurations



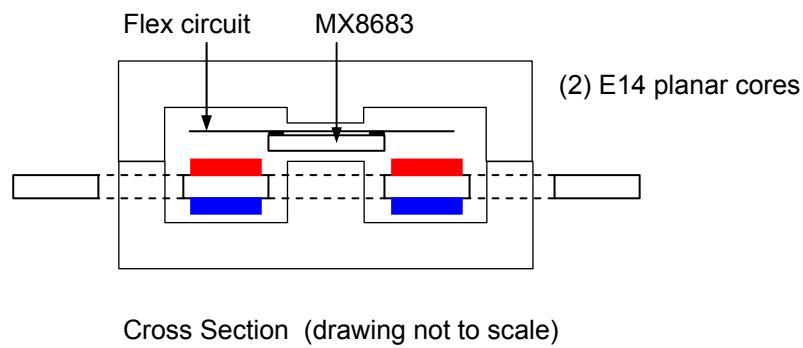
Sensor Location

8 Lead DFN 4x4 mm
(Top View - Drawing not to scale)

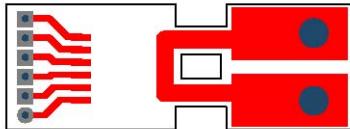


Application Example

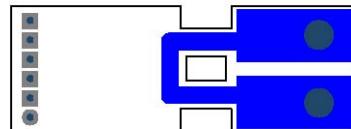
This application example illustrates one method of incorporating the MX8683 into a power circuit board design. The double-sided 8oz copper traces carry 20A (10A on the top trace and 10A on the bottom trace) around the center section of the planar E-core. The MX8683 is mounted on a small single layer flex circuit that effectively adds a third layer. The flex also fans out the fine pitch DFN package to a pitch compatible with the power board. The magnetic circuit consists of two ferrite E14 planar cores. The center post of one of the cores is gapped to accommodate the MX8683 package thickness plus the flex circuit thickness. For the 20A full scale application a gap of 47 to 52 mils is appropriate (1.2 to 1.32 mm). The gain trim range of the MX8683 can accommodate even larger gaps if required.



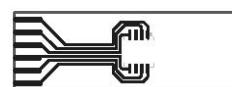
PCB top layer: (scale 1X)



PCB bottom layer: (top view, 1X)



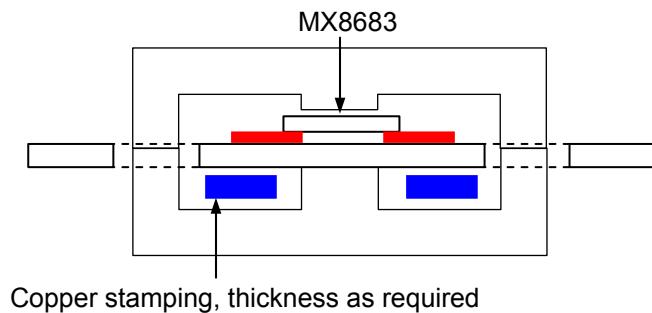
Flex circuit: (component side, 1X)



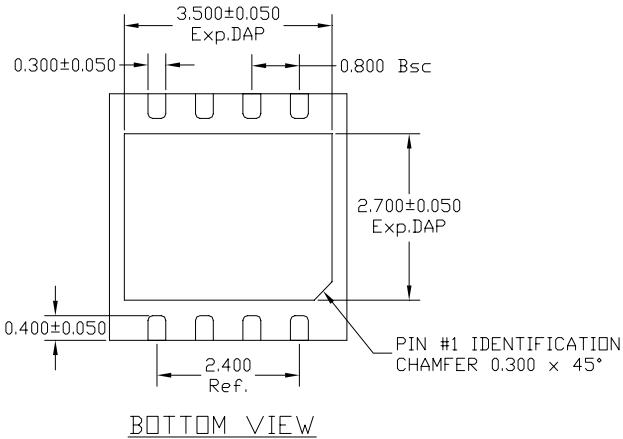
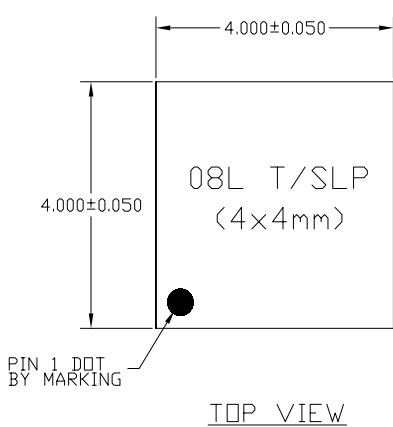
Design alternatives:

Multi-layer boards may be used with the MX8683 mounted directly on the board. The use of an E-I core pair results in a lower profile than E-E however a thinner board must be used.

An example of a low-power circuit board with an added high-current copper strap:

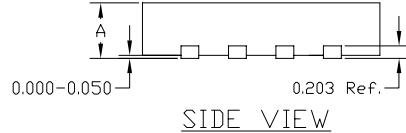


8 Lead DFN



NOTE:
1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE
BUT WITH DIFFERENT THICKNESS:

A	TSLP		SLP			
	MAX.	0.800	0.900	NOM.	0.750	0.850
MIN.	0.700	0.800				



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Specification: MX8683
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