



N-Channel Enhancement-Mode MOSFET

Characteristics

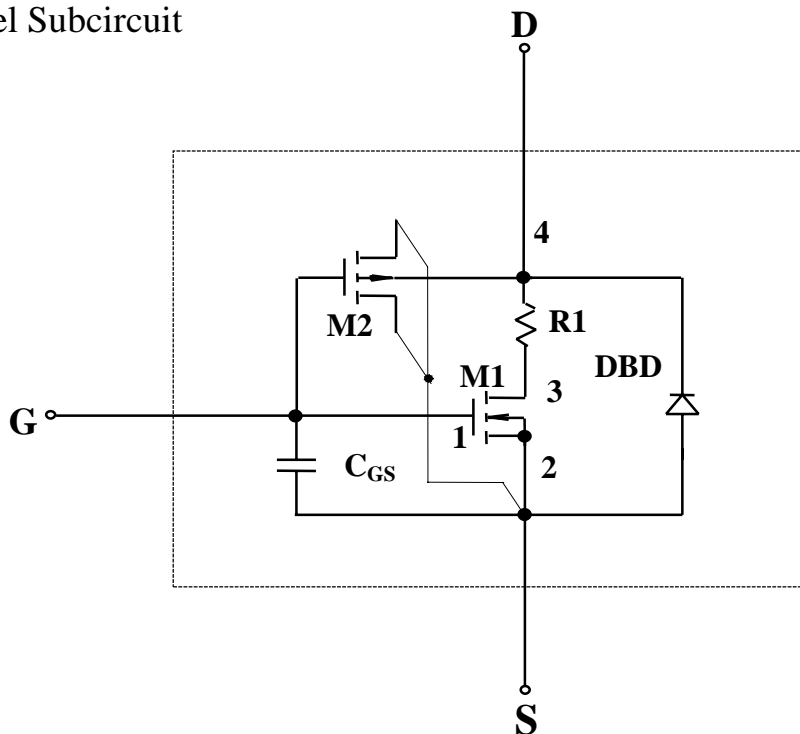
- N-channel Vertical DMOS
- Macro-Model (Subcircuit)
- Level 3 MOS
- Applicable for Both Linear and Switch Mode
- Applicable Over a -55 to 125°C Temperature Range
- Models Gate Charge, Transient, and Diode Reverse Recovery Characteristics

Description

The attached SPICE Model describes typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model was extracted and optimized over a 25°C to 125°C temperature range under pulse conditions for 0 to 10 volt gate drives. Saturated output impedance model accuracy has been maximized for gate biases near threshold. A novel gate-to-drain feedback

capacitance network is used to model gate charge characteristics while avoiding convergence problems of switched C_{gd} model. Model parameter values are optimized to provide a best fit to measured electrical data and are not intended as an exact physical description of a device.

Model Subcircuit



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



Model Evaluation

N-Channel Device ($T_J=25^{\circ}\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Typ	Unit
Static				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2.85	V
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{V}, V_{GS} = 10\text{V}$	221	A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\text{V}, I_D = 7.5\text{A}$ $V_{GS} = 6\text{V}, I_D = 6.5\text{A}$	0.021 0.026	Ω
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{V}, I_D = 7.5\text{A}$	19.6	S
Diode Forward Voltage ^b	V_{SD}	$I_S = 2.1\text{A}, V_{GS} = 0\text{V}$	0.76	V
Dynamic				
Total Gate Charge	Q_g	$V_{DS} = 30\text{V}, V_{GS} = 10\text{V},$ $I_D = 7.5\text{A}$	31	nC
Gate-Source Charge	Q_{gs}		7.7	
Gate-Drain Charge	Q_{gd}		8.3	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{V}, R_L = 30\Omega$ $I_D \cong 1\text{A}, V_{GEN} = 10\text{V},$ $R_G = 6\Omega$	12	ns
Rise Time	t_r		10	
Turn-Off Delay Time	$t_{d(off)}$		41	
Fall Time	t_f		27	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.1\text{A},$ $di/dt = 100\text{A}/\mu\text{s}$	46	

Notes:

- a) For design aid only; not subject to production testing
- b) Pulse test: Pulse Width $\leq 300\mu\text{sec}$, Duty Cycle $\leq 2\%$



SPICE Device Model Si4450DY

Comparison of Model with Measured Data
($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

