

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic (JT) DIPs

description

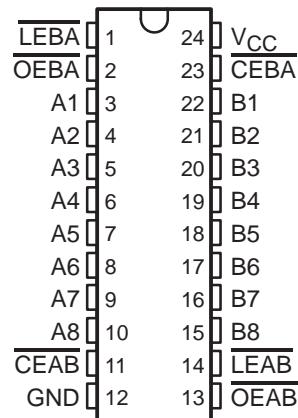
These octal transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT543 contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable (\overline{LEAB} or \overline{LEBA}) and output-enable (\overline{OEAB} or \overline{OEBA}) inputs are provided for each register to permit independent control in either direction of data flow.

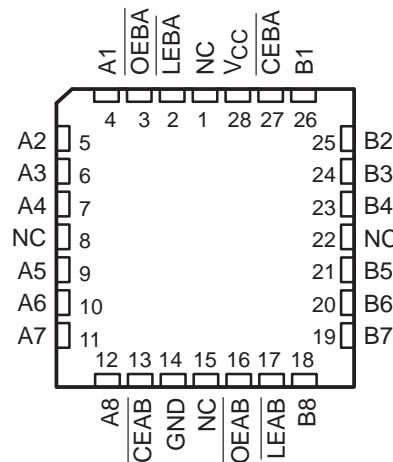
The A-to-B enable (\overline{CEAB}) input must be low in order to enter data from A or to output data from B. If \overline{CEAB} is low and \overline{LEAB} is low, the A-to-B latches are transparent; a subsequent low-to-high transition of \overline{LEAB} puts the A latches in the storage mode. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the \overline{CEBA} , \overline{LEBA} , and \overline{OEBA} inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

SN54LVT543 . . . JT PACKAGE
 SN74LVT543 . . . DB, DW, OR PW PACKAGE
 (TOP VIEW)



SN54LVT543 . . . FK PACKAGE
 (TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN54LVT543, SN74LVT543

3.3-V ABT OCTAL REGISTERED TRANSCEIVERS

WITH 3-STATE OUTPUTS

SCBS137D – MAY 1992 – REVISED JULY 1995

description (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT543 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT543 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVT543 is characterized for operation from -40°C to 85°C .

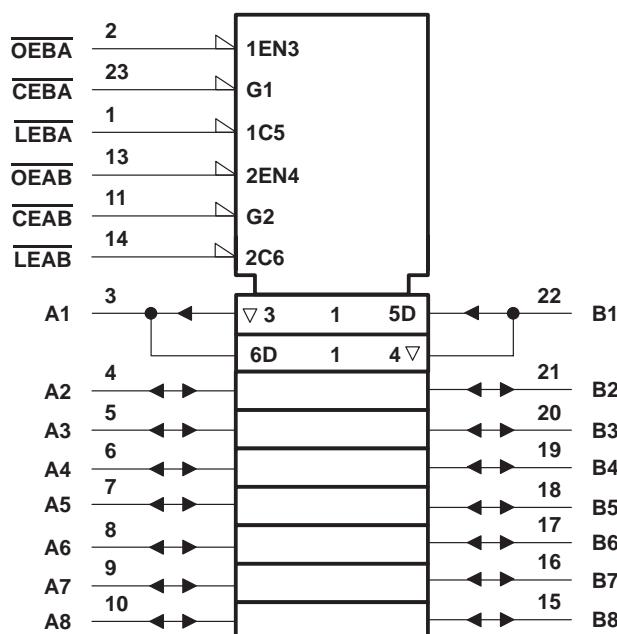
FUNCTION TABLE[†]

INPUTS				OUTPUT
CEAB	LEAB	OEAB	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0^{\ddagger}
L	L	L	L	L
L	L	L	H	H

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

[‡] Output level before the indicated steady-state input conditions were established

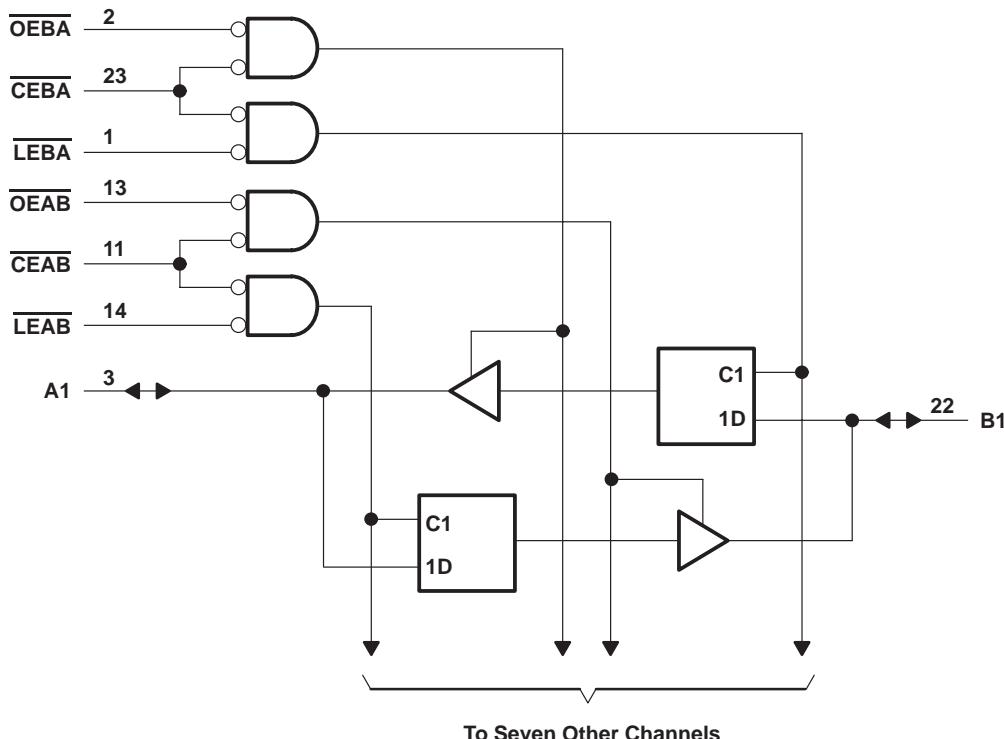
logic symbol[§]



[§] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DB, DW, JT, and PW packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.
For more information, refer to the *Package Thermal Considerations* application note in the 1994 ABT Advanced BiCMOS Technology Data Book, literature number SCBD002B.

**SN54LVT543, SN74LVT543
3.3-V ABT OCTAL REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS**

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recommended operating conditions (see Note 4)

		SN54LVT543		SN74LVT543		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	2.7	3.6	2.7	3.6	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage		5.5		5.5	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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SN54LVT543, SN74LVT543
3.3-V ABT OCTAL REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS
SCBS137D – MAY 1992 – REVISED JULY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54LVT543			SN74LVT543			UNIT			
		MIN	TYP†	MAX	MIN	TYP†	MAX				
V_{IK}	$V_{CC} = 2.7 \text{ V}$, $I_I = -18 \text{ mA}$			-1.2			-1.2	V			
V_{OH}	$V_{CC} = \text{MIN to MAX}^‡$, $I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$			$V_{CC} - 0.2$			V			
	$V_{CC} = 2.7 \text{ V}$, $I_{OH} = -8 \text{ mA}$	2.4			2.4						
	$V_{CC} = 3 \text{ V}$	$I_{OH} = -24 \text{ mA}$	2			2					
		$I_{OH} = -32 \text{ mA}$									
V_{OL}	$V_{CC} = 2.7 \text{ V}$	$I_{OL} = 100 \mu\text{A}$	0.2			0.2		V			
		$I_{OL} = 24 \text{ mA}$	0.5			0.5					
	$V_{CC} = 3 \text{ V}$	$I_{OL} = 16 \text{ mA}$	0.4			0.4					
		$I_{OL} = 32 \text{ mA}$	0.5			0.5					
		$I_{OL} = 48 \text{ mA}$	0.55								
		$I_{OL} = 64 \text{ mA}$				0.55					
I_I	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$	Control inputs	± 1			± 1		μA			
	$V_{CC} = 0 \text{ or MAX}^‡$, $V_I = 5.5 \text{ V}$		10			10					
	$V_{CC} = 3.6 \text{ V}$	$V_I = 5.5 \text{ V}$	A or B ports \S	20			20				
		$V_I = V_{CC}$		5			5				
		$V_I = 0$		-10			-10				
I_{off}	$V_{CC} = 0$, $V_I \text{ or } V_O = 0 \text{ to } 4.5 \text{ V}$						± 100	μA			
$I_{I(\text{hold})}$	$V_{CC} = 3 \text{ V}$	$V_I = 0.8 \text{ V}$	A or B ports	75			75		μA		
		$V_I = 2 \text{ V}$		-75			-75				
I_{OZH}	$V_{CC} = 3.6 \text{ V}$, $V_O = 3 \text{ V}$						1	μA			
I_{OZL}	$V_{CC} = 3.6 \text{ V}$, $V_O = 0.5 \text{ V}$						-1	μA			
I_{CC}	$V_{CC} = 3.6 \text{ V}$, $V_I = V_{CC} \text{ or GND}$	$I_O = 0$	Outputs high	0.13 0.19			0.13 0.19		mA		
			Outputs low	8.8 12			8.8 12				
			Outputs disabled	0.13 0.19			0.13 0.19				
$\Delta I_{CC}^¶$	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at $V_{CC} \text{ or GND}$			0.2			0.2				
C_I	$V_I = 3 \text{ V or } 0$			4.5			4.5				
C_{IO}	$V_O = 3 \text{ V or } 0$			11			11				

† All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused terminals at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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SN54LVT543, SN74LVT543**3.3-V ABT OCTAL REGISTERED TRANSCEIVERS****WITH 3-STATE OUTPUTS**

SCBS137D – MAY 1992 – REVISED JULY 1995

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVT543		SN74LVT543		UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
			MIN	MAX	MIN	MAX		
t _W	Pulse duration, LEAB or LEBA low		3.3	3.3	3.3	3.3	ns	
t _{SU}	Setup time	A or B before LEAB or LEBA↑	Data high	0	0	0	0	ns
			Data low	0.8	1.1	0.8	1.1	
	A or B before CEAB or CEBA↑	Data high	0	0	0	0		
		Data low	0.9	1.2	0.9	1.2		
t _H	Hold time		A or B after LEAB or LEBA↑	1.7	1.7	1.7	1.7	ns
	A or B after CEAB or CEBA↑			1.8	1.8	1.8	1.8	

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT543				SN74LVT543				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		
t _{PLH}	A or B	B or A	1	4.9	5.7	1	2.9	4.7	5.5	ns		
t _{PHL}			1	4.8	6	1	3.3	4.6	5.8			
t _{PLH}	LE	A or B	1	6.1	7.5	1	4	5.9	7.3	ns		
t _{PHL}			1	5.9	7.5	1	4.1	5.7	7.3			
t _{PZH}	OE	A or B	1	6	7.8	1	4.1	5.8	7.6	ns		
t _{PZL}			1.1	6.6	8.4	1.1	4.5	6.4	8.2			
t _{PHZ}	OE	A or B	2.4	6.7	7.3	2.4	4.8	6.5	7.1	ns		
t _{PLZ}			2	6	6.1	2	4	5.8	5.9			
t _{PZH}	CE	A or B	1	6.2	7.8	1	4.2	6	7.6	ns		
t _{PZL}			1.4	6.9	8.5	1.4	4.7	6.7	8.3			
t _{PHZ}	CE	A or B	2.3	6.6	7.3	2.3	4.7	6.4	7.1	ns		
t _{PLZ}			2	5.6	5.8	2	3.8	5.4	5.6			

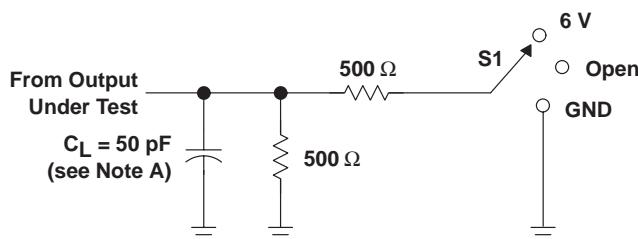
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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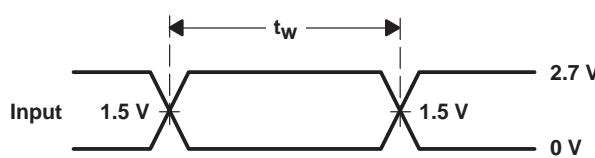
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PARAMETER MEASUREMENT INFORMATION

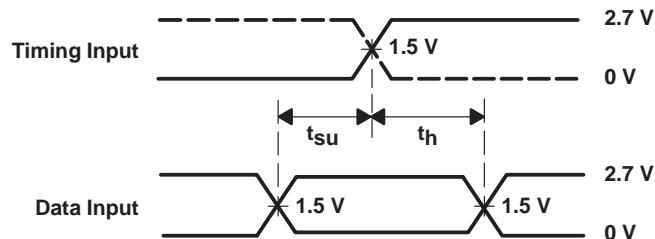


TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	6 V
tPHZ/tPZH	GND

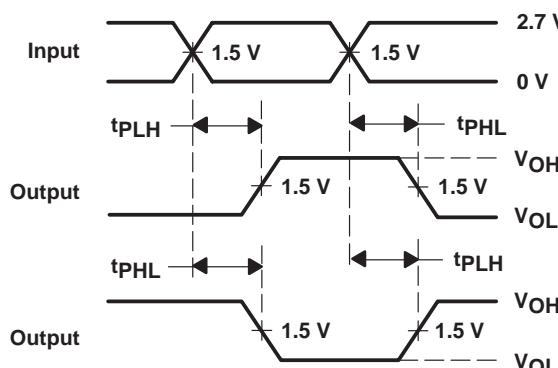
LOAD CIRCUIT FOR OUTPUTS



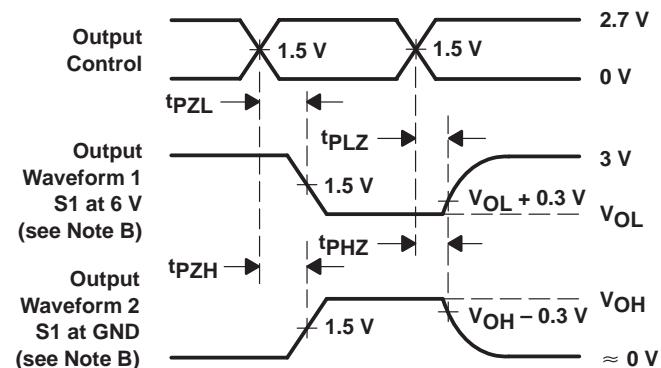
VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_f \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVT543DBLE	OBsolete	SSOP	DB	24		TBD	Call TI	Call TI
SN74LVT543DW	NRND	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVT543NSR	OBsolete	SO	NS	24		TBD	Call TI	Call TI
SN74LVT543PWLE	OBsolete	TSSOP	PW	24		TBD	Call TI	Call TI
SN74LVT543PWR	NRND	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

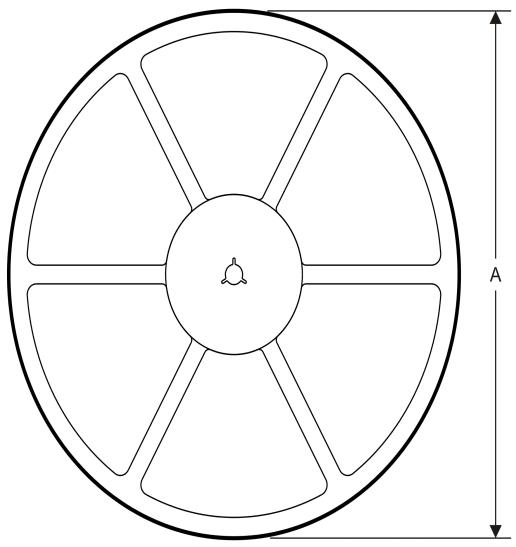
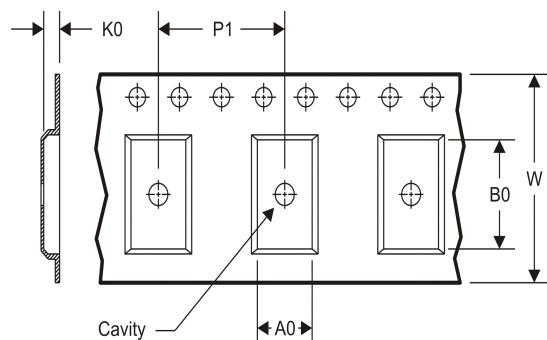
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

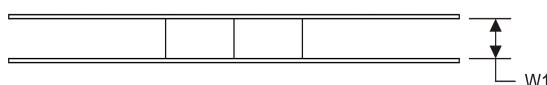
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers


TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVT543PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

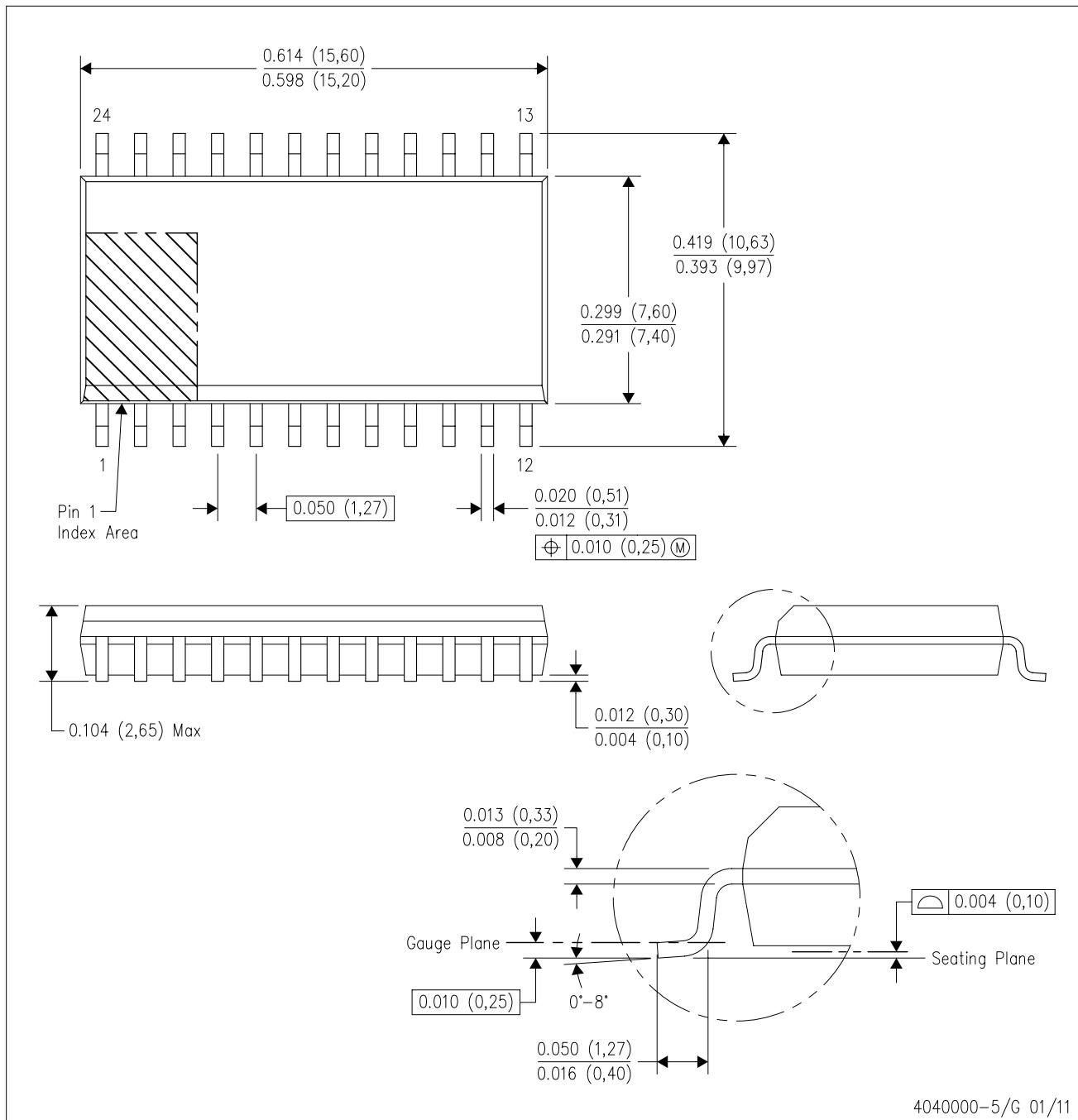
TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT543PWR	TSSOP	PW	24	2000	367.0	367.0	38.0

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

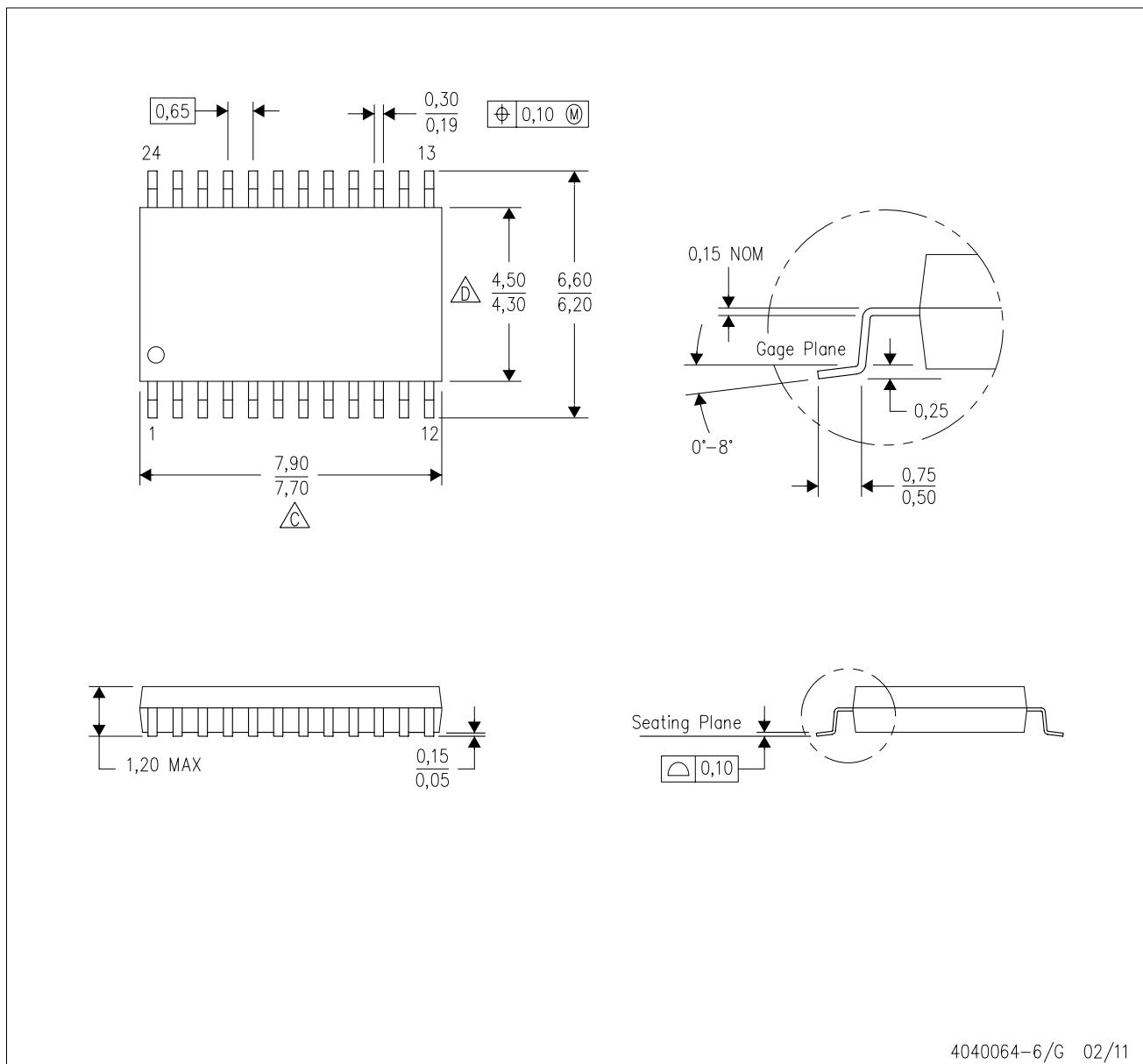


NOTES:

- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AD.

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

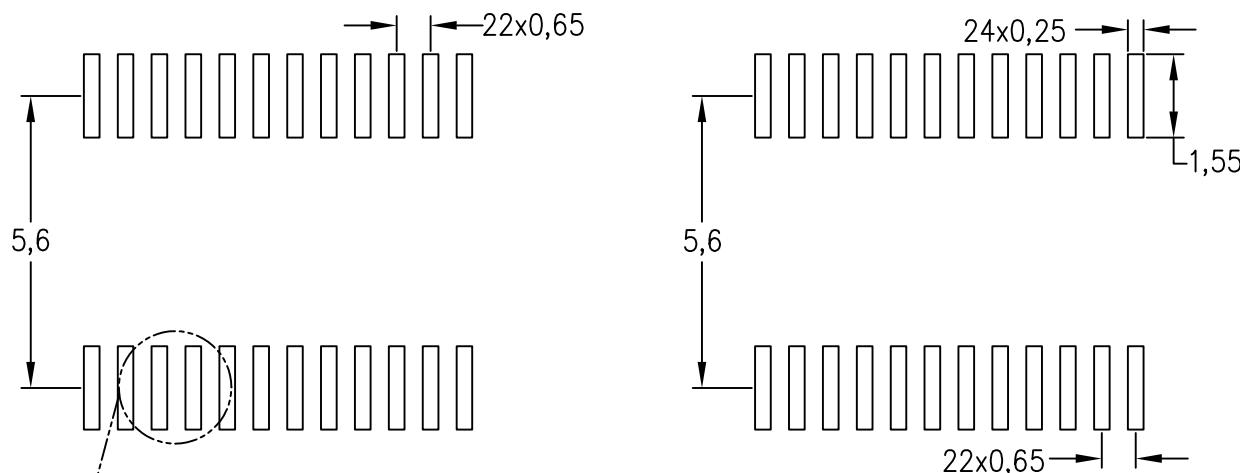
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PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

Example
Non Soldermask Defined PadExample
Solder Mask Opening
(See Note F)

Pad Geometry

1,6

All Around

4211284-4/E 07/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



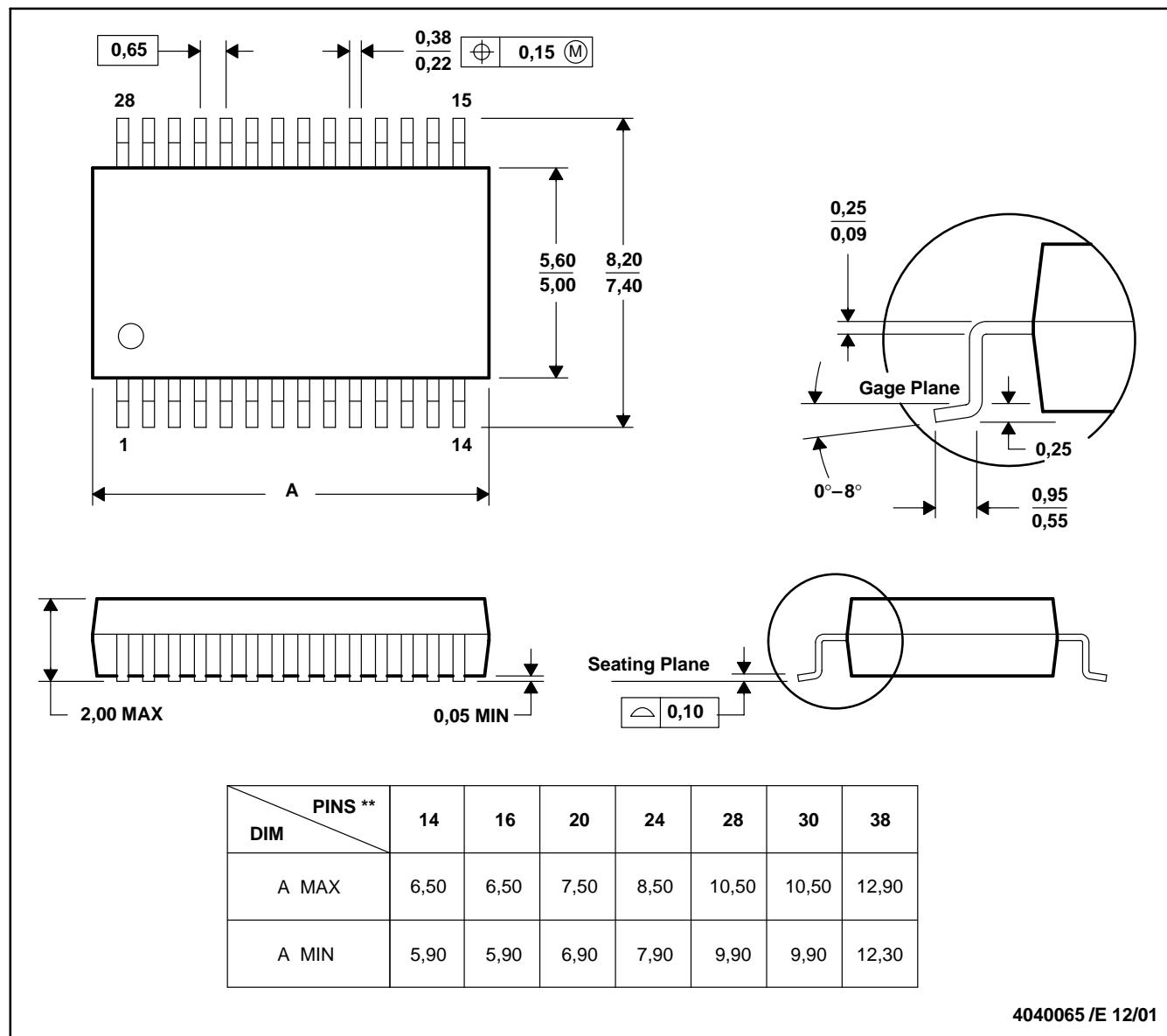
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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