PT6705 Series

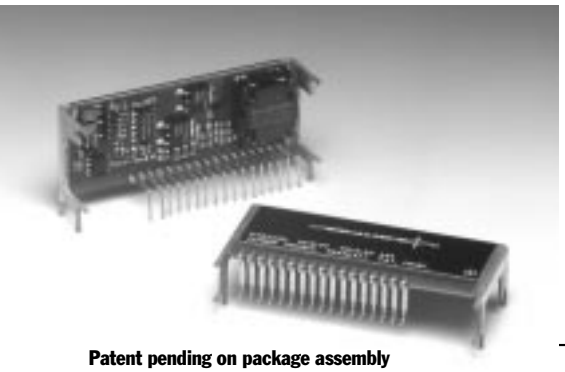
13 Amp 5V/3.3V Input Adjustable Integrated Switching Regulator

EXCALIBUR

Power Trends Products from Texas Instruments

SLTS099

(Revised 6/30/2000)



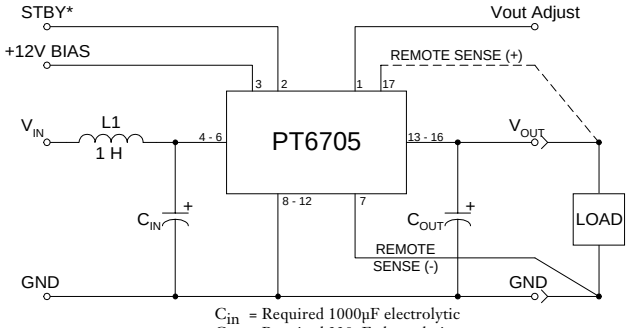
Patent pending on package assembly

- +3.3V/5V input (+12V Bias)
- Adjustable Output Voltage
- 90% Efficiency
- Differential Remote Sense
- 17-pin Space-Saving Package
- Solderable Copper Case
- Short Circuit Protection

The PT6705 is a series of low-cost, high-performance, 13 Amp Integrated Switching Regulators (ISRs) housed in a unique, space-saving 17-pin SIP package. The PT6705 will operate off either a 5V or 3.3V input bus to provide a low-voltage power source for the industry's latest high-speed, low-voltage µPs, and bus drivers.

The PT6705 incorporates internal short circuit protection, and requires a +12V/50mA bias input for operation.

Standard Application



C_{in} = Required 1000µF electrolytic
C_{out} = Required 330µF electrolytic
L1 = Optional 1µH input choke

Pin-Out Information

Pin	Function	Pin	Function
1	V_{out} Adjust	10	GND
2	STBY*	11	GND
3	+12V Bias Input	12	GND
4	V_{in}	13	V_{out}
5	V_{in}	14	V_{out}
6	V_{in}	15	V_{out}
7	Remote Sense Gnd (4)	16	V_{out}
8	GND	17	Remote Sense V_{out}
9	GND		

For STBY* pin
open = output enabled
ground = output disabled.

Specifications

Characteristics (T_a = 25°C unless noted)	Symbols	Conditions		PT6705 SERIES Min	Typ	Max	Units
Output Current	I_o	T_a = +60°C, 200 LFM, pkg N T_a = +25°C, natural convection		0.1 (1) 0.1 (1)	— —	13.0 13.0	A
Input Voltage Range	V_{in}	0.1A ≤I_o ≤13A	PT6705/6 PT6707/8	4.5 3.1	— —	5.5 5.5	V
External Bias Voltage Range	V_b	0.1A ≤I_o ≤13A, –40°C ≤Ta ≤+85°C		11.5	12.0	13.0	V
External Bias Current	I_b	0.1A ≤I_o ≤13A, –40°C ≤Ta ≤+85°C		—	—	50	mA
Output Voltage Tolerance	ΔV_o	V_{in} = +5V, V_b = +12V, I_o =13A -40°C ≤ T_a ≤ +85°C		V_o-0.03	—	V_o+0.03	V
Short-Circuit Threshold	I_{sc}	V_{in} = +5V, V_b = +12V		—	18	30	A
Line Regulation	Reg_{line}	4.5V ≤V_{in} ≤ 5.5V, V_b = +12V, I_o =13A		—	±5	—	mV
Load Regulation	Reg_{load}	V_{in} = +5V, Vb = +12V, 0.1 ≤I_o ≤13A		—	±10	—	mV
V_o Ripple/Noise	V_n	V_{in} = +5V, V_b = +12V, I_o =13A		—	35	—	mV
Transient Response with C_{out} = 330µF	t_{tr} V_{os}	I_o step between 6.5A and 13A V_o over/undershoot		— —	50 100	— —	µSec mV
Efficiency	η	V_{in} = +5V, I_o = 9A, V_b =+12V	V_o = 3.3V V_o = 2.5V V_o = 1.8V V_o = 1.5V	— — — —	91 88 85 83	— — — —	%
Switching Frequency	f_o	4.5V ≤V_{in} ≤5.5V, V_b = +12V 0.1A ≤ I_o ≤ 13A		300	350	400	kHz
Absolute Maximum Operating Temperature Range	T_a	Over V_{in} Range		-40 (2)	—	+85 (3)	°C
Storage Temperature	T_s	—		-40	—	+125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1msec, Half sine, mounted to a fixture		—	500	—	G
Mechanical Vibration		Per Mil-STD-883D, Method 2007.2, 20-2000 Hz, Soldered in a PC board		—	15	—	G
Weight	—	—		—	26	—	grams

Notes: *(1) The ISR-will operate down to no load with reduced specifications.*
(2) For operation below 0°C, Cin and Cout must have stable characteristics. Use either low ESR tantalum or Oscon® capacitors.
(3) See Safe Operating Area curves, or contact the factory for appropriate derating.
(4) If the remote sense ground is not used, pin 7 must be connected to pin 8 for optimum output voltage accuracy.

PT6705 Series

13 Amp 5V/3.3V Input Adjustable Integrated Switching Regulator

Ordering Information

PT6705❑ = 3.3 Volts
PT6706❑ = 2.5 Volts
PT6707❑ = 1.8 Volts
PT6708❑ = 1.5 Volts

PT Series Suffix (PT1234X)

Case/Pin Configuration	
Vertical Through-Hole	**N**
Horizontal Through-Hole	**A**
Horizontal Surface Mount	**C**

(For dimensions and PC board layout, see Package Styles 1340 and 1350.)

PT6700 Product Family

	Input Voltage	Vout Adjust	OVP/ Pwr Good	Requires +12V Bias
PT6701	5V	VID	✓	
PT6702	3.3V	VID	✓	
PT6705	5V	Resistor		✓
PT6715	5V	Resistor		
PT6721	12V	VID	✓	
PT6725	12V	Resistor		

Filter/Capacitor Selection

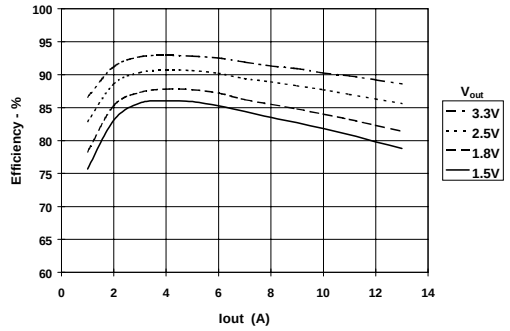
Output Capacitors: *The PT6705 requires a minimum ouput capacitance of 330µF for proper operation. The maximum allowable output capacitance is 15,000µF.*

Input Filter: *An input filter is optional for most applications. The input inductor must be sized to handle 10ADC with a typical value of 1µH. The input capacitance must be rated for a minimum of 2.0Arms of ripple current. For transient or dynamic load applications, additional capacitance may be required.*

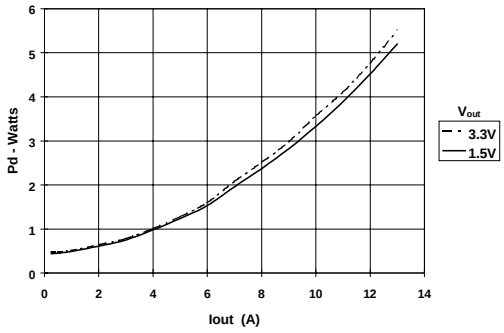
TYPICAL CHARACTERISTICS

All Models, V_{in} =5.0V *(Note A)*

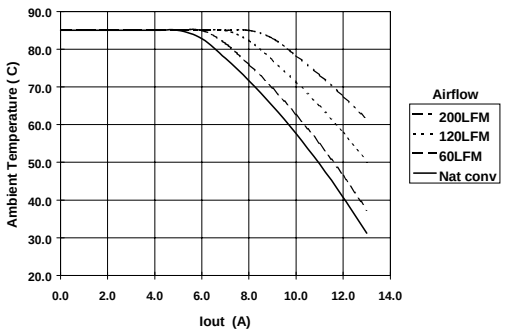
Efficiency vs Output Current



Power Dissipation vs Output Current

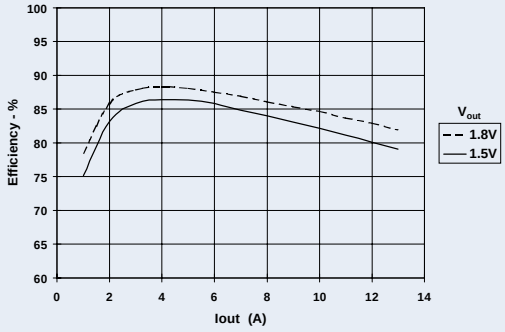


Safe Operating Area, PT6705, V_{in} =5.0V *(Note B)*

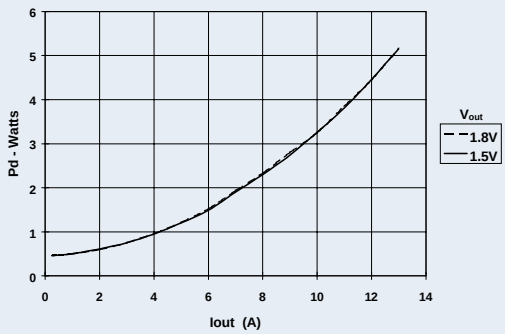


PT6707, PT6708, V_{in} =3.3V *(Note A)*

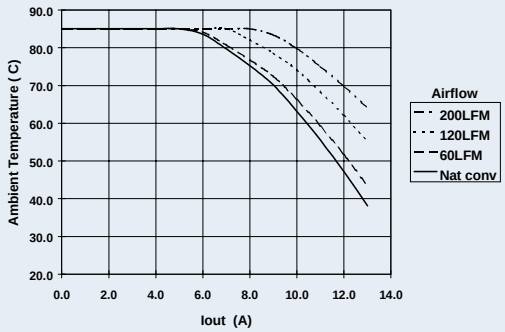
Efficiency vs Output Current



Power Dissipation vs Output Current



Safe Operating Area, PT6707, V_{in} =3.3V *(Note B)*



Note A: *All data in the above graphs has been developed from actual products tested at 25°C. This data is considered typcial for the ISR.*
Note B: *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures.*

Adjusting the Output Voltage of the PT6705 and PT6715 Excalibur™ Converters

Both the PT6705 and PT6715 series ISRs are non-programmable versions of the PT6700 Excalibur™ family of converters. These regulators have a fixed output voltage, which may be adjusted higher or lower than the factory trimmed pre-set voltage using a single external resistor. Table 1 gives the allowable adjustment range for each model as V_a (min) and V_a (max).

Adjust Up: An increase in the output voltage is obtained by adding a resistor R2, between pin 1 (V_o adjust) and pin 7 (–Remote Sense).

Adjust Down: Add a resistor (R1), between pin 1 (V_o adjust) and pin 17 (+Remote Sense).

Refer to Figure 1 and Table 2 for both the placement and value of the required resistor, either (R1) or R2 as appropriate.

Notes:

1. Use only a single 1% resistor in either the (R1) or R2 location. Place the resistor as close to the ISR as possible.
2. Never connect capacitors from V_o adjust to either GND, V_{out}, or the Remote Sense pins. Any capacitance added to the V_o adjust pin will affect the stability of the ISR.
3. If the Remote Sense feature is not being used, pin 7 must be connected to pin 8 for optimum output voltage accuracy. Correspondingly the resistors (R1) and R2 may be then be connected from V_o Adjust to either V_{out} or GND respectively.
4. The PT6705 series requires a 12V external bias voltage in order to operate (see data sheet). An external bias voltage is not required for the PT6715 series.
5. Adjusting the output voltage of the PT6705 and PT6715 (3.3V models) higher than the factory pre-trimmed output voltage may require an increase in the minimum input voltage. These two models must comply with the following requirements for V_{in}(min).

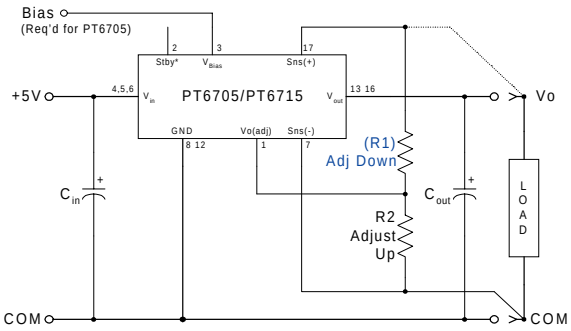
PT670x models:

V_{in}(min) = (V_a + 1)V

PT671x models:

V_{in}(min) = (V_a + 1)V or 4.5V, whichever is greater.

Figure 1



The values of (R1) [adjust down], and R2 [adjust up], can also be calculated using the following formulas.

$$(R1) = \frac{10\cdot(V_a - 1.27)}{(V_o - V_a)} - R_s \quad k\Omega$$

$$R2 = \frac{12.7}{V_a - V_o} - R_s \quad k\Omega$$

Where: V_o = Original output voltage
V_a = Adjusted output voltage
R_s = Series resistance value from Table 1

Table 1

PT6705/PT6715 SERIES ADJUSTMENT PARAMETERS

Series Pt #				
12V Bias (4)	PT6708	PT6707	PT6706	PT6705
No-Bias	PT6718	PT6717	PT6716	PT6715
V_o (nom)	1.5	1.8	2.5	3.3
V_a (min)	1.47	1.75	2.25	2.75
V_a (max)	1.73	2.0	2.85	3.75
R_S (kΩ)	49.9	49.9	33.2	24.9

Table 2

PT6705/PT6715 SERIES ADJUSTMENT RESISTOR VALUES

Series Pt #				
12V Bias [4]	**PT6708**	**PT6707**	**PT6706**	**PT6705**
No Bias	**PT6718**	**PT6717**	**PT6716**	**PT6715**
V_o (nom)	**1.5**	**1.8**	**2.5**	**3.3**
V_a (req'd)				
1.47	(16.8)kΩ			
1.5				
1.55	204.0kΩ			
1.6	77.1kΩ			
1.65	34.8kΩ			
1.7	13.6kΩ			
1.75		(46.1)kΩ		
1.8				
1.85		204.0kΩ		
1.9		77.1kΩ		
1.95		34.8kΩ		
2.0		13.6kΩ		
2.05				
2.1				
2.15				
2.2				
2.25			(6.0)kΩ	
2.3			(18.3)kΩ	
2.35			(38.8)kΩ	
2.4			(79.8)kΩ	
2.45			(203.0)kΩ	
2.5				
2.55			221.0kΩ	
2.6			93.8kΩ	
2.65			51.5kΩ	
2.7			30.3kΩ	
2.75			17.6kΩ	(2.0)kΩ
2.8			9.1kΩ	(5.7)kΩ
2.85			3.1kΩ	(10.2)kΩ
2.9				(15.9)kΩ
2.95				(23.1)kΩ
3.0				(32.8)kΩ
3.05				(46.3)kΩ
3.1				(66.6)kΩ
3.15				(100.0)kΩ
3.2				(168.0)kΩ
3.25				(371.0)kΩ
3.3				
3.35				229.0kΩ
3.4				102.0kΩ
3.45				59.8kΩ
3.5				38.6kΩ
3.55		Requires V_{in} > 4.5Vdc [5]		25.9kΩ
3.6				17.4kΩ
3.65				11.4kΩ
3.7				6.9kΩ
3.75				3.3kΩ

R1 = (Blue) R2 = Black

Package Style 1340

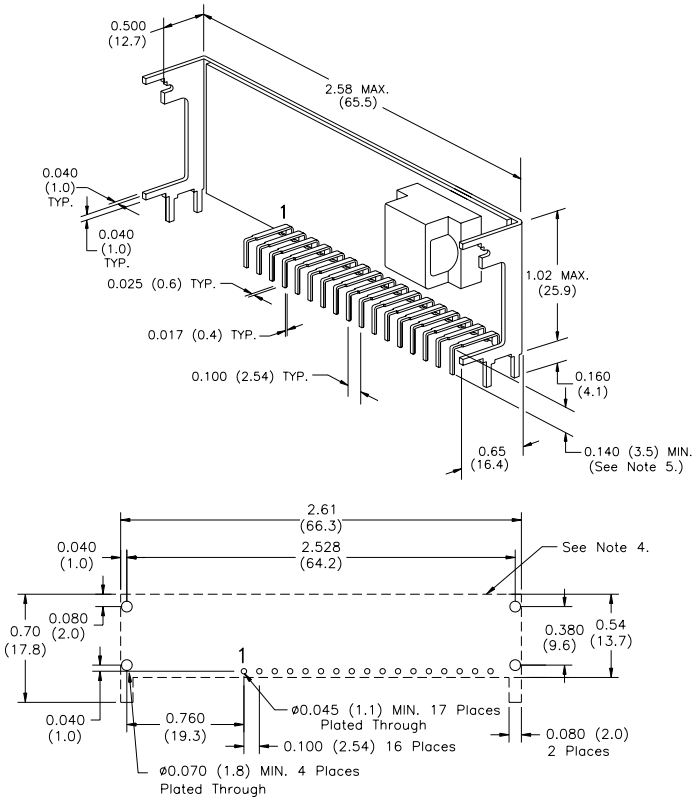
Power Trends Products from Texas Instruments

Suffix N

(Revised 6/30/2000)

PACKAGE INFORMATION AND DIMENSIONS

Vertical Through-Hole Mount (Suffix N)



PC Layout

Notes: (Rev. E)

1: All dimensions are in inches (mm).
2: 2 place decimals are ±.030 (±0.8mm).
3: 3 place decimals are ±.010 (±0.3mm).
4: Recommended mechanical keep out area (dotted line).
5: Electrical pin length mounted on printed circuit board seating plane to pin end.

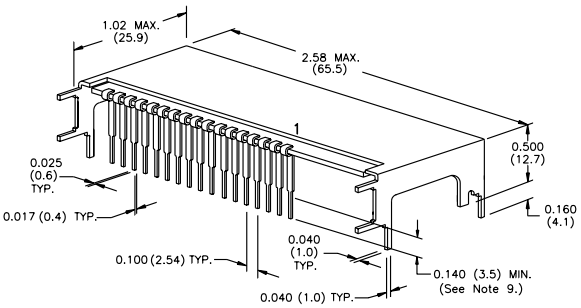
Package Style 1350

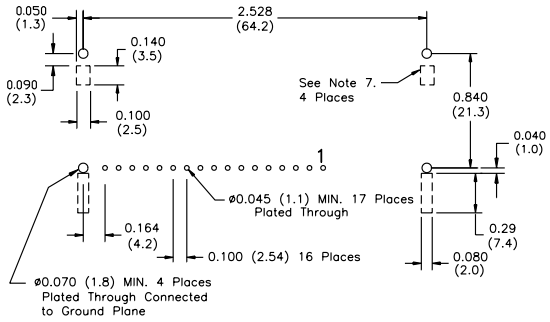
Suffix A, C

(Revised 6/30/2000)

PACKAGE INFORMATION AND DIMENSIONS

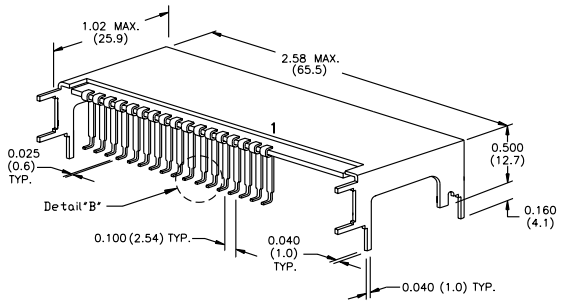
Horizontal Through–Hole Mount (Suffix A)

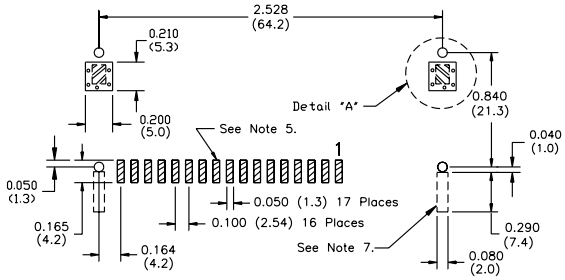




PC Layout

Horizontal Surface Mount (Suffix C)

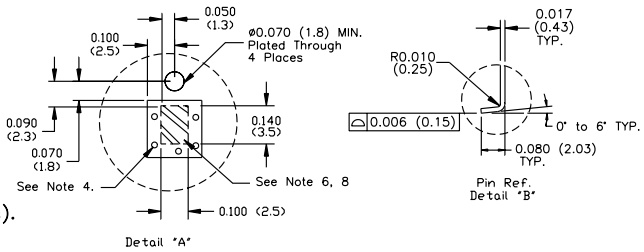




PC Layout

Notes: (Rev. E)

1: All dimensions are in inches (mm).
2: 2 place decimals are ±.030 (±0.8mm)
3: 3 place decimals are ±.010 (±0.3mm).
4: Vias are recommended to improve copper adhesion.
5: Power pin connections should utilize two or more vias per input, ground and output pin.
6: Solder mask openings to copper island for solder joints to mechanical pins.
7: Recommended mechanical keep out area (dotted lines).
8: Electrically connect case to ground plane.
9: Electrical pin length (Horizontal Through– Hole) mounted on printed circuit board seating plane to pin end.



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