TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6J05

ROW DRIVER FOR A DOT MATRIX LCD

The T6J05 is a 128-channel-output row driver for an STN dot matrix LCD. The T6J05 features an 80-V LCD drive voltage. The T6J05 is able to drive LCD panels with a duty ratio of up to 1/480. It is recommended for use with the T6C71.

Unit: mm

T6J05	Lead Pitch	
	IN	OUT
(UAM, 3NS)	0.8	0.20
(UBM, 3NS)	0.8	0.24
(UDN, 3NS)	0.8	0.18

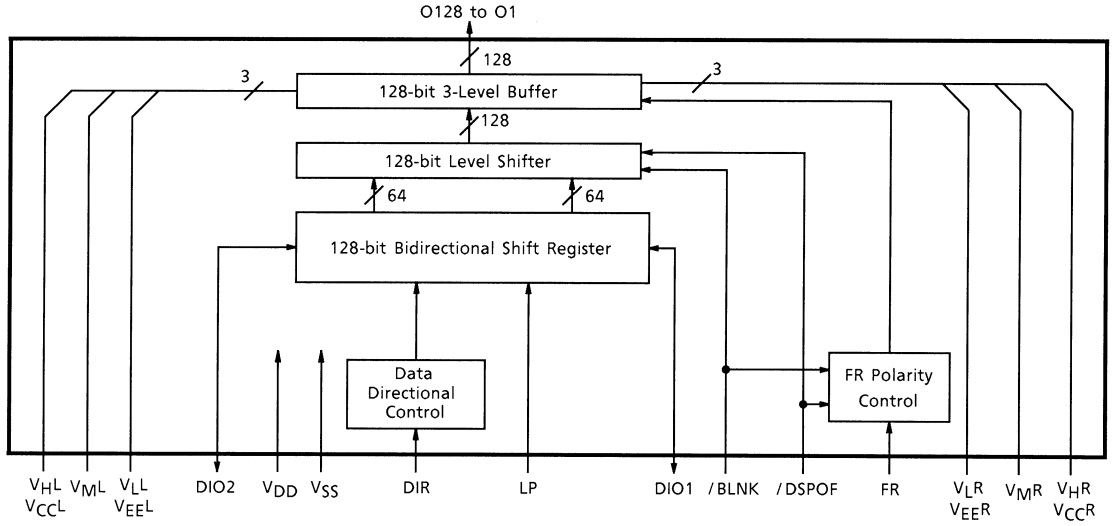
Please contact Toshiba or an authorized Toshiba dealer for information on package dimensions.

TCP (Tape Carrier Package)

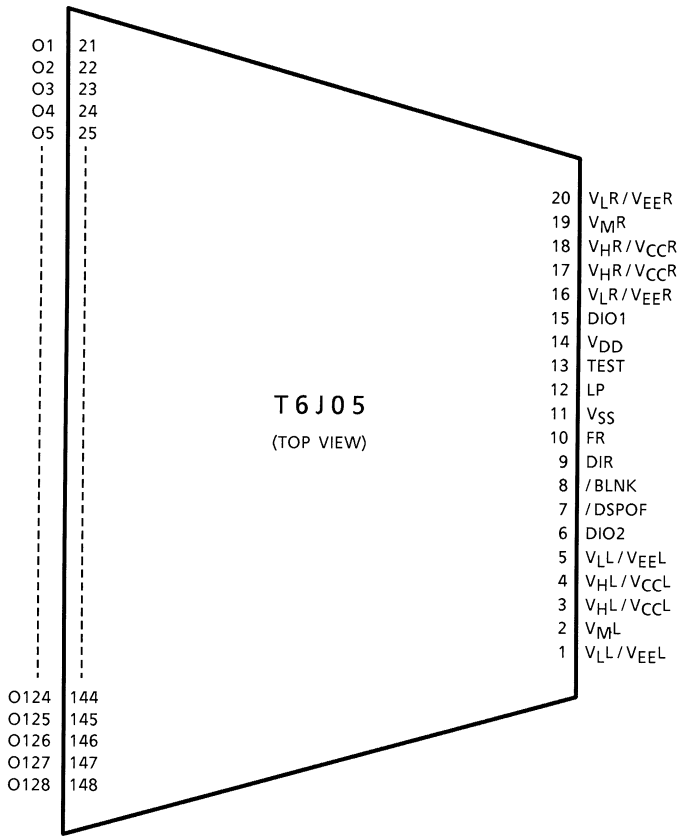
Features

- Display duty application : to 1/480
- LCD drive signal : 128
- Data transfer : 128-bit bidirectional
  (1) O1 → O128
  (2) O128 → O1
- LCD drive voltage : V_{CC} = 18.5 to 42.5 V, V_M = 2.5 V, V_{EE} = −13.5 to −37.5 V
- Power supply voltage : 2.7 to 5.5 V
- Operating temperature : −20 to 75°C
- LCD drive output resistance : 0.6 kΩ (typ.) (V_{CC} = V_H = 32.5 V, V_{EE} = V_L = −27.5 V)
- Display-off function : When/DSPOF is L, all LCD drive outputs (O1 to O128) remain at the V_M level.
- LCD drive output timing : Change on falling edge of LP
- Blanking function : Provision of a blanking interval prevents excessively high voltages being applied to the electrodes of the liquid crystal panel.
  /BLNK = L: Blanking. All LCD drive outputs (O1 to O128) are set to the V_M level.
  /BLNK = H: (O1 to O128) are operational.

Block Diagram



Pin Assignment



Note: The above diagram shows the pin configuration of the LSI chip, not that of the tape carrier package. It short-circuits V_{LL} and V_{EEL}/V_{HL} and V_{CCL} on the chip.

Pin Functions

Pin Name	I / O	Functions	Level
O1 to O128	Output	Output for LCD drive signal	V_H / V_M / V_L
DIO1, DIO2	I / O	Input / output for shift data DIR = L: DIO1 is input, DIO2 is output DIR = H: DIO1 is output, DIO2 is input	V_{DD} to V_{SS}
LP	Input	(Shift Clock Pulse) Input for shift clock pulse	
FR	Input	(Frame) Input for frame signal	
DIR	Input	(Direction) Input for data flow direction select	
/ DSPOF	Input	(Display Off) / DSPOF = L: Display−off mode, (O1 to O128) remain at the V_M level. Latch outputs cleared after release / DSPOF = H: Display−on mode, (O1 to O128) are operational	
/ BLNK	Input	(Blanking Function) Blanking−off mode. (O1 to O128) remain at V_M level. Latch outputs not cleared Blanking−on mode. (O1 to O128) are operational	
TEST	Input	(Test) Fix to L	
V_{DD}	—	Power supply for internal logic (5 V)	—
V_{SS}	—	Power supply for internal logic (0 V)	
V_HL / R V_{CC}L / R	—	Power supply for LCD drive circuit	
V_ML / R	—	Power supply for LCD drive circuit	
V_LL / R V_{EE}L / R	—	Power supply for LCD drive circuit	

Relation Between FR, Data Input and Output Level Format

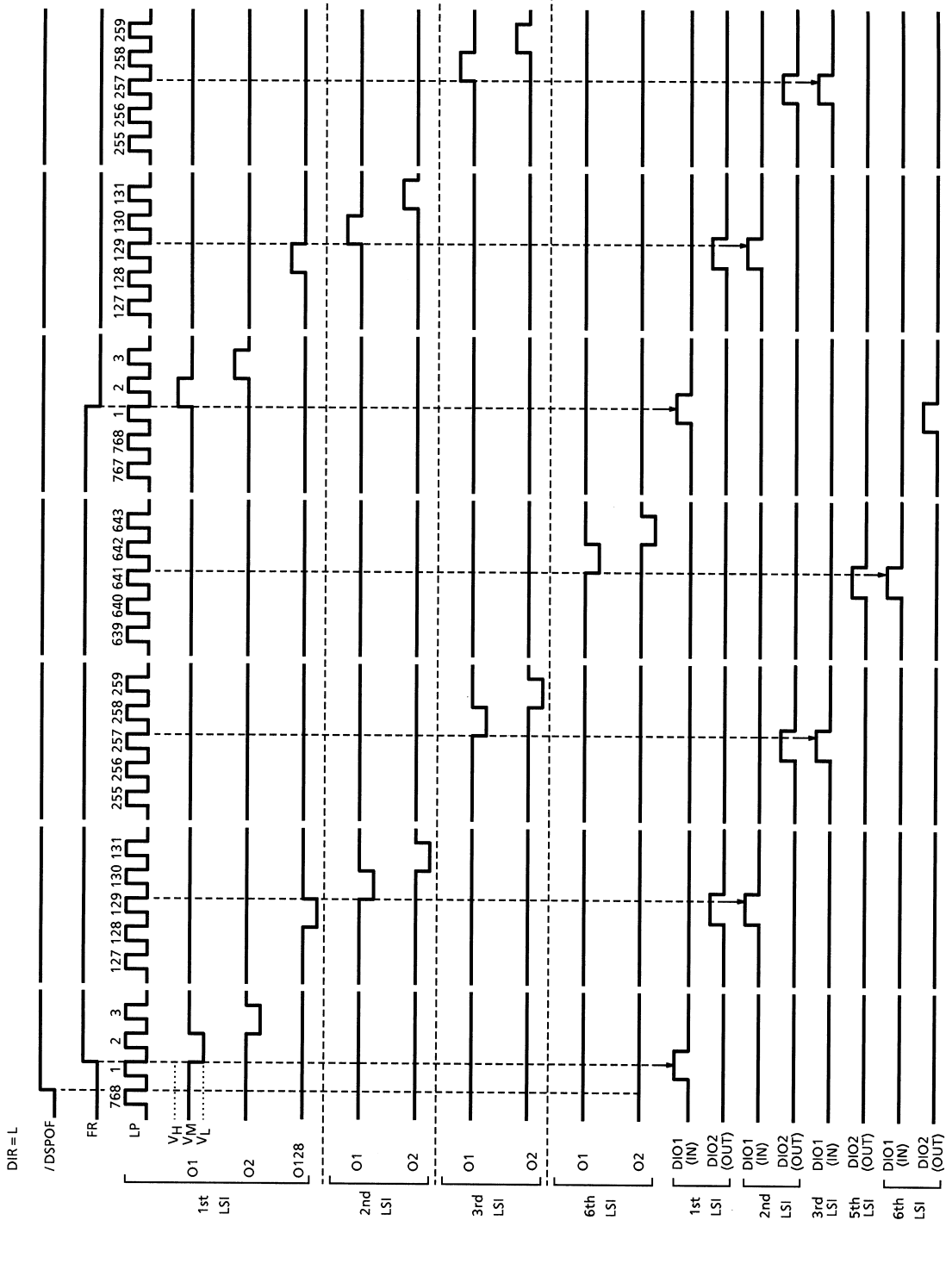
F R	Data Input	/ Dspof Or / Blnk	Output Level
L	L	H	V_M
L	H	H	V_H
H	L	H	V_M
H	H	H	V_L
*	*	L	V_M

*: Don't Care

Data Input Format

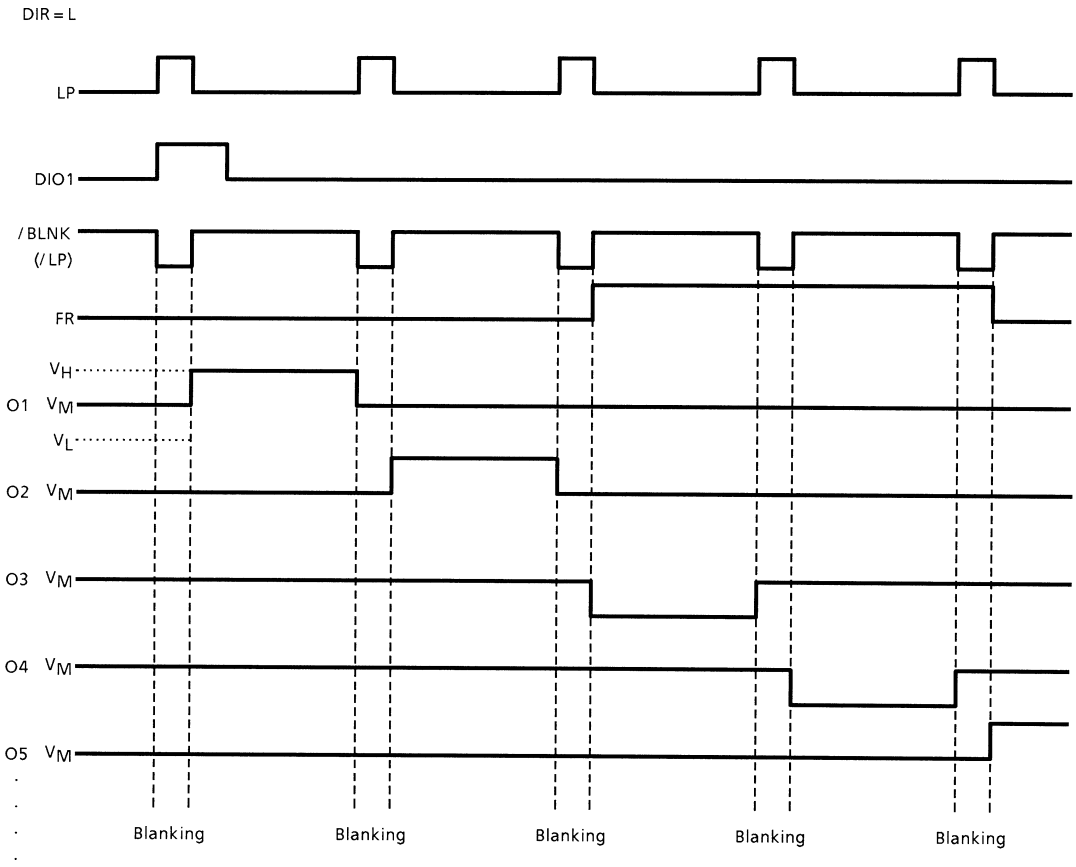
Dual	Data Flow	Data Input Terminals	
		DIO1	DIO2
L	O1 → O128	IN	OUT
H	O128 → O1	OUT	IN

Timing Diagram 1



T6J05 – 5

Timing Diagram 2 (Blanking function)



Absolute Maximum Ratings

(Ensure that the following conditions are maintained, $V_{CC} \geq V_H \geq V_{DD} \geq V_M \geq V_{SS} \geq V_L \geq V_{EE}$) (Note 1)

Item	Symbol	Pin Name	Rating	Unit
Supply Voltage 1	V_{DD}	V_{DD}	−0.3 to 7.0	V
Supply Voltage 2	$V_{CC} - V_{EE}$	$V_{CC}L$ / R, $V_{EE}L$ / R	−0.3 to 85	V
	$V_H - V_{EE}$	$V_H L$ / R, $V_{EE}L$ / R	−0.3 to 85	
Supply Voltage 3	$V_M - V_{EE}$	$V_M L$ / R, $V_{EE}L$ / R	−0.3 to 85	V
Supply Voltage 4	$V_L - V_{EE}$	$V_L L$ / R, $V_{EE}L$ / R	−0.3 to 85	V
Input Voltage	V_{IN}	(Note 2)	−0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opr}	—	−20 to 75	°C
Storage Temperature	T_{stg}	—	−40 to 125	°C

Note 1: Input voltage: $V_{SS} \rightarrow V_{DD} \rightarrow V_{EE}$ / $V_L \rightarrow V_{CC}$ / $V_H \rightarrow V_M$

Note 2: LP, FR, DIR, DUAL, DIO1, DIO2, DMIN, / DSPOF, / BLNK, TEST

Electrical Characteristics

DC Characteristics(Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Ta = −20 to 75°C)
(Ensure that the following conditions are maintained, $V_{CC} \geq V_H \geq V_{DD} \geq V_M \geq V_{SS} \geq V_L \geq V_{EE}$)

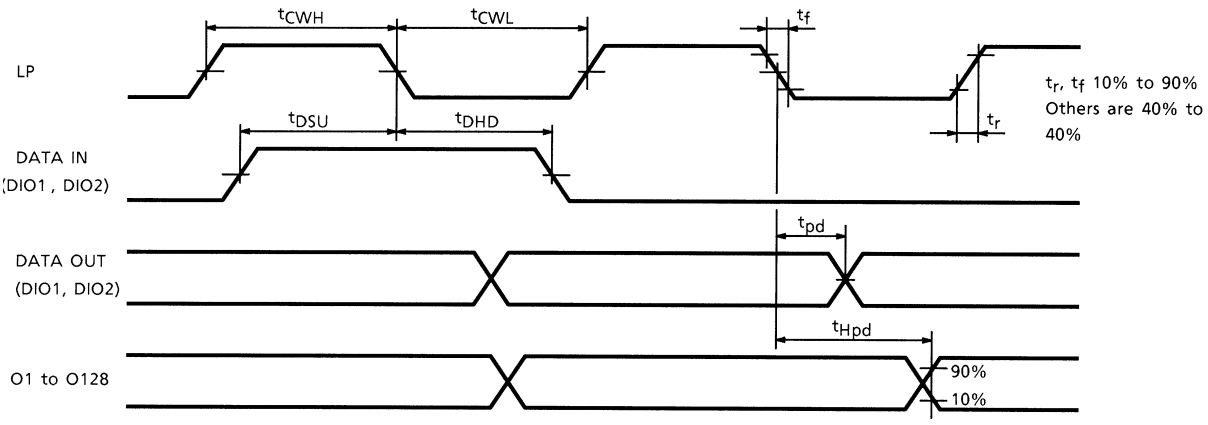
Item		Symbol	Test Circuit	Test Condition			Min	Typ.	Max	Unit	Pin Name
Supply Voltage 1		V_{DD}	—	—			2.7	5.0	5.5	V	V_{DD}
Supply Voltage 2		$V_{CC}-V_M$ V_M-V_{EE}	—	—			16	—	40	V	$V_{CC}L$ / R $V_{EE}L$ / R
Input Voltage	H Level	V_{IH}	—	(Note 3)			0.6 V_{DD}	—	V_{DD}	V	(Note 2)
	L Level	V_{IL}		(Note 3)			0	—	0.2 V_{DD}		
Output Voltage	H Level	V_{OH}	—	I_{OH} = −0.5 mA			V_{DD} − 0.5	—	V_{DD}	V	DIO1 DIO2
	L Level	V_{OL}		I_{OL} = 0.5 mA			0	—	0.5		
Output Resistance	H Level	R_{OH}	—	$V_{OUT} = V_H$ − 0.5 V		(Note 4)	—	0.6	1.2	kΩ	O1 to O128
	M Level	R_{OM}		$V_{OUT} = V_M$ + 0.5 V		(Note 4)	—	0.6	1.2		
		R_{OM}		$V_{OUT} = V_M$ − 0.5 V		(Note 4)	—	0.6	1.2		
	L Level	R_{OL}		$V_{OUT} = V_L$ + 0.5 V		(Note 4)	—	0.6	1.2		
Current Consumption		I_{SS} Ope	—	V_{DD} = 5.5 V	$V_{CC} - V_{EE}$ = 80 V	Function (Note 5)	—	—	60	μA	V_{DD}
				V_{DD} = 2.7 V			—	—	30		
		I_{CC} Ope		V_{DD} = 5.5 V		Function (Note 5)	—	—	200		$V_{CC}L$ / R
				V_{DD} = 2.7 V			—	—	200		
		I_{CC} Leak		V_{DD} = 5.5 V		Standby	−10	—	10		$V_{CC}L$ / R

Note 3: V_{DD} = 4.5 to 5.5 V, V_{DD} = 2.7 V: V_{IH} = 0.7 V_{DD} (min), V_{IL} = 0.2 V_{DD} (max)

Note 4: V_{DD} = 2.7 V, V_H = 32.5 V, V_M = 2.5 V, V_L = − 27.5 V

Note 5: No load, f_{LP}= 48 kHz, f_{FR} = 2.4 kHz, f_{DIO} = 400 Hz, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$

AC Characteristics



Test Conditions (1) (V_{DD} = 4.5 to 5.5 V)

Item		Symbol	Test Condition	Min	Max	Unit
LP Pulse Width H		t_{CWH}	LP	30	—	ns
LP Pulse Width L		t_{CWL}	LP	195	—	ns
Input Rise / Fall Time		t_r, t_f	LP, FR, DIO1, DIO2	—	50	ns
Data Set−up Time		t_{DSU}	DIO1, DIO2	30	—	ns
Data Hold Time		t_{DHD}	DIO1, DIO2	30	—	ns
Output Data Delay Time	(Note 6)	t_{pd}	DIO1, DIO2	40	150	ns
LCD Drive Data Delay Time	(Note 7)	t_{Hpd}	O1 to O128	—	1.0	μs

Note 6: C_L = 30 pF
Note 7: No load, V_{SS} = 0 V, V_M = 2.5 V, V_H = 42.5 V, V_L = −37.5 V

Test Conditions (2) (V_{DD} = 2.7 to 4.5 V)

Item		Symbol	Test Condition	Min	Max	Unit
LP Pulse Width H		t_{CWH}	LP	100	—	ns
LP Pulse Width L		t_{CWL}	LP	400	—	ns
Input Rise / Fall Time		t_r, t_f	LP, FR, DIO1, DIO2	—	50	ns
Data Set−up Time		t_{DSU}	DIO1, DIO2	60	—	ns
Data Hold Time		t_{DHD}	DIO1, DIO2	30	—	ns
Output Data Delay Time	(Note 8)	t_{pd}	DIO1, DIO2	40	400	ns
LCD Drive Data Delay Time	(Note 9)	t_{Hpd}	O1 to O128	—	1.2	μs

Note 8: C_L = 30 pF
Note 9: No load, V_{SS} = 0 V, V_M = 2.5 V, V_H = 42.5 V, V_L = −37.5 V

Handling Precautions

- Insert the bypass capacitor (0.1 μF) between V_{DD} and V_{SS} to decrease power supply noise.
  Position the bypass capacitor as close to the LSI as possible.
- Set/DSPDF to L at power on so as to protect power supply IC.
- Pay attention to measure and treatment of latch-up because being high-withstand pressure product.

RESTRICTIONS ON PRODUCT USE

000707EBE

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury (“Unintended Usage”). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer’s own risk.
- Polyimide base film is hard and thin. Be careful not to injure yourself on the film or to scratch any other parts with the film. Try to design and manufacture products so that there is no chance of users touching the film after assembly, or if they do , that there is no chance of them injuring themselves. When cutting out the film, try to ensure that the film shavings do not cause accidents. After use, treat the leftover film and reel spacers as industrial waste.
- Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases this can cause the device to malfunction.
  This is especially true for devices in which the surface (back), or side of the chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. Exposure to light both during regular operation and during inspection must be taken into account.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.