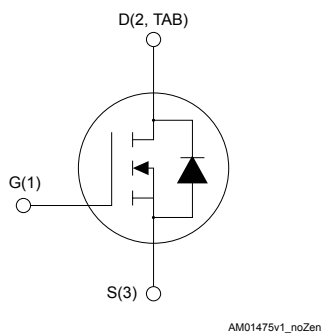
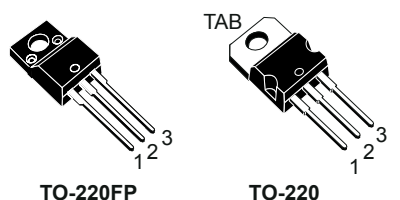


N-channel 650 V, 390 mΩ typ., 8.5 A MDmesh M5 Power MOSFET in a TO-220FP and TO-220 packages



Features

Order code	$V_{DS} @ T_J \text{ max.}$	$R_{DS(on)} \text{ max.}$	I_D
STF12N65M5	710 V	430 mΩ	8.5 A
STP12N65M5			

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.



Product status links

[STF12N65M5](#)

[STP12N65M5](#)

Product summary

Order code	STF12N65M5
Marking	12N65M5
Package	TO-220FP
Packing	Tube
Order code	STP12N65M5
Marking	12N65M5
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP	TO-220	
V_{DS}	Drain-source voltage	650		V
V_{GS}	Gate-source voltage	25		V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	8.5 ⁽¹⁾	8.5	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	5.4 ⁽¹⁾	5.4	
$I_{DM}^{(2)}$	Drain current (pulsed)	34	34	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	25	70	W
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	2.5		A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	150		mJ
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$, $T_C = 25\text{ °C}$)	2.5		kV
T_{stg}	Storage temperature range	-55 to 150		°C
T_J	Operating junction temperature range			°C

1. Limited by maximum junction temperature.
2. Pulse width is limited by safe operating area.
3. $I_{SD} \leq 8.5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220FP	TO-220	
R_{thJC}	Thermal resistance, junction-to-case	5.00	1.79	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5		°C/W

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 4.3\text{ A}$		390	430	m Ω

1. Specified by design, not tested in production.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	900	-	pF
C_{oss}	Output capacitance		-	22	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0\text{ V}$	-	64	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	21	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	5	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 4.25\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 17. Test circuit for gate charge behavior)	-	20	-	nC
Q_{gs}	Gate-source charge		-	4.8	-	nC
Q_{gd}	Gate-drain charge		-	8.3	-	nC

- $C_{o(tr)}$ is an equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.
- $C_{o(er)}$ is an equivalent capacitance that provides the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 400\text{ V}$, $I_D = 5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	22.6	-	ns
$t_{r(v)}$	Voltage rise time		-	17.6	-	ns
$t_{f(i)}$	Current fall time	(see Figure 18. Test circuit for inductive load switching and diode recovery times and Figure 21. Switching time waveform)	-	15.6	-	ns
$t_{c(off)}$	Crossing time		-	23.4	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		8.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		34	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 8.5 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 8.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 100 \text{ V}$ (see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	230		ns
Q_{rr}	Reverse recovery charge		-	2.2		μC
I_{RRM}	Reverse recovery current		-	19		A
t_{rr}	Reverse recovery time	$I_{SD} = 8.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 100 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	280		ns
Q_{rr}	Reverse recovery charge		-	2.7		μC
I_{RRM}	Reverse recovery current		-	19		A

1. Pulse width is limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

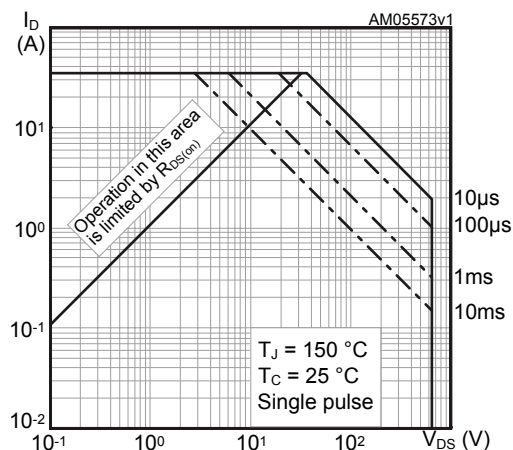
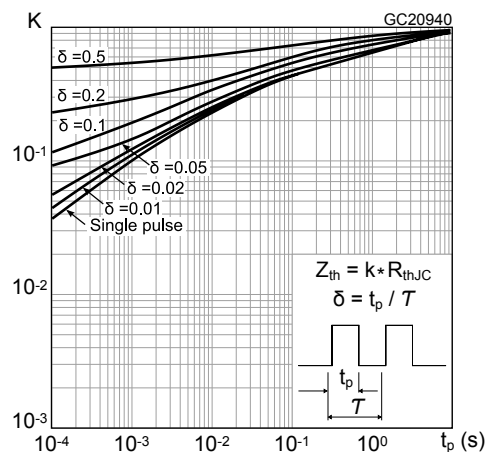
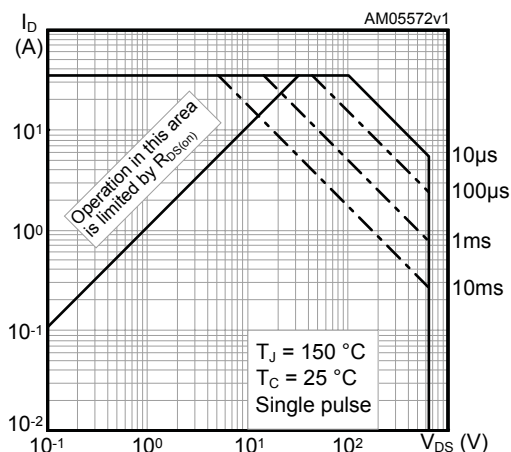
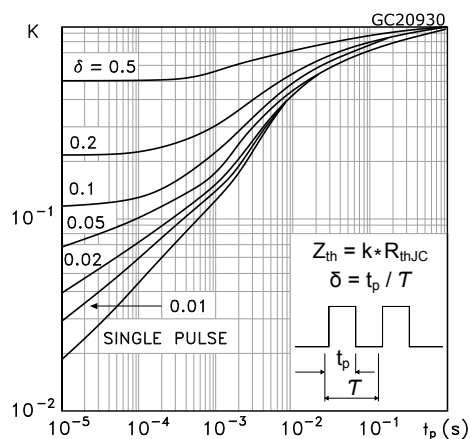
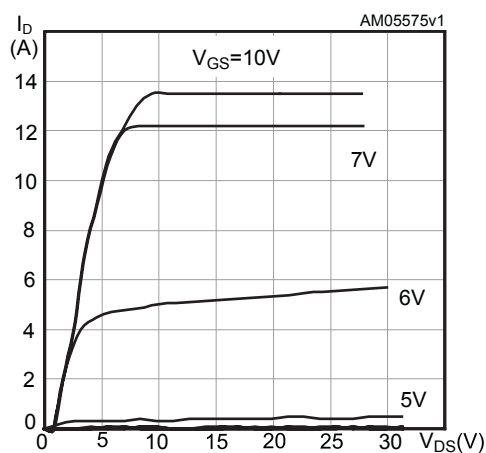
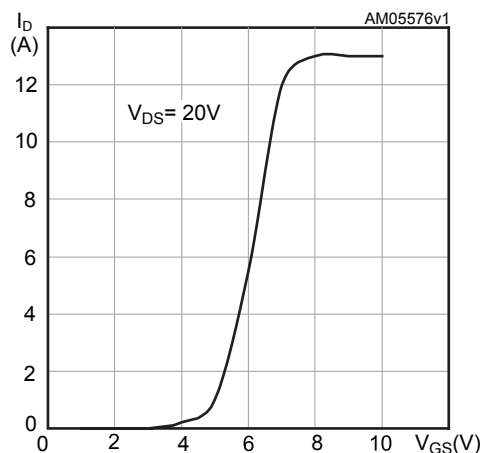
Figure 1. Safe operating area for TO-220FP

Figure 2. Normalized transient thermal impedance for TO-220FP

Figure 3. Safe operating area for TO-220

Figure 4. Normalized transient thermal impedance for TO-220

Figure 5. Typical output characteristics

Figure 6. Typical transfer characteristics


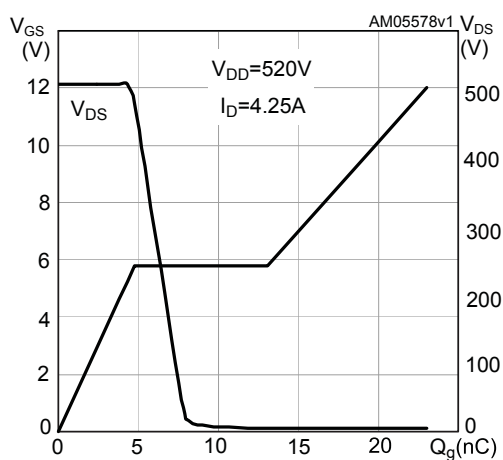
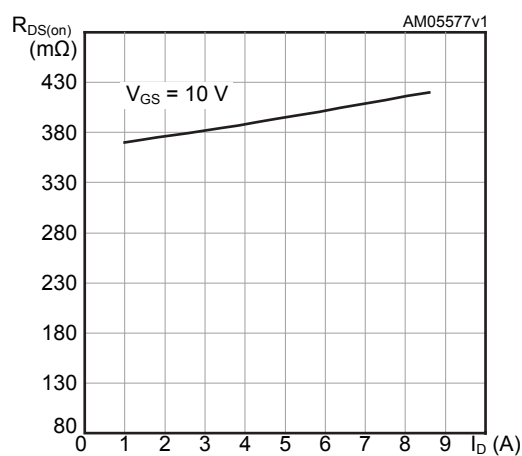
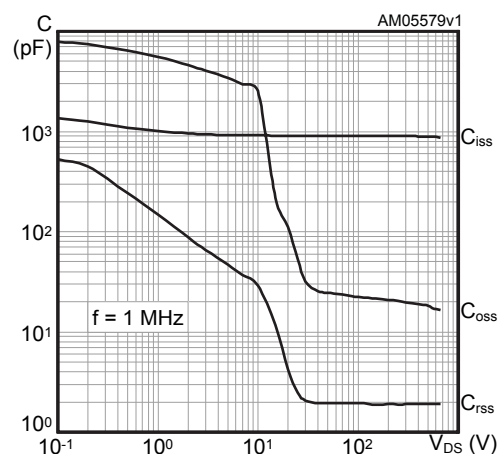
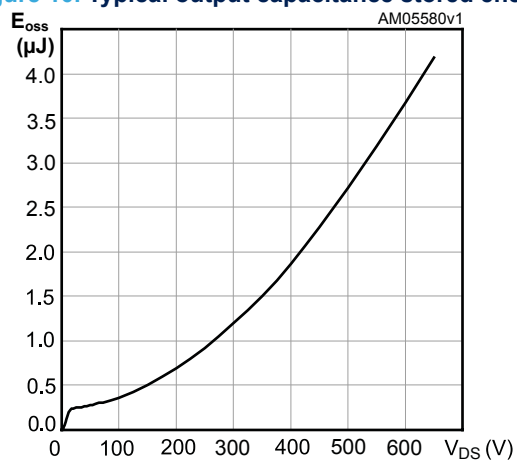
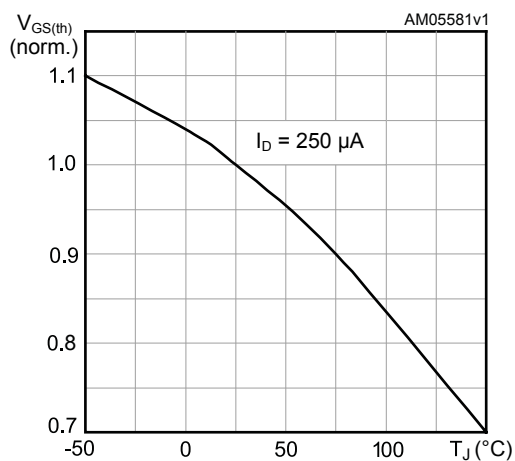
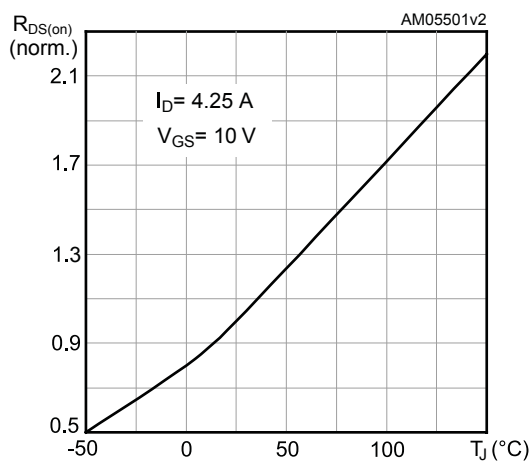
Figure 7. Typical gate charge characteristics

Figure 8. Typical drain-source on-resistance

Figure 9. Typical capacitance characteristics

Figure 10. Typical output capacitance stored energy

Figure 11. Normalized gate threshold voltage vs temperature

Figure 12. Normalized on-resistance vs temperature


Figure 13. Normalized breakdown voltage vs temperature

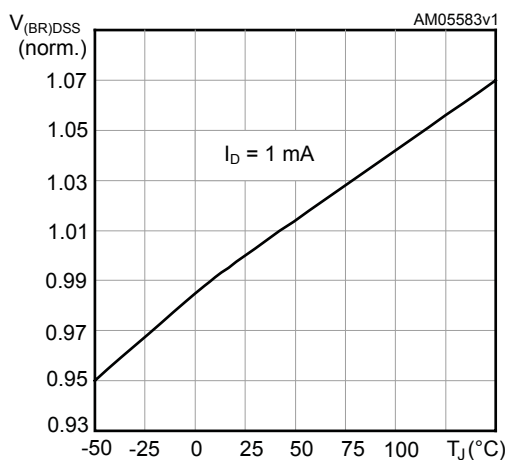


Figure 14. Typical reverse diode forward characteristics

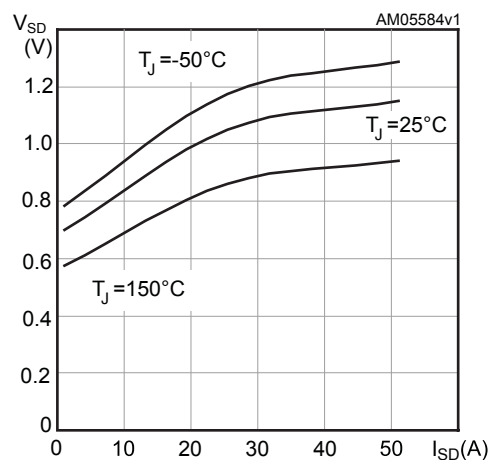
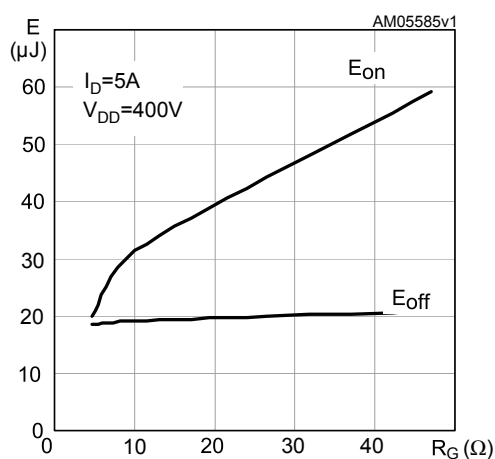
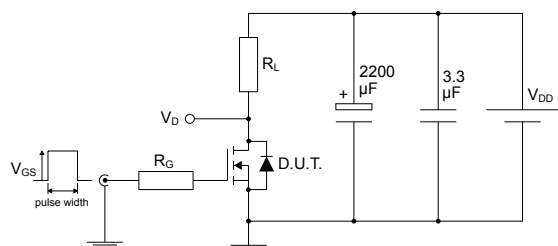


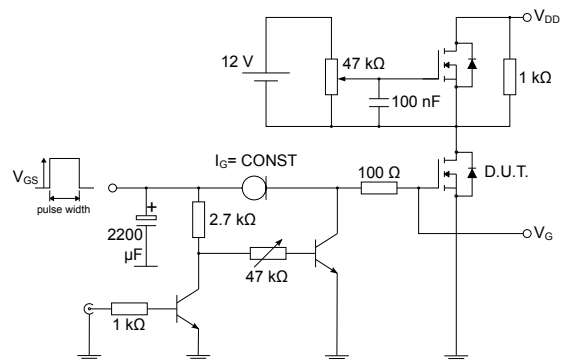
Figure 15. Typical switching energy vs gate resistance



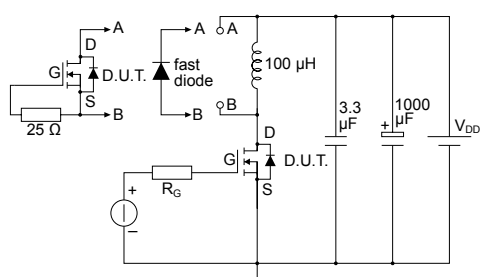
3 Test circuits

Figure 16. Test circuit for resistive load switching times


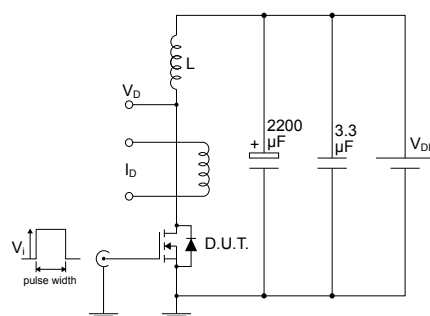
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Figure 17. Test circuit for gate charge behavior


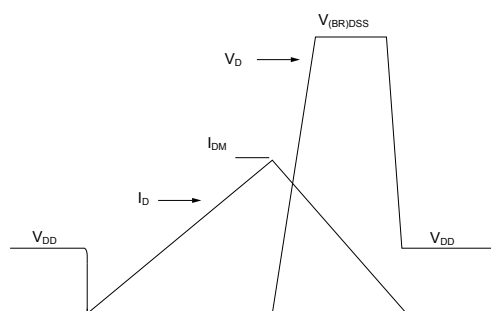
AM01469v1

Figure 18. Test circuit for inductive load switching and diode recovery times


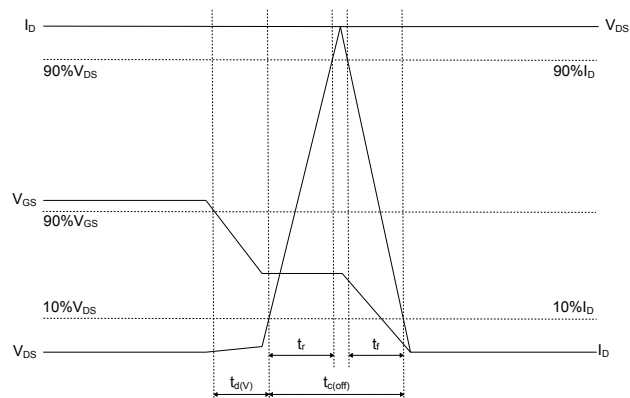
AM01470v1

Figure 19. Unclamped inductive load test circuit


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Figure 20. Unclamped inductive waveform


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Figure 21. Switching time waveform


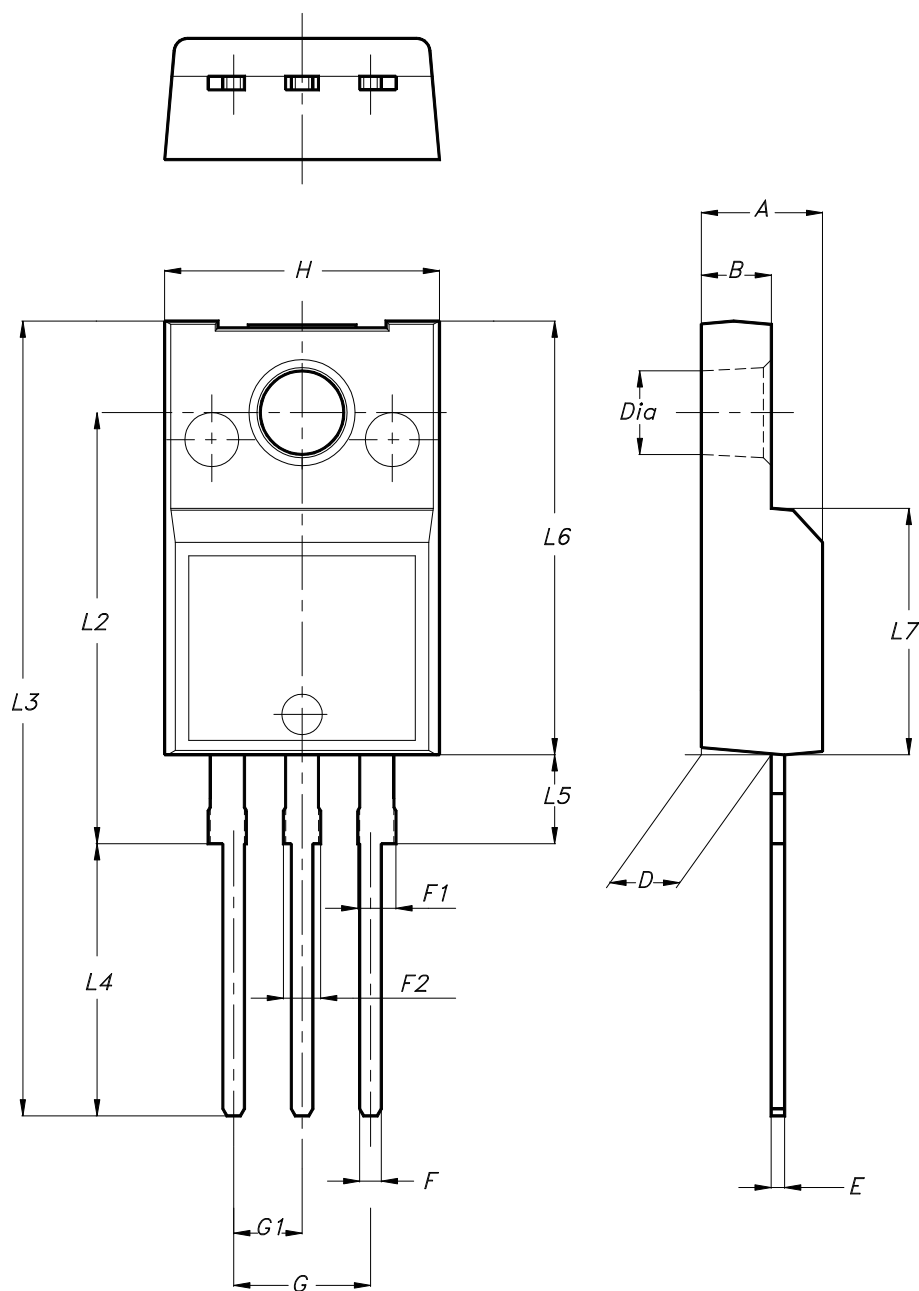
AM05540v2

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP package information

Figure 22. TO-220FP package outline



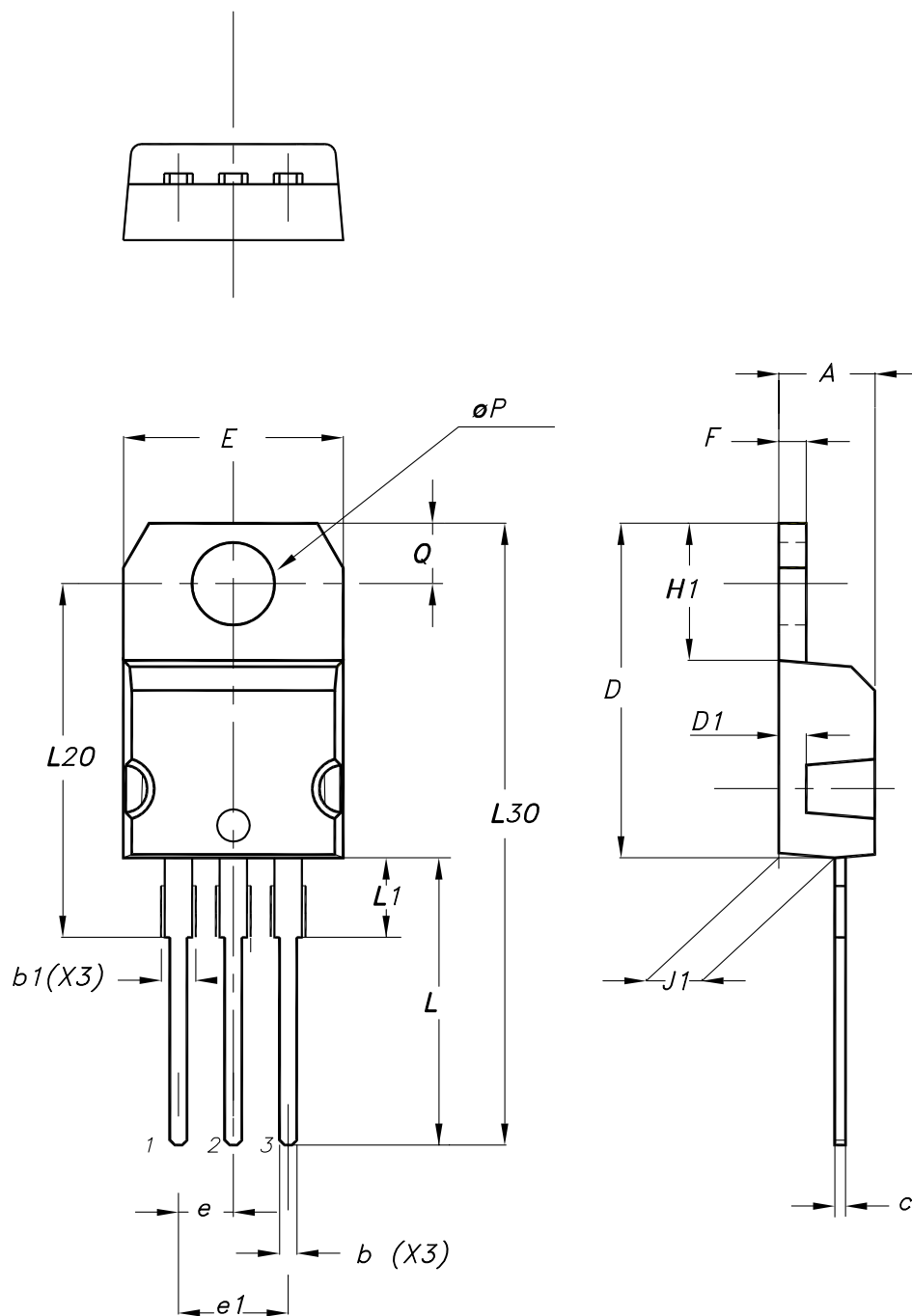
7012510_Rev_13_B

Table 7. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.2 TO-220 type A package information

Figure 23. TO-220 type A package outline



0015988_typeA_Rev_23

Table 8. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

Revision history

Table 9. Document revision history

Date	Version	Changes
24-Feb-2009	1	First release.
27-Feb-2009	2	Corrected package information on first page.
21-Jan-2010	3	Document status promoted from preliminary data to datasheet.
29-Jun-2010	4	– <i>Figure 15: Normalized on resistance vs temperature</i> has been updated. – V_{GS} value in <i>Table 4</i> has been corrected.
22-Jun-2011	5	Updated <i>Figure 18</i> and <i>Figure 20</i> . Updated gate charge in <i>Table 5</i> and switching time in <i>Table 6</i> .
11-Mar-2022	6	The part numbers STD12N65M5, STI12N65M5 and STU12N65M5 have been removed and the document has been updated accordingly. Updated title, Features and Description on cover page. Modified R_g value in the Table 4. Dynamic . Updated Section 4 Package information . Minor text changes.

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