NJD35N04G, NJVNJD35N04G, NJVNJD35N04T4G

NPN Darlington Power Transistor

This high voltage power Darlington has been specifically designed for inductive applications such as Electronic Ignition, Switching Regulators and Motor Control.

Features

- Exceptional Safe Operating Area
- High V_{CE}; High Current Gain
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These are Pb−Free Devices*

Benefits

- Reliable Performance at Higher Powers
- Designed for Inductive Loads
- Very Low Current Requirements

Applications

- Internal Combustion Engine Ignition Control
- Switching Regulators
- Motor Controls
- Light Ballast
- Photo Flash

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	V_{CEO}	350	Vdc
Collector−Base Breakdown Voltage	V_{CBO}	700	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	700	Vdc
Emitter−Base Voltage	V_{EBO}	5.0	Vdc
Collector Current Continuous Peak	 I_C I_{CM}	 4.0 8.0	Adc
Base Current	I_B	0.5	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	 45 0.36	 W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

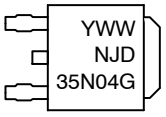
ON Semiconductor®

http://onsemi.com

DARLINGTON POWER TRANSISTORS 4 AMPERES 350 VOLTS 45 WATTS

DPAK
CASE 369C
STYLE 1

MARKING DIAGRAM



Y = Year
WW = Work Week
NJD35N04 = Device Code
G = Pb−Free Device

ORDERING INFORMATION

Device	Package	Shipping†
NJD35N04G	DPAK (Pb−Free)	75 Units / Rail
NJVNJD35N04G	DPAK (Pb−Free)	75 Units / Rail
NJD35N04T4G	DPAK (Pb−Free)	2,500 / Tape & Reel
NJVNJD35N04T4G	DPAK (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Junction−to−Case Junction−to−Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 2.78 71.4	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 10 mA, L = 10 mH)	$V_{CEO(sus)}$	 350	 –	 –	V
Collector Cutoff Current (V_{CE} = 500 V) (I_B = 0) (V_{CE} = 500 V, T_C = 125°C)	I_{CES}	– –	– –	50 250	μA
Collector Cutoff Current (V_{CE} = 250 V) (I_B = 0) (V_{CE} = 200 V, T_C = 125°C)	I_{CEO}	– –	– –	50 250	μA
Emitter Cutoff Current (V_{BE} = 5.0 Vdc)	I_{EBO}	–	–	5.0	μA
ON CHARACTERISTICS					
Collector−Emitter Saturation Voltage (I_C = 2.0 A, I_B = 20 mA) (I_C = 2.0 A, I_B = 20 mA 125°C)	$V_{CE(sat)}$	 – –	 – –	 1.5 1.5	V
Base−Emitter Saturation Voltage (I_C = 2.0 A, I_B = 20 mA) (I_C = 2.0 A, I_B = 20 mA 125°C)	$V_{BE(sat)}$	 – –	 – –	 2.0 2.0	V
Base−Emitter On Voltage (I_C = 2.0 A, V_{CE} = 2.0 V) (I_C = 2.0 A, V_{CE} = 2.0 V, 25°C)	$V_{BE(on)}$	 – –	 – –	 2.0 2.0	V
DC Current Gain (I_C = 2.0 A, V_{CE} = 2.0 V) (I_C = 4.0 A, V_{CE} = 2.0 Vdc)	h_{FE}	 2000 300	 – –	 – –	–
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (I_C = 2.0 A, V_{CE} = 10 V, f = 1.0 MHz)	f_T	 90	 –	 –	MHz
Output Capacitance (V_{CB} = 10 V, I_E = 0, f = 0.1 MHz)	C_{ob}	 –	 60	 –	pF
SWITCHING CHARACTERISTICS					
V_{CC} = 12 V, V_{clamp} = 250 V, L = 4 mH I_C = 2 A, I_{B1} = 20 mA, I_{B2} = −20 mA	t_s t_f	– –	18 0.8	– –	μSec

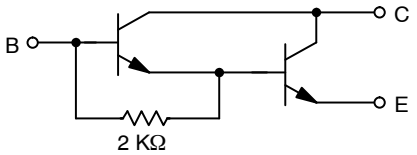


Figure 1. Darlington Circuit Schematic

TYPICAL CHARACTERISTICS

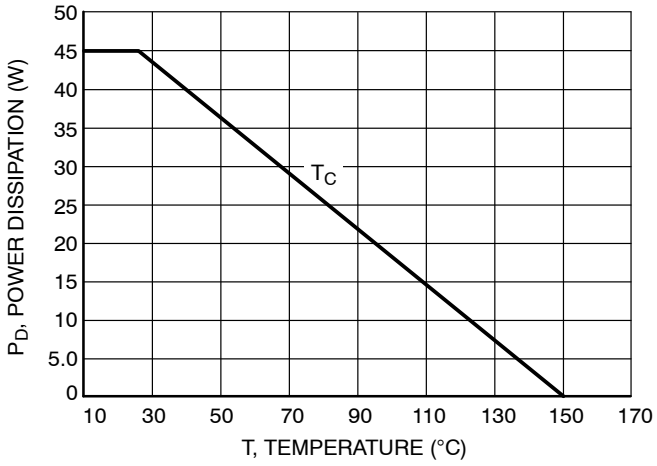


Figure 2. Power Derating

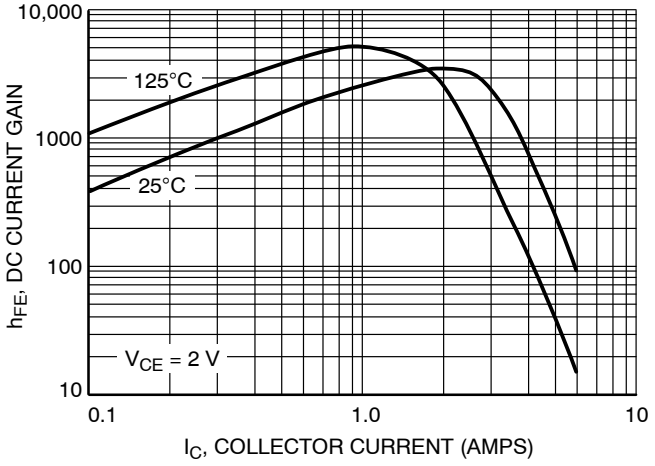


Figure 3. DC Current Gain

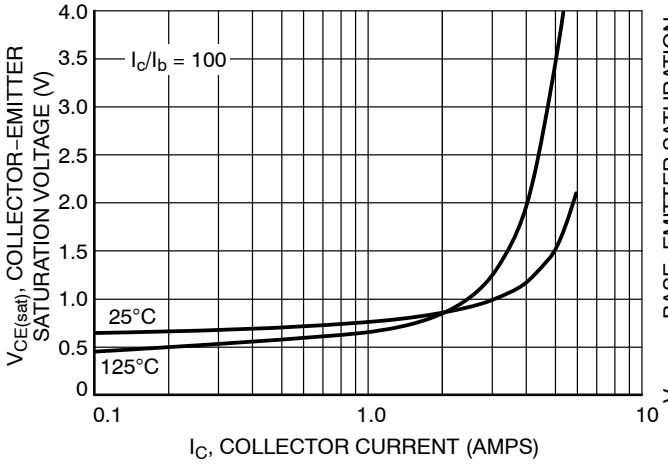


Figure 4. Collector−Emitter Saturation Voltage

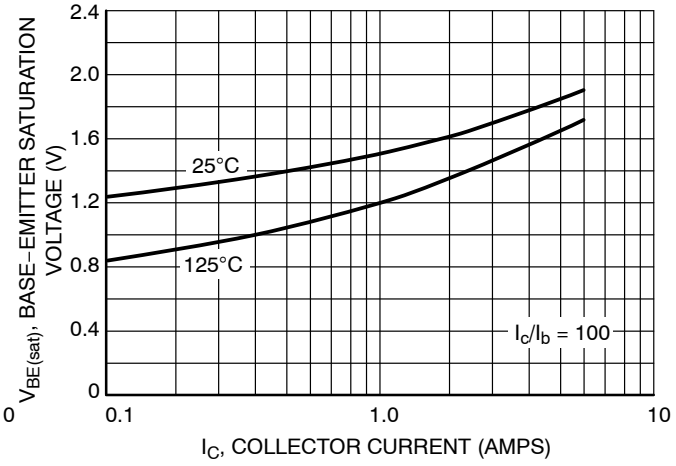


Figure 5. Base−Emitter Saturation Voltage

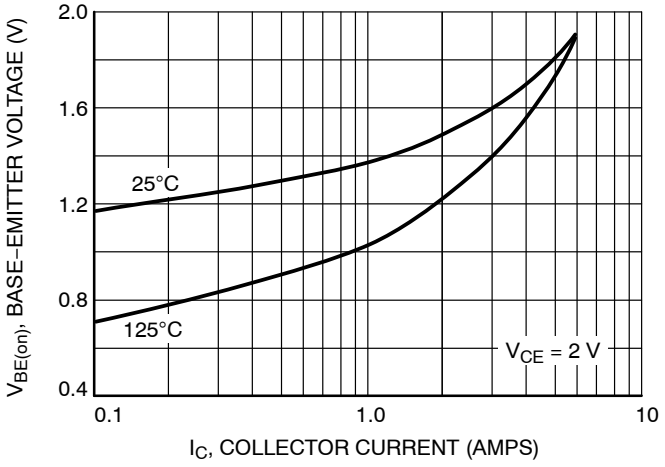


Figure 6. Base−Emitter Voltage

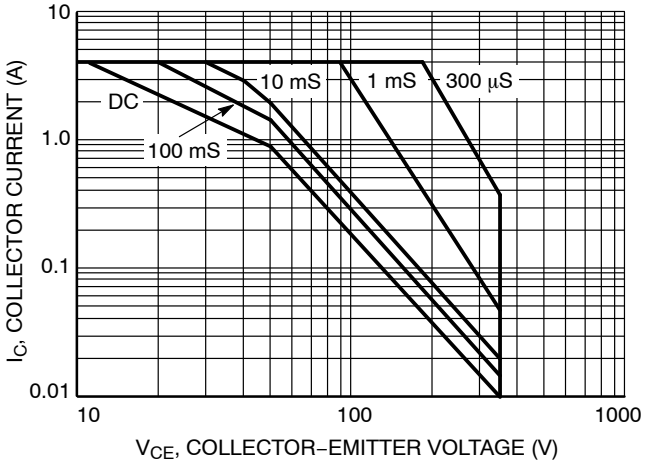
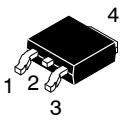


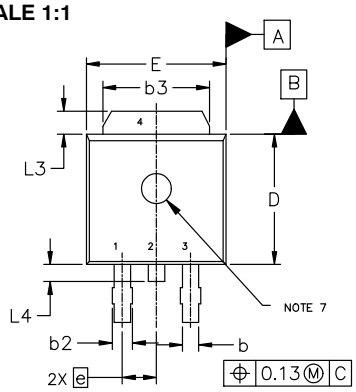
Figure 7. Forward Bias Safe Operating Area (FBSOA)



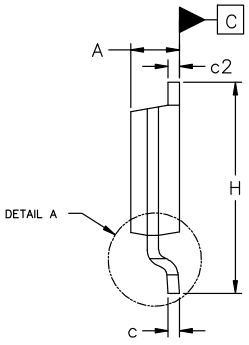
SCALE 1:1

DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

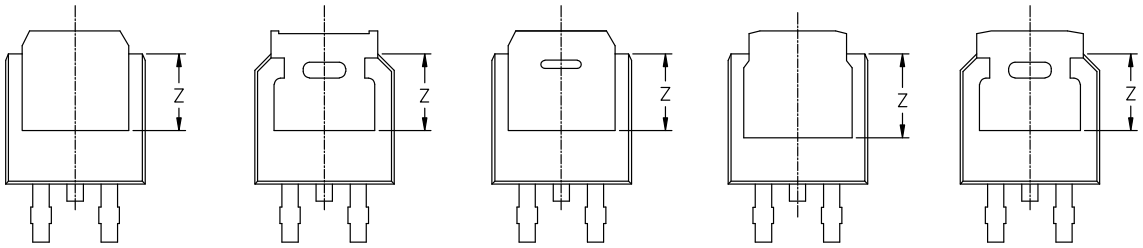


TOP VIEW



SIDE VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---

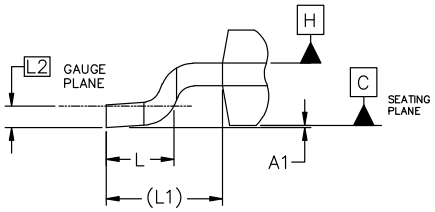


BOTTOM VIEW

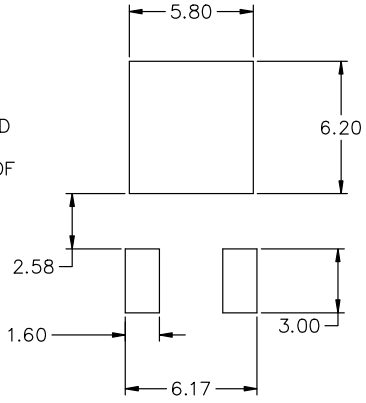
ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



DETAIL A
ROTATED 90° CW



RECOMMENDED MOUNTING FOOTPRINT*

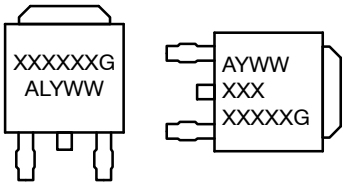
*FOR ADDITIONAL INFORMATION ON OUR PB–FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON10527D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DPAK3 6.10x6.54x2.28, 2.29P**	**PAGE 1 OF 2**

DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

GENERIC MARKING DIAGRAM*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

ADDITIONAL INFORMATION

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