AMMP-6522

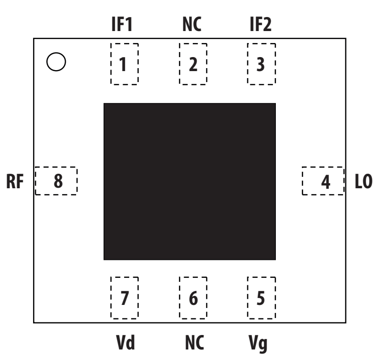
7 to 20 GHz GaAs MMIC LNA/IRM Receiver in SMT Package

Data Sheet

Description

Avago's AMMP-6522 is an easy-to-use broadband integrated receiver in a surface mount package. The MMIC includes a 3-stage LNA to provide gain amplification and a gate-pumped image-reject mixer for frequency translation. The overall receiver performs Single Side Band down-conversion in the 7 to 20 GHz RF signal range. The LO and RF are matched to 50 Ω. The IF output is provided in 2-port format where an external 90-degree hybrid can be utilized for full image rejection. The LNA requires a 4 V, 75 mA power supply, where the mixer bias is a simple -1 V, 0.1 mA. The MMIC is fabricated using PHEMT technology. The surface mount package allows elimination of "chip & wire" assembly for lower cost. This MMIC is a cost effective alternative to multi-chip solution that have higher loss and complex assembly.

Package Diagram



Features

- 5x5 mm Surface Mount Package
- Integrated Low Noise Amplifier
- Integrated Image Reject Mixer
- 50 Ω Input and Output Match
- Single Supply Bias Pin

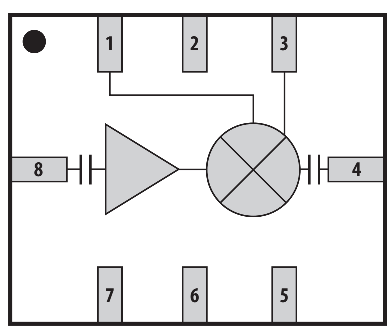
Specifications Vd = 4.0 V (75 mA), Vg = -1.0 V (0.1 mA)

- RF frequency: 7 to 20 GHz
- IF frequency: DC to 3.5 GHz
- Conversion Gain (RF/IF): 13 dB
- Input Intercept Point: -4 dBm
- Image Suppression: 15 dB
- Total Noise Figure: 2.4 dB

Application

- Microwave radio systems
- Satellite VSAT, DBS Up/Down Link
- LMDS & Pt-Pt mmW Long Haul
- Broadband Wireless Access (including 802.16 and 802.20 WiMax)
- WLL and MMDS loops

Functional Block Diagram



PIN	FUNCTION
1	IF1
2	NC
3	IF2
4	LO
5	Vg
6	NC
7	Vd
8	RF

TOP VIEW
PACKAGE BASE: GND

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A) :40V
ESD Human Body Model (Class 1A) :150V
Refer to Avago Technologies Application Note A004R: Electrostatic Discharge, Damage and Control.

Note: MSL Rating = Level 2A

Electrical Specifications

1. Small/Large -signal data measured in a fully de-embedded test fixture form TA = 25°C.
2. Pre-assembly into package performance verified 100% on-wafer per AMMC-6522 published specifications.
3. This final package part performance is verified by a functional test correlated to actual performance at one or more frequencies.
4. Specifications are derived from measurements in a 50 Ω test environment. Aspects of the amplifier performance may be improved over a more narrow bandwidth by application of additional conjugate, linearity, or low noise (Γopt) matching.
5. NF is measure on-wafer. Additional bond wires (-0.2nH) at Input could improve NF at some frequencies.

Table 1. RF Electrical Characteristics

TA=25°C, Vd=4.0V, Vg=-1V, Zo=50 Ω, LO=+15dBm, IF=2GHz [1]

	RF=8GHz, LO=10GHz			RF=18GHz, LO=20GHz				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Comment**
Noise Figure into 50 Ω, NF		2.6	3.3		3	3.3	dB	
Conversion Gain, CG	12	13		12	14		dB	
Input Third Order Intercept, IIP3	-8	-6		-5	-0.4		dBm	
Image Rejection, Sup	15	29		15	30		dB	

Note:
1. All tested parameters are guaranteed with the following measurement accuracy:
   RF=8GHz: ±0.6dB for Conversion Gain, ±10dB for IRR, ±0.5dB for NF, ±0.8dBm for IIP3
   RF=18GHz: ±1.8dB for Conversion Gain, ±1.6dB for IRR, ±0.6dB for NF, ±1.7dBm for IIP3

Table 2. Recommended Operating Range

1. Ambient operational temperature TA = 25°C unless otherwise noted.
2. Channel-to-backside Thermal Resistance (Tchannel (Tch) = 34°C) as measured using infrared microscopy. Thermal Resistance at backside temperature (Tb) = 25°C calculated from measured data.

Description	Min.	Typical	Max.	Unit	Comments
Drain Supply Current, Id		75	95	mA	Vd = 4.0 V
Drain Supply Voltage, Vd	3	4	5	V	
Gate Supply Voltage, Vg	-1.2	-1.0	-0.8	V	Ig = 0.1mA
RF Frequency, RFfreq	7		20	GHz	
LO Frequency, LOfreq	5		22	GHz	
IF Frequency, IFfreq [1]	DC		3.5	GHz	
LO Drive Power, LO	+10	+15	+22	dBm	

Note:
1. Use IF = DC with caution. Please see "Biasing and Operation" for more details.

Table 3. Thermal Properties

Parameter	Test Conditions	Value
Thermal Resistance, θjc	Ambient operational temperature TA = 25°C Channel-to-backside Thermal Resistance Tchannel(Tch)=34°C Thermal Resistance at backside temperature Tb=25°C	θjc = 27 °C/W

Absolute Minimum and Maximum Ratings

Table 4. Minimum and Maximum Ratings

Description Pin	Min.	Max.	Unit	Comments
Drain to Ground Supply Voltage, Vd		5.5	V	
Gate to Ground Voltage, Vg		+0.8	V	
Drain Current , Id		100	mA	
Gate Current, Ig		1	mA	
RF CW Input Power, Pin		10	dBm	CW
Channel Temperature, Tch		+150	°C	
Storage Temperature, Tstg	-65	+150	°C	
Maximum Assembly Temperature, Tmax		260	°C	20 second maximum

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to this device.

AMMP-6522 Typical Performance[1,2]

(T_A = 25°C, Vd = 4 V, Id = 75 mA, V_g = -1 V, I_g = 0 mA, Z_{in} = Z_{out} = 50 Ω), IF Freq = 2 GHz, LO Power = +15 dBm unless noted)

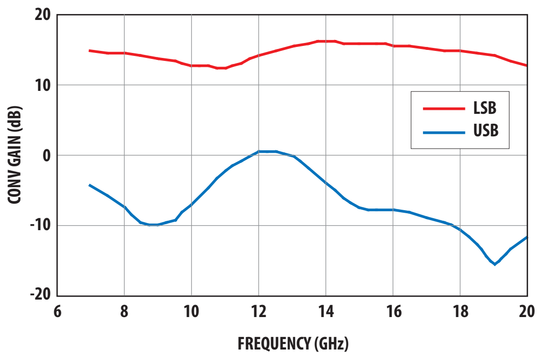


Figure 1. Receiver conversion gain

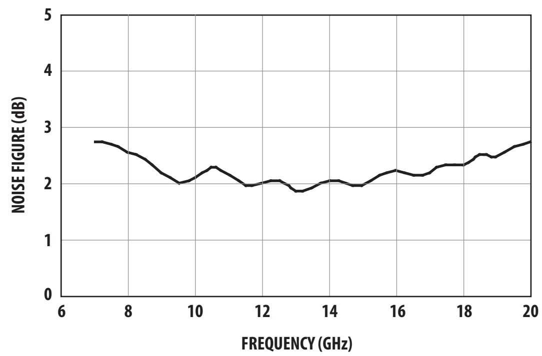


Figure 2. Typical noise figure

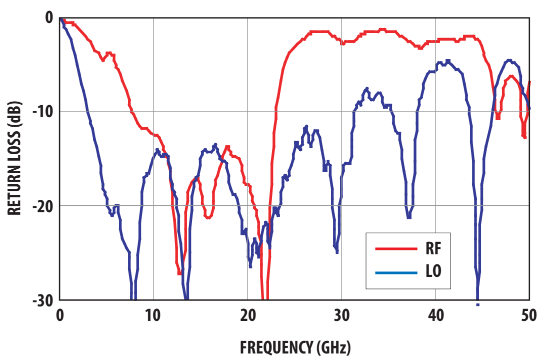


Figure 3. Return loss at RF & LO ports

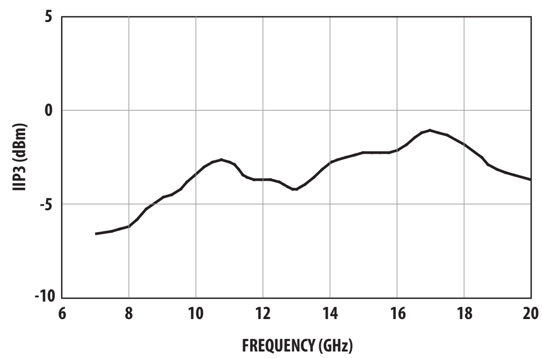


Figure 4. Typical input IP3

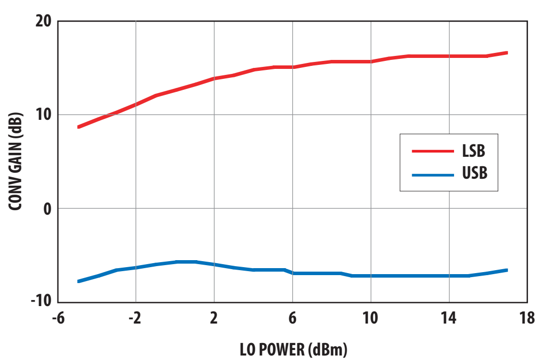


Figure 5. Conv gain vs. LO power (RF = 15 GHz)

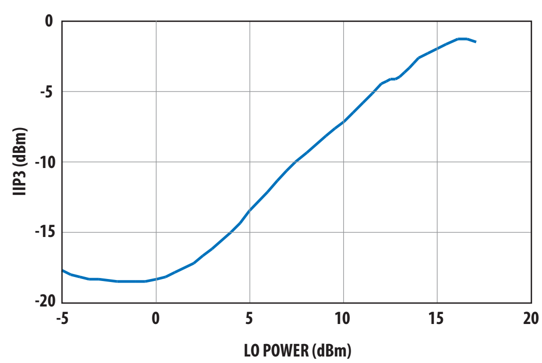


Figure 6. Input IP3 vs. LO power (RF = 15 GHz)

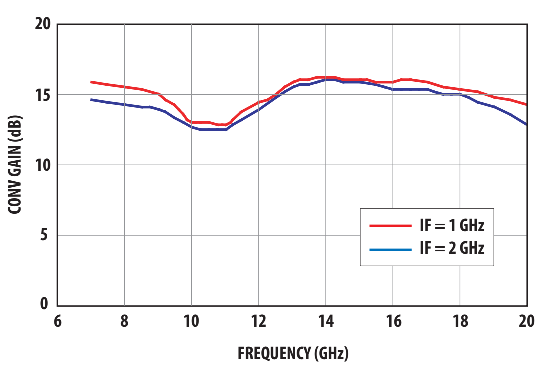


Figure 7. LSB conversion gain at two IF frequencies

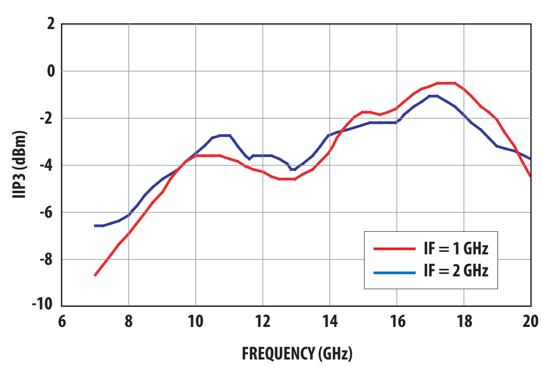


Figure 8. Input IP3 at two IF frequencies

AMMP-6522 Typical Performance (cont.)[1,2]

(T_A = 25°C, Vd = 4 V, Id = 75 mA, V_g = -1 V, I_g = 0 mA, Z_{in} = Z_{out} = 50 Ω), IF Freq = 2 GHz, LO Power = +15 dBm unless noted)

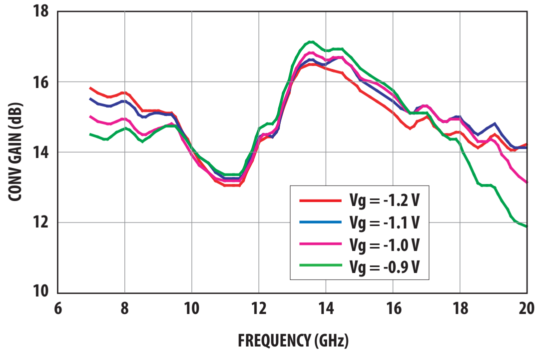


Figure 9. Conversion gain over Vg

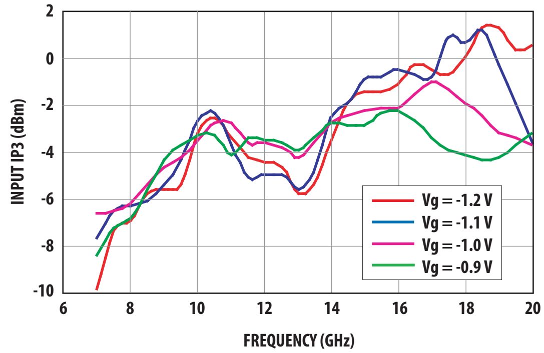


Figure 10. Input IP3 over Vga

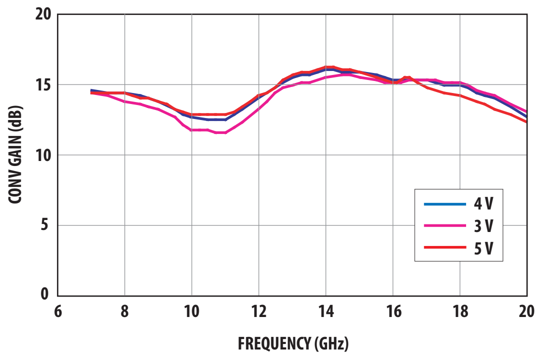


Figure 11. Receiver conversion gain over Vd

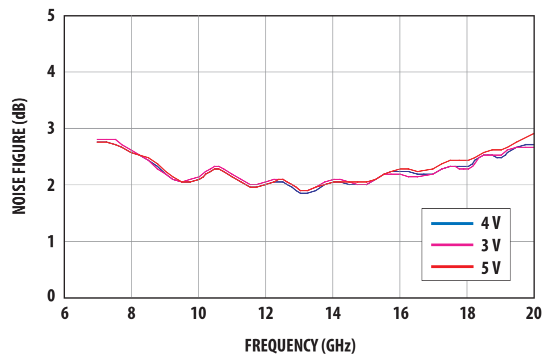


Figure 12. Noise figure over Vd

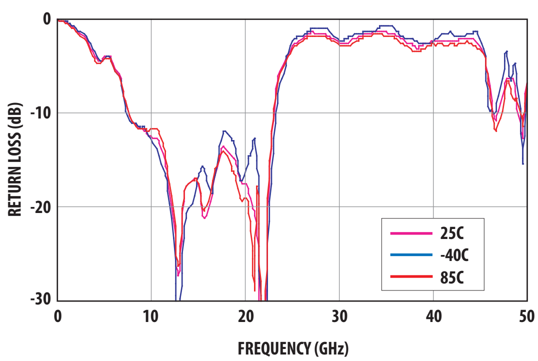


Figure 13. Return loss at RF over temperature

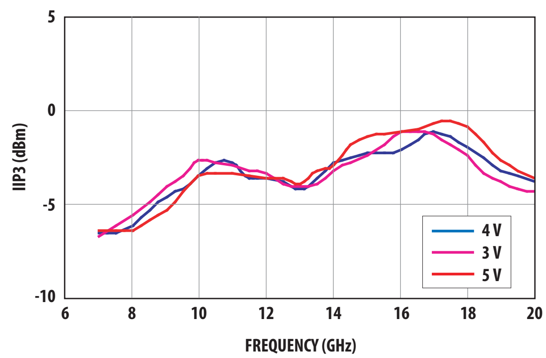


Figure 14. Input IP3 over Vd

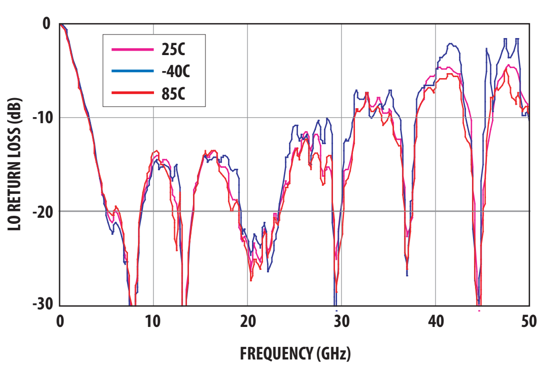


Figure 15. Return loss at LO over temperature

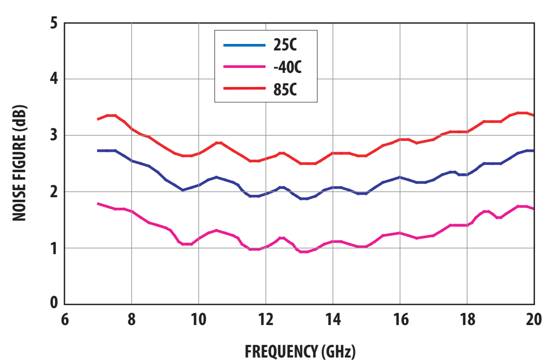


Figure 16. Noise figure over temperature

Notes:

1. S-parameters are measured with R&D Eval Board as shown in Figure 19. Board and connector effects are included in the data.
2. Noise Figure is measured with R&D Eval Board as shown in Figure 19, and with a 3-dB pad at input. Board and connector losses are already de-embeded from the data.

Biasing and Operation

The AMMP-6522 is normally biased with a positive drain supply connected to the Vd pin and a negative gate voltage connected to the Vg pin through bypass capacitors as shown in Figure 17. The recommended drain supply voltage is 4 V and gate bias voltage is -1 V. The corresponding currents are 75 mA and 0.1 mA respectively. The typical required LO level is +15 dBm and it should come from a low noise driver to ensure that overall Front End NF is low.

The image rejection performance is dependent on the selection of the IF quadrature hybrid. The performance of the IF hybrid as well as the phase balance and VSWR of the interface to the AMMP-6522 will affect the overall front end performance.

There is minimal performance degradation if Vdd is lowered to 3 V or raised to 5 V. If lower current is required, then Vd = 3 V will provide considerably similar RF performance.

The recommended Vg is -1 V. However, depending on the operating frequency, Vg can be changed to achieve better performance for that particular frequency. Please refer to Figures 9 and 10 for how to best select the appropriate Vg for the intended frequency of operation.

Theoretically IF frequencies can be as low as DC. However, when direct conversion is used (IF = DC), a so-called phenomenon DC-offset could occur at the two IF outputs. In most practical applications, IF should be more than a few hundreds kHz to avoid DC-offset correction.

Refer the Absolute Maximum Ratings table for allowed DC and thermal condition.

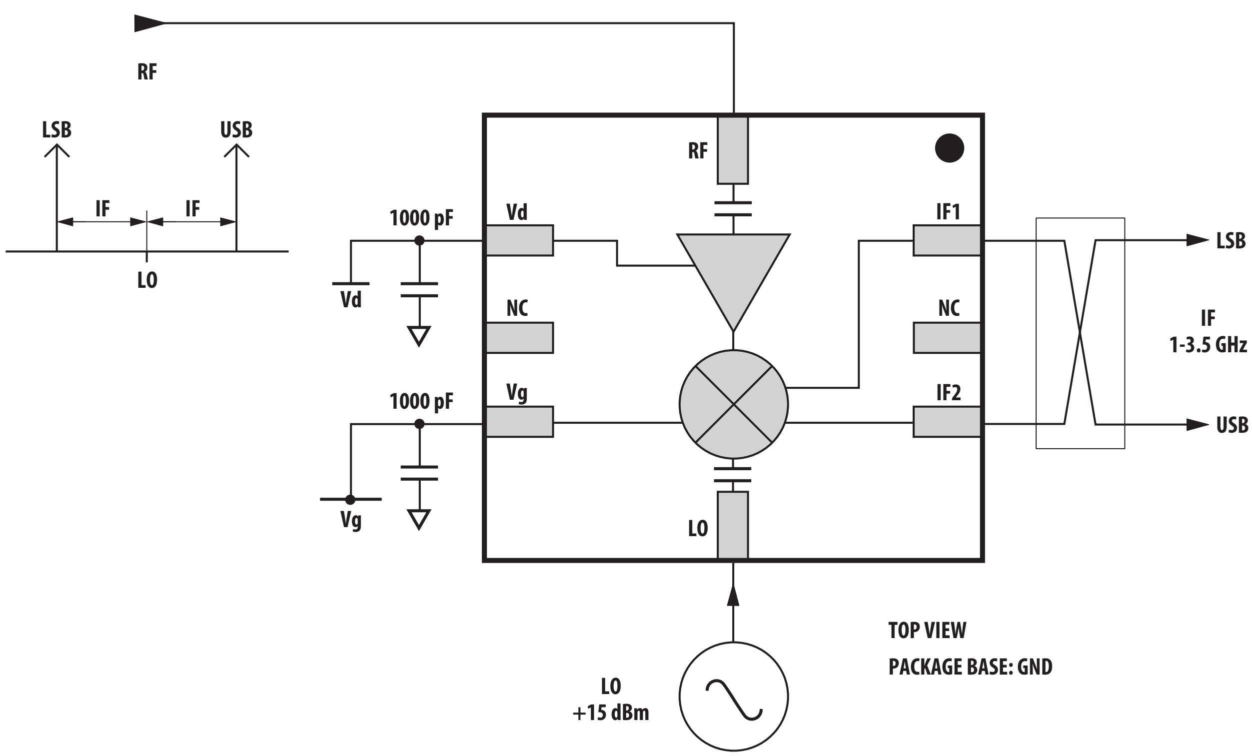


Figure 17. Application of receiver with IF Balun

AMMP-6522 Part Number Ordering Information

Part Number	Devices per Container	Container
AMMP-6522-BLKG	10	Antistatic bag
AMMP-6522-TR1G	100	7" Reel
AMMP-6522-TR2G	500	7" Reel

Package Dimension, PCB Layout and Tape and Reel information

Please refer to Avago Technologies Application Note 5520, AMxP-xxxx production Assembly Process (Land Pattern A).

AV02-0244EN - July 8, 2013