

Transil™, transient voltage suppressor in 0.3 mm pitch

Datasheet — production data

Features

- Strong ESD and EOS protection
- Very low clamping factor V_{CL}/V_{BR}
- Unidirectional device
- Fast response time
- Very thin package
- Very small PCB area
- RoHS compliant

Complies with the following standards:

- IEC 61000-4-2 level 4
 - ±15 kV (air discharge)
 - ±8 kV (contact discharge)

Description

The ESDA18-1F4 is a single line diode designed specifically for the protection of integrated circuits in portable equipment and miniaturized electronics devices subject to ESD and EOS transient overvoltages.

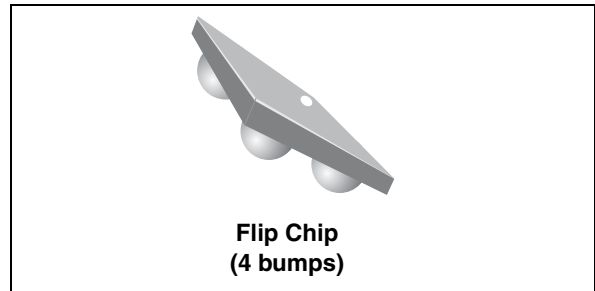


Figure 1. Pin configuration (bump side)

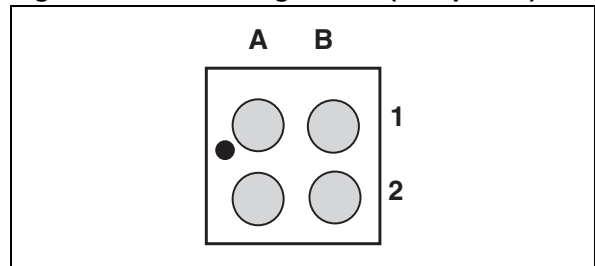
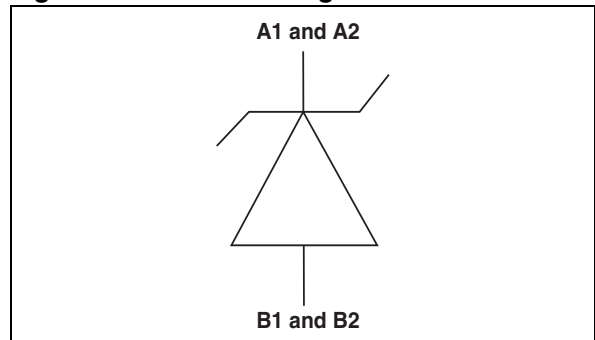


Figure 2. Device configuration



Note: B1 and B2 bumps must be grounded on the PCB together

TM: Transil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25\text{ °C}$)

Symbol	Parameter	Test condition	Value	Unit
P_{PP}	Peak pulse power dissipation (8/20 μ s pulse)	T_j initial = T_{amb}	350	W
T_j	Maximum operating junction temperature		125	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		-55 to +150	$^{\circ}\text{C}$

Figure 3. Electrical characteristics - definitions

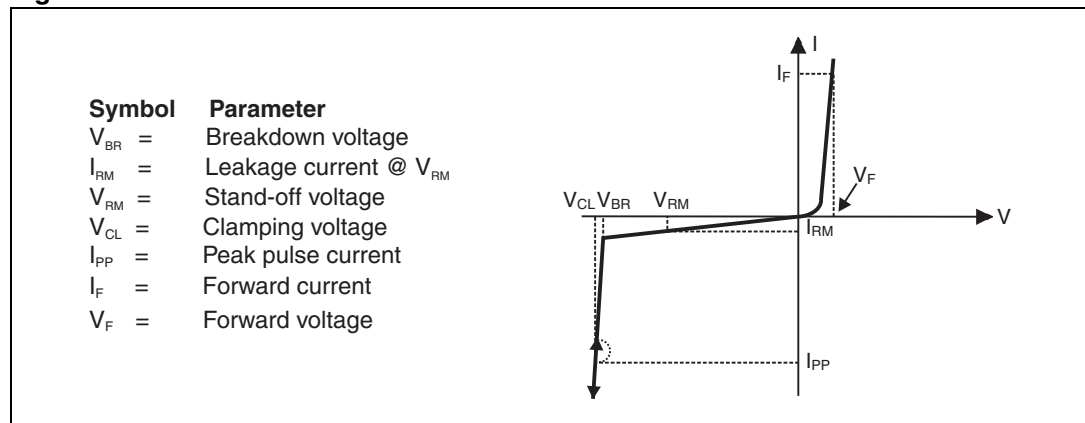


Table 2. Electrical characteristics - values ($T_{amb} = 25\text{ °C}$)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1\text{ mA}$	15		18	V
I_{RM}	$V_{RM} = 12\text{ V}$			250	nA
V_{CL}	$I_{PP} = 1\text{ A}^{(1)}$			20	V
V_F	$I_F = 850\text{ mA}$			1.7	V
C_{line}	$V_R = 0\text{ V}$, $V_{OSC} = 30\text{ mV}$, $F = 1\text{ MHz}$		120		pF

1. 8 / 20 μ s pulse waveform

Figure 4. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

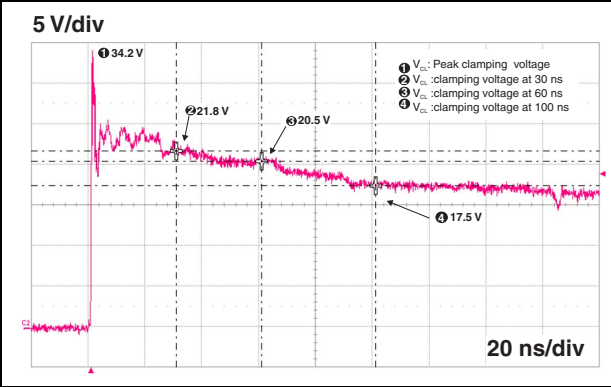


Figure 5. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

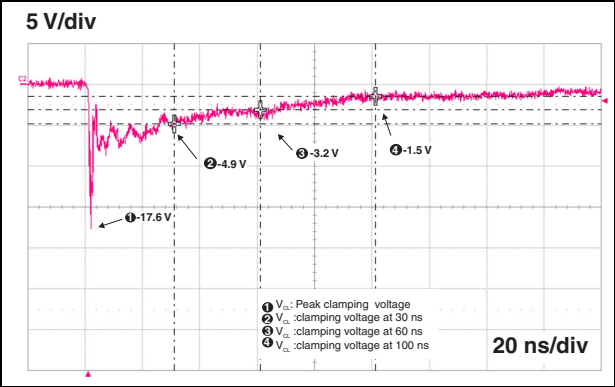


Figure 6. Junction capacitance versus reverse applied voltage (typical values)

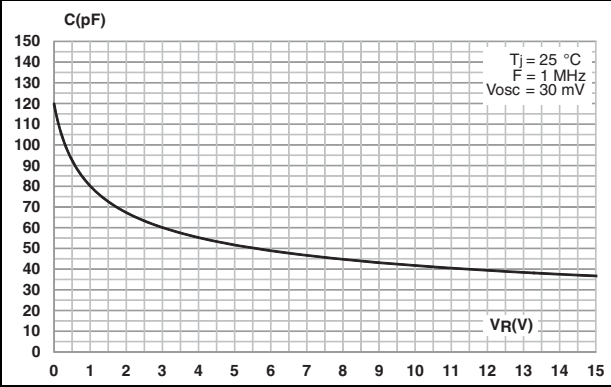


Figure 7. Insertion losses versus frequency (typical values)

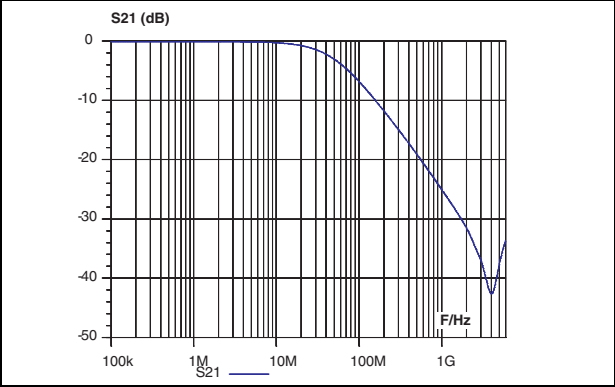


Figure 8. Peak pulse power versus exponential pulse duration (maximum values)

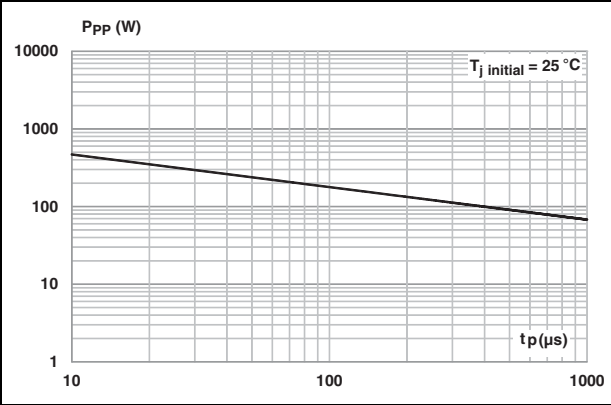


Figure 9. Variation of peak pulse power versus initial junction temperature (maximum values)

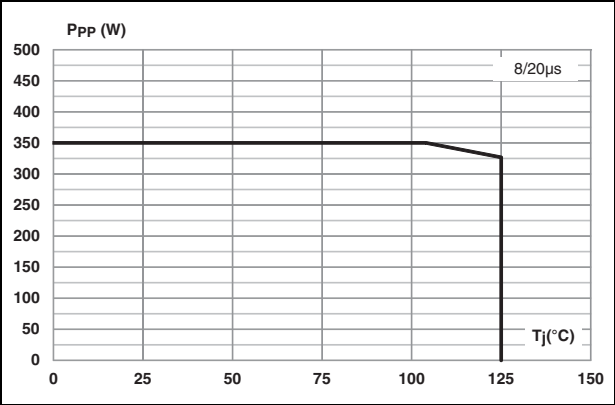


Figure 10. Clamping voltage versus peak-pulse current (typical values)

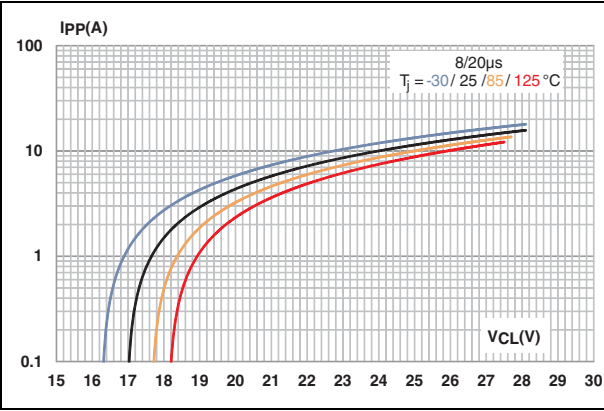
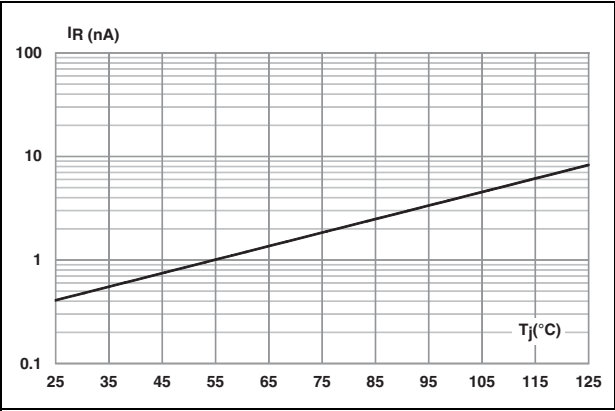
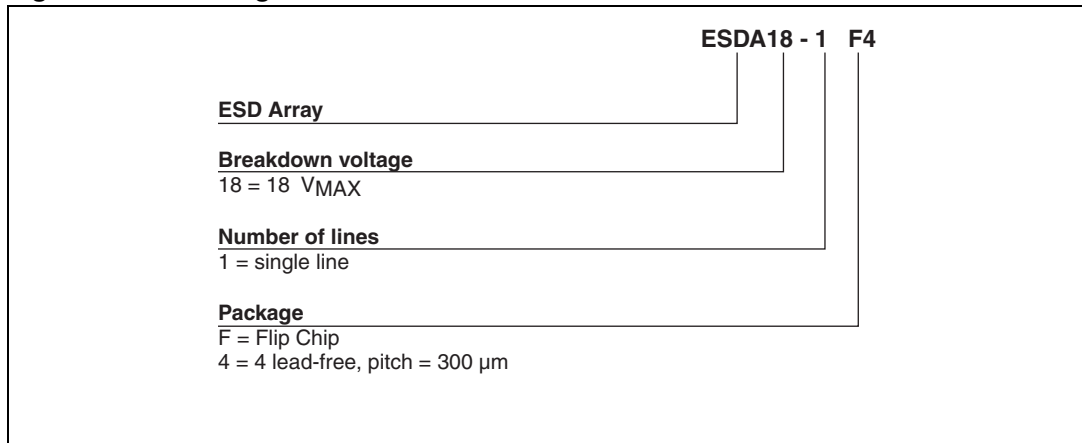


Figure 11. Variation of leakage current versus junction temperature (typical values)



2 Ordering information scheme

Figure 12. Ordering information scheme



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 13. Package dimensions

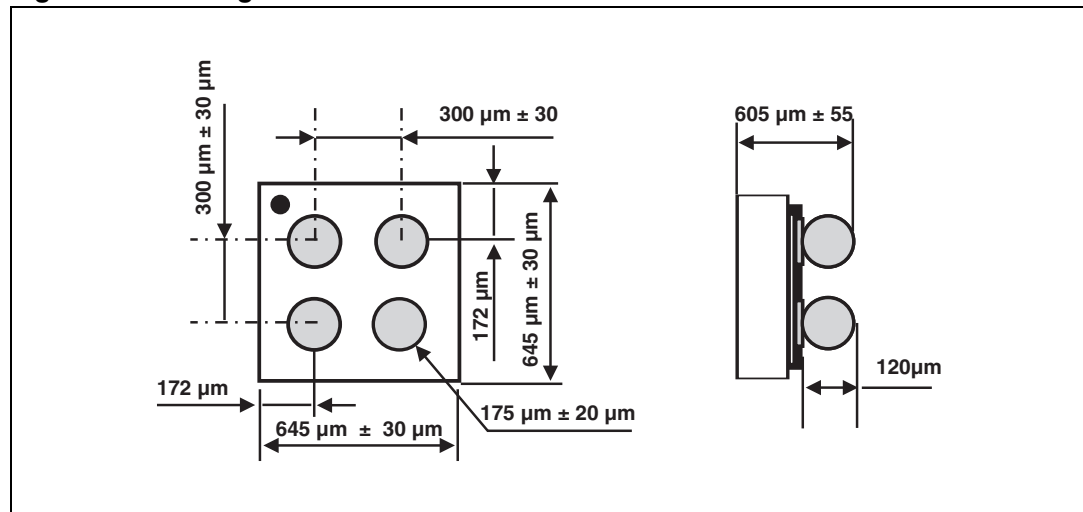
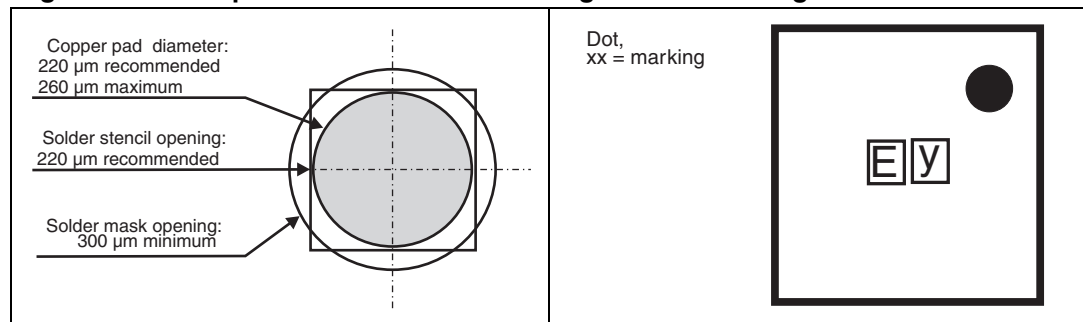
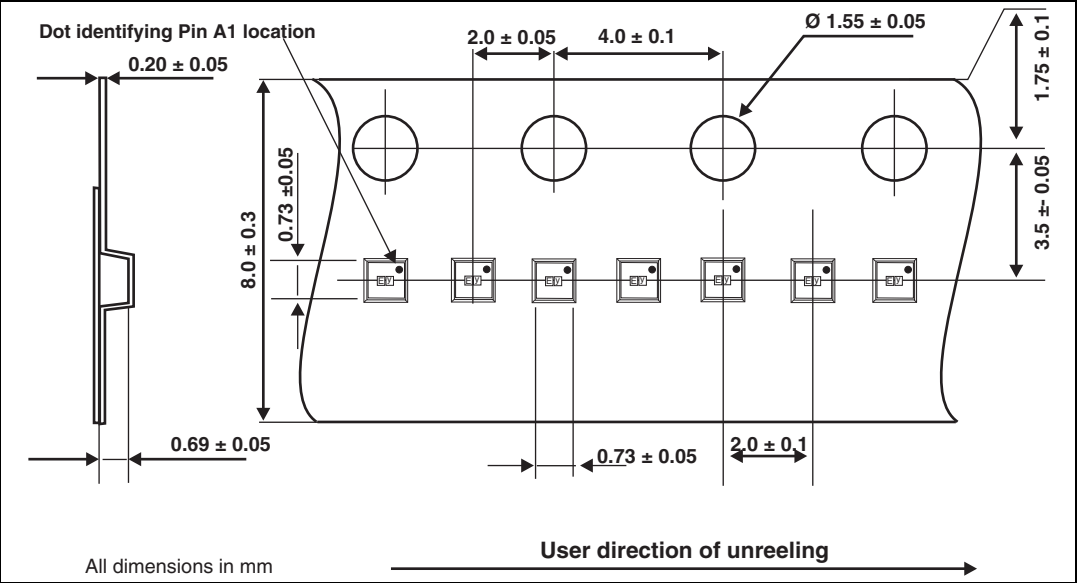


Figure 14. Foot print recommendations **Figure 15. Marking**



Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 16. Tape and reel specifications



4 Ordering information

Table 3. Ordering information

Order code	Marking ⁽¹⁾	Package	Weight	Base qty	Delivery mode
ESDA18-1F4	EY	Flip Chip	0.527 mg	10 000	Tape and reel (7")

1. The marking can be rotated by 90° to differentiate assembly location

5 Revision history

Table 4. Document revision history

Date	Revision	Changes
24-Oct-2012	1	Initial release.

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