S71GL-N Based MCPs

Stacked Multi-Chip Product (MCP)
Flash Memory and RAM
64/32 Megabit (4/2M x 16-bit) CMOS 3.0 Volt-Only Page Mode Flash Memory and 32/16 Megabit (2M/1M x 16-bit) Pseudo Static RAM

Data Sheet *(Advance Information)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S71GL-N_00 **Revision** 07 **Issue Date** May 8, 2012

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Data Sheet *(Advance Information)*

Distinctive Characteristics

MCP Features

- **Power supply voltage of 2.7 to 3.1 volt**
- **High performance**
  - 90 ns access time (90 ns Flash, 70 ns pSRAM/SRAM)
  - 25 ns page read times
- **Packages**
  - 7 x 9 x 1.2 mm 56 ball FBGA
- **Operating Temperature**
  - –25°C to +85°C

General Description

The S71GL-N product series consists of S29GL-N Flash memory with pSRAM combinations defined as:

		Flash Memory Density	
		32 Mb	**64 Mb**
pSRAM Density	16 Mb	S71GL032NA0	S71GL064NA0
	32 Mb		S71GL064NB0

For detailed specifications, please refer to the individual data sheets.

Document	Publication Identification Number (PID)
S29GL-N	S29GL-N_00
SPH016D970R1R (16 Mb pSRAM Type 9/10)	SPH016D970R1R
32 Mb pSRAM Type 8	pSRAM_31
SPH032D970R1R (32 Mb pSRAM Type 9)	SPH032D970R1R

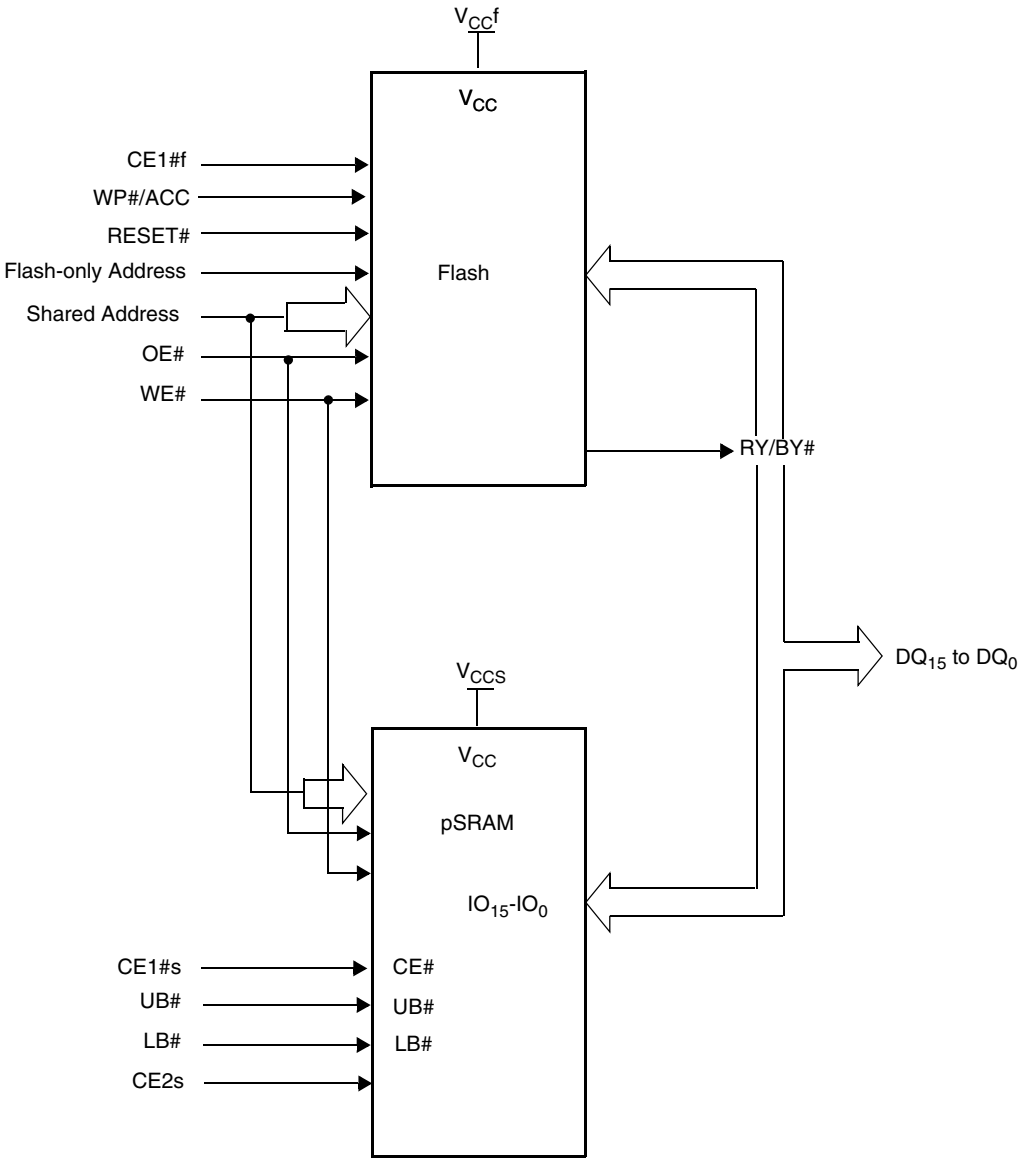
Publication Number S71GL-N_00 **Revision** 07 **Issue Date** May 8, 2012

1. Product Selector Guide

Device-Model# (Note)	(p)SRAM density	(p)SRAM type	Package
S71GL032NA0-0B	16 Mb	pSRAM 10	TLC056
S71GL032NA0-0F		pSRAM 10	
S71GL032NA0-0K		pSRAM 9	
S71GL032NA0-0P			
S71GL064NA0-0B		pSRAM 10	TSC056
S71GL064NA0-0F		pSRAM 10	
S71GL064NB0-0K	32 Mb	pSRAM 9	
S71GL064NB0-0P			
S71GL064NB0-0U		pSRAM 8	
S71GL064NB0-0Z			

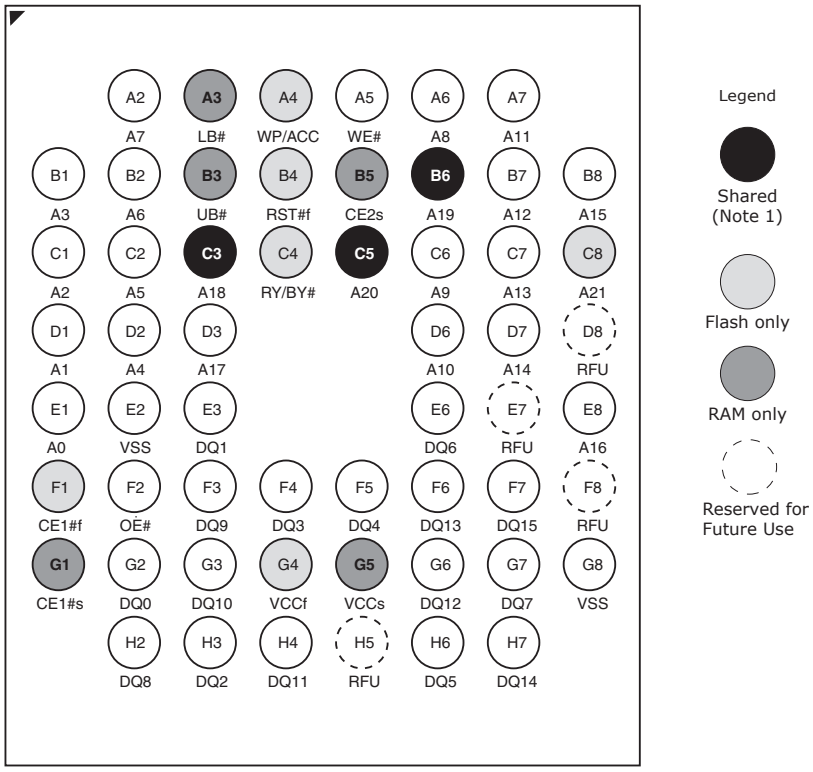
Note:
Please see the valid combinations table for the model# description.

2. MCP Block Diagram



3. Connection Diagram

56-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)



Note:
May be shared depending on density.

MCP	Flash-only Addresses	Shared Addresses
S71GL032NA0	A20	A19-A0
S71GL064NB0	A21	A20-A0
S71GL064NA0	A21-A20	A19-A0

3.1 Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

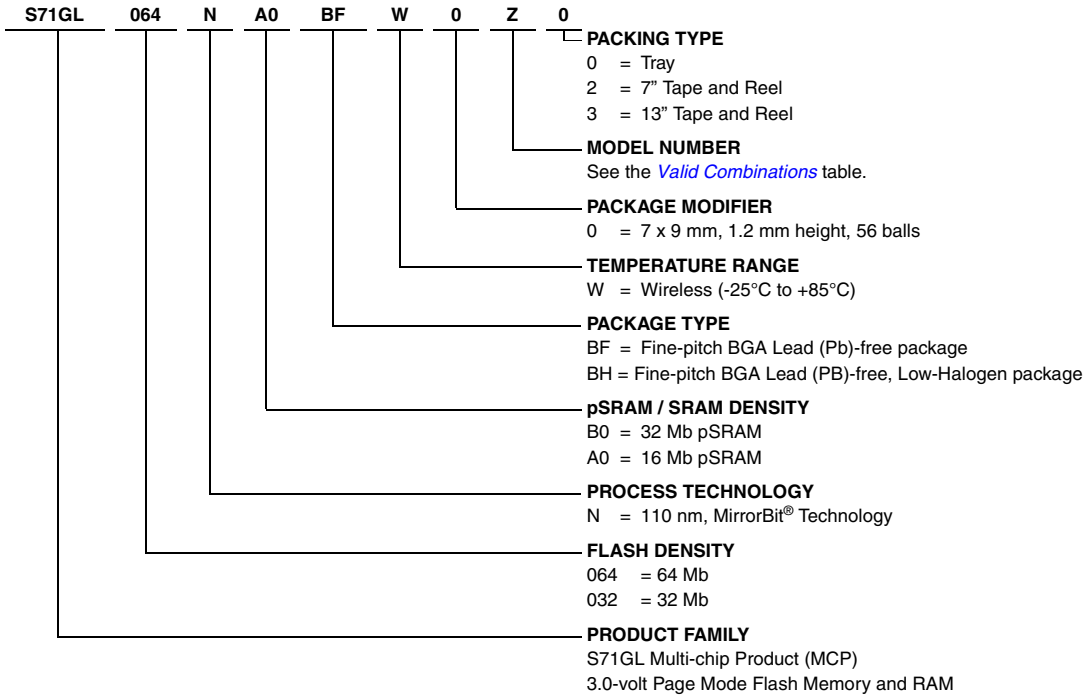
Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

4. Pin Description

Pin	Description
A21–A0	22 Address Inputs (Common and Flash only) (A20-A0 for the S71GL032N)
DQ15–DQ0	16 Data Inputs/Outputs (Common)
CE1#f	Chip Enable (Flash)
CE1#s	Chip Enable 1 (pSRAM/SRAM)
CE2s	Chip Enable 2 (pSRAM/SRAM)
OE#	Output Enable (Common)
WE#	Write Enable (Common)
RY/BY#	Ready/Busy Output (Flash 1)
UB#	Upper Byte Control (pSRAM/SRAM)
LB#	Lower Byte Control (pSRAM/SRAM)
RESET#	Hardware Reset Pin, Active Low (Flash)
WP#/ACC	Hardware Write Protect/Acceleration Pin (Flash)
$V_{CC}f$	Flash 3.0 volt-only single power supply (see *Product Selector Guide* for speed options and voltage supply tolerances)
V_{CCS}	pSRAM/SRAM Power Supply
V_{SS}	Device Ground (Common)
NC	Not Connected. No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB).

5. Ordering Information

The order number is formed by a valid combinations of the following:



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 5.1 Valid Combinations

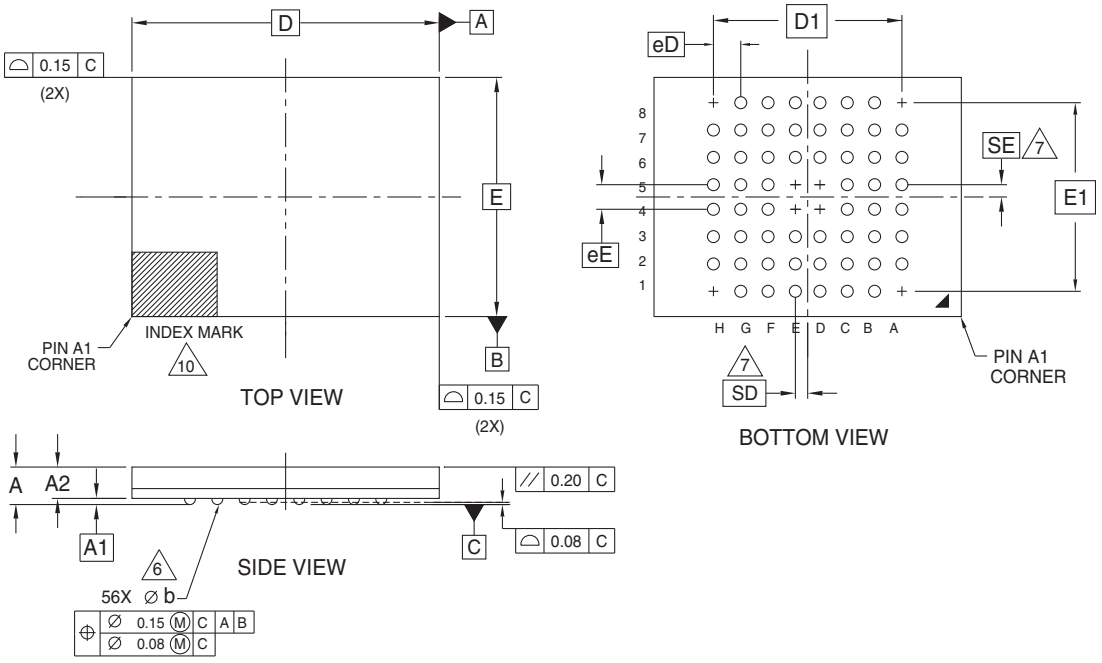
S71GL064N Valid Combinations				Speed Options (ns)/Boot Sector Option	(p)SRAM Type/ Access Time (ns)	Package Marking
Base Ordering Part Number	Package & Temperature	Package Modifier/Model Number	Packing Type			
S71GL032NA0	BHW	0B	0, 2, 3 (1)	90 / Bottom Boot Sector	pSRAM 10 / 70	TLC056
		0F		90 / Top Boot Sector		
S71GL032NA0	BHW	0K		90 / Bottom Boot Sector	pSRAM 9 / 70	
		0P		90 / Top Boot Sector		
S71GL064NA0	BHW	0B		90 / Bottom Boot Sector	pSRAM 10 / 70	TSC056
		0F		90 / Top Boot Sector		
S71GL064NB0	BFW, BHW	0K		90 / Bottom Boot Sector	pSRAM 9 / 70	
S71GL064NB0		0P		90 / Top Boot Sector		
S71GL064NB0	BHW	0U		90 / Bottom Boot Sector	pSRAM 8 / 70	
S71GL064NB0		0Z		90 / Top Boot Sector		

Note:

1. Type 0 is standard. Specify other options as required.

6. Physical Dimensions

6.1 TLC056—56-ball Fine-Pitch Ball Grid Array (FBGA) 9 x 7 mm Package



PACKAGE	TLC 056			
JEDEC	N/A			
D x E	9.00 mm x 7.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		9.00 BSC.		BODY SIZE
E		7.00 BSC.		BODY SIZE
D1		5.60 BSC.		MATRIX FOOTPRINT
E1		5.60 BSC.		MATRIX FOOTPRINT
MD		8		MATRIX SIZE D DIRECTION
ME		8		MATRIX SIZE E DIRECTION
n		56		BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
		A1,A8,D4,D5,E4,E5,H1,H8		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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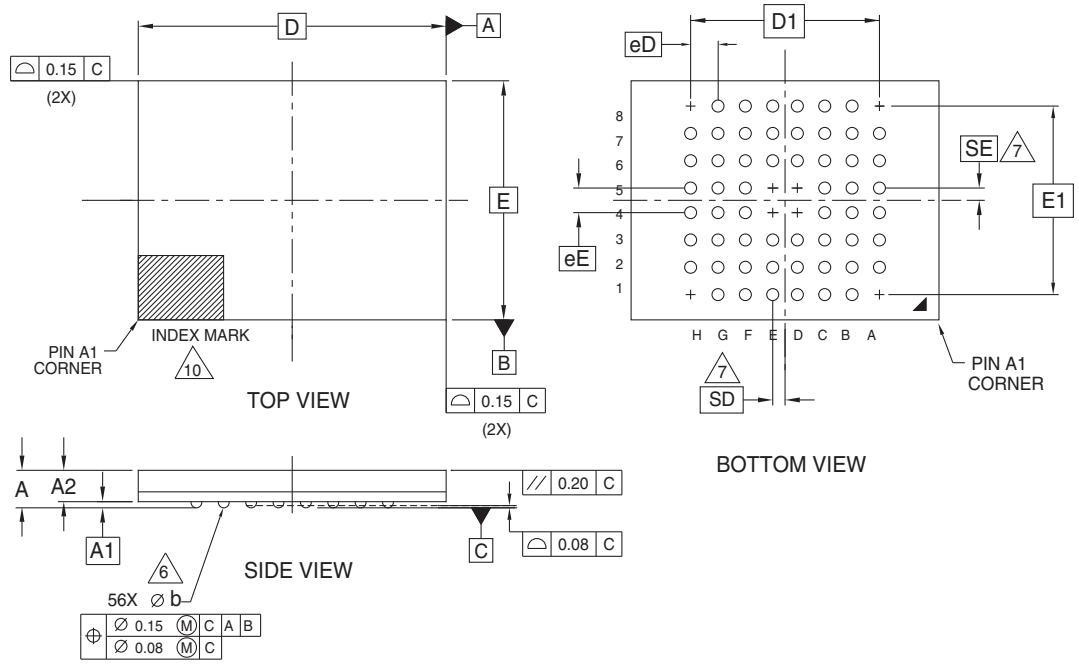
6.2 TSC056—56-ball Fine-Pitch Ball Grid Array (FBGA) 9 x 7 mm Package



PACKAGE	TSC 056			
JEDEC	N/A			
D x E	9.00 mm x 7.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		9.00 BSC.		BODY SIZE
E		7.00 BSC.		BODY SIZE
D1		5.60 BSC.		MATRIX FOOTPRINT
E1		5.60 BSC.		MATRIX FOOTPRINT
MD		8		MATRIX SIZE D DIRECTION
ME		8		MATRIX SIZE E DIRECTION
n		56		BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
		A1,A8,D4,D5,E4,E5,H1,H8		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

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7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

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9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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7. Revision History

Section	Description
Revision 01 (May 14, 2007)	
	Initial release.
Revision 02 (June 19, 2007)	
Global	Editorial changes to valid combinations table
Revision 03 (March 25, 2008)	
Ordering Information	Added Low-Halogen option to package type.
Revision 04 (October 31, 2008)	
General Description	Added pSRAM Type 8, 90 nm
Product Selector Guide	Added pSRAM Type 8, 90 nm Changed S71GL064Nxx-xx package to TSC056
Ordering Information	Changed S71GL064Nxx-xx package to TSC056
Physical Dimensions	Added TSC056
Revision 05 (January 20, 2009)	
Global	Added OPNs S71GL032NA0BHW0B/0F and S71GL064NA0BHW0B/0F
General Description	Added pSRAM Type 10
Revision 06 (January 13, 2010)	
General Description	Updated Table with current pSRAM offerings
Global	Removed pSRAM Type 7 MCPs Added 32 Mb and 64 Mb pSRAM Type 9 MCPs
Revision 07 (May 8, 2012)	
Global	Removed 4 Mb and 8 Mb pSRAM Updated Document and Publication Identification Number descriptions

Colophon

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