LP5951 Micropower, 150mA Low-Dropout CMOS Voltage Regulator

Check for Samples: LP5951

FEATURES

- **Excellent Line Transient Response: ±2mV typ.**
- **Excellent PSRR: -60dB at 1kHz typ.**
- **Low Quiescent Current of 29µA typ.**
- **1.8 to 5.5V Input Voltage Range**
- **Small SC70-5 and SOT-23-5 Packages**
- **Fast Turn-on Time of 30µs typ.**
- **Typ. < 1nA Quiescent Current in Shutdown**
- **Ensured 150mA Output Current**
- **Output Voltage Range: 1.3V to 3.7V**
- **Logic Controlled Enable 0.4V/0.9V**
- **Good Load Transient Response of 50mVpp typ.**
- **Thermal-overload and Short-circuit Protection**
- **-40°C to +125°C Junction Temperature Range**

APPLICATIONS

- **General Purpose**

DESCRIPTION

The LP5951 regulator is designed to meet the requirements of portable, battery-powered systems providing a regulated output voltage and low quiescent current. When switched to shutdown mode via a logic signal at the Enable pin, the power consumption is reduced to virtually zero.

The LP5951 is designed to be stable with small 1µF ceramic capacitors.

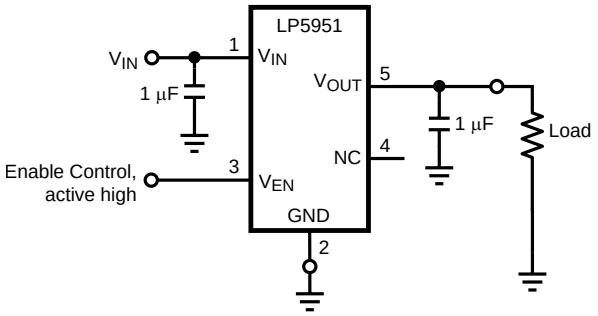
The LP5951 also features internal protection against short-circuit currents and over-temperature conditions.

Performance is specified for a -40°C to 125°C temperature range.

The device is available in SOT-23-5 and SC70-5 package.

The device is available in fixed output voltages in the range of 1.3V to 3.7V. For availability, please contact your local TI sales office.

Typical Application Circuit



Connection Diagram

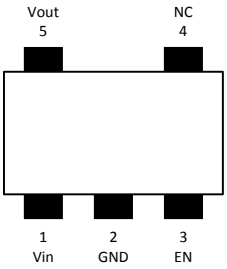


Figure 1. 5-Lead SOT-23 Package – Top View
See Package Number DBV

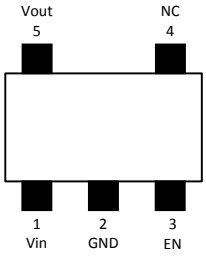


Figure 2. 5-Lead SC70 Package – Top View
See Package Number DCK

PIN DESCRIPTIONS

Pin Number	Pin Name	Description
1	V_{IN}	Input Voltage. Input range: 1.8V to 5.5V
2	GND	Ground
3	EN	Enable pin logic input: Low = shutdown, High = normal operation. This pin should not be left floating.
4	NC	No internal connection
5	V_{OUT}	Regulated output voltage

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

V_{IN} pin: Voltage to GND		-0.3V to 6.5V
EN pin: Voltage to GND		-0.3V to (V_{IN}+0.3V) with 6.5V max
Continuous Power Dissipation[3]		Internally Limited
Junction Temperature ($T_{J\text{-}MAX}$)		150°C
Storage Temperature Range		-65°C to + 150°C
Package Peak Reflow Temperature (10-20 sec.)		240°C
Package Peak Reflow Temperature (Pb-free, 10-20 sec.)		260°C
ESD Rating[4]	Human Body Model:	2.0kV
	Machine Model	200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 160°C (typ.) and disengages at T_J = 140°C (typ.).
(4) The Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin. (MIL-STD-883 3015.7)

Operating Ratings (1) (2)

Input Voltage Range (V_{IN})	1.8V to 5.5V
V_{EN} Input Voltage	0 to (V_{IN} + 0.3V)
Junction Temperature (T_J) Range	-40°C to + 125°C
Ambient Temperature (T_A) Range	See (3)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}) (1)	
SOT-23-5 Package	220°C/W
SC70-5 Package	415°C/W

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special attention must be paid to thermal dissipation issues in board design.

Electrical Characteristics (1) (2)

Typical values and limits appearing in standard typeface are for T_A = 25°C. Limits appearing in **boldface** type apply over the full operating temperature range: -40°C ≤ T_J ≤ +125°C. Unless otherwise noted, V_{IN} = $V_{OUT(NOM)}$ + 1V, C_{IN} = 1µF, C_{OUT} = 1µF, V_{EN} = 0.9V.

Symbol	Parameter	Condition	Typ	Limit		Units
				Min	Max	
V_{IN}	Input Voltage	V_{IN} ≥ $V_{OUT(NOM)}$ + V_{DO}		**1.8**	**5.5**	V
ΔV_{OUT}	Output Voltage Tolerance	I_{OUT} = 1mA -30°C ≤ T_J ≤ +125°C		-2.0 **-3.5**	2.0 **3.5**	% %
	Line Regulation Error	V_{IN} = $V_{OUT(NOM)}$ + 1V to 5.5V I_{OUT} = 1mA	0.1			%/V
	Load Regulation Error	I_{OUT} = 1mA to 150mA	-0.01			%/mA
V_{DO}	Output Voltage Dropout (3)	I_{OUT} = 150mA V_{OUT} ≥ 2.5V V_{OUT} < 2.5V	 200		 **250** **350**	 mV mV
I_Q	Quiescent Current	V_{EN} = 0.9V, I_{LOAD} = 0 V_{EN} = 0.9V, I_{LOAD} = 150mA V_{EN} = 0V	29 33 0.005		**55** **70** 1	µA µA µA
I_{SC}	Output Current (short circuit)	V_{IN} = $V_{OUT(NOM)}$ + 1V	400	**150**		mA
PSRR	Power Supply Rejection Ratio	Sine modulated V_{IN} f = 100Hz f = 1kHz f = 10kHz	 60 60 50			 dB dB dB
E_N	Output Noise	BW = 10Hz - 100kHz	125			μV_{RMS}
TSD	Thermal Shutdown		160			°C
	Temperature Hysteresis		20			°C

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are ensured by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(3) Dropout voltage is defined as the input to output voltage differential at which the output voltage falls to 100mV below the nominal output voltage. This specification does not apply for output voltages below 1.8V.

Enable Control Characteristics

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
I_{EN}	Maximum Input Current at V_{EN} Input	0V ≤ V_{EN} ≤ V_{IN}, V_{IN} = 5.5V		**-1**	**1**	µA
V_{IL}	Low Input Threshold (shutdown)	V_{IN} = 1.8..5.5V			**0.4**	V
V_{IH}	High Input Threshold (enable)	V_{IN} = 1.8..5.5V		**0.9**		V

Transient Characteristics

Symbol	Parameter	Conditions	Typical	Limit		Units
				Min	Max	
ΔV_{OUT}	Dynamic Line Transient	V_{IN} = $V_{OUT(NOM)}$ + 1V to $V_{OUT(NOM)}$ + 1V + 0.6V in 30µs, no load	±2			mV
ΔV_{OUT}	Dynamic Load Transient	I_{OUT} = 0mA to 150mA in 10µs I_{OUT} = 150mA to 0mA in 10µs I_{OUT} = 1mA to 150mA in 1µs I_{OUT} = 150mA to 1mA in 1µs	-30 20 -50 40			mV mV mV mV
ΔV_{OUT}	Overshoot on Startup	Nominal conditions	10			mV
T_{ON}	Turn on time	I_{OUT} = 1mA	30			µs

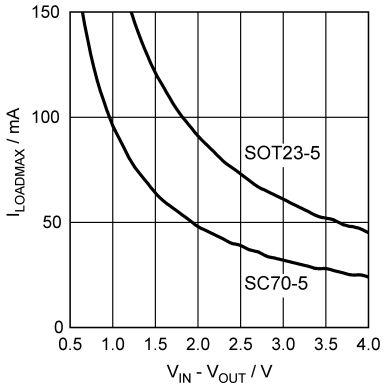
Output Capacitor, Recommended Specification

Symbol	Parameter	Conditions	Value	Limit (1)		Units
				Min	Max	
C_{OUT}	Output Capacitance	Capacitance (2) I_{OUT} = 150mA, V_{IN} = 5.0V	1.0	0.7	47	µF
		ESR		0.003	0.300	Ω

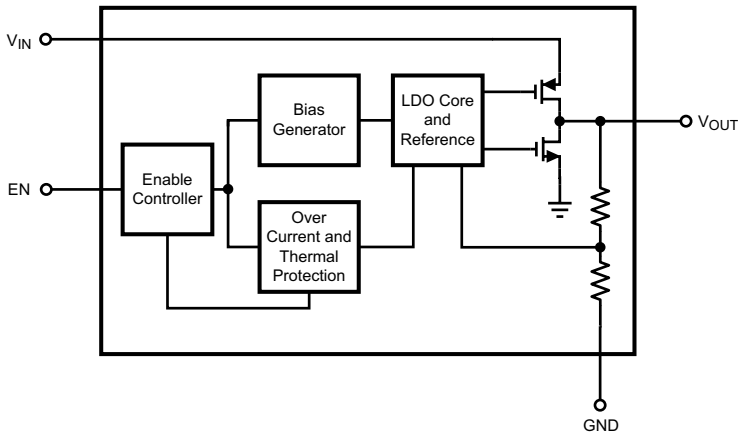
(1) Min and Max limits are ensured by design
(2) The capacitor tolerance should be 30% or better over temperature. The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R. However, dependent on application, X5R, Y5V, and Z5U can also be used. The shown minimum limit represents real minimum capacitance, including all tolerances and must be maintained over temperature and dc bias voltage (See capacitor section in Applications Hints)

Output Current Derating

Maximum Load Current vs V_{IN} - V_{OUT}, T_A = 85°C, V_{OUT} = 1.5V



Block Diagram



Typical Performance Characteristics

Unless otherwise specified, C_{IN} = 1µF ceramic, C_{OUT} = 1µF ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1V, T_A = 25°C, Enable pin is tied to V_{IN}.

Load Transient Response

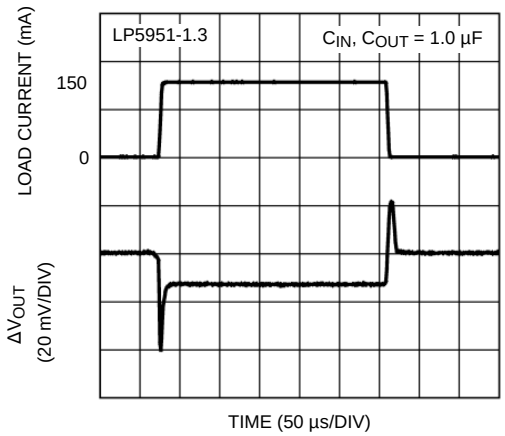


Figure 3.

Load Transient Response

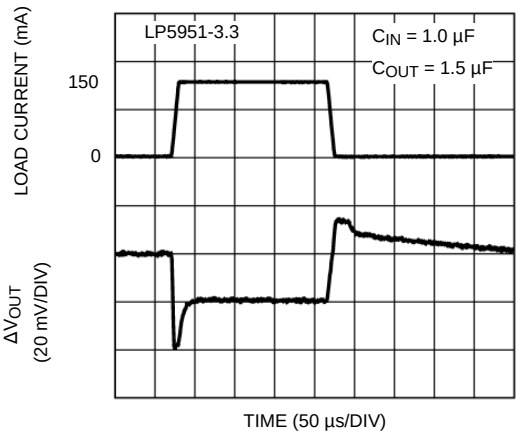


Figure 4.

Line Transient Response

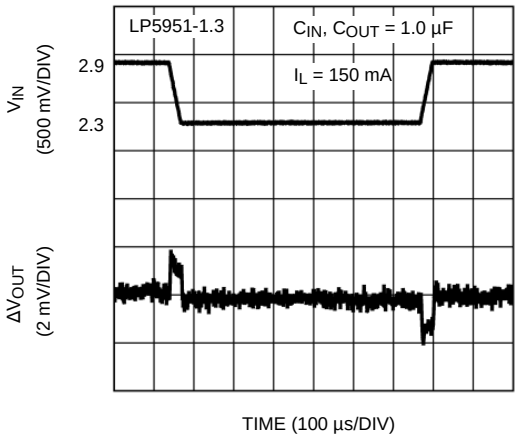


Figure 5.

Line Transient Response

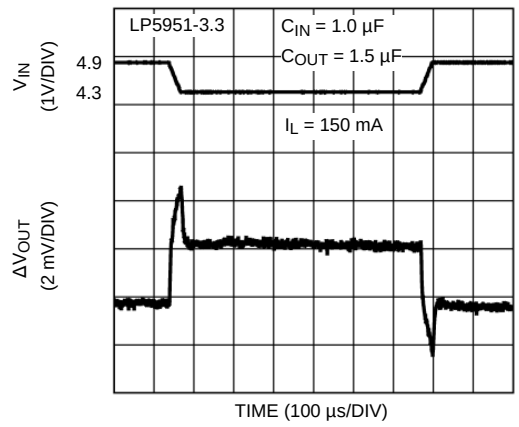


Figure 6.

Enable Start-up Time

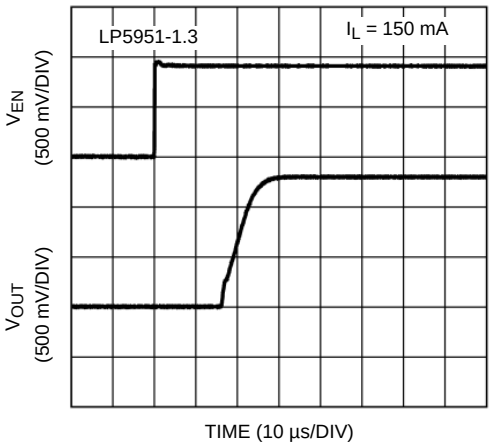


Figure 7.

Enable Start-up Time

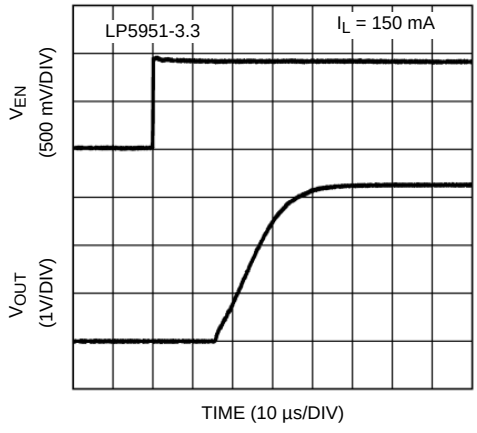


Figure 8.

Typical Performance Characteristics (continued)

Unless otherwise specified, C_{IN} = 1µF ceramic, C_{OUT} = 1µF ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1V, T_A = 25°C, Enable pin is tied to V_{IN}.

Output Voltage Change vs Temperature

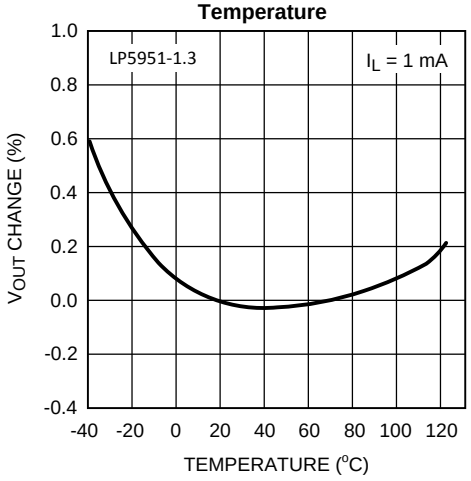


Figure 9.

Ground Current vs V_{IN}

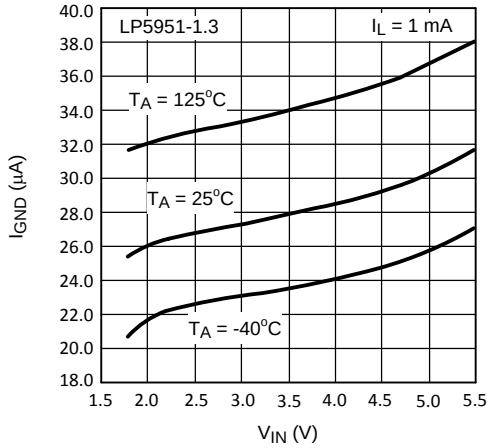


Figure 10.

Power Supply Rejection Ratio

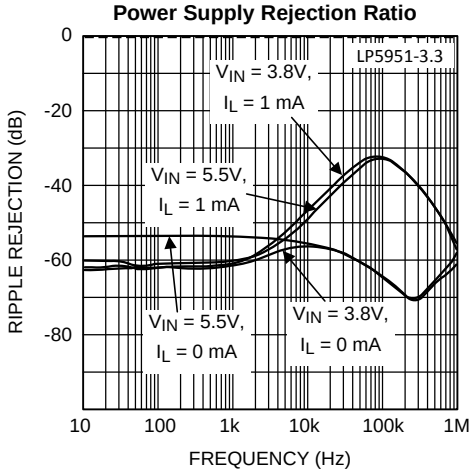


Figure 11.

APPLICATION HINTS

POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

As stated (see below(1)) in the electrical specification section, the allowable power dissipation for the device in a given package can be calculated using the equation:

$$P_D = (T_{J(MAX)} - T_A) / \theta_{JA} \quad (1)$$

With a θ_{JA} = 220°C/W, the device in the SOT-23-5 package returns a value of 454 mW with a maximum junction temperature of 125°C at T_A of 25°C.

The actual power dissipation across the device can be estimated by the following equation:

$$P_D \approx (V_{IN} - V_{OUT}) * I_{OUT} \quad (2)$$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

EXTERNAL CAPACITORS

As is common with most regulators, the LP5951 requires external capacitors to ensure stable operation. The LP5951 is specifically designed for portable applications requiring minimum board space and the smallest size components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitor is required for stability. It is recommended that a 1.0µF capacitor be connected between the LP5951 input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain ≥0.7µF over the entire operating temperature range.

OUTPUT CAPACITOR

The LP5951 is designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types X7R, Z5U, or Y5V) in the 1.0µF range (up to 47µF) and with ESR between 3 mΩ to 500 mΩ is suitable in the LP5951 application circuit.

This capacitor must be located a distance of not more than 1cm from the V_{OUT} pin and returned to a clean analogue ground.

It is also possible to use tantalum or film capacitors at the device output, V_{OUT}, but these are not as attractive for reasons of size and cost (see the section CAPACITOR CHARACTERISTICS).

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

CAPACITOR CHARACTERISTICS

The LP5951 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 1µF to 4.7µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1µF ceramic capacitor is in the range of 3mΩ to 40mΩ, which easily meets the ESR requirement for stability for the LP5951.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, Figure 12 shows a typical graph comparing different capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, increasing the DC Bias condition can result in the capacitance value falling below the minimum value given in the recommended capacitor specifications table (0.7µF in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

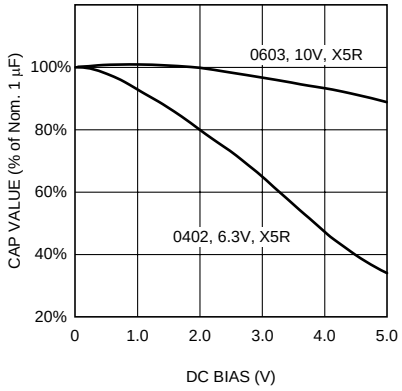


Figure 12. Graph Showing A Typical Variation In Capacitance vs DC Bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of -55°C to +85°C. Many large value ceramic capacitors, larger than 1µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 4.7µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

NO-LOAD STABILITY

The LP5951 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

ENABLE OPERATION

The LP5951 may be switched ON or OFF by a logic input at the Enable pin, V_{EN}. A logic high at this pin will turn the device on. When the enable pin is low, the regulator output is off and the device typically consumes 5nA.

If the application does not require the Enable switching feature, the V_{EN} pin should be tied to V_{IN} to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the V_{EN} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under Enable Control Characteristics, V_{IL} and V_{IH}.

FAST TURN OFF AND ON

The controlled switch-off feature of the device provides a fast turn off by discharging the output capacitor via an internal FET device. This discharge is current limited by the RDSon of this switch.

Fast turn-on is ensured by an optimized architecture allowing a very fast ramp of the output voltage to reach the target voltage.

SHORT-CIRCUIT PROTECTION

The LP5951 is short circuit protected and in the event of a peak over-current condition, the output current through the PMOS will be limited.

If the over-current condition exists for a longer time, the average power dissipation will increase depending on the input to output voltage difference until the thermal shutdown circuitry will turn off the PMOS.

Please refer to the Thermal Properties section for power dissipation calculations.

THERMAL-OVERLOAD PROTECTION

Thermal-Overload Protection limits the total power dissipation in the LP5951. When the junction temperature exceeds T_J = 160°C typ., the shutdown logic is triggered and the PMOS is turned off, allowing the device to cool down. After the junction temperature dropped by 20°C (temperature hysteresis), the PMOS is activated again. This results in a pulsed output voltage during continuous thermal-overload conditions.

The Thermal-Overload Protection is designed to protect the LP5951 in the event of a fault condition. For normal, continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C (see Absolute Maximum Ratings).

REVERSE CURRENT PATH

The internal PFET pass device in LP5951 has an inherent parasitic body diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 50mA.

For currents above this limit an external Schottky diode must be connected from V_{OUT} to V_{IN} (cathode on V_{IN}, anode on V_{OUT}).

EVALUATION BOARDS

For availability of evaluation boards, see the LP5951 product folder. For information regarding evaluation boards, see the TI AN-1486 Application Report (SNVA169).

SUGGESTED CAPACITORS AND THEIR SUPPLIERS

Capacitance / µF	Model	Vendor	Type	Case Size / Inch (mm)
1.0	C1608X5R1A105K	TDK	Ceramic, X5R	0603 (1608)
1.0	C1005X5R1A105K	TDK	Ceramic, X5R	0402 (1005)

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F **Page**

- Changed layout of National Data Sheet to TI format 11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5951MF-1.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKRB	Samples
LP5951MF-1.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKAB	Samples
LP5951MF-1.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKBB	Samples
LP5951MF-2.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKCB	Samples
LP5951MF-2.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKEB	Samples
LP5951MF-2.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKFB	Samples
LP5951MF-3.0	ACTIVE	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	LKGB	Samples
LP5951MF-3.0/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKGB	Samples
LP5951MF-3.3	ACTIVE	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	LKHB	Samples
LP5951MF-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKHB	Samples
LP5951MFX-1.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKRB	Samples
LP5951MFX-1.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKAB	Samples
LP5951MFX-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKBB	Samples
LP5951MFX-2.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKCB	Samples
LP5951MFX-2.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKEB	Samples
LP5951MFX-2.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKFB	Samples
LP5951MFX-3.0/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKGB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5951MFX-3.3/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LKHB	Samples
LP5951MG-1.3/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L23	Samples
LP5951MG-1.5	ACTIVE	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 125	L2B	Samples
LP5951MG-1.5/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L2B	Samples
LP5951MG-1.8/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L3B	Samples
LP5951MG-2.0/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L4B	Samples
LP5951MG-2.5/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L5B	Samples
LP5951MG-2.8/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L6B	Samples
LP5951MG-3.0/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L7B	Samples
LP5951MG-3.3/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LAB	Samples
LP5951MG-3.7/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L44	Samples
LP5951MGX-1.3/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L23	Samples
LP5951MGX-1.5/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L2B	Samples
LP5951MGX-1.8/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L3B	Samples
LP5951MGX-2.0/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L4B	Samples
LP5951MGX-2.5/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L5B	Samples
LP5951MGX-2.8/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L6B	Samples
LP5951MGX-3.0/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L7B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5951MGX-3.3/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		LAB	Samples
LP5951MGX-3.7/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L44	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

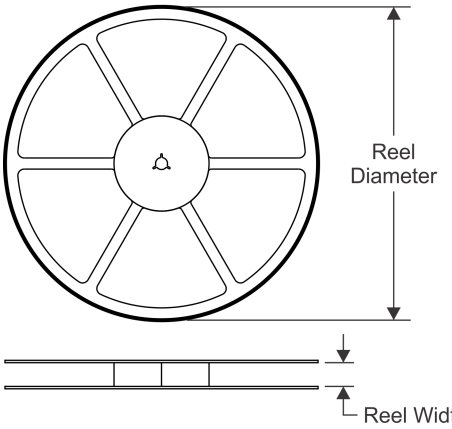
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

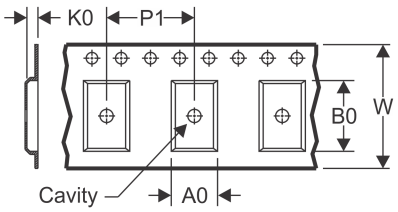
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

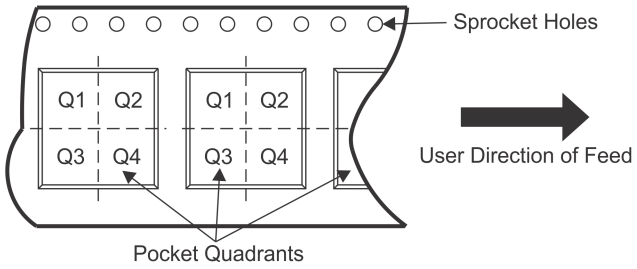


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

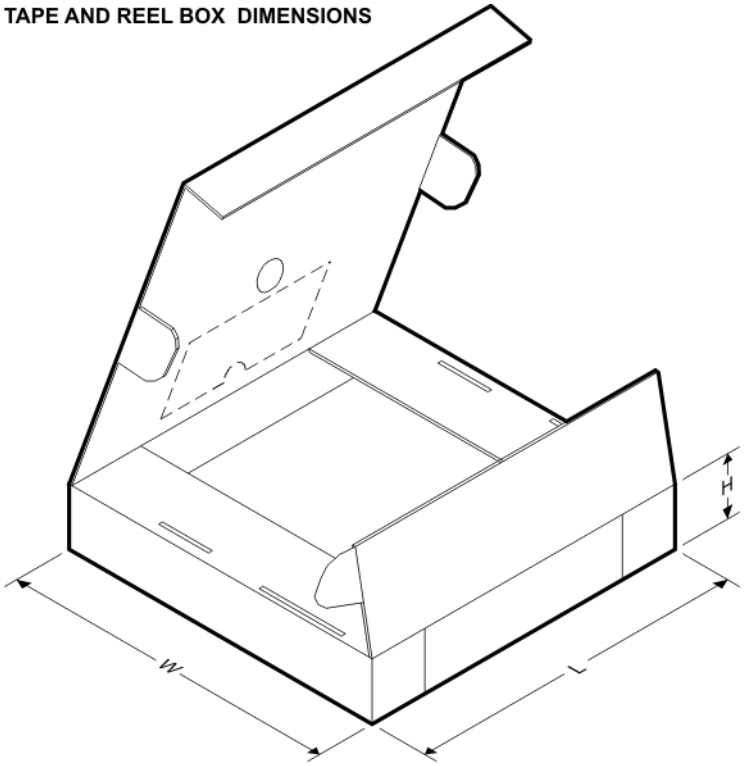


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5951MF-1.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MF-1.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MF-1.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MF-2.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MF-2.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MF-2.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MF-3.0	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MF-3.0/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MF-3.3	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MF-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MFX-1.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MFX-1.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MFX-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MFX-2.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MFX-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MFX-2.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MFX-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP5951MFX-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5951MG-1.3/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MG-1.5	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MG-1.5/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MG-1.8/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MG-2.0/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MG-2.5/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MG-2.8/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MG-3.0/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MG-3.3/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MG-3.7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MGX-1.3/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MGX-1.5/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MGX-1.8/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MGX-2.0/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MGX-2.5/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MGX-2.8/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MGX-3.0/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MGX-3.3/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LP5951MGX-3.7/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

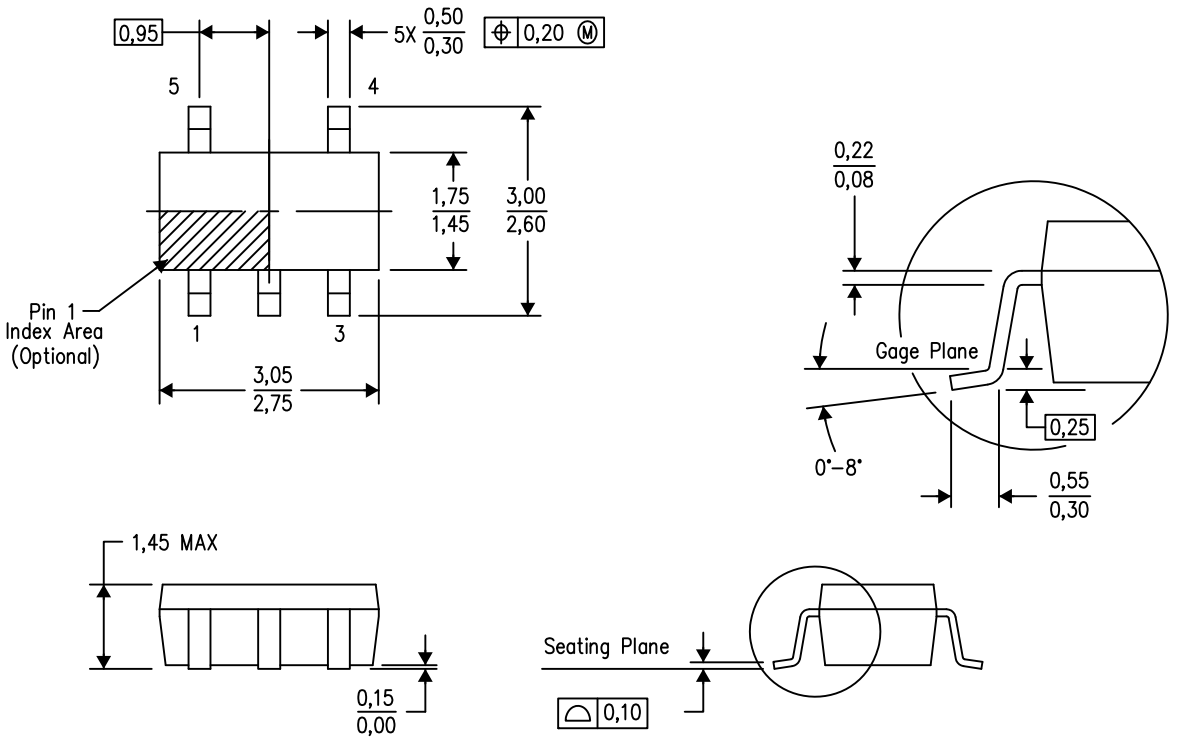
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5951MF-1.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP5951MF-1.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP5951MF-1.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP5951MF-2.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP5951MF-2.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP5951MF-2.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP5951MF-3.0	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP5951MF-3.0/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP5951MF-3.3	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP5951MF-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LP5951MFX-1.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5951MFX-1.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5951MFX-1.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5951MFX-2.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5951MFX-2.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5951MFX-2.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5951MFX-3.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5951MFX-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP5951MG-1.3/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LP5951MG-1.5	SC70	DCK	5	1000	210.0	185.0	35.0
LP5951MG-1.5/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LP5951MG-1.8/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LP5951MG-2.0/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LP5951MG-2.5/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LP5951MG-2.8/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LP5951MG-3.0/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LP5951MG-3.3/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LP5951MG-3.7/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LP5951MGX-1.3/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LP5951MGX-1.5/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LP5951MGX-1.8/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LP5951MGX-2.0/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LP5951MGX-2.5/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LP5951MGX-2.8/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LP5951MGX-3.0/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LP5951MGX-3.3/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LP5951MGX-3.7/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0

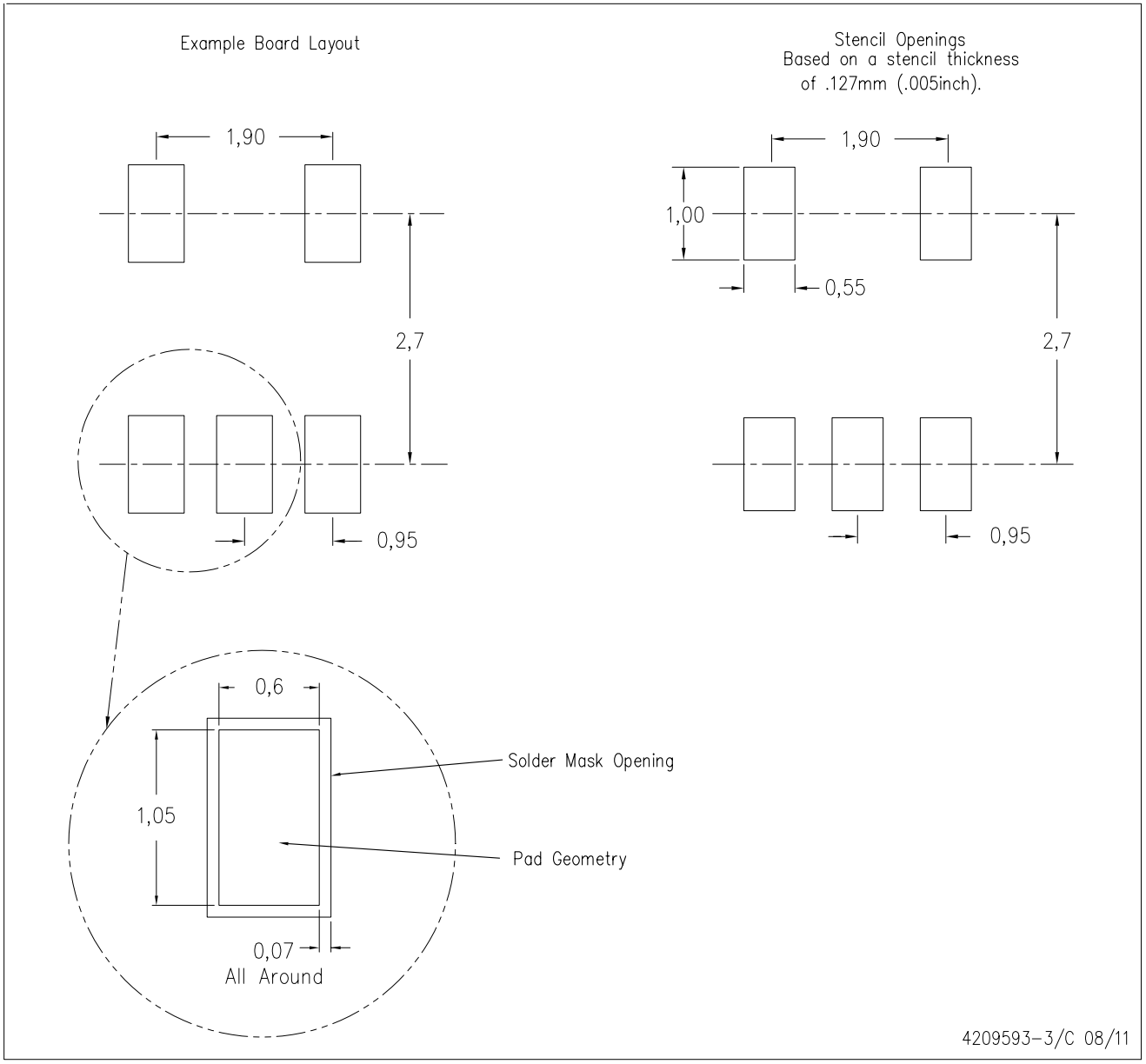
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/L 08/2013

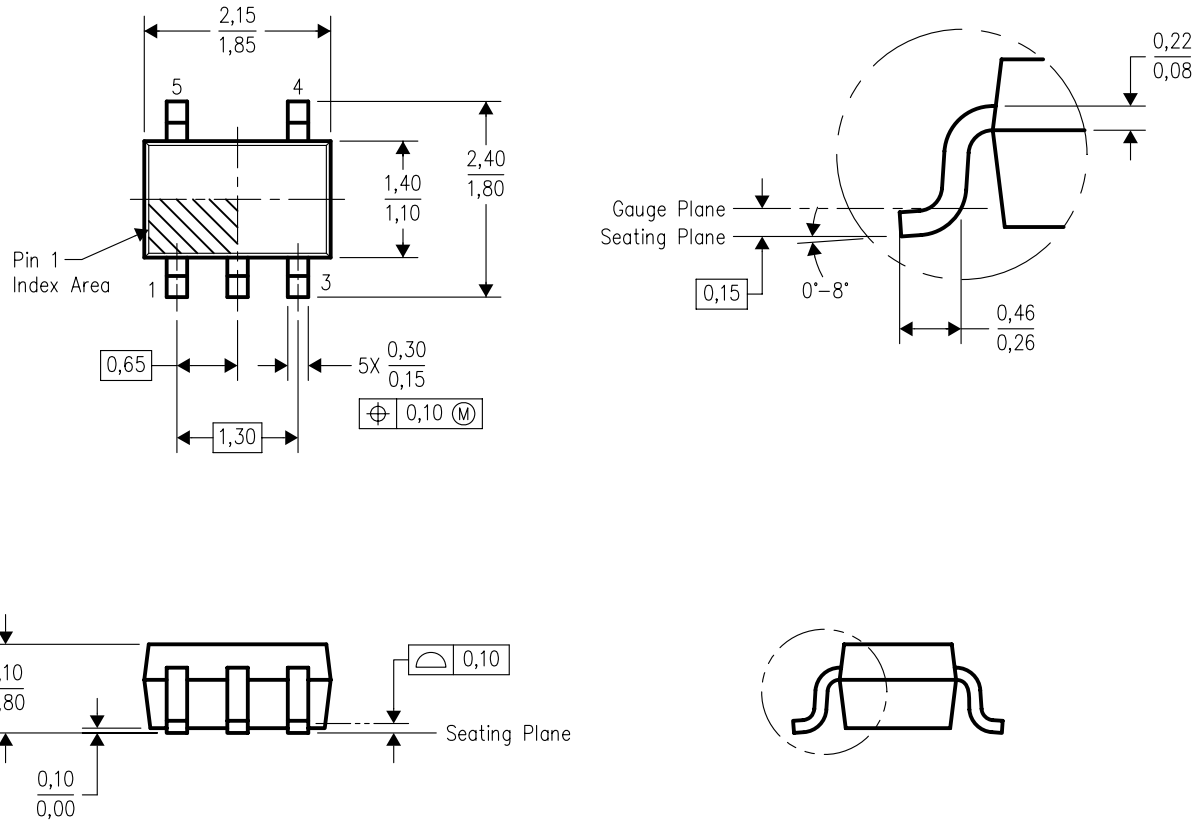
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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