

TOSHIBA Silicon Monolithic

Bi-Polor Digital Integrated Circuit

TD62001P/AP/F/AF

TD62002P/AP/F/AF

TD62003P/AP/F/AF

TD62004P/AP/F/AF

7CH Darlington Sink Driver

Product Description:

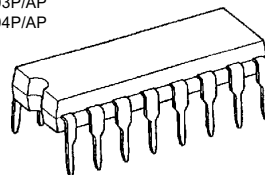
The products are high voltage, high current darlington drivers comprised of seven NPN darlington pairs.

All units feature integral clamp diodes for switching inductive loads. Applications include relay, hammer, lamp, and display (LED) drivers.

Features:

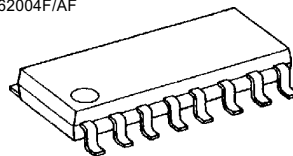
- Output current (single output) 500mA (Max.)
- High sustaining voltage output
35V (Min.) (P and F series)
50V (Min.) (AP and AF series)
- Output clamp diodes
- Inputs compatible with various types of logic
- Package type-P, AP: DIP-16pin
- Package type-F, AF: SOP-16pin

TD62001P/AP
TD62002P/AP
TD62003P/AP
TD62004P/AP



Weight DIP16-P-300A: 1.11g (Typ.)

TD62001F/AF
TD62002F/AF
TD62003F/AF
TD62004F/AF



Weight SOP16-P-225: 0.16g (Typ.)

TYPE	INPUT BASE RESISTOR	DESIGNATION
TD62001P/AP/F/AF	External	General Purpose
TD62002P/AP/F/AF	10.5-k Ω +7V Zener diode	14~25V P-MOS
TD62003P/AP/F/AF	2.7k Ω	TTL, 5V C-MOS
TD62004P/AP/F/AF	10.5k Ω	6~15V P-MOS, C-MOS

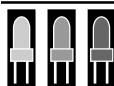
MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Output Sustaining Voltage	V _{CE(SUS)}	-0.5~35	V
		-0.5~50	
Output Current	I _{OUT}	500	mA / ch
Input Voltage	V _{IN} (Note 1)	-0.5~30	V
Input Current	I _{IN} (Note 2)	25	mA
Clamp Diode Reverse Voltage	V _R	35	V
		50	
Clamp Diode Forward Current	I _F	500	mA
Power Dissipation	P _D	1.0	W
		1.47	
		0.54 / 0.69*	
Operating Temperature	T _{opr}	-30~75	°C
		-40~85	
Storage Temperature	T _{stg}	-55~150	°C

Note1 Except TD62001P/AP/F/AF

Note2 Only TD62001P/AP/F/AF

* On Glass Epoxy PCB (30×30×1.6mm Cu 50%)



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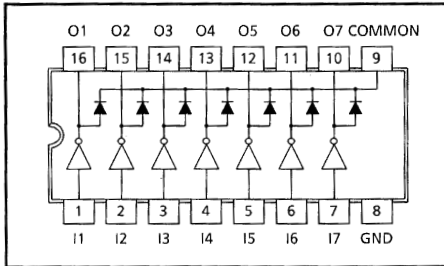
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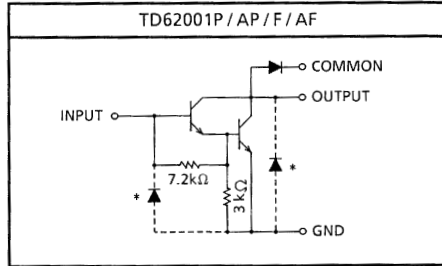
TOSHIBA Silicon Monolithic Bi-Polar Digital Integrated Circuit

TD62001P/AP/F/AF, TD62002P/AP/F/AF, TD62003P/AP/F/AF, TD62004P/AP/F/AF

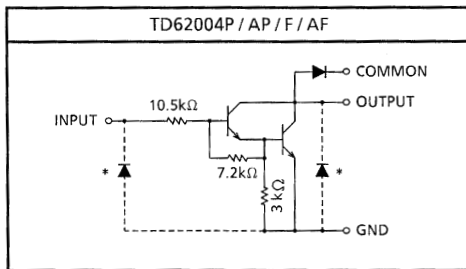
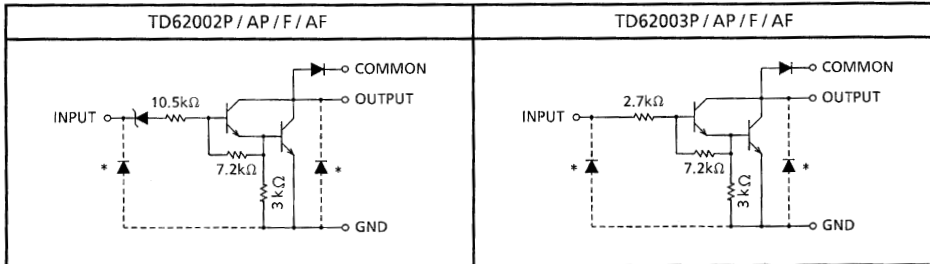
PIN CONNECTION (TOP VIEW)



SCHEMATICS (EACH DRIVER)



SCHEMATICS (EACH DRIVER)



* : Parasitic Diodes

The input and output parasitic diodes cannot be used as clamp diodes.

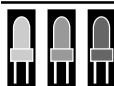
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TD62001P/AP/F/AF, TD62002P/AP/F/AF, TD62003P/AP/F/AF, TD62004P/AP/F/AF

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim 85^\circ\text{C}$ and $T_a = -30 \sim 75^\circ\text{C}$ for only Type-P)

CHARACTERISTIC		SYMBOL	CONDITION		MIN	TYP	MAX	UNIT
Output Sustaining Voltage	P, F	V _{CE(SUS)}			0	—	35	V
	AP, AF				0	—	50	
Output Current	P	I _{OUT}	TPW = 25ms	Duty = 10%	0	—	295	mA / ch
				Duty = 50%	0	—	95	
	7 Circuits		Duty = 10%	0	—	370		
			Duty = 50%	0	—	130		
	AP		T _a = 85°C	Duty = 10%	0	—	233	
				Duty = 50%	0	—	70	
F, AF	T _j = 120°C							
Input Voltage	Except TD62001P / AP / F / AF	V _{IN}			0	—	24	V
Input Voltage (Output On)	TD62002	V _{IN(ON)}	I _{OUT} = 400mA h _{FE} = 800		14.5	—	24	V
	TD62003				2.8	—	24	
	TD62004				6.2	—	24	
Input Voltage (Output Off)	TD62001	V _{IN(OFF)}			0	—	0.6	V
	TD62002				0	—	7.4	
	TD62003				0	—	0.7	
	TD62004				0	—	1.0	
Input Current	Only TD62001P / AP / F / AF	I _{IN}			0	—	10	mA
Clamp Diode Reverse Voltage	P, F	V _R			—	—	35	V
	AP, AF				—	—	50	
Clamp Diode Forward Current		I _F			—	—	350	mA
Power Dissipation	P	P _D	T _a = T _{opr} (max.)		—	—	0.6	W
	AP				—	—	0.76	
	AF, F		※ 1 T _a = T _{opr} (max.)		—	—	0.36	

※1 On Glass Epoxy PCB (30×30×1.6mm Cu 50%)



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ELECTRICAL CHARACTERISTICS (Ta=25°C unless otherwise noted)

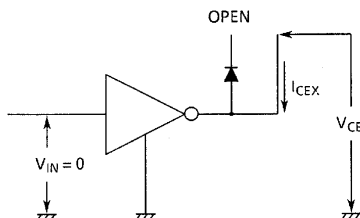
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN	TYP	MAX	UNIT	
Output Leakage Current	AP, AF	I _{CEX}	1	V _{CE} =50V, T _a =25°C	—	—	50	μA	
	F			V _{CE} =50V, T _a =85°C	—	—	100		
				V _{CE} =35V, T _a =25°C	—	—	50		
				V _{CE} =35V, T _a =85°C	—	—	100		
				V _{CE} =35V, T _a =25°C	—	—	50		
	P			V _{CE} =35V, T _a =75°C	—	—	100		
Collector-Emitter Saturation Voltage		V _{CE(sat)}	2	I _{OUT} =350mA, I _{IN} =500μA	—	1.3	1.6	V	
				I _{OUT} =200mA, I _{IN} =350μA	—	1.1	1.3		
				I _{OUT} =100mA, I _{IN} =250μA	—	0.9	1.1		
DC Current Transfer Ratio		h _{FE}	2	V _{CE} =2V, I _{OUT} =350mA	1000	—	—		
Input Current (Output On)	TD62002	I _{IN(ON)}	3	V _{IN} =20V, I _{OUT} =350mA	—	1.1	1.7	mA	
	TD62003			V _{IN} =2.4V, I _{OUT} =350mA	—	0.4	0.7		
	TD62004			V _{IN} =9.5V, I _{OUT} =350mA	—	0.8	1.2		
Input Current (Output Off)	P	I _{IN(OFF)}	4	I _{OUT} =500μA, T _a =75°C	50	65	—	μA	
	AP, F, AF			I _{OUT} =500μA, T _a =85°C	50	65	—		
Input Voltage (Output On)	TD62002	V _{IN(ON)}	5	V _{CE} =2V h _{FE} =800	I _{OUT} =350mA	—	—	13.7	V
	TD62003				I _{OUT} =200mA	—	—	11.4	
					I _{OUT} =350mA	—	—	2.6	
					I _{OUT} =200mA	—	—	2.0	
					I _{OUT} =350mA	—	—	4.7	
	TD62004				I _{OUT} =200mA	—	—	4.4	
Clamp Diode Reverse Current	AP, AF	I _R	6	V _R =50V, T _a =25°C	—	—	50	μA	
	F			V _R =50V, T _a =85°C	—	—	100		
				V _R =35V, T _a =25°C	—	—	50		
				V _R =35V, T _a =85°C	—	—	100		
				V _R =35V, T _a =25°C	—	—	50		
	P			V _R =35V, T _a =75°C	—	—	100		
Clamp Diode Forward Voltage		V _F	7	I _F =350mA	—	—	2.0	V	
Input Capacitance		C _{IN}	—		—	15	—	pF	
Turn-On Delay	P, F	t _{ON}	8	V _{OUT} =35V, R _L =87.5Ω C _L =15pF	—	0.1	—	μs	
	AP, AF			V _{OUT} =50V, R _L =125Ω C _L =15pF	—	0.1	—		
Turn-Off Delay	P, F	t _{OFF}	8	V _{OUT} =35V, R _L =87.5Ω C _L =15pF	—	0.2	—		
	AP, AF			V _{OUT} =50V, R _L =125Ω C _L =15pF	—	0.2	—		

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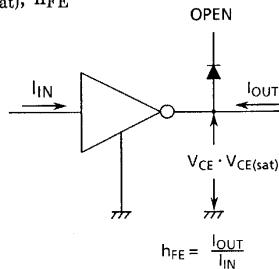
TD62001P/AP/F/AF, TD62002P/AP/F/AF, TD62003P/AP/F/AF, TD62004P/AP/F/AF

TEST CIRCUIT

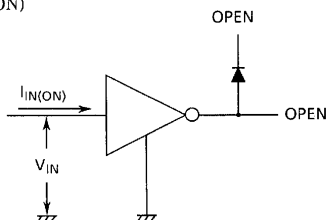
1. I_{CEX}



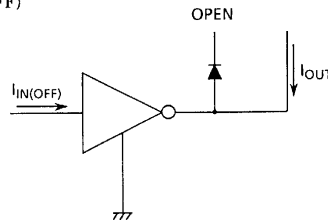
2. $V_{CE(sat)}$, h_{FE}



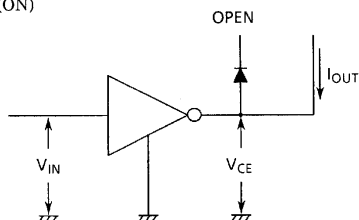
3. $I_{IN(ON)}$



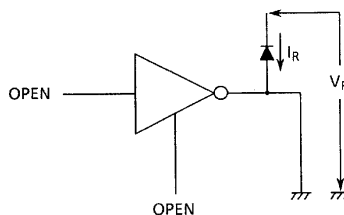
4. $I_{IN(OFF)}$



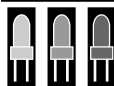
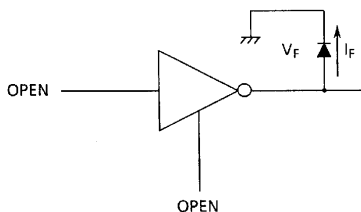
5. $V_{IN(ON)}$



6. I_R



7. V_F



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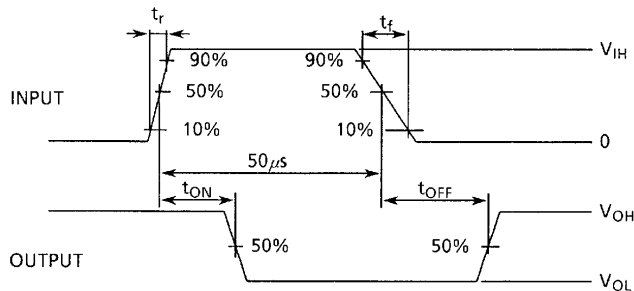
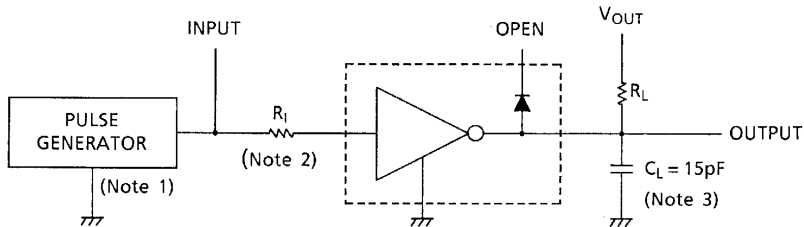
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8. t_{ON} , t_{OFF}



(Note 1) : Pulse Width $50\mu s$, Duty Cycle 10%
Output Impedance 50Ω , $t_r \leq 5ns$, $t_f \leq 10ns$

(Note 2) :

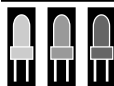
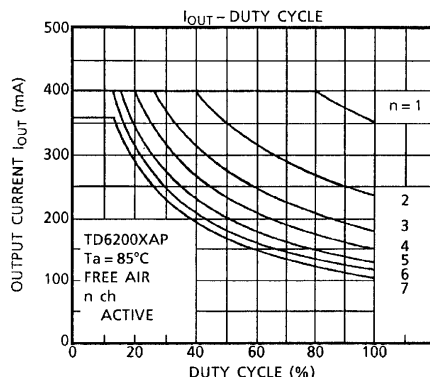
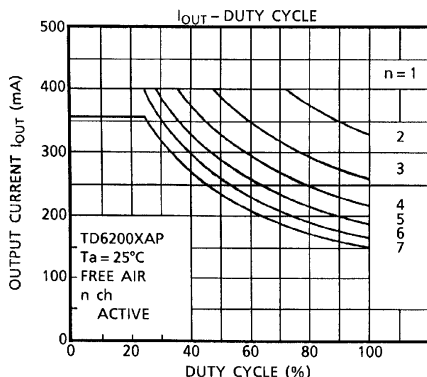
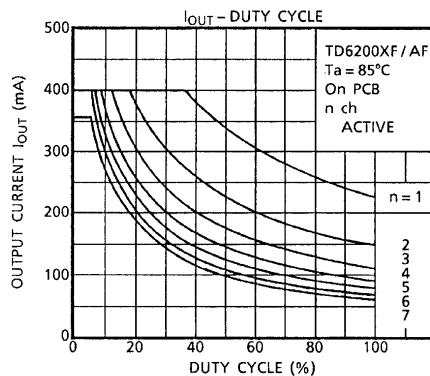
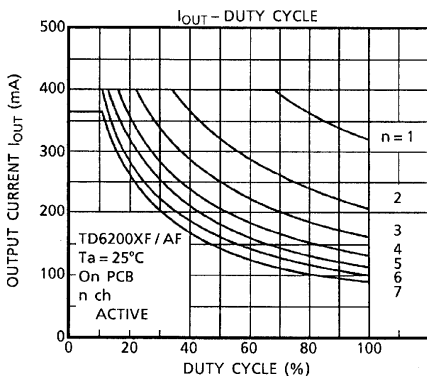
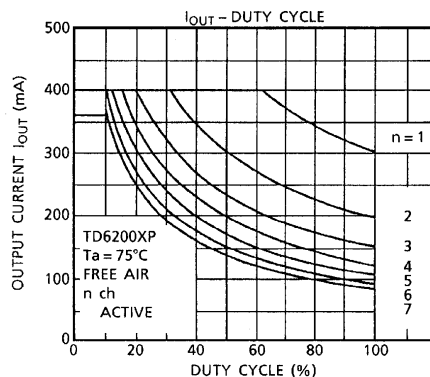
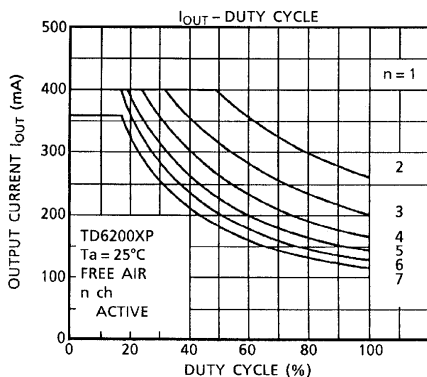
Input Condition

TYPE NUMBER	R_I	V_{IH}
TD62001P / AP / F / AF	$2.7k\Omega$	3V
TD62002P / AP / F / AF	0	13V
TD62003P / AP / F / AF	0	3V
TD62004P / AP / F / AF	0	8V

(Note 3) : CL includes probe and jig capacitance.

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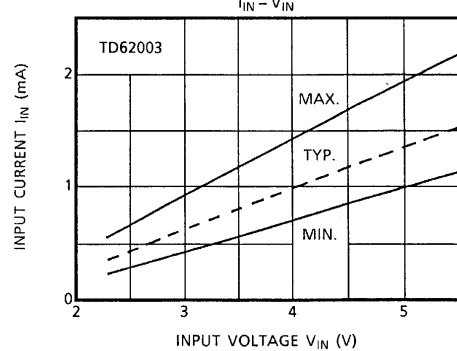
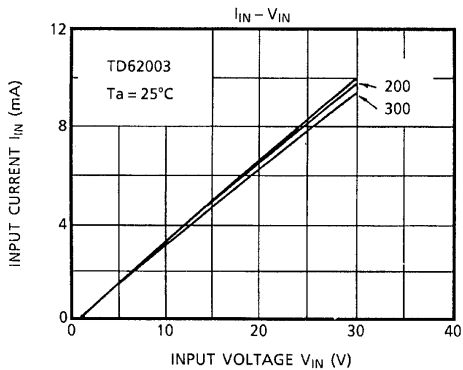
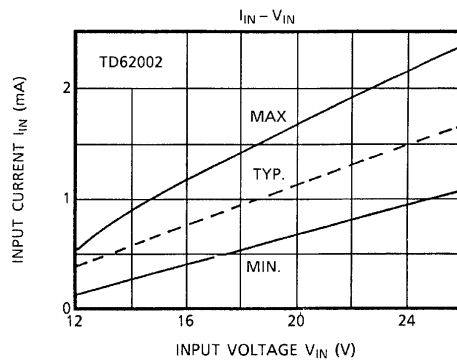
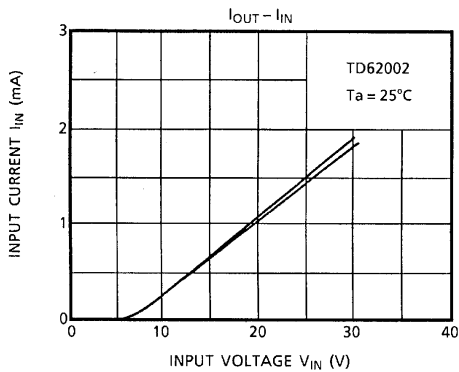
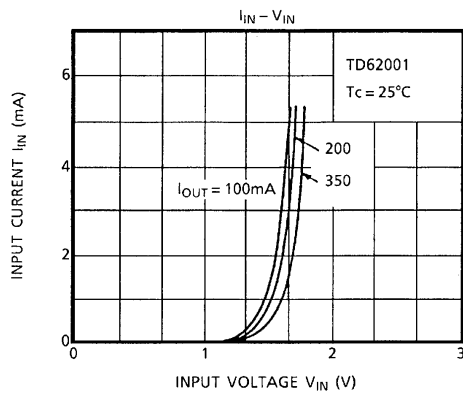
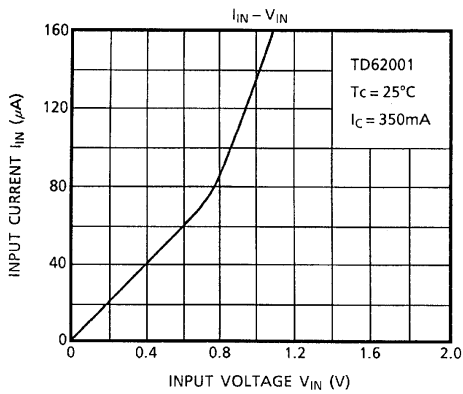
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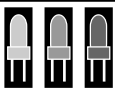
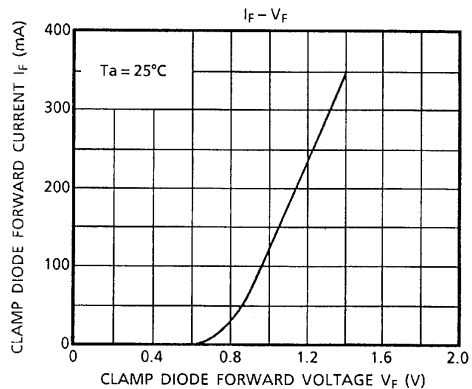
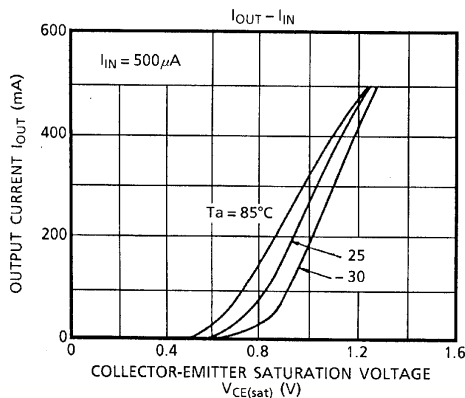
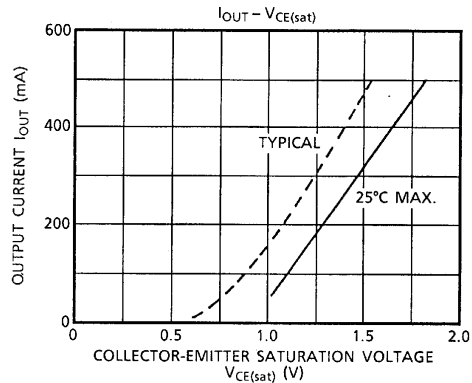
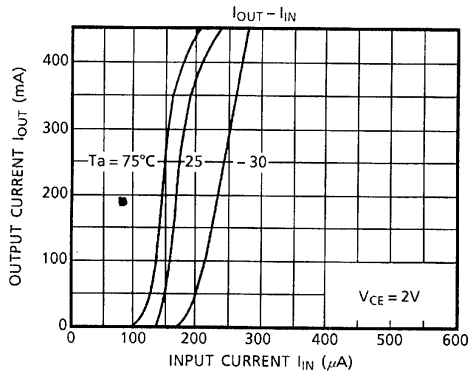
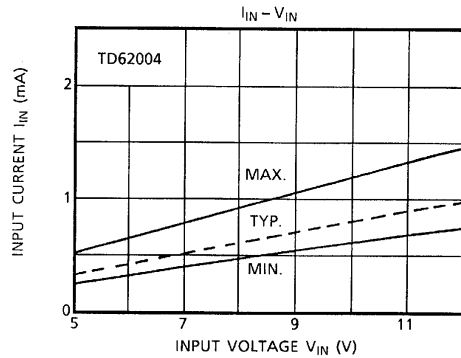
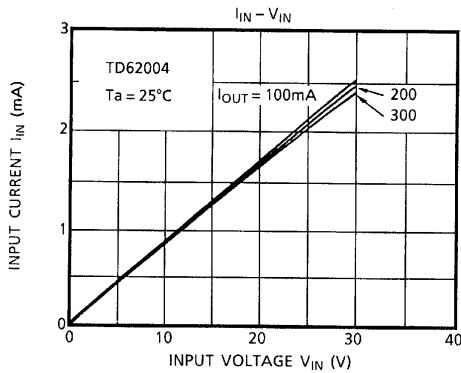
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