FAIRCHILD SEMICONDUCTOR®

October 2007

FAN5631 / FAN5632
Regulated Step-Down Charge Pump DC/DC Converter

Features

- 90% Peak Efficiency
- Low EMI
- Low Ripple
- Selectable Output Voltage:1.2V/1.5V for FAN5631
- Efficiency Optimizer Feature for FAN5632
- Input Voltage Range: 2.2V to 5.5V
- Output Current: Up to 250mA
- ±5% Output Voltage Accuracy
- 30µA Operating Current
- I_{CC}<1mA in Shutdown Mode
- 1.5MHz Operating Frequency
- Shutdown Isolates Output from Input
- Soft-Start Limits Inrush Current
- Short-Circuit and Over-Temperature Protection
- Minimum External Component Count
- 10-Lead 3x3mm MLP Package

Applications

- Cell Phones
- Handheld Computers
- Portable Electronic Equipment
- Core Supply to Next-Generation Processors
- Low-Voltage DC Bus
- Digital Cameras
- DSP Supplies

Description

The FAN5631/FAN5632 is an advanced, third-generation switched capacitor step-down DC/DC converter utilizing Fairchild's proprietary ScalarPump technology. This innovative architecture utilizes scalar switch re-configuration and fractional switching techniques to produce low output ripple, lower ESR spikes, and improve efficiency over a wide load range.

The FAN5631/FAN5632 produces a fixed regulated output voltage from an input voltage of 2.2V to 5V.

To maximize efficiency, the FAN5631/5632 achieves regulation by skipping pulses. Depending on load current, the size of the switches are scaled dynamically; consequently, current spikes and EMI are minimized. An internal soft-start circuitry prevents excessive current from the supply. The device is internally protected against short-circuit and over-temperature conditions.

The FAN5631 has a dual-output voltage feature. When V_{SEL} is high, V_{OUT} is 1.5V; and when V_{SEL} is low, V_{OUT} is 1.2V.

The FAN5632 has an efficiency optimizer feature that, when enabled, changes the switch mode configuration from 2:1 to 1:1 at the lower threshold of V_{IN}. The efficiency is maintained at its peak level over a wider range of input voltages. In addition, V_{OUT} varies from 1.2V to 1.5V as a result of this efficiency optimization. If the efficiency optimizer is not enabled, V_{OUT} is regulated to 1.5V.

Both the FAN5631 and FAN5632 are available in a 10-lead 3x3mm MLP package.

Ordering Information

Part Number	Package	Packing Method
FAN5631MPX	10-Lead 3x3mm Molded Leadless Package (MLP)	Tape and Reel
FAN5632MPX	10-Lead 3x3mm Molded Leadless Package (MLP)	Tape and Reel

All packages are lead free per JEDEC: J-STD-020B standard.

Typical Application

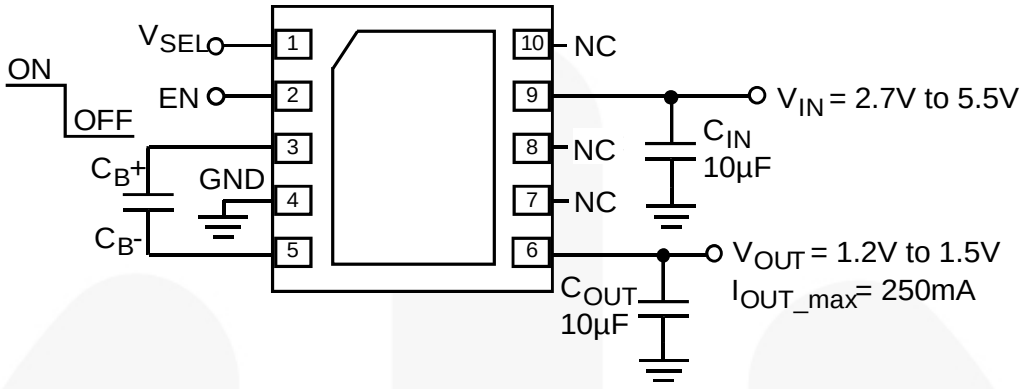
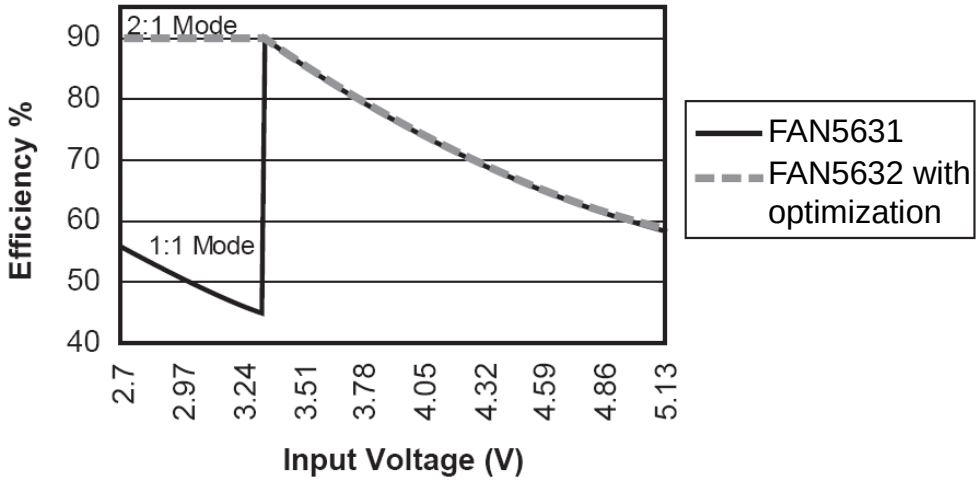


Figure 1. Typical Application



Average Efficiency (over V_{IN}=2.7V to 5V) = 66%, with optimization = 77%
Average Efficiency (over V_{IN}=2.7V to 4.2V) = 67%, with optimization = 84%

Figure 2. Typical Efficiency Graph

Pin Configuration

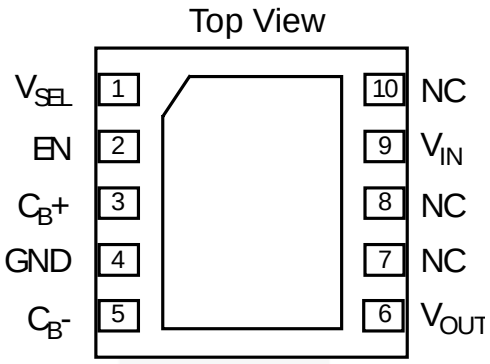


Figure 3. Pin Assignments

Pin Definitions

Pin #	Name	Description
1	V_{SEL}	**Output Voltage Select Logic Input Pin**. The V_{SEL} pin cannot be left floating and must be connected to either a logic high or logic low level. **FAN5631**: If a logic low is applied to the V_{SEL} pin, V_{OUT} is 1.2V; if a logic high is applied, V_{OUT} is 1.5V. **FAN5632**: If a logic low is applied to the V_{SEL} pin, the efficiency optimization mode is enabled and the output voltage accuracy is relaxed to meet optimum efficiency. If a logic high is applied, the device operates like a typical charge pump converter.
2	EN	**Enable Input Pin**. If a logic high is applied to the EN pin, the device is enabled. If a logic low is applied, the device is disabled and the supply current is reduced to less than 1µA. The EN pin cannot be left floating and must be connected to a logic high or logic low level.
3	C_B+	**Bucket Capacitor Positive Pin**.
4	GND	**Ground Pin**. This pin is connected to the internal MOSFET switches. This pin must be externally connected to GND.
5	C_B-	**Bucket Capacitor Negative Pin**.
6	V_{OUT}	**Output Voltage Pin**.
7	NC	**Not Connected**. This pin is not internally connected.
8	NC	**Not Connected**. This pin is not internally connected.
9	V_{IN}	**Supply Voltage Input**.
10	NC	**Not Connected**. This pin is not internally connected.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	V_{IN} to GND	-0.3	6.0	V
	All other pins to GND	-0.3	V_{IN} + 0.3	
I_{LOAD}	Load Current		0.5	A
Θ_{JC}	Thermal Resistance Junction-to-Tab(1)		8	°C/W
T_L	Lead Temperature, Soldering 10 Seconds		+260	°C
T_J	Junction Temperature	-40	+150	°C
T_{STG}	Storage Temperature	-65	+150	°C
ESD(2)	Human Body Model, JESD22-A114	2.5		kV
	Charged Device Model, JESD22-C101	0.2		

Notes:

1. Junction-to-ambient thermal resistance, $\theta_{JA,}$ is a strong function of PCB material, board thickness, thickness and number of copper planes, number of via used, diameter of via used, available copper surface, and attached heat sink characteristics. The estimated value for zero air flow at 0.5W is 60°C/W.
2. Using Mil Std. 883E, method 3015.7 (Human Body Model) and EIA/JESD22C101-A (Charged Device Model).

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Range	2.2		5.5	V
I_{OUT}	Output Current (V_{IN} > 2.V)			250	mA
T_A	Operating Ambient Temperature Range	-40	+25	+85	°C

Electrical Characteristic

V_{IN} = 2.2V to 5.5V, I_{OUT} = 1mA, C_{IN} = 10µF, C_{OUT} = 10µF, C_B = 1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{UVLO}	Input Under-voltage Lockout			2		V
	No-load Supply Current	No Switching			60	µA
V_{OUT}	Output Voltage	FAN5631, SEL to High		1.5		V
		FAN5631, SEL to Low		1.2		
		FAN5632, SEL to High		1.5		
		FAN5632, SEL to Low		Variable between 1.5 and 1.2		
	Output Voltage Accuracy	1mA ≤ I_{OUT} ≤ 150mA, V_{IN}=2.7V to 5.5V	-5		+5	%
R_{LOAD}	Load Regulation	0mA ≤ I_{OUT} ≤ 150mA, V_{IN}=3.6V		0.25		mV/mA
R_{LINE}	Line Regulation	I_{OUT}=0.1mA		0.2	4.0	mV/V
I_{SD}	Shutdown Supply Current	V_{EN}=0V		0.1	1.0	µA
I_{SC}	Output Short-circuit Current (3)	V_{OUT} ≤ 150mA		25		mA
	Peak Efficiency			90		%
	V_{IN} at Configuration Change	V_{IN} Decreasing		2.22xV_{OUT}		V
F_{OSC}	Oscillator Frequency			1.5		MHz
TSD	Thermal Shutdown Threshold			150		°C
TSD_{HYS}	Thermal Shutdown Threshold Hysteresis			15		°C
V_{IH}	Enable Logic Input High Voltage		1.3			V
V_{IL}	Enable Logic Input Low Voltage				0.4	V
I_{EN}	Enable Logic Input Current		-1		1	µA
V_{IH}	V_{SEL} Logic Input High Voltage		1.3			V
V_{IL}	V_{SEL} Logic Input Low Voltage				0.4	V
I_{IN}	V_{SEL} Logic Input Current		-1		1	µA
t_{ON}	V_{OUT} Turn-On Time			1.6		ms

Note:

3. The short-circuit protection is designed to protect against pre-existing short-circuit conditions, such as assembly shorts, that exist prior to device power-up. The short-circuit current limit is $25mA_{Average}$. Short-circuit currents in normal operation are inherently limited by the on resistance of the internal FET. Since this resistance is in the range of 1Ω, in some cases, thermal shutdown may occur. Immediately following the first thermal shutdown event, the short-circuit condition is treated as pre-existing and the load current reduces to $25mA_{Average}$.

Typical Performance Characteristics

T_A = 25°C, V_{OUT} = 1.5V, V_{IN} = 3.6V, C_{IN} = 10µF, C_{OUT} = 10µF, C_B = 1µF, unless otherwise noted.

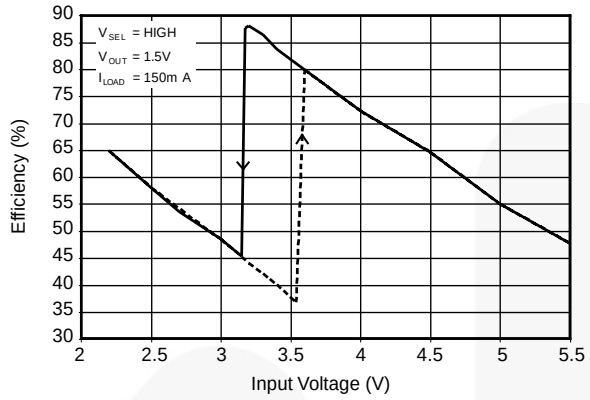


Figure 4. Efficiency vs. Input Voltage

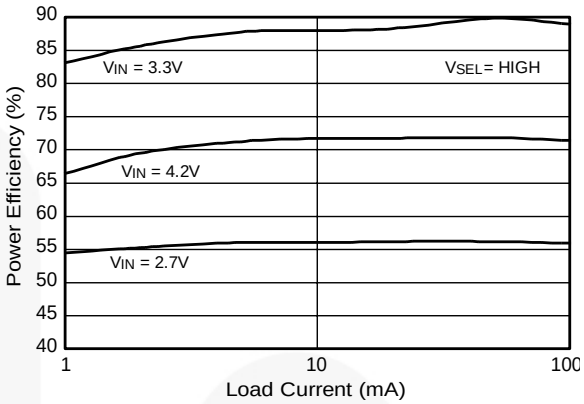


Figure 5. Efficiency vs. Load Current

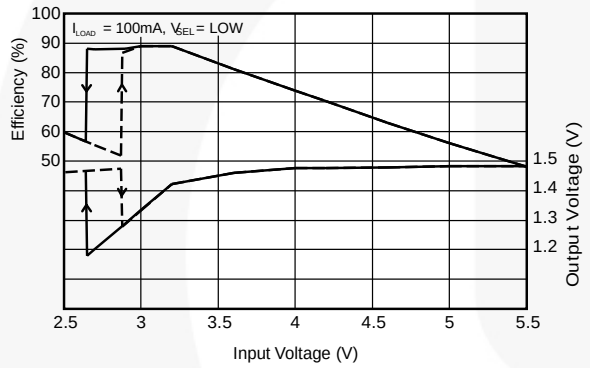


Figure 6. FAN5632 Efficiency Optimizer Efficiency and Output Voltage vs. Input Voltage

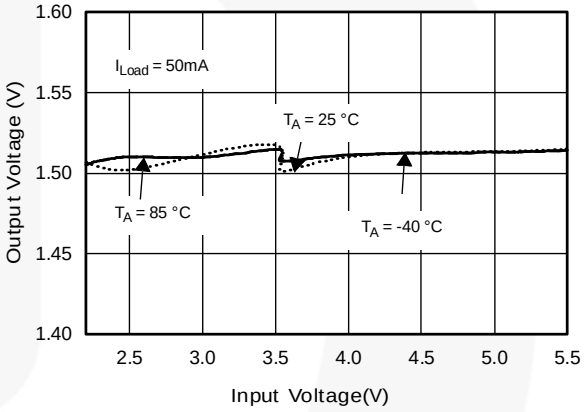


Figure 7. Line Regulation

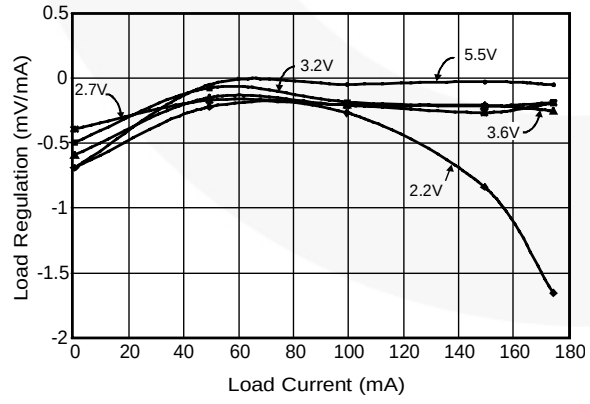


Figure 8. Load Regulation

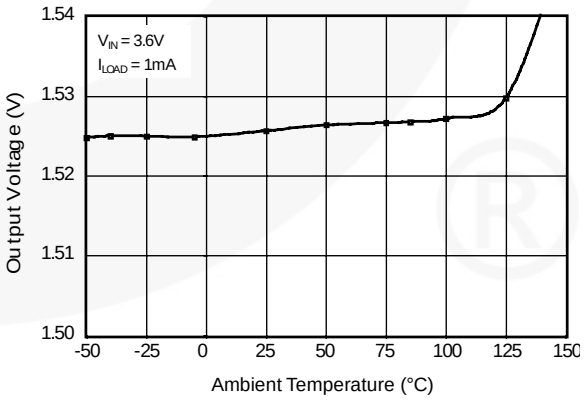


Figure 9. Thermal Regulation

Typical Performance Characteristics (Continued)

T_A = 25°C, V_{OUT} = 1.5V, V_{IN} = 3.6V, C_{IN} = 10µF, C_{OUT} = 10µF, C_B = 1µF, unless otherwise noted.

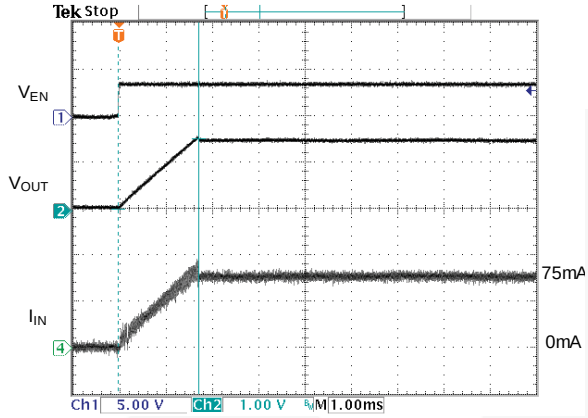


Figure 10. Start-Up

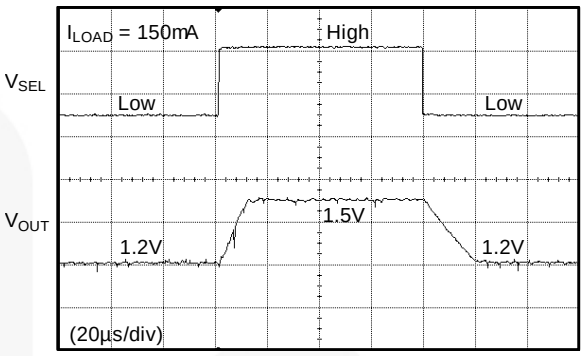


Figure 11. Dynamic V_{OUT} Change (FAN5631)

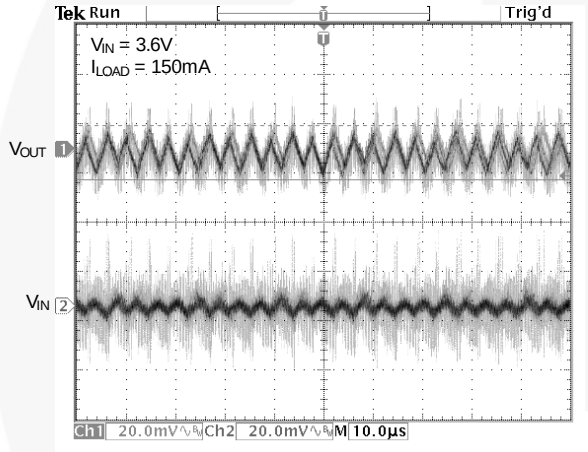


Figure 12. Voltage Ripple

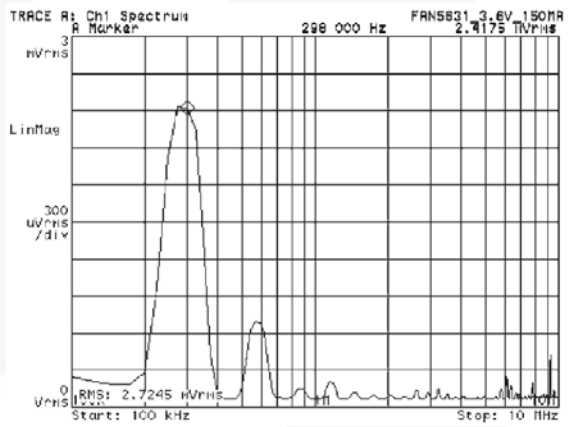


Figure 13. Output Voltage Ripple Spectrum

Block Diagram

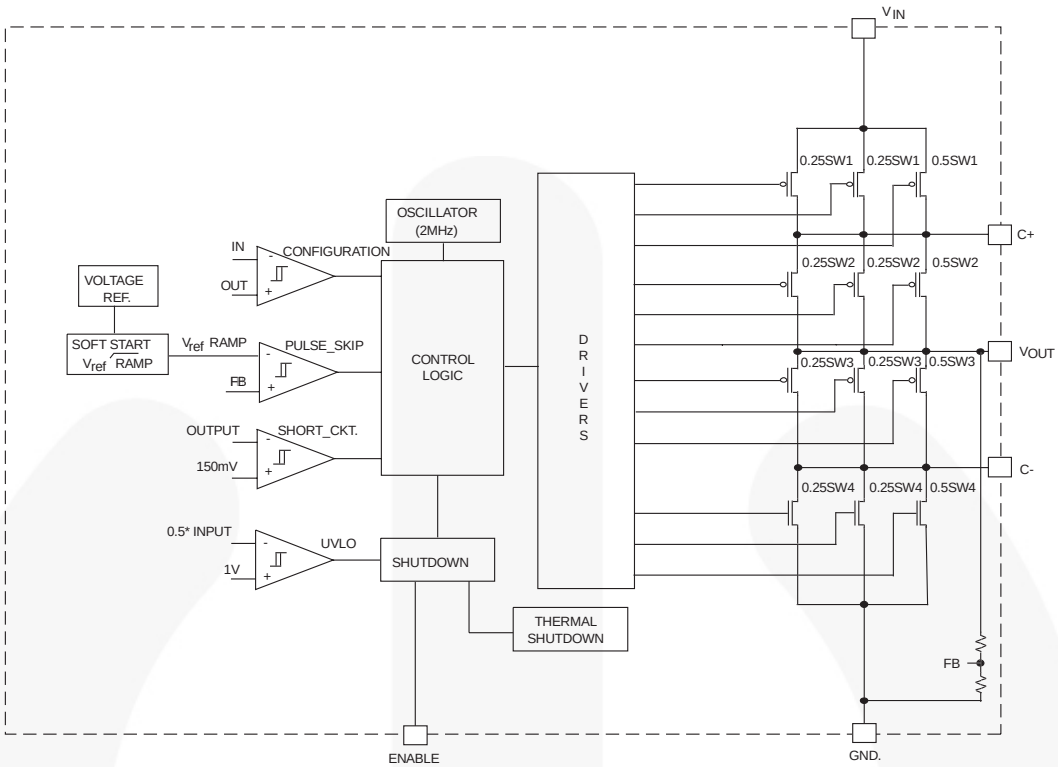


Figure 14. Block Diagram

Detailed Description

The FAN5631 / FAN5632 switched capacitor DC/DC converter automatically configures switches to achieve high efficiency and provides a regulated output voltage by means of pulse skipping, pulse frequency modulation (PFM). An internal soft-start circuit prevents excessive inrush current from the supply. Each switch is split into three segments. Based on the values of V_{IN}, V_{OUT}, and I_{OUT}; an internal circuit determines the number of segments used to reduce current spikes.

Step-Down Charge Pump Operation

When $V_{IN} \geq 2 \times V_{OUT}/9$, the 2:1 configuration shown in Figure 15 is enabled. The factor 0.9 is used instead of 1 to account for the effect of resistive losses across the switches and to accommodate hysteresis in the voltage detector comparator. Two-phase, non-overlapping clock signals are generated to drive four switches. When switches 1 and 3 are on, switches 2 and 4 are off and C_B is charged. When switches 2 and 4 are on, 1 and 3 are off and charge is transferred from C_B to C_{OUT}.

When $V_{IN} \geq 2 \times V_{OUT}/9$, the 1:1 configuration shown in Figure 16 is enabled. In the 1:1 configuration, switch 3 is always off and the switch 4 is always on. At 1.6V output setting, the configuration changes from 2:1 to 1:1 at V_{IN}=3.56V. At 1.3V output setting, the change occurs at V_{IN}=3.06V.

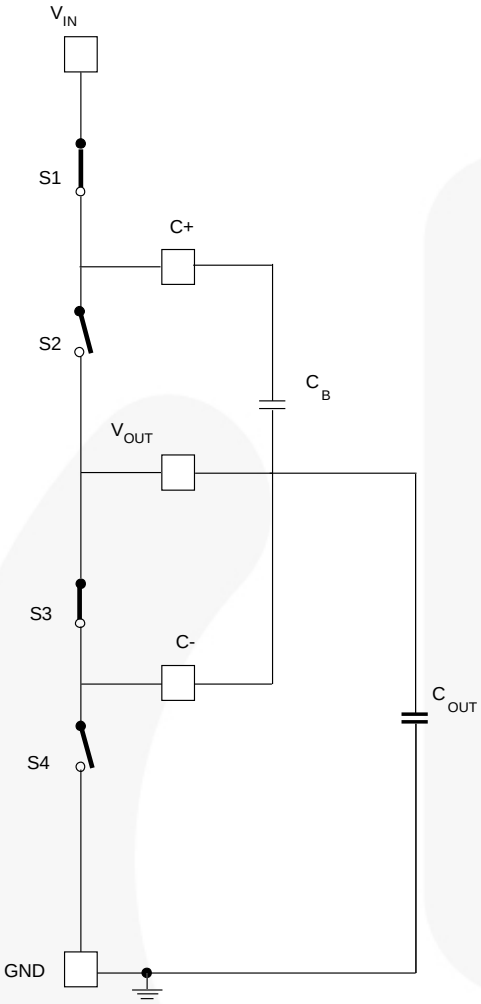
Pulse-skipping PFM and Fractional Switch Operation

When the regulated output voltage reaches its upper limit, the switches are turned off and the output voltage reaches its lower limit. In a step-down 2:1 mode of operation, with 1.6V output as an example; when the output reaches about 1.62V (upper limit), the control logic turns off all switches: switching stops completely. This is pulse-skipping mode. Since the supply is isolated from the output, the output voltage drops. Once the output is dropped to about 1.58V (lower limit), the device returns to regular switching mode with one quarter of each switch turning on first. Another quarter of each switch is turned on if V_{OUT} cannot reach regulation by the third charge cycle. Full switch operation occurs only during star-up or under heavy-load condition, when half switch operation cannot achieve regulation within seven charge cycles.

Soft-Start

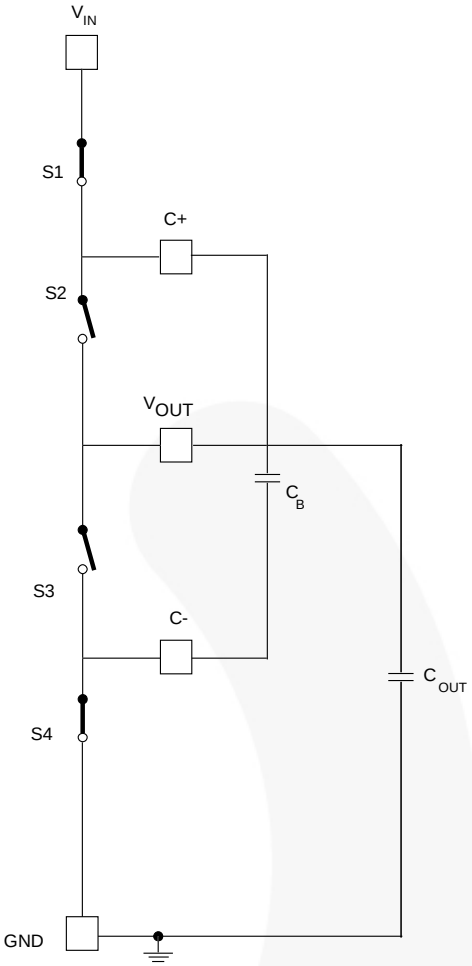
The soft-start feature limits inrush current when the device is initially powered up and enabled. The reference voltage is used to control the rate of the output voltage ramp-up to its final value. Typical start-up time is 1ms. Since the rate of the output voltage ramp-up is controlled by an internally generated slow ramp, pulse-skipping occurs and inrush current is automatically limited.

Switch Configuration



2:1 configuration
Switches in charging phase
Reverse all switches for pumping phase

Figure 15. 2:1 Configuration



1:1 configuration
Switch 3 is always off
Switch 4 is always on
Switches 1 and 2 are in phase 1
Reverse position of switches 1&2 for phase 2

Figure 16. 1:1 Configuration

Shutdown, UVLO, Short-Circuit, Current-Limit and Thermal Shutdown

The device has an active-low shutdown pin to decrease supply current to less than 1μA. In shutdown mode, the supply is disconnected from the output. UVLO triggers when supply voltage drops below 2V. When the output voltage is lower than 150mV, a short-circuit protection is triggered. In this mode, 15 out of 16 pulses during the switching are skipped and the supply current is limited. Thermal shutdown triggers at 150ºC.

Efficiency Optimizer (FAN5632)

In the FAN5632, V_{SEL} can be tied to ground to enable the efficiency optimizer feature. To achieve an optimized efficiency, the switch mode configuration transition point is shifted from a 2:1 to a 1:1 mode until the output voltage falls to 20% of its nominal value. For example, when the nominal output voltage is 1.5V, the output voltage is allowed to drop to 1.2V. This maintains a peak efficiency of 85% for the input voltage range of 2.9V to 3.5V. For normal operation, tie V_{SEL} high.

Applications Information

The FAN5631/FAN5632 requires one ceramic bucket capacitor in the 0.1µF to 1µF range, one 10µF output bypass capacitor, and one 10µF input bypass capacitor. To obtain optimum output ripple and noise performance, low-ESR (<0.05Ω) ceramic input and output bypass capacitors are recommended. X5R- and X7R-rated capacitors provide adequate performance over the -40°C to 85°C temperature range.

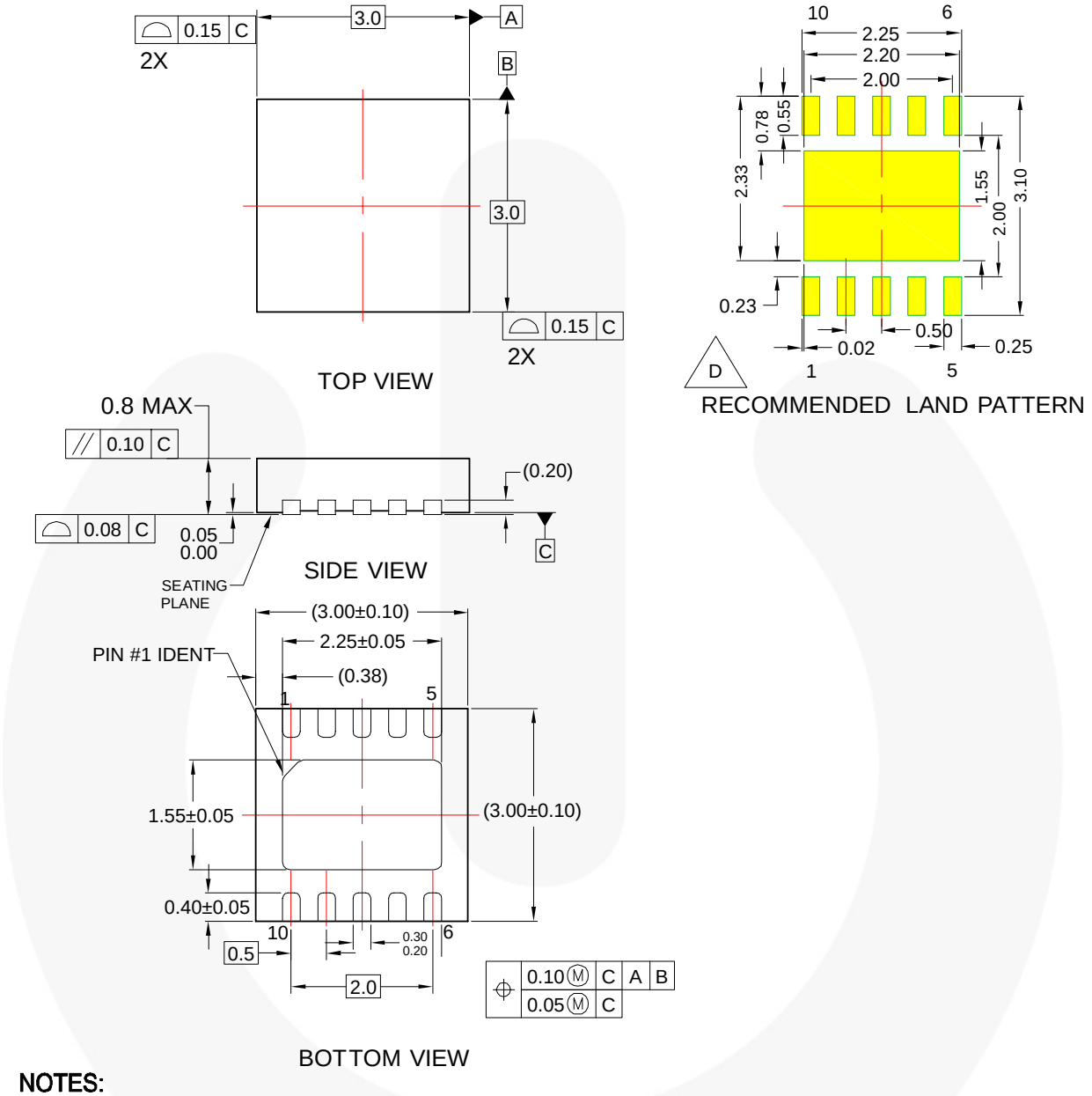
The bucket capacitor's value is dependent on load current requirements. A 1µF bucket capacitor works well in all applications at all load currents, while a 0.1µF capacitor supports most applications under 100mA of load current. The choice of bucket capacitor values should be verified in the actual application at the lowest input voltage and highest load current. A 30% margin of safety is recommended to account for the tolerance of the bucket capacitor and the variations in the on-resistance of the internal switches.

One of the key benefits of the ScalarPump architecture is that the dynamically scaled on resistance of the switches effectively reduces the peak current in the bucket capacitor and therefore input and output ripple currents are also reduced. Nevertheless, due to the ESR of the input and output bypass capacitors, these current spikes generate voltage spikes at the input and output pins. These ESR spikes can be filtered because their frequencies lie at up to 12 times the clock frequencies. In applications where conductive and radiated EMI/RFI interference must be low as possible, consider additional input and output filtering.

Layout Considerations

While evaluating any switched capacitor DC-DC converter, be careful to keep the power supply source impedance low; use of long wires causing high lead inductances and resistive losses should be avoided. A carefully laid-out ground plane is essential because current spikes are generated as the bucket capacitor is charged and discharged. The input and output bypass capacitors should be placed as close to the device pins as possible.

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION WEED-5

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. LAND PATTERN DIMENSIONS ARE NOMINAL REFERENCE VALUES ONLY

MLP10BrevA

Figure 17. 10-lead, Molded Leadless Package (MLP)

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