



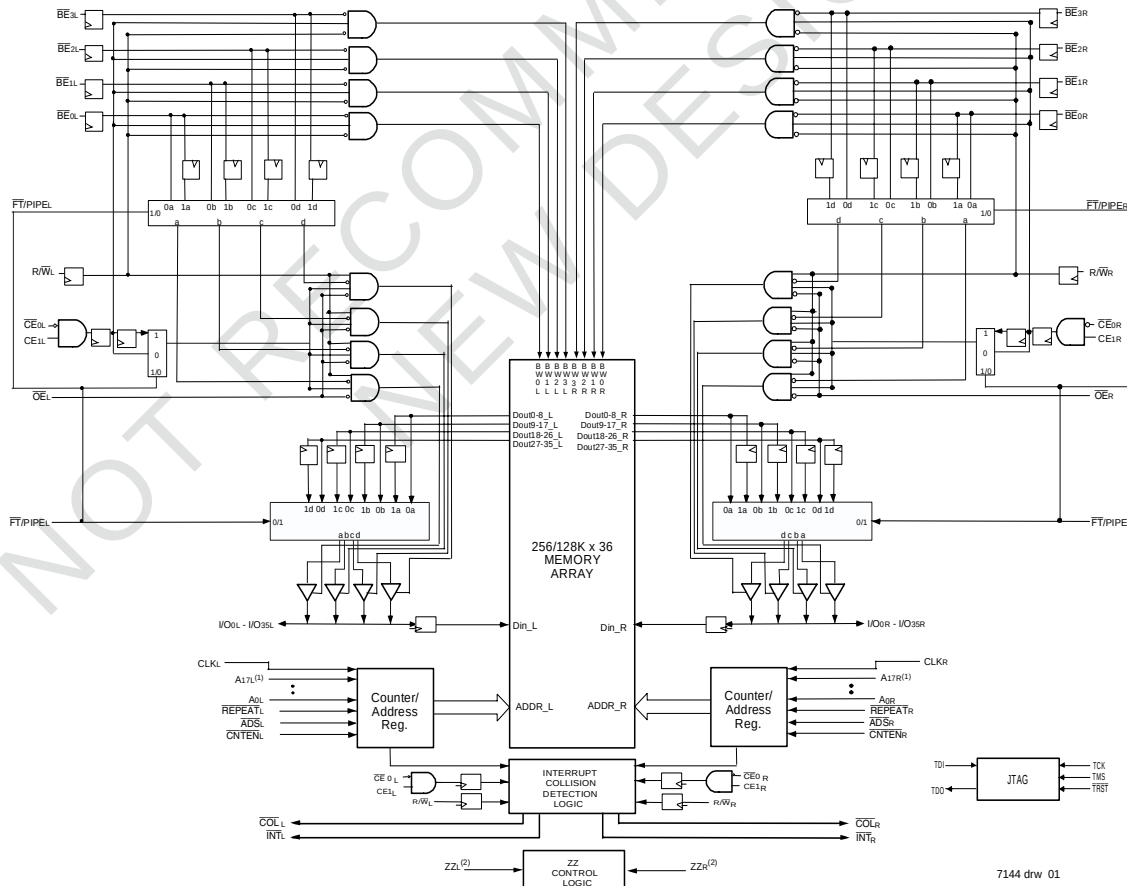
HIGH-SPEED 1.8V 256/128K x 36 SYNCHRONOUS DUAL-PORT STATIC RAM WITH 3.3V/2.5V/1.8V INTERFACE

IDT70P3519/99

Features:

- ♦ True Dual-Port memory cells which allow simultaneous access of the same memory location
- ♦ Low Power
- ♦ High-speed data access
 - Commercial: 3.4 (200MHz)/3.6ns (166MHz)
 - Industrial: 3.6ns (166MHz)
- ♦ Selectable Pipelined or Flow-Through output mode
- ♦ Dual chip enables allow for depth expansion without additional logic
- ♦ Full synchronous operation on both ports
 - 5ns cycle time, 200MHz operation (14Gbps bandwidth)
 - Fast 3.4ns clock to data out
 - 1.5ns setup to clock and 0.5ns hold on all control, data, and address inputs @ 200MHz
 - Data input, address, byte enable and control registers
 - Self-timed write allows fast cycle time
- ♦ Counter enable and repeat features
- ♦ Interrupt and Collision Detection Flags
- ♦ Separate byte controls for multiplexed bus and bus matching compatibility
- ♦ Dual Cycle Deselect (DCD) for Pipelined Output Mode
- ♦ 1.8V ($\pm 100\text{mV}$) power supply for core
- ♦ LVTTTL compatible, 1.8V to 3.3V power supply for I/Os and control signals on each port
- ♦ Industrial temperature range (-40°C to $+85^{\circ}\text{C}$) is available at 166MHz
- ♦ Available in a 256-pin Ball Grid Array (BGA) and 208-pin fine pitch Ball Grid Array (fpBGA)
- ♦ Supports JTAG features compliant with IEEE 1149.1
- ♦ Green parts available, see ordering information

Functional Block Diagram



NOTES:

1. Address A17 is a NC for the IDT70P3599.
- +. The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. All static inputs, i.e., PL/FTx and the sleep mode pins themselves (ZZx) are not affected during sleep mode.

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JUNE 2009

Description:

The IDT70P3519/99 is a high-speed 256/128K x 36 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70P3519/99 has been optimized for applications having unidirectional

or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}_0$ and CE_1 , permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70P3519/99 can support an operating voltage of 3.3V, 2.5V or 1.8V on one or both ports. The power supply for the core of the device (V_{DD}) is 1.8V.

NOT RECOMMENDED FOR
NEW DESIGNS

Pin Configuration (2,3,4)

70P3519/99BC

BC-256⁽⁵⁾

256-Pin BGA

Top View⁽⁶⁾

02/12/08

A1 NC	A2 TDI	A3 NC	A4 A17L ⁽¹⁾	A5 A14L	A6 A11L	A7 A8L	A8 BE ₂ L	A9 CE ₁ L	A10 OE _L	A11 CNTEN _L	A12 A5L	A13 A2L	A14 A0L	A15 NC	A16 NC
B1 I/O18L	B2 NC	B3 TDO	B4 NC	B5 A15L	B6 A12L	B7 A9L	B8 BE ₃ L	B9 CE ₀ L	B10 R/W _L	B11 REPEAT _L	B12 A4L	B13 A1L	B14 VDD	B15 I/O17L	B16 NC
C1 I/O18R	C2 I/O19L	C3 VSS	C4 A16L	C5 A13L	C6 A10L	C7 A7L	C8 BE ₁ L	C9 BE ₀ L	C10 CLK _L	C11 ADS _L	C12 A6L	C13 A3L	C14 NC	C15 I/O17R	C16 I/O16L
D1 I/O20R	D2 I/O19R	D3 I/O20L	D4 PIPE/FTL	D5 VDDQL	D6 VDDQL	D7 VDDQR	D8 VDDQR	D9 VDDQL	D10 VDDQL	D11 VDDQR	D12 VDDQR	D13 VDD	D14 I/O15R	D15 I/O15L	D16 I/O16R
E1 I/O21R	E2 I/O21L	E3 I/O22L	E4 VDDQL	E5 VDD	E6 VDD	E7 INT _L	E8 VSS	E9 VSS	E10 VSS	E11 VDD	E12 VDD	E13 VDDQR	E14 I/O13L	E15 I/O14L	E16 I/O14R
F1 I/O23L	F2 I/O22R	F3 I/O23R	F4 VDDQL	F5 VDD	F6 NC	F7 COL _L	F8 VSS	F9 VSS	F10 VSS	F11 VSS	F12 VDD	F13 VDDQR	F14 I/O12R	F15 I/O13R	F16 I/O12L
G1 I/O24R	G2 I/O24L	G3 I/O25L	G4 VDDQR	G5 VSS	G6 VSS	G7 VSS	G8 VSS	G9 VSS	G10 VSS	G11 VSS	G12 VSS	G13 VDDQL	G14 I/O10L	G15 I/O11L	G16 I/O11R
H1 I/O26L	H2 I/O25R	H3 I/O26R	H4 VDDQR	H5 VSS	H6 VSS	H7 VSS	H8 VSS	H9 VSS	H10 VSS	H11 VSS	H12 VSS	H13 VDDQL	H14 I/O9R	H15 I/O9L	H16 I/O10R
J1 I/O27L	J2 I/O28R	J3 I/O27R	J4 VDDQL	J5 ZZR	J6 VSS	J7 VSS	J8 VSS	J9 VSS	J10 VSS	J11 VSS	J12 ZZL	J13 VDDQR	J14 I/O8R	J15 I/O7R	J16 I/O8L
K1 I/O29R	K2 I/O29L	K3 I/O28L	K4 VDDQL	K5 VSS	K6 VSS	K7 VSS	K8 VSS	K9 VSS	K10 VSS	K11 VSS	K12 VSS	K13 VDDQR	K14 I/O6R	K15 I/O6L	K16 I/O7L
L1 I/O30L	L2 I/O31R	L3 I/O30R	L4 VDDQR	L5 VDD	L6 NC	L7 COL _R	L8 VSS	L9 VSS	L10 VSS	L11 VSS	L12 VDD	L13 VDDQL	L14 I/O5L	L15 I/O4R	L16 I/O5R
M1 I/O32R	M2 I/O32L	M3 I/O31L	M4 VDDQR	M5 VDD	M6 VDD	M7 INT _R	M8 VSS	M9 VSS	M10 VSS	M11 VDD	M12 VDD	M13 VDDQL	M14 I/O3R	M15 I/O3L	M16 I/O4L
N1 I/O33L	N2 I/O34R	N3 I/O33R	N4 PIPE/FTL	N5 VDDQR	N6 VDDQR	N7 VDDQL	N8 VDDQL	N9 VDDQR	N10 VDDQR	N11 VDDQL	N12 VDDQL	N13 VDD	N14 I/O2L	N15 I/O1R	N16 I/O2R
P1 I/O35R	P2 I/O34L	P3 TMS	P4 A16R	P5 A13R	P6 A10R	P7 A7R	P8 BE ₁ R	P9 BE ₀ R	P10 CLK _R	P11 ADS _R	P12 A6R	P13 A3R	P14 I/O0L	P15 I/O0R	P16 I/O1L
R1 I/O35L	R2 NC	R3 TRST	R4 NC	R5 A15R	R6 A12R	R7 A9R	R8 BE ₃ R	R9 CE ₀ R	R10 R/W _R	R11 REPEAT _R	R12 A4R	R13 A1R	R14 NC	R15 NC	R16 NC
T1 NC	T2 TCK	T3 NC	T4 A17R ⁽¹⁾	T5 A14R	T6 A11R	T7 A8R	T8 BE ₂ R	T9 CE ₁ R	T10 OE _R	T11 CNTEN _R	T12 A5R	T13 A2R	T14 A0R	T15 NC	T16 NC

NOTES:

1. Pin is a NC for IDT70P3599.
2. All VDD pins must be connected to 1.8V power supply.
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

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Pin Configuration (2,3,4) (con't.)

02/12/08

A1 I/O19L	A2 I/O18L	A3 VSS	A4 TDO	A5 COL	A6 A16L	A7 A12L	A8 A8L	A9 BE1L	A10 VDD	A11 CLKL	A12 CNTENL	A13 A4L	A14 A0L	A15 NC	A16 I/O17L	A17 VSS
B1 I/O20R	B2 VSS	B3 I/O18R	B4 TDI	B5 A17L ⁽¹⁾	B6 A13L	B7 A9L	B8 BE2L	B9 CE0L	B10 VSS	B11 ADSL	B12 A5L	B13 A1L	B14 NC	B15 VDDQR	B16 I/O16L	B17 I/O15R
C1 VDDQL	C2 I/O19R	C3 VDDQR	C4 PL/FTL	C5 INTL	C6 A14L	C7 A10L	C8 BE3L	C9 CE1L	C10 VSS	C11 R/WL	C12 A6L	C13 A2L	C14 VDD	C15 I/O16R	C16 I/O15L	C17 VSS
D1 I/O22L	D2 VSS	D3 I/O21L	D4 I/O20L	D5 A15L	D6 A11L	D7 A7L	D8 BE0L	D9 VDD	D10 OE	D11 REPEATL	D12 A3L	D13 VDD	D14 I/O17R	D15 VDDQL	D16 I/O14L	D17 I/O14R
E1 I/O23L	E2 I/O22R	E3 VDDQR	E4 I/O21R	70P3519/99BF BF-208⁽⁵⁾ 208-Pin fpBGA Top View⁽⁶⁾									E14 I/O12L	E15 I/O13R	E16 VSS	E17 I/O13L
F1 VDDQL	F2 I/O23R	F3 I/O24L	F4 VSS										F14 VSS	F15 I/O12R	F16 I/O11L	F17 VDDQR
G1 I/O26L	G2 VSS	G3 I/O25L	G4 I/O24R										G14 I/O9L	G15 VDDQL	G16 I/O10L	G17 I/O11R
H1 VDD	H2 I/O26R	H3 VDDQR	H4 I/O25R										H14 VDD	H15 I/O9R	H16 VSS	H17 I/O10R
J1 VDDQL	J2 VDD	J3 VSS	J4 ZZR										J14 ZZL	J15 VDD	J16 VSS	J17 VDDQR
K1 I/O28R	K2 VSS	K3 I/O27R	K4 VSS										K14 I/O7R	K15 VDDQL	K16 I/O8R	K17 VSS
L1 I/O29R	L2 I/O28L	L3 VDDQR	L4 I/O27L										L14 I/O6R	L15 I/O7L	L16 VSS	L17 I/O8L
M1 VDDQL	M2 I/O29L	M3 I/O30R	M4 VSS										M14 VSS	M15 I/O6L	M16 I/O5R	M17 VDDQR
N1 I/O31L	N2 VSS	N3 I/O31R	N4 I/O30L										N14 I/O3R	N15 VDDQL	N16 I/O4R	N17 I/O5L
P1 I/O32R	P2 I/O32L	P3 VDDQR	P4 I/O35R	P5 TRST	P6 A16R	P7 A12R	P8 A8R	P9 BE1R	P10 VDD	P11 CLKR	P12 CNTENR	P13 A4R	P14 I/O2L	P15 I/O3L	P16 VSS	P17 I/O4L
R1 VSS	R2 I/O33L	R3 I/O34R	R4 TCK	R5 A17R ⁽¹⁾	R6 A13R	R7 A9R	R8 BE2R	R9 CE0R	R10 VSS	R11 ADSR	R12 A5R	R13 A1R	R14 NC	R15 VDDQL	R16 I/O1R	R17 VDDQR
T1 I/O33R	T2 I/O34L	T3 VDDQL	T4 TMS	T5 INTR	T6 A14R	T7 A10R	T8 BE3R	T9 CE1R	T10 VSS	T11 R/WR	T12 A6R	T13 A2R	T14 VSS	T15 I/O0R	T16 VSS	T17 I/O2R
U1 VSS	U2 I/O35L	U3 PL/FTR	U4 COLR	U5 A15R	U6 A11R	U7 A7R	U8 BE0R	U9 VDD	U10 OE	U11 REPEATR	U12 A3R	U13 A0R	U14 VDD	U15 NC	U16 I/O0L	U17 I/O1L

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NOTES:

1. Pin is a NC for IDT70P3599.
2. All VDD pins must be connected to 1.8V power supply.
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 15mm x 15mm x 1.4mm with 0.8mm ball pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables (Input) ⁽⁵⁾
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable (Input)
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable (Input)
A_{0L} - $A_{17L}^{(4)}$	A_{0R} - $A_{17R}^{(4)}$	Address (Input)
I/O_{0L} - I/O_{35L}	I/O_{0R} - I/O_{35R}	Data Input/Output
CLK_L	CLK_R	Clock (Input)
$PL/\overline{FT}_L$	$PL/\overline{FT}_R$	Pipeline/Flow-Through (Input)
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable (Input)
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable (Input)
$\overline{REPEAT}_L$	$\overline{REPEAT}_R$	Counter Repeat ⁽²⁾
$\overline{BE}_{0L}$ - $\overline{BE}_{3L}$	$\overline{BE}_{0R}$ - $\overline{BE}_{3R}$	Byte Enables (9-bit bytes) (Input) ⁽⁵⁾
V_{DDQL}	V_{DDQR}	Power (I/O Bus) (3.3V, 2.5V or 1.8V) ⁽¹⁾ (Input)
ZZ_L	ZZ_R	Sleep Mode pin ⁽³⁾ (Input)
V_{DD}		Power (1.8V) ⁽¹⁾ (Input)
V_{SS}		Ground (0V) (Input)
TDI		Test Data Input
TDO		Test Data Output
TCK		Test Logic Clock (10MHz) (Input)
TMS		Test Mode Select (Input)
$\overline{TRST}$		Reset (Initialize TAP Controller) (Input)
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag (Output)
$\overline{COL}_L$	$\overline{COL}_R$	Collision Alert (Output)

7144 tbl 01

NOTES:

- V_{DD} and V_{DDQX} must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
- When $\overline{REPEAT}_x$ is asserted, the counter will reset to the last valid address loaded via $\overline{ADS}_x$.
- The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. All static inputs, i.e., $PL/\overline{FT}_x$ and the sleep mode pins themselves (ZZ_x) are not affected during sleep mode.
- Address A_{17x} is a NC for the IDT70P3599.
- Chip Enables and Byte Enables are double buffered when $PL/\overline{FT} = V_{IH}$, i.e., the signals take two cycles to deselect.

Truth Table I—Read/Write and Enable Control^(1,2,3,4)

$\overline{OE}$	CLK	$\overline{CE}_0$	CE_1	$\overline{BE}_3$	$\overline{BE}_2$	$\overline{BE}_1$	$\overline{BE}_0$	R/ $\overline{W}$	ZZ	Byte 3 I/O ₂₇₋₃₅	Byte 2 I/O ₁₈₋₂₆	Byte 1 I/O ₉₋₁₇	Byte 0 I/O ₀₋₈	MODE
X	↑	H	X	X	X	X	X	X	L	High-Z	High-Z	High-Z	High-Z	Deselected—Power Down
X	↑	X	L	X	X	X	X	X	L	High-Z	High-Z	High-Z	High-Z	Deselected—Power Down
X	↑	L	H	H	H	H	H	X	L	High-Z	High-Z	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	H	H	L	L	L	High-Z	High-Z	High-Z	D _{IN}	Write to Byte 0 Only
X	↑	L	H	H	H	L	H	L	L	High-Z	High-Z	D _{IN}	High-Z	Write to Byte 1 Only
X	↑	L	H	H	L	H	H	L	L	High-Z	D _{IN}	High-Z	High-Z	Write to Byte 2 Only
X	↑	L	H	L	H	H	H	L	L	D _{IN}	High-Z	High-Z	High-Z	Write to Byte 3 Only
X	↑	L	H	H	H	L	L	L	L	High-Z	High-Z	D _{IN}	D _{IN}	Write to Lower 2 Bytes Only
X	↑	L	H	L	L	H	H	L	L	D _{IN}	D _{IN}	High-Z	High-Z	Write to Upper 2 bytes Only
X	↑	L	H	L	L	L	L	L	L	D _{IN}	D _{IN}	D _{IN}	D _{IN}	Write to All Bytes
L	↑	L	H	H	H	H	L	H	L	High-Z	High-Z	High-Z	D _{OUT}	Read Byte 0 Only
L	↑	L	H	H	H	L	H	H	L	High-Z	High-Z	D _{OUT}	High-Z	Read Byte 1 Only
L	↑	L	H	H	L	H	H	H	L	High-Z	D _{OUT}	High-Z	High-Z	Read Byte 2 Only
L	↑	L	H	L	H	H	H	H	L	D _{OUT}	High-Z	High-Z	High-Z	Read Byte 3 Only
L	↑	L	H	H	H	L	L	H	L	High-Z	High-Z	D _{OUT}	D _{OUT}	Read Lower 2 Bytes Only
L	↑	L	H	L	L	H	H	H	L	D _{OUT}	D _{OUT}	High-Z	High-Z	Read Upper 2 Bytes Only
L	↑	L	H	L	L	L	L	H	L	D _{OUT}	D _{OUT}	D _{OUT}	D _{OUT}	Read All Bytes
H	↑	X	X	X	X	X	X	X	L	High-Z	High-Z	High-Z	High-Z	Outputs Disabled
X	X	X	X	X	X	X	X	X	H	High-Z	High-Z	High-Z	High-Z	Sleep Mode

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- $\overline{ADS}$, $\overline{CNTEN}$, $\overline{REPEAT}$ = X.
- $\overline{OE}$ and ZZ are asynchronous input signals.
- It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

7144 tbl 02

Truth Table II—Address Counter Control^(1,2)

Address	Previous Internal Address	Internal Address Used	CLK	$\overline{ADS}^{(4)}$	$\overline{CNTEN}^{(5)}$	$\overline{REPEAT}^{(4,6)}$	I/O ⁽³⁾	MODE
An	X	An	↑	L	X	H	D _{IO} (n)	External Address Used
X	An	An + 1	↑	H	L	H	D _{IO} (n+1)	Counter Enabled—Internal Address generation
X	An + 1	An + 1	↑	H	H	H	D _{IO} (n+1)	External Address Blocked—Counter disabled (An + 1 reused)
X	X	An	↑	X	X	L	D _{IO} (n)	Counter Set to last valid $\overline{ADS}$ load

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- Read and write operations are controlled by the appropriate setting of R/ $\overline{W}$, $\overline{CE}_0$, CE_1 , $\overline{BE}_n$ and $\overline{OE}$.
- Outputs configured in flow-through output mode: if outputs are in pipelined mode the data out will be delayed by one cycle.
- $\overline{ADS}$ and $\overline{REPEAT}$ are independent of all other memory control signals including $\overline{CE}_0$, CE_1 and $\overline{BE}_n$.
- The address counter advances if $\overline{CNTEN}$ = V_{IL} on the rising edge of CLK, regardless of all other memory control signals including $\overline{CE}_0$, CE_1 , $\overline{BE}_n$.
- When $\overline{REPEAT}$ is asserted, the counter will reset to the last valid address loaded via $\overline{ADS}$. This value is not set at power-up: a known location should be loaded via $\overline{ADS}$ during initialization if desired. Any subsequent $\overline{ADS}$ access during operations will update the $\overline{REPEAT}$ address location.

7144 tbl 03

Recommended Operating Temperature and Supply Voltage⁽¹⁾

Grade	Ambient Temperature	GND	V _{DD}
Commercial	0°C to +70°C	0V	1.8V $\pm$ 100mV
Industrial	-40°C to +85°C	0V	1.8V $\pm$ 100mV

NOTES:

7144 tbl 04

1. This is the parameter TA. This is the "instant on" case temperature.

Recommended DC Operating Conditions with V_{DDQ} at 1.8V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	1.7	1.8	1.9	V
V _{DDQ}	I/O Supply Voltage	1.7	1.8	1.9	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	0.7 V _{DDQ}	—	V _{DDQ} + 100mV ⁽²⁾	V
V _{IH}	Input High Voltage - JTAG ⁽³⁾	0.7 V _{DDQL}	—	V _{DDQL} + 100mV ⁽²⁾	V
V _{IH}	Input High Voltage - ZZ, PIPE/ $\overline{FT}$	V _{DDQ} - 0.2V	—	V _{DDQ} + 100mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.3 V _{DDQ}	V
V _{IL}	Input Low Voltage - ZZ, PIPE/ $\overline{FT}$	-0.3 ⁽¹⁾	—	0.2	V

7144 tbl 05c

NOTES:

1. V_{IL} (min.) = -0.75V for pulse width less than tc_{yc}/2, or 5ns, whichever is less.
2. V_{IH} (max.) = V_{DDQ} + 0.75V for pulse width less than tc_{yc}/2 or 5ns, whichever is less.
3. JTAG is driven by the left port V_{DDQL}.

Recommended DC Operating Conditions with V_{DDQ} at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	1.7	1.8	1.9	V
V _{DDQ}	I/O Supply Voltage	2.4	2.5	2.6	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	1.7	—	V _{DDQ} + 100mV ⁽²⁾	V
V _{IH}	Input High Voltage - JTAG ⁽³⁾	1.7	—	V _{DDQL} + 100mV ⁽²⁾	V
V _{IH}	Input High Voltage - ZZ, PIPE/ $\overline{FT}$	V _{DDQ} - 0.2V	—	V _{DDQ} + 100mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.7	V
V _{IL}	Input Low Voltage - ZZ, PIPE/ $\overline{FT}$	-0.3 ⁽¹⁾	—	0.2	V

7144 tbl 05a

NOTES:

1. V_{IL} (min.) = -1.0V for pulse width less than tc_{yc}/2 or 5ns, whichever is less.
2. V_{IH} (max.) = V_{DDQ} + 1.0V for pulse width less than tc_{yc}/2 or 5ns, whichever is less.
3. JTAG is driven by the left port V_{DDQL}.

Recommended DC Operating Conditions with V_{DDQ} at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	1.7	1.8	1.9	V
V _{DDQ}	I/O Supply Voltage	3.15	3.3	3.45	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.0	—	V _{DDQ} + 150mV ⁽²⁾	V
V _{IH}	Input High Voltage - JTAG ⁽³⁾	2.0	—	V _{DDQL} + 150mV ⁽²⁾	V
V _{IH}	Input High Voltage - ZZ, PIPE/FT	V _{DDQ} - 0.2V	—	V _{DDQ} + 150mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V
V _{IL}	Input Low Voltage - ZZ, PIPE/FT	-0.3 ⁽¹⁾	—	0.2	V

NOTES:

7144 tbl 05b

1. V_{IL} (min.) = -1.0V for pulse width less than tcyc/2, or 5ns, whichever is less.
2. V_{IH} (max.) = V_{DDQ} + 1.0V for pulse width less than tcyc/2 or 5ns, whichever is less.
3. JTAG is driven by the left port V_{DDQL}.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
V _{TERM} (V _{DD})	V _{DD} Terminal Voltage with Respect to GND	- 0.5 to + 2.5	V
V _{TERM} ⁽²⁾ (V _{DDQ})	V _{DDQ} Terminal Voltage with Respect to GND	- 0.3 to + 4.2	V
V _{TERM} ⁽²⁾ (INPUTS and I/O's)	Input and I/O Terminal Voltage with Respect to GND	- 0.3 to min. {V _{DDQ} + 0.3, 4.2} ⁽⁴⁾	V
T _{BIAS} ⁽³⁾	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
T _{JN}	Junction Temperature	+150	°C
I _{OUT} (For V _{DDQ} = 3.3V)	DC Output Current	50	mA
I _{OUT} (For V _{DDQ} = 2.5V)	DC Output Current	40	mA
I _{OUT} (For V _{DDQ} = 1.8V)	DC Output Current	35	mA

7144 tbl 06

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any Input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
3. Ambient Temperature under DC Bias. No AC Conditions. Chip Deselected.
4. V_{TERM} (Inputs and I/O's) -0.3 to min {V_{DDQ} + 0.3, 4.2} means that the range is -0.3V to either V_{DDQ} +0.3V or 4.2V whichever is less.

Capacitance⁽¹⁾

(TA = +25°C, F = 1.0MHz)

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	8	pF
C _{OUT} ⁽³⁾	Output Capacitance	V _{OUT} = 3dV	10.5	pF

7144 tbl 07

NOTES:

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- C_{OUT} also references C_{I/O}.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 1.8V ± 100mV)

Symbol	Parameter	Test Conditions	70P3519/99S		Unit
			Min.	Max.	
I _{LI}	Input Leakage Current	V _{DDQ} = Max., V _{IN} = 0V to V _{DDQ}	—	10	μA
I _{LI}	JTAG & ZZ Input Leakage Current ⁽¹⁾	V _{DDQL} = Max., V _{IN} = 0V to V _{DDQL}	—	30	μA
I _{LO}	Output Leakage Current ⁽²⁾	$\overline{CE}_0 = V_{IH}$ or CE ₁ = V _{IL} , V _{OUT} = 0V to V _{DDQ}	—	10	μA
V _{OL} (3.3V)	Output Low Voltage	I _{OL} = +4mA, V _{DDQ} = Min.	—	0.4	V
V _{OH} (3.3V)	Output High Voltage	I _{OH} = -4mA, V _{DDQ} = Min.	2.4	—	V
V _{OL} (2.5V)	Output Low Voltage	I _{OL} = +2mA, V _{DDQ} = Min.	—	0.4	V
V _{OH} (2.5V)	Output High Voltage	I _{OH} = -2mA, V _{DDQ} = Min.	2.0	—	V
V _{OL} (1.8V)	Output Low Voltage	I _{OL} = +2mA, V _{DDQ} = Min.	—	0.4	V
V _{OH} (1.8V)	Output High Voltage	I _{OH} = -2mA, V _{DDQ} = Min.	V _{DDQ} - 0.40	—	V

7144 tbl 08

NOTES:

- Applicable only for TMS, TDI and $\overline{TRST}$ inputs.
- Outputs tested in tri-state mode.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽³⁾ ($V_{DD} = 1.8V \pm 100mV$)

Symbol	Parameter	Test Condition	Version	70P3519/99 S200 Com'l Only		70P3519/99 S166 Com'l & Ind		Unit
				Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	
IDD	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R = V_{IL}$, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L S	226	325	190	285	mA
			IND S	—	—	190	325	
ISB1 ⁽⁶⁾	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L S	120	195	102	170	mA
			IND S	—	—	102	205	
ISB2 ⁽⁶⁾	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^*A = V_{IL}$ and $\overline{CE}^*B = V_{IH}^{(5)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L S	176	265	148	230	mA
			IND S	—	—	148	270	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DDQ} - 0.2V$, $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(2)}$	COM'L S	15	45	15	45	mA
			IND S	—	—	15	60	
ISB4 ⁽⁶⁾	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^*A \leq 0.2V$ and $\overline{CE}^*B \geq V_{DDQ} - 0.2V^{(5)}$ $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L S	176	265	148	230	mA
			IND S	—	—	148	270	
IZZ	Sleep Mode Current (Both Ports - TTL Level Inputs)	$ZZ_L = ZZ_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L S	15	45	15	45	mA
			IND S	—	—	15	60	

7144 tbl 09

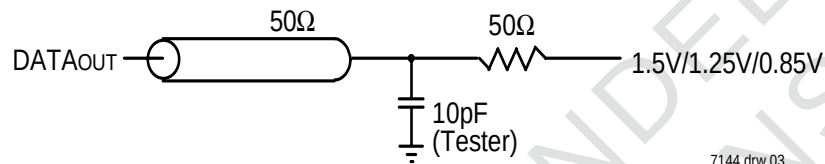
NOTES:

- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of $1/t_{CYC}$, using "AC TEST CONDITIONS".
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 1.8V$, $T_A = 25^\circ C$ for Typ, and are not production tested. $I_{DD} DC(f=0) = 15mA$ (Typ).
- $\overline{CE}_X = V_{IL}$ means $\overline{CE}_{0X} = V_{IL}$ and $CE_{1X} = V_{IH}$
 $\overline{CE}_X = V_{IH}$ means $\overline{CE}_{0X} = V_{IH}$ or $CE_{1X} = V_{IL}$
 $\overline{CE}_X \leq 0.2V$ means $\overline{CE}_{0X} \leq 0.2V$ and $CE_{1X} \geq V_{DDQ} - 0.2V$
 $\overline{CE}_X \geq V_{DDQ} - 0.2V$ means $\overline{CE}_{0X} \geq V_{DDQ} - 0.2V$ or $CE_{1X} \leq 0.2V$
 "X" represents "L" for left port or "R" for right port.
- ISB1, ISB2 and ISB4 will all reach standby levels (ISB3) on the appropriate port(s) if ZZ_L and/or $ZZ_R = V_{IH}$.

AC Test Conditions (V_{DDQ} - 3.3V/2.5V/1.8V)

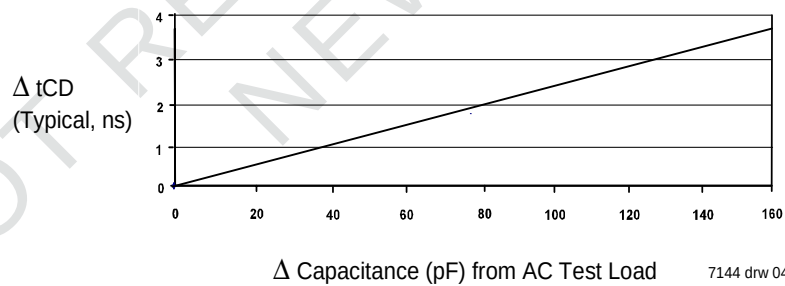
Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.4V/GND to 1.7V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.4V/GND to 1.7V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V/1.25V/0.85V
Output Reference Levels	1.5V/1.25V/0.85V
Output Load	Figure 1

7144 tbl 10



7144 drw 03

Figure 1. AC Output Test load.



7144 drw 04

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)^(2,3) ($V_{DD} = 1.8V \pm 100mV$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$)

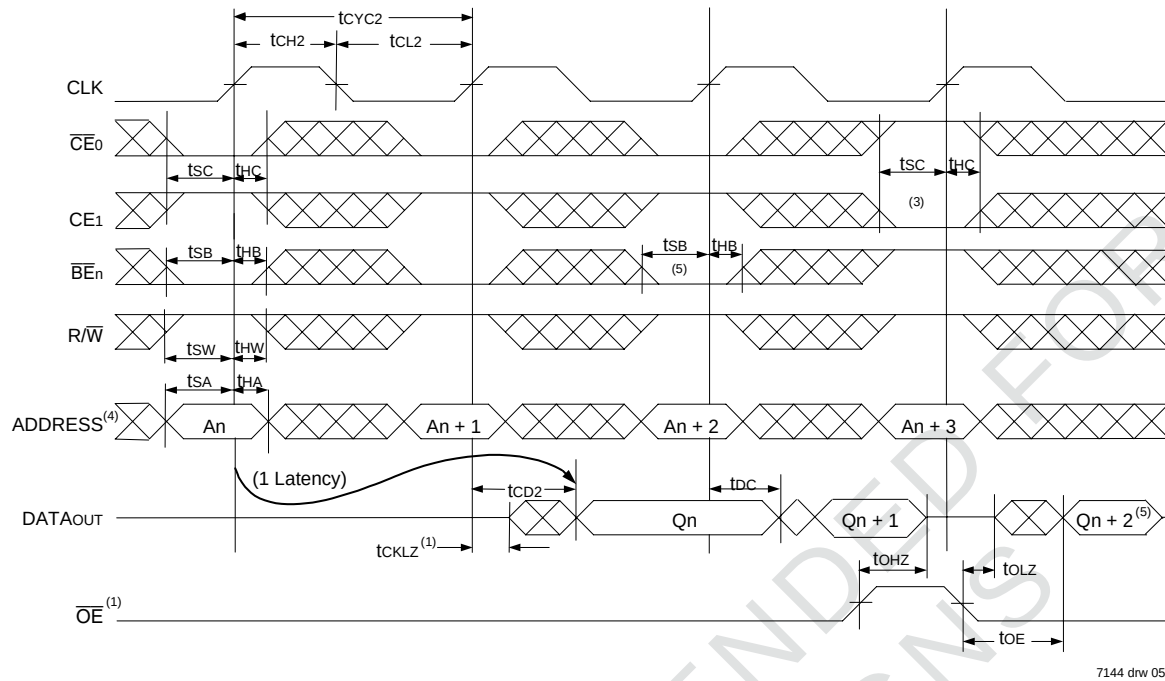
Symbol	Parameter	70P3519/99 S200 Com'l Only		70P3519/99 S166 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	
tcYC1	Clock Cycle Time (Flow-Through) ⁽¹⁾	15	—	20	—	ns
tcYC2	Clock Cycle Time (Pipelined) ⁽¹⁾	5	—	6	—	ns
tCH1	Clock High Time (Flow-Through) ⁽¹⁾	6	—	8	—	ns
tCL1	Clock Low Time (Flow-Through) ⁽¹⁾	6	—	8	—	ns
tCH2	Clock High Time (Pipelined) ⁽²⁾	2	—	2.4	—	ns
tCL2	Clock Low Time (Pipelined) ⁽¹⁾	2	—	2.4	—	ns
tSA	Address Setup Time	1.5	—	1.7	—	ns
tHA	Address Hold Time	0.5	—	0.5	—	ns
tSC	Chip Enable Setup Time	1.5	—	1.7	—	ns
tHC	Chip Enable Hold Time	0.5	—	0.5	—	ns
tSB	Byte Enable Setup Time	1.5	—	1.7	—	ns
tHB	Byte Enable Hold Time	0.5	—	0.5	—	ns
tSW	R/W Setup Time	1.5	—	1.7	—	ns
tHW	R/W Hold Time	0.5	—	0.5	—	ns
tSD	Input Data Setup Time	1.5	—	1.7	—	ns
tHD	Input Data Hold Time	0.5	—	0.5	—	ns
tSAD	$\overline{ADS}$ Setup Time	1.5	—	1.7	—	ns
tHAD	$\overline{ADS}$ Hold Time	0.5	—	0.5	—	ns
tSCN	$\overline{CNTEN}$ Setup Time	1.5	—	1.7	—	ns
tHCN	$\overline{CNTEN}$ Hold Time	0.5	—	0.5	—	ns
tSRPT	$\overline{REPEAT}$ Setup Time	1.5	—	1.7	—	ns
tHRPT	$\overline{REPEAT}$ Hold Time	0.5	—	0.5	—	ns
tOE	Output Enable to Data Valid	—	4.4	—	4.4	ns
tOLZ ⁽⁴⁾	Output Enable to Output Low-Z	1	—	1	—	ns
tOHZ ⁽⁴⁾	Output Enable to Output High-Z	1	3.4	1	3.6	ns
tCD1	Clock to Data Valid (Flow-Through) ⁽¹⁾	—	10	—	12	ns
tCD2	Clock to Data Valid (Pipelined) ⁽¹⁾	—	3.4	—	3.6	ns
tDC	Data Output Hold After Clock High	1	—	1	—	ns
tCKHZ ⁽⁴⁾	Clock High to Output High-Z	1	3.4	1	3.6	ns
tCKLZ ⁽⁴⁾	Clock High to Output Low-Z	1	—	1	—	ns
tINS	Interrupt Flag Set Time	—	7	—	7	ns
tNR	Interrupt Flag Reset Time	—	7	—	7	ns
tCOLS	Collision Flag Set Time	—	3.4	—	3.6	ns
tCOLR	Collision Flag Reset Time	—	3.4	—	3.6	ns
tzZSC	Sleep Mode Set Cycles	2	—	2	—	cycles
tzZRC	Sleep Mode Recovery Cycles	3	—	3	—	cycles
Port-to-Port Delay						
tCO	Clock-to-Clock Offset	4	—	5	—	ns
toFS	Clock-to-Clock Offset for Collision Detection	Please refer to Collision Detection Timing Table on Page 21				

NOTES:

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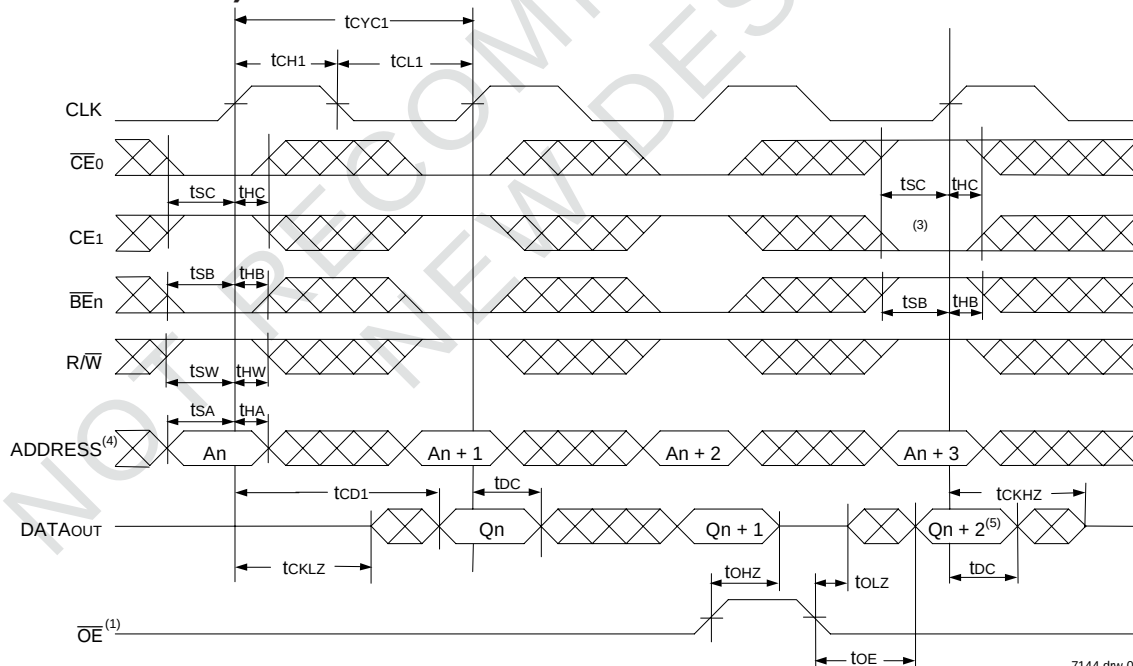
1. The Pipelined output parameters (tcyc2, tcd2) apply to either or both left and right ports when $PL/\overline{FT}x = V_{DD}$ (1.8V). Flow-through parameters (tcyc1, tcd1) apply when $PL/\overline{FT} = V_{SS}$ (0V) for that port.
2. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$) and $PL/\overline{FT}$. $PL/\overline{FT}$ should be treated as DC signals, i.e. steady state during operation.
3. These values are valid for any level of V_{DDQ} (3.3V/2.5V/1.8V).
4. Guaranteed by design (not production tested).

Timing Waveform of Read Cycle for Pipelined Operation ($\overline{\text{FT}}/\text{PIPE} \cdot \text{x} = \text{V}_{\text{IH}}$)^(1,2)



7144 drw 05

Timing Waveform of Read Cycle for Flow-through Output ($\overline{\text{FT}}/\text{PIPE} \cdot \text{x} = \text{V}_{\text{IL}}$)^(1,2,6)

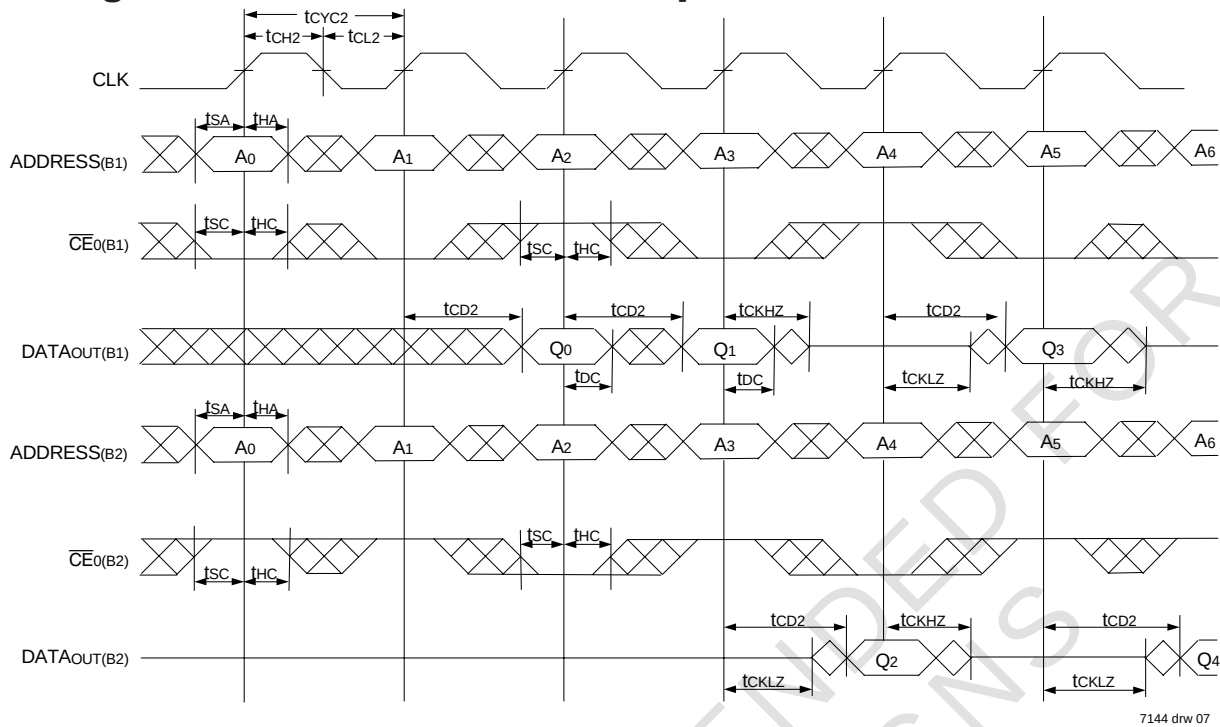


7144 drw 06

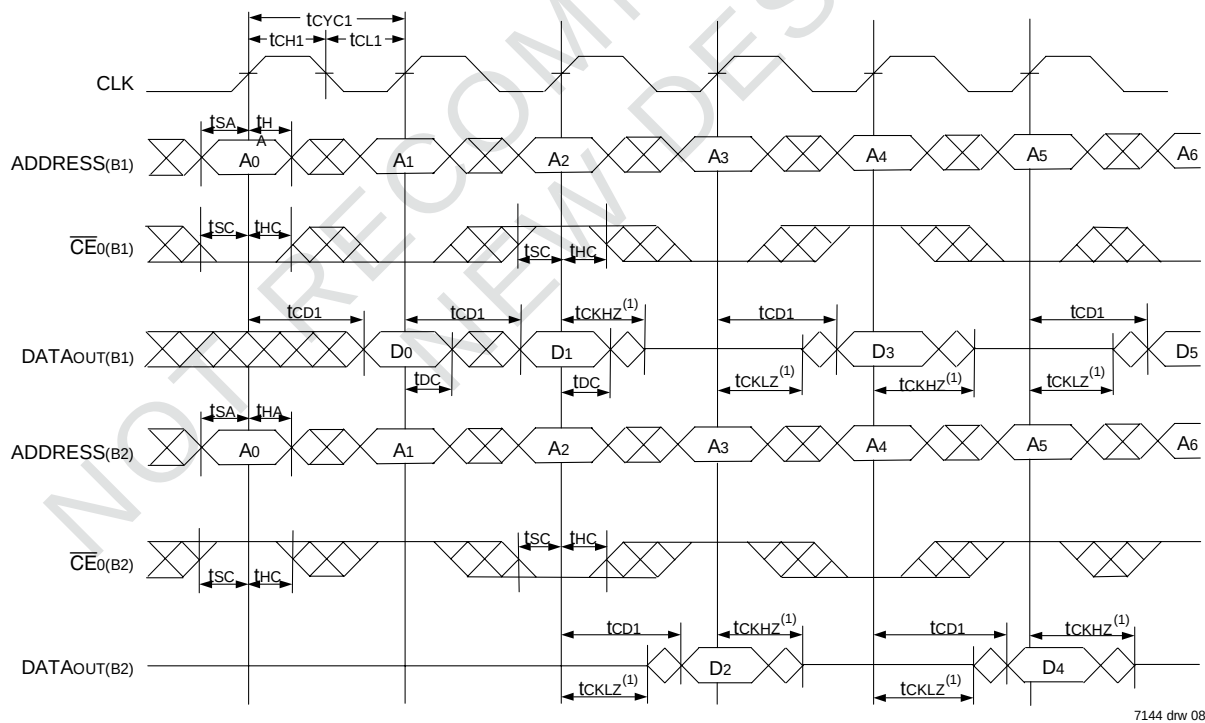
NOTES:

1. $\overline{\text{OE}}$ is asynchronously controlled; all other inputs depicted in the above waveforms are synchronous to the rising clock edge.
2. $\overline{\text{ADS}} = \text{V}_{\text{IL}}$, $\overline{\text{CNTEN}}$ and $\overline{\text{REPEAT}} = \text{V}_{\text{IH}}$.
3. The output is disabled (High-Impedance state) by $\overline{\text{CE}}_0 = \text{V}_{\text{IH}}$, $\text{CE}_1 = \text{V}_{\text{IL}}$, $\overline{\text{BE}}_n = \text{V}_{\text{IH}}$ following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{\text{ADS}} = \text{V}_{\text{IL}}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If $\overline{\text{BE}}_n$ was HIGH, then the appropriate Byte of DATA_{out} for Q_{n+2} would be disabled (High-Impedance state).
6. "x" denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Multi-Device Pipelined Read^(1,2)



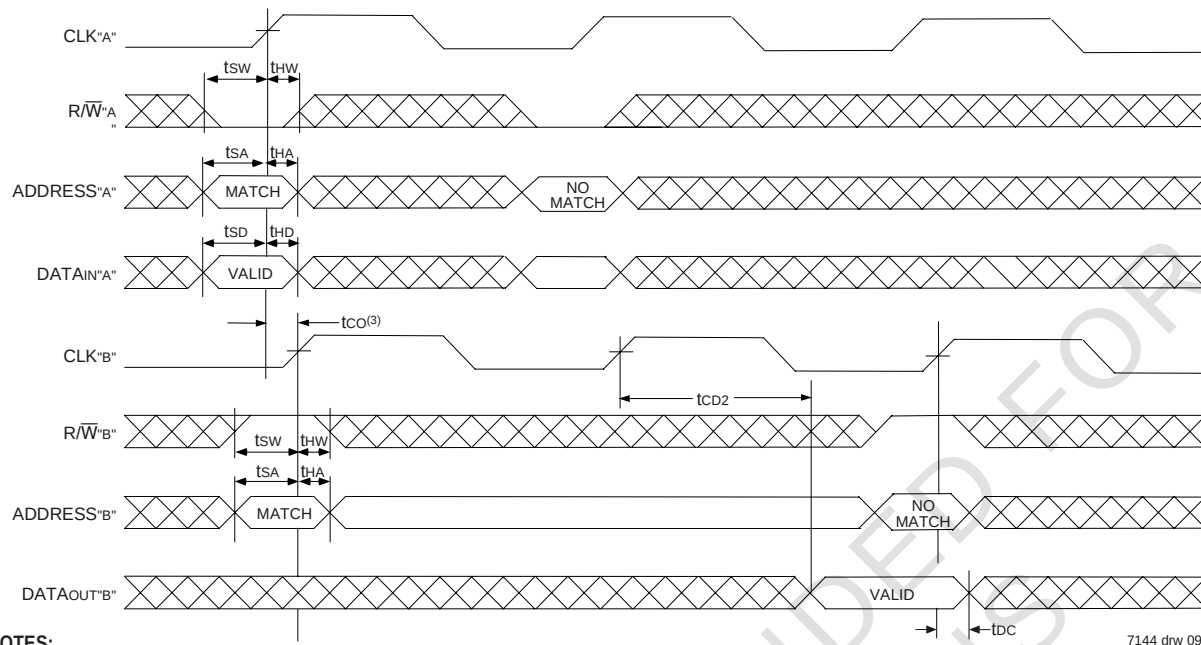
Timing Waveform of a Multi-Device Flow-Through Read^(1,2)



NOTES:

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70P3519/99 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. $\overline{BEN}$, $\overline{OE}$, and $\overline{ADS} = V_{IL}$; $\overline{CE1(B1)}$, $\overline{CE1(B2)}$, $R/\overline{W}$, $\overline{CNTEN}$, and $\overline{REPEAT} = V_{IH}$.

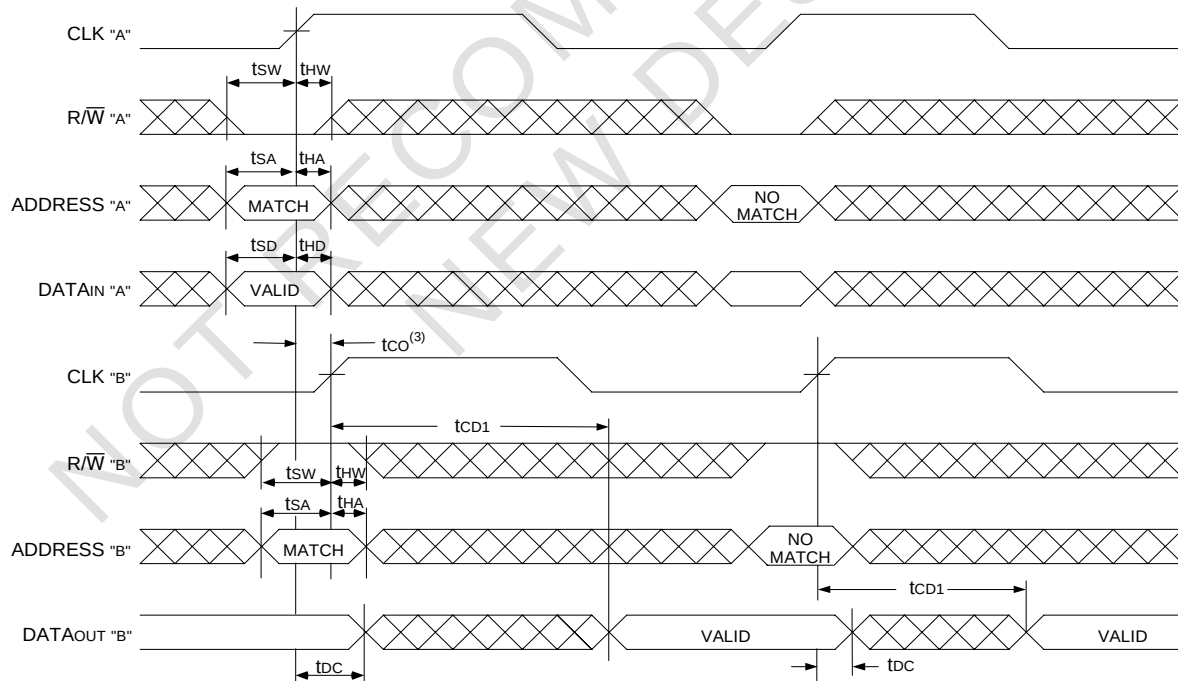
Timing Waveform of Left Port Write to Pipelined Right Port Read^(1,2,4)



NOTES:

1. $\overline{CE_0}$, $\overline{BE_n}$, and $\overline{ADS} = V_{IL}$; $\overline{CE_1}$, $\overline{CNTEN}$, and $\overline{REPEAT} = V_{IH}$.
2. $\overline{OE} = V_{IL}$ for Port "B", which is being read from. $\overline{OE} = V_{IH}$ for Port "A", which is being written to.
3. If $t_{co} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{co} + 2 t_{cyc2} + t_{cd2}$). If $t_{co} >$ minimum, then data from Port "B" read is available on first Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{co} + t_{cyc2} + t_{cd2}$).
4. All timing is the same for Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A"

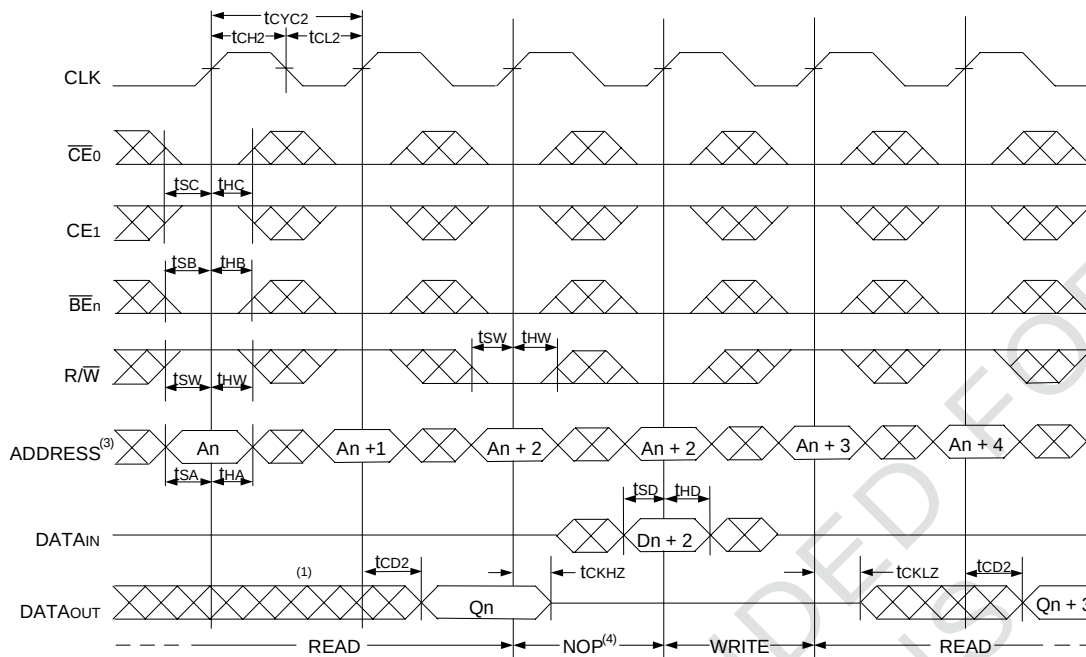
Timing Waveform with Port-to-Port Flow-Through Read^(1,2,4)



NOTES:

1. $\overline{CE_0}$, $\overline{BE_n}$, and $\overline{ADS} = V_{IL}$; $\overline{CE_1}$, $\overline{CNTEN}$, and $\overline{REPEAT} = V_{IH}$.
2. $\overline{OE} = V_{IL}$ for the Right Port, which is being read from. $\overline{OE} = V_{IH}$ for the Left Port, which is being written to.
3. If $t_{co} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (i.e., time from write to valid read on opposite port will be $t_{co} + t_{cyc} + t_{cd1}$). If $t_{co} >$ minimum, then data from Port "B" read is available on first Port "B" clock cycle (i.e., time from write to valid read on opposite port will be $t_{co} + t_{cd1}$).
4. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽²⁾

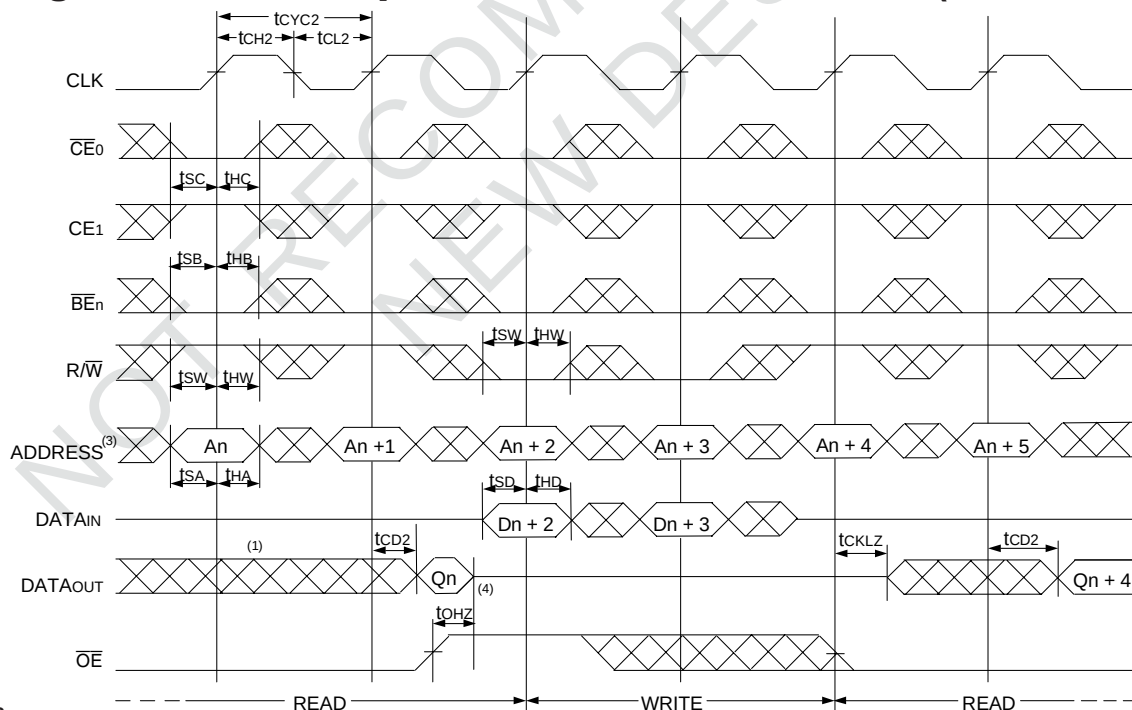


NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE}_0$, $\overline{BE}_n$, and $\overline{ADS} = V_{IL}$; $\overline{CE}_1$, $\overline{CNTEN}$, and $\overline{REPEAT} = V_{IH}$. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

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Timing Waveform of Pipelined Read-to-Write-to-Read($\overline{OE}$ Controlled)⁽²⁾



NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE}_0$, $\overline{BE}_n$, and $\overline{ADS} = V_{IL}$; $\overline{CE}_1$, $\overline{CNTEN}$, and $\overline{REPEAT} = V_{IH}$.
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

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The diagram illustrates the timing relationships for the 7144 device. It includes signals for clock (CLK), chip enable (CE0, CE1), bus enable (BE[n]), read/write (R/W), address (ADDRESS), data input (DATAin), and data output (DATAout). Key timing parameters are defined: t_{CH1} and t_{CL1} for clock high/low pulse widths; t_{SC} and t_{HC} for CE0 setup/hold times; t_{SB} and t_{HB} for BE[n] setup/hold times; t_{SW} and t_{HW} for R/W setup/hold times; t_{SA} and t_{HA} for address setup/hold times; t_{SD} and t_{HD} for data input setup/hold times; t_{CD1} for data output delay; t_{DC} for data output hold time; t_{CKHZ} for clock period; and t_{CKLZ} for clock low-to-high transition time. The diagram shows a sequence of operations: READ, NOP, WRITE, and READ, with data values Q_n , Q_{n+1} , Q_{n+3} , and Q_{n+4} indicated.

The timing diagram for the 7144 device shows the following signals and their timing relationships:

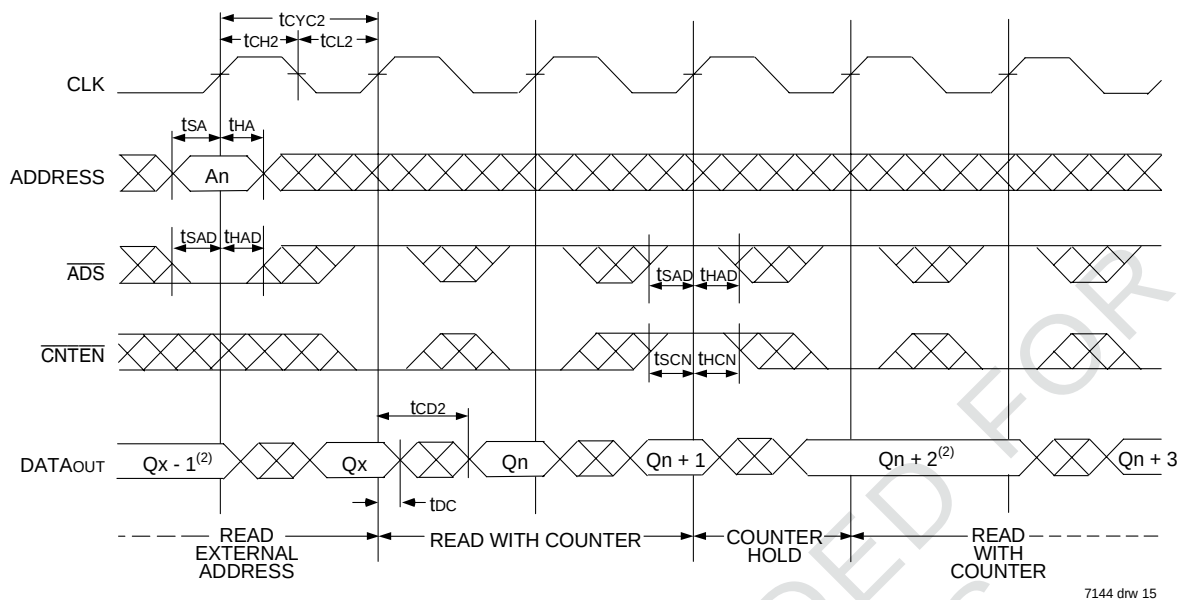
- CLK**: Clock signal.
- CE0**: Chip Enable 0.
- CE1**: Chip Enable 1.
- BEn**: Bank Enable.
- R/W**: Read/Write control signal.
- ADDRESS⁽³⁾**: Address bus.
- DATAin**: Data input bus.
- DATAout**: Data output bus.
- OE**: Output Enable.

The diagram is divided into three main sections: **READ**, **WRITE**, and **READ**. Key timing parameters shown include:

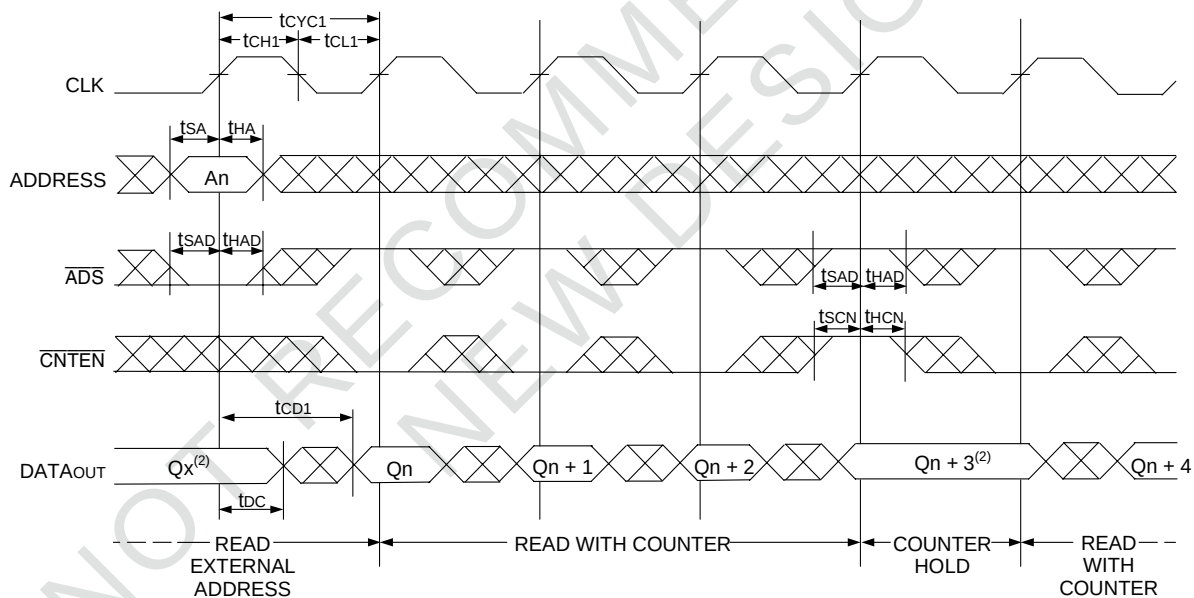
- tCH1**: Clock-to-Header 1 delay.
- tCL1**: Clock-to-Header 1 delay.
- tSC**: Setup time for CE0.
- tHC**: Hold time for CE0.
- tSB**: Setup time for BEn.
- tHB**: Hold time for BEn.
- tSW**: Setup time for R/W.
- tHW**: Hold time for R/W.
- tSA**: Setup time for ADDRESS.
- tHA**: Hold time for ADDRESS.
- tSD**: Setup time for DATAin.
- tHD**: Hold time for DATAin.
- tCD1**: Data-to-Header 1 delay.
- tDC**: Data-to-Header 1 delay.
- tOHZ**: Output Enable to High-Z delay.
- tOE**: Output Enable delay.
- tCKLZ**: Clock-to-Low-Z delay.

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Timing Waveform of Pipelined Read with Address Counter Advance⁽¹⁾



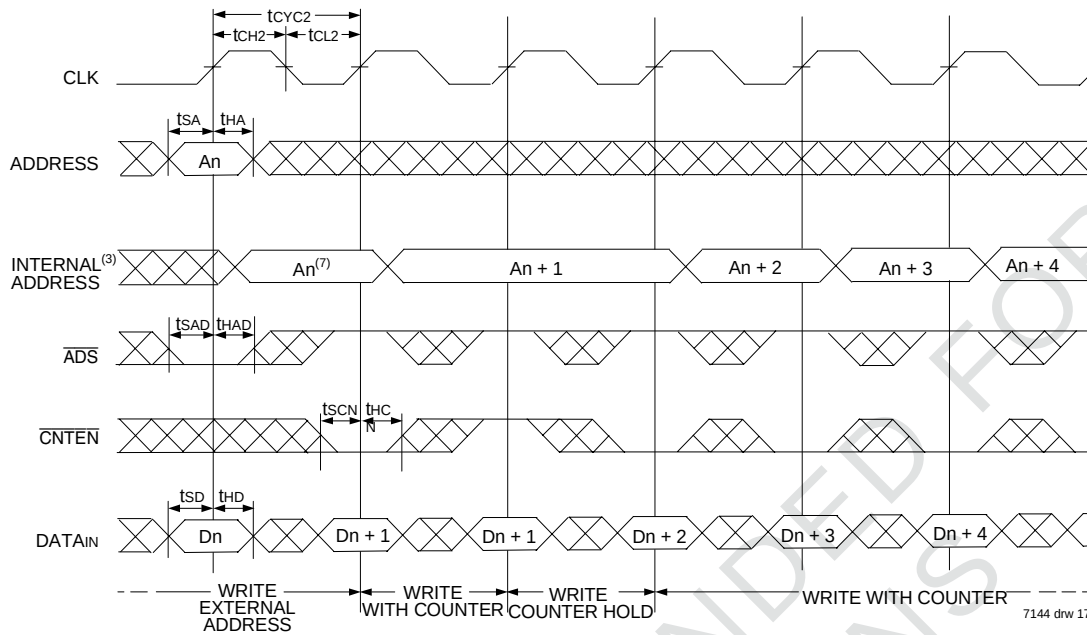
Timing Waveform of Flow-Through Read with Address Counter Advance⁽¹⁾



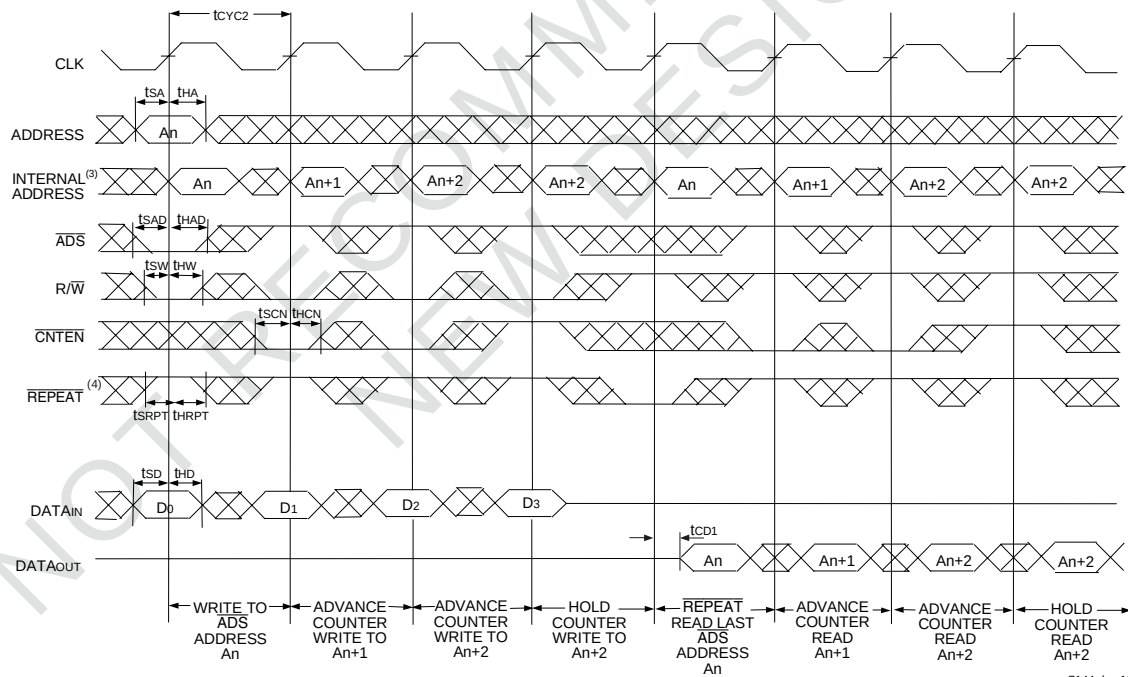
NOTES:

1. $\overline{CE}_0$, $\overline{OE}$, $\overline{BE}_n = V_{IL}$; $\overline{CE}_1$, $R/\overline{W}$, and $\overline{REPEAT} = V_{IH}$.
2. If there is no address change via $\overline{ADS} = V_{IL}$ (loading a new address) or $\overline{CNTEN} = V_{IL}$ (advancing the address), i.e. $\overline{ADS} = V_{IH}$ and $\overline{CNTEN} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-through or Pipelined Inputs)⁽¹⁾



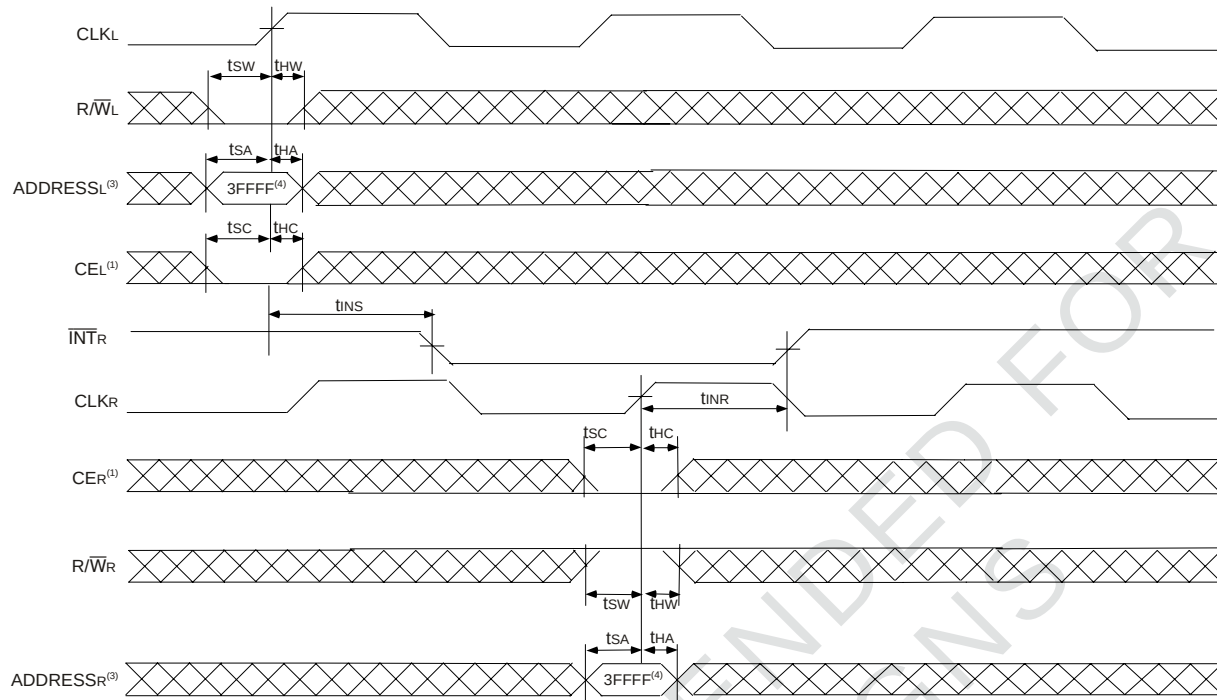
Timing Waveform of Counter Repeat^(2,6)



NOTES:

1. $\overline{CE}_0$, $\overline{BE}_n$, and $R/\overline{W} = V_{IL}$; CE_1 and $\overline{REPEAT} = V_{IH}$.
2. $\overline{CE}_0$, $\overline{BE}_n = V_{IL}$; $CE_1 = V_{IH}$.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS} = V_{IL}$ and equals the counter output when $\overline{ADS} = V_{IH}$.
4. No dead cycle exists during REPEAT operation. A READ or WRITE cycle may be coincidental with the counter REPEAT cycle: Address loaded by last valid $\overline{ADS}$ load will be accessed. For more information on REPEAT function refer to Truth Table II.
5. $CNTEN = V_{IL}$ advances Internal Address from 'An' to 'An+1'. The transition shown indicates the time required for the counter to advance. The 'An+1' Address is written to during this cycle.
6. For Pipelined Mode user should add 1 cycle latency for outputs as per timing waveform of read cycle for pipelined operations.

Waveform of Interrupt Timing⁽²⁾



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NOTES:

1. $CE_0 = V_{IL}$ and $CE_1 = V_{IH}$
2. All timing is the same for Left and Right ports.
3. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.
4. For IDT70P3599, the Interrupt Address is 1FFFF.

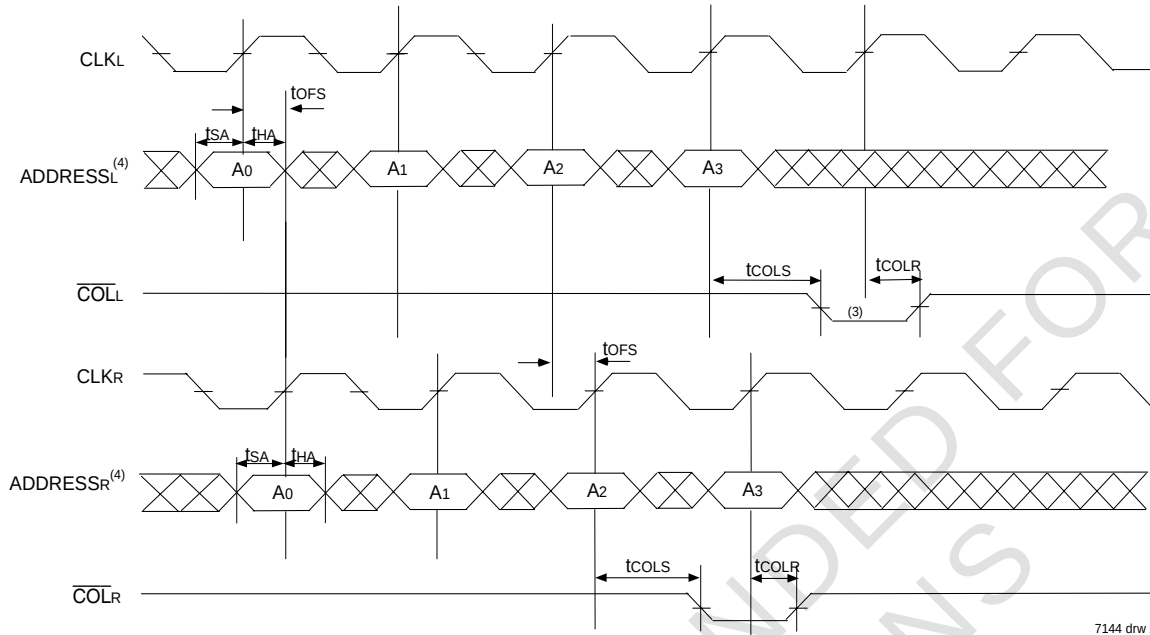
Truth Table III — Interrupt Flag⁽¹⁾

Left Port					Right Port					Function
CLKL	R/WL ⁽²⁾	CEL ⁽²⁾	A17L-A0L ^(3,4)	INTL	CLKR	R/WR ⁽²⁾	CEr ⁽²⁾	A17R-A0R ^(3,4)	INTR	
↑	L	L	3FFFF	X	↑	X	X	X	L	Set Right INT _R Flag
↑	X	X	X	X	↑	H	L	3FFFF	H	Reset Right INT _R Flag
↑	X	X	X	L	↑	L	L	3FFFE	X	Set Left INT _L Flag
↑	H	L	3FFFE	H	↑	X	X	X	X	Reset Left INT _L Flag

NOTES:

1. INT_L and INT_R must be initialized at power-up by Resetting the flags.
2. $CE_0 = V_{IL}$ and $CE_1 = V_{IH}$. R/W and CE are synchronous with respect to the clock and need valid set-up and hold times.
3. A17x is a NC for IDT70P3599, therefore Interrupt Addresses are 1FFFF and 1FFFE.
4. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

7144 tbl 12

Waveform of Collision Timing^(1,2)**Both Ports Writing with Left Port Clock Leading****NOTES:**

- $\overline{CE}_0 = V_{IL}$, $CE_1 = V_{IH}$.
- For reading port, $\overline{OE}$ is a Don't care on the Collision Detection Logic. Please refer to Truth Table IV for specific cases.
- Leading Port Output flag might output $3t_{OFS} + t_{COLS}$ after Address match.
- Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

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Collision Detection Timing^(3,4)

Cycle Time	t_{OFS} (ns)	
	Region 1 (ns) ⁽¹⁾	Region 2 (ns) ⁽²⁾
5ns	0 - 2.8	2.81 - 4.6
6ns	0 - 3.8	3.81 - 5.6
7.5ns	0 - 5.3	5.31 - 7.1

7144 tbl 13

NOTES:

- Region 1**
Both ports show collision after 2nd cycle for Addresses 0, 2, 4 etc.
- Region 2**
Leading port shows collision after 3rd cycle for addresses 0, 3, 6, etc. while trailing port shows collision after 2nd cycle for addresses 0, 2, 4 etc.
- All the production units are tested to midpoint of each region.
- These ranges are based on characterization of a typical device.

Truth Table IV — Collision Detection Flag

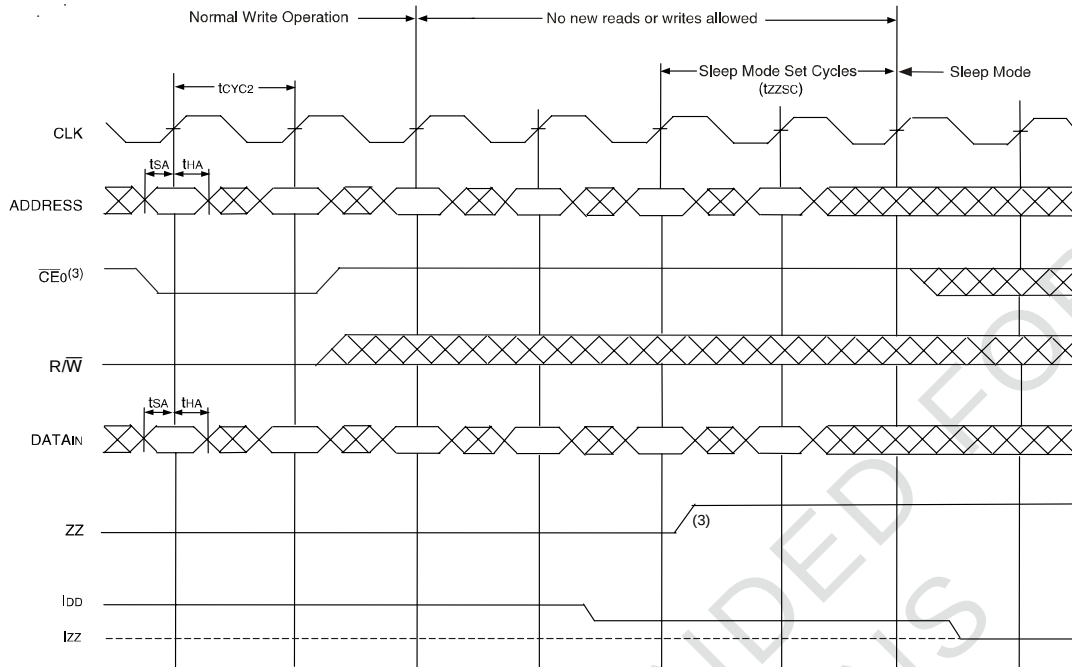
Left Port					Right Port					Function
CLKL	$R/\overline{WL}^{(1)}$	$CE_L^{(1)}$	A17L-A0L ⁽²⁾	$\overline{COLL}$	CLKR	$R/\overline{WR}^{(1)}$	$CE_R^{(1)}$	A17R-A0R ⁽²⁾	$\overline{COLR}$	
↑	H	L	MATCH	H	↑	H	L	MATCH	H	Both ports reading. Not a valid collision. No flag output on either port.
↑	H	L	MATCH	L	↑	L	L	MATCH	H	Left port reading, Right port writing. Valid collision, flag output on Left port.
↑	L	L	MATCH	H	↑	H	L	MATCH	L	Right port reading, Left port writing. Valid collision, flag output on Right port.
↑	L	L	MATCH	L	↑	L	L	MATCH	L	Both ports writing. Valid collision. Flag output on both ports.

NOTES:

- $\overline{CE}_0 = V_{IL}$ and $CE_1 = V_{IH}$. $R/\overline{W}$ and CE are synchronous with respect to the clock and need valid set-up and hold times.
- Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

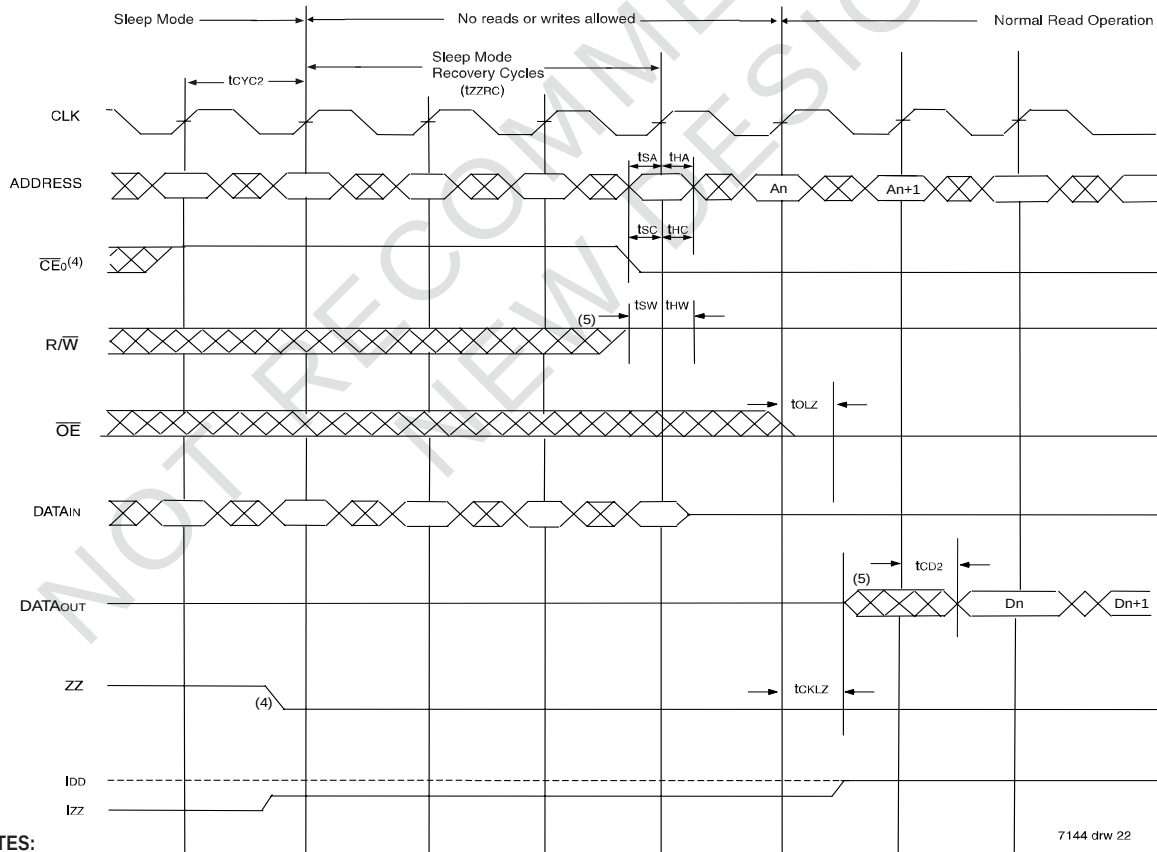
7144 tbl 14

Timing Waveform - Entering Sleep Mode^(1,2)



7144 drw 21

Timing Waveform - Exiting Sleep Mode^(1,2)



7144 drw 22

NOTES:

1. $CE_1 = V_{IH}$.
2. All timing is same for Left and Right ports.
3. $\overline{CE}_0$ has to be deactivated ($\overline{CE}_0 = V_{IH}$) three cycles prior to asserting ZZ ($ZZx = V_{IH}$) and held for two cycles after asserting ZZ ($ZZx = V_{IH}$).
4. $\overline{CE}_0$ has to be deactivated ($\overline{CE}_0 = V_{IH}$) one cycle prior to de-asserting ZZ ($ZZx = V_{IL}$) and held for three cycles after de-asserting ZZ ($ZZx = V_{IL}$).
5. The device must be in Read Mode (R/W High) when exiting sleep mode. Outputs are active but data is not valid until the following cycle.

Functional Description

The IDT70P3519/99 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse width is independent of the cycle time.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE0}$ or a LOW on $CE1$ for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70P3519/99 for depth expansion configurations. Two cycles are required with $\overline{CE0}$ LOW and $CE1$ HIGH to re-activate the outputs.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INTL}$) is asserted when the right port writes to memory location 3FFFE (1FFFE for IDT70P3599), where a write is defined as $\overline{CE_R} = R/\overline{W_R} = V_{IL}$ per the Truth Table. The left port clears the interrupt through access of address location 3FFFE (1FFFE for IDT70P3599) when $\overline{CEL} = V_{IL}$ and $R/\overline{WL} = V_{IH}$. Likewise, the right port interrupt flag ($\overline{INTR}$) is asserted when the left port writes to memory location 3FFFF (1FFF for IDT70P3599) and to clear the interrupt flag ($\overline{INTR}$), the right port must read the memory location 3FFFF (1FFFF for IDT70P3599). The message (36 bits) at 3FFFE or 3FFFF (1FFFF or 1FFFE for IDT70P3599) is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FFFE and 3FFFF (1FFFF or 1FFFE for IDT70P3599) are not used as mail boxes, but as part of the random access memory. Refer to Truth Table III for the interrupt operation.

Collision Detetion

Collision is defined as accessing the same memory address from both ports resulting in the potential for either reading or writing incorrect data to a specific address. For the specific cases: (a) Both ports reading - no data is corrupted, lost, or incorrectly output, so no collision flag is output on either port. (b) One port writing, the other port reading - the end result of the write will still be valid. However, the reading port might capture data that is in a state of transition and hence the reading port's collision flag is output. (c) Both ports writing - there is a risk that the two ports will interfere with each other, and the data stored in memory will not be a valid write from either port (it may essentially be a random combination of the two). Therefore, the collision flag is output on both ports. Please refer to Truth Table IV for all of the above cases.

The alert flag ($\overline{COLx}$) is asserted on the 2nd or 3rd rising clock edge of the affected port following the collision, and remains low for one cycle. Please refer to Collision Detection Timing table on Page 21. During that next cycle, the internal arbitration is engaged in resetting the alert flag (this avoids a specific requirement on the part of the user to reset the alert flag). If two collisions occur on subsequent clock cycles, the second collision may not generate the appropriate alert flag. A third collision will generate the

proper alert flag. In the event that a user initiates a burst access on both ports with the same starting address on both ports and one or both ports writing during each access (i.e., imposes a long string of collisions on contiguous clock cycles), the alert flag will be asserted and cleared every other cycle. Please refer to the Collision Detection timing waveform on Page 21.

Collision detection on the IDT70P3519/99 represents an advance in functionality over other sync multi-ports, which have no such capability. The IDT70P3519/99 sustains the key features of bandwidth and flexibility. The collision detection function is very useful in the case of bursting data, or a string of accesses made to sequential addresses, in that it indicates a problem within the burst, giving the user the option of either repeating the burst or continuing to watch the alert flag to see whether the number of collisions increases above an acceptable threshold value. Offering this function on chip also allows users to reduce their need for arbitration circuits, typically done in CPLD's or FPGA's. This reduces board space and design complexity, and gives the user more flexibility in developing a solution.

Sleep Mode

The IDT70P3519/99 is equipped with an optional sleep or low power mode on both ports. The sleep mode pin on both ports is asynchronous and active high. During normal operation, the ZZ pin is pulled low. When ZZ is pulled high, the port will enter sleep mode where it will meet lowest possible power conditions. The sleep mode timing diagram shows the modes of operation: Normal Operation, No Read/Write Allowed and Sleep Mode.

For normal operation all inputs must meet setup and hold times prior to sleep and after recovering from sleep. Clocks must also meet cycle high and low times during these periods. Three cycles prior to asserting ZZ ($ZZx = V_{IH}$) and three cycles after de-asserting ZZ ($ZZx = V_{IL}$), the device must be disabled via the chip enable pins. If a write or read operation occurs during these periods, the memory array may be corrupted. Validity of data out from the RAM cannot be guaranteed immediately after ZZ is asserted (prior to being in sleep). When exiting sleep mode, the device must be in Read mode ($R/\overline{Wx} = V_{IH}$) when chip enable is asserted, and the chip enable must be valid for one full cycle before a read will result in the output of valid data.

During sleep mode the RAM automatically deselects itself. The RAM disconnects its internal clock buffer. The external clock may continue to run without impacting the RAMs sleep current (I_{ZZ}). All outputs will remain in high-Z state while in sleep mode. All inputs are allowed to toggle. The RAM will not be selected and will not perform any reads or writes.

Depth and Width Expansion

The IDT70P3519/99 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70P3519/99 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 72-bits or wider.

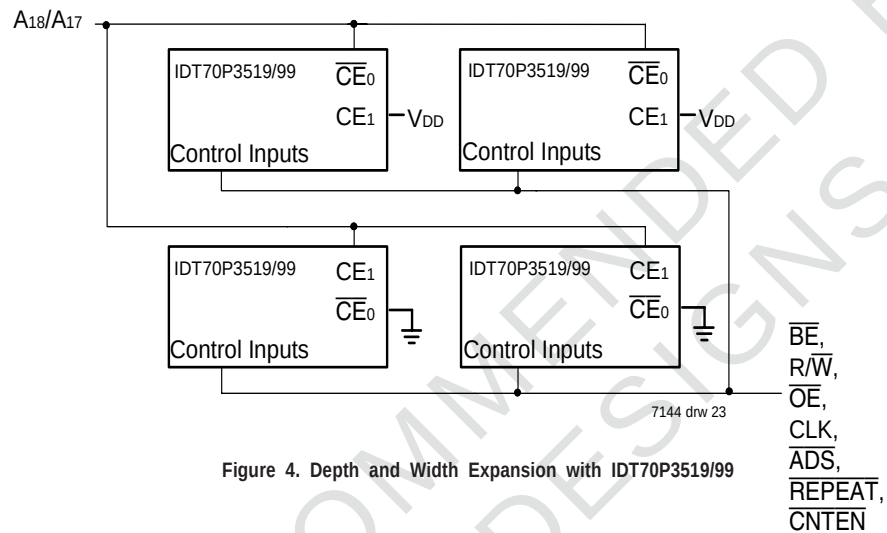


Figure 4. Depth and Width Expansion with IDT70P3519/99

NOTE:

1. A_{18} is for IDT70P3519, A_{17} is for IDT70P3599.

JTAG Timing Specifications

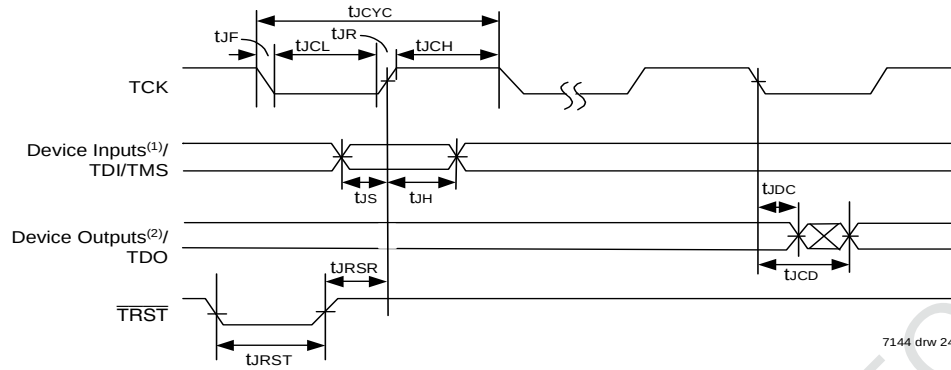


Figure 5. Standard JTAG Timing

NOTES:

1. Device inputs = All device inputs except TDI, TMS, and TRST.
2. Device outputs = All device outputs except TDO.

JTAG AC Electrical Characteristics (1,2,3,4)

Symbol	Parameter	70P3519/99		
		Min.	Max.	Units
t _{JCYC}	JTAG Clock Input Period	100	—	ns
t _{JCH}	JTAG Clock HIGH	40	—	ns
t _{JCL}	JTAG Clock Low	40	—	ns
t _{JR}	JTAG Clock Rise Time	—	3 ⁽¹⁾	ns
t _{JF}	JTAG Clock Fall Time	—	3 ⁽¹⁾	ns
t _{JRST}	JTAG Reset	50	—	ns
t _{JRSR}	JTAG Reset Recovery	50	—	ns
t _{JCD}	JTAG Data Output	—	25	ns
t _{JDC}	JTAG Data Output Hold	0	—	ns
t _{JST}	JTAG Setup	15	—	ns
t _{JH}	JTAG Hold	15	—	ns

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NOTES:

1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0x0	Reserved for version number
IDT Device ID (27:12)	0x380 ⁽¹⁾	Defines IDT part number
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register

NOTE:

1. Device ID for IDT70P3599 is 0x383.

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Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
Boundary Scan (BSR)	Note (3)

7144 tbl 17

System Interface Parameters

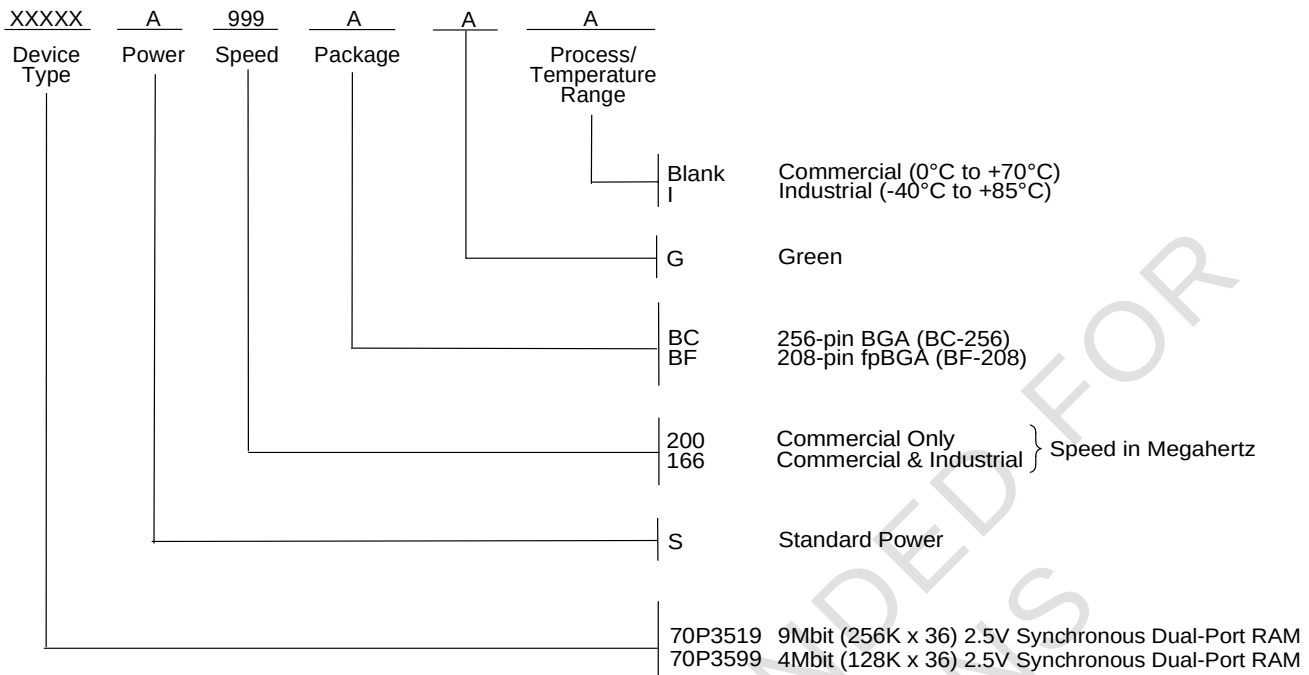
Instruction	Code	Description
EXTEST	0000	Forces contents of the boundary scan cells onto the device outputs ⁽¹⁾ . Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0100	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state except $\overline{\text{COLx}}$ & $\overline{\text{INTx}}$ outputs.
CLAMP	0011	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.
SAMPLE/PRELOAD	0001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs ⁽²⁾ to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	0101, 0111, 1000, 1001, 1010, 1011, 1100	Several combinations are reserved. Do not use codes other than those identified above.
PRIVATE	0110, 1110, 1101	For internal use only.

NOTES:

1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{\text{TRST}}$.
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.

7144 tbl 18

Ordering Information



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IDT Clock Solution for IDT70P3519/99 Dual-Port

IDT Dual-Port Part Number	Dual-Port I/O Specifications		Clock Specifications				IDT PLL Clock Device	IDT Non-PLL Clock Device
	Voltage	I/O	Input Capacitance	Input Duty Cycle Requirement	Maximum Frequency	Jitter Tolerance		
70P3519/99	2.5	LVTTTL	3.5-6pF	40%	200	75ps	5T2010 5T9010	5T905, 5T9050 5T907, 5T9070

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Datasheet Document History:

07/07/08: Initial Datasheet
01/19/09: Page 28 Removed "IDT" from orderable part number
06/08/09: Removed preliminary status



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