

NUD4021, NUD4022, NUD4023

Advance Information Switching LED Current Source

This integrated Switching LED Driver provides a regulated dc current to an LED powered from a standard automotive 12 V system. It is a low cost switching device which utilizes a minimal of external components that can be used to power high intensity LEDs for a number of applications.

The NUD4021 is recommended for currents of 50 mA to 400 mA, while the NUD4022/NUD4023 is recommended for currents of 300 mA to 2.0 A.

Features

- High Power Conversion Efficiency
- Output Current in Excess of 1.0 A
- Thermal Protection
- Adjustable LED Current
- 80 V Rating for Automotive Immunity
- Internal SENSEFET™ for Lossless Current Sensing
- Automotive Compliant
- These are Pb-Free Devices

Typical Applications

- Automotive LED Lighting
- 12 V Current Source

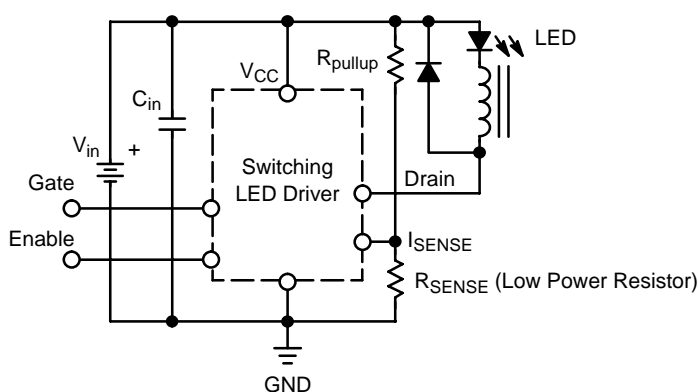


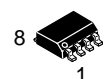
Figure 1. Typical System Schematic



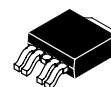
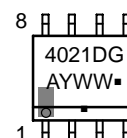
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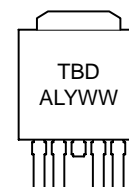
MARKING DIAGRAMS & PIN ASSIGNMENTS



SO-8
CASE 751



DPAK 5
CASE 175AA



TBD = Specific Device Code
A = Assembly Location
Y = Year
W, WW = Work Week
▪ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NUD4021DR2G	SO-8 (Pb-Free)	3000/Tape & Reel
NUD4022NT4G	DPAK (Pb-Free)	2500/Tape & Reel
NUD4023NT4G	DPAK (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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FUNCTIONAL PIN DESCRIPTION

Pin 4021	Pin 4022	Pin 4023	Function	Description
1	N/C	1	Enable	This pin is in a high state for operation and in a low state for shutdown, which turns off the power FET.
2	2	N/C	Gate	This pin is the gate of the power MOSFET. A capacitor can be added to ground to reduce the switching speed of the MOSFET.
3	4	4	I _{SENSE}	The output of the SENSEFET. A resistor from this pin to ground converts the drain current (divided by the sense ratio) to a voltage.
4	5	5	V _{CC}	Input voltage to the LED driver. This voltage is compatible with a 12 V automotive electrical system.
5,6,7	1	2	Ground	The reference node to this chip, also the source of the power FET.
8	3	3	Drain	This is the drain of the internal power FET which conducts pulsed current through the LEDs that are connected in series to it.

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V _{CC}	Input Voltage, Operating (V _{CC} to Ground) V _{CC} pin connected directly to the input voltage V _{CC} pin connected through a 10k resistor	24 80	V
V _{DD}	Drain Voltage, Operating (Drain to Ground) Transient (300 ms) Steady-State	100 80	V
V _{EN}	Enable Voltage, Operating (Enable to ground)	12	V
I _{Davg}	Drain Current, Continuous (Note 1)	SO-8 DPAK 0.4 2.0	A
I _{Dpk}	Drain Current, Peak	SO-8 DPAK 1.5 4.0	A
E _{LD}	Load Dump Pulse, Drain-to-Source. (Note 3), (Note 4) (R _{SOURCE} =0.5 Ω, t=300 ms), (V _{CC} pin tied to V _{bat} , Enable open, L=330 μH, R _{sense} =1.2 Ω)	60	V
Rev-Bat	Reverse Battery, Drain-to-Source, (V _{CC} pin tied to V _{bat}) (A diode in series with V _{CC} is required to protect the LED Load)	-14	V
Dual-Volt	Dual Voltage Jump Start, 2 minutes (Drain-to-Source), (Note 4) (V _{CC} pin tied to V _{bat} , Enable open, L=330 μH, R _{sense} =1.2 Ω)	24	V
ESD	Human Body Model (HBM) According to EIA/JESD22/A114 Specification	TBD	V

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Rating	Value	Unit
T _J	Operating Temperature Range	-40 to 150	°C
T _J	Non-Operating Temperature Range	-55 to 175	°C
T _L	Lead Temperature, Soldering (1/8" from case for 10 sec)	260	°C
P _D	Total Power Dissipation (T _A = 25°C), (Note 1) Derated above 25°C	SO-8 DPAK 1.13 2.4 SO-8 DPAK 9.0 19.0	W mW/°C
R _{θJA}	Thermal Resistance Junction-to-Ambient, (Note 1)	SO-8 DPAK 110 52	°C/W
R _{θJL}	Thermal Resistance Junction-to-Lead, (Note 1)	SO-8 DPAK 77 4.7	°C/W

1. Mounted on FR4 Board, 1 in sq pad, 1 oz coverage.

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ELECTRICAL CHARACTERISTICS ($V_{CC} = 12\text{ V}$, $T_J = 25^\circ\text{C}$, unless otherwise noted)

Symbol	Characteristics	Min	Typ	Max	Unit
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POWER FET

V_{BRDSS}	Drain-to-Source Breakdown Voltage (Gate pin tied to ground, $I_D = 1\text{ mA}$)	80	–	–	V
I_{DSS}	Drain-to-Source Leakage Current (Gate pin tied to ground, $V_{DS} = 80\text{ V}$)	–	–	10	μA
V_{SD}	Source-Drain Body Diode (Forward On-Voltage)	–	1.1	–	V
$R_{DS(ON)}$	ON Resistance ($I_D = 100\text{ mA}$, Enable open, I_{sense} tied to ground)	2500	3000	3500	$\text{m}\Omega$
	($I_D = 1.0\text{ A}$, Enable open, I_{sense} tied to ground)	375	450	525	

CURRENT REGULATION

I_{LED}	LED Current Regulation ($V_{LED}=3.5\text{ V}$, $R_{sense}=1.2\text{ }\Omega$, $C_{in}=100\text{ }\mu\text{F}$, $L=330\text{ }\mu\text{H}$, $R_{pullup}=1.1\text{ k}\Omega$) SO-8 ($V_{LED}=3.5\text{ V}$, $R_{sense}=TBD$, $C_{in}=100\text{ }\mu\text{F}$, $L=TBD$, $R_{pullup}=TBD$) DPAK	297 630	330 700	363 770	mA
t_{Offmax}	Maximum Off Time	–	TBD	–	μs
t_{Offmin}	Minimum Off Time	–	TBD	–	μs

THERMAL SHUTDOWN

T_{SD}	Thermal Limit Shutdown Temperature, (Note 2)	–	150	–	$^\circ\text{C}$
T_{hyst}	Thermal Hysteresis	–	30	–	$^\circ\text{C}$

ENABLE/PWM

V_{ENhigh}	Logic Level High, (Turn-on)	2.1	–	–	V
V_{ENlow}	Logic Level Low, (Turn-off)	–	–	1.9	V
f_{PWM}	PWM Frequency, (Note 2)	–	100	–	Hz
R_{pullup}	Internal Pull up Resistance, (Terminated to a 7.7 V source)	400	500	600	$\text{k}\Omega$

BIAS SUPPLY (V_{CC})

I_{BIAS}	Bias Current ($V_{CC}=12\text{ V}$, Enable & Gate open, $I_{sense}=1.2\text{ }\Omega$, No Load)	–	1.0	–	mA
V_{min}	Minimum Operating Voltage	8.0	–	–	V

2. Verified by design.
3. Non-repetitive load dump pulse per Figure 3.
4. Tested with a Load = One LED ($V_f = 3.5\text{ V}$, $I_f = 0.350\text{ mA}$).

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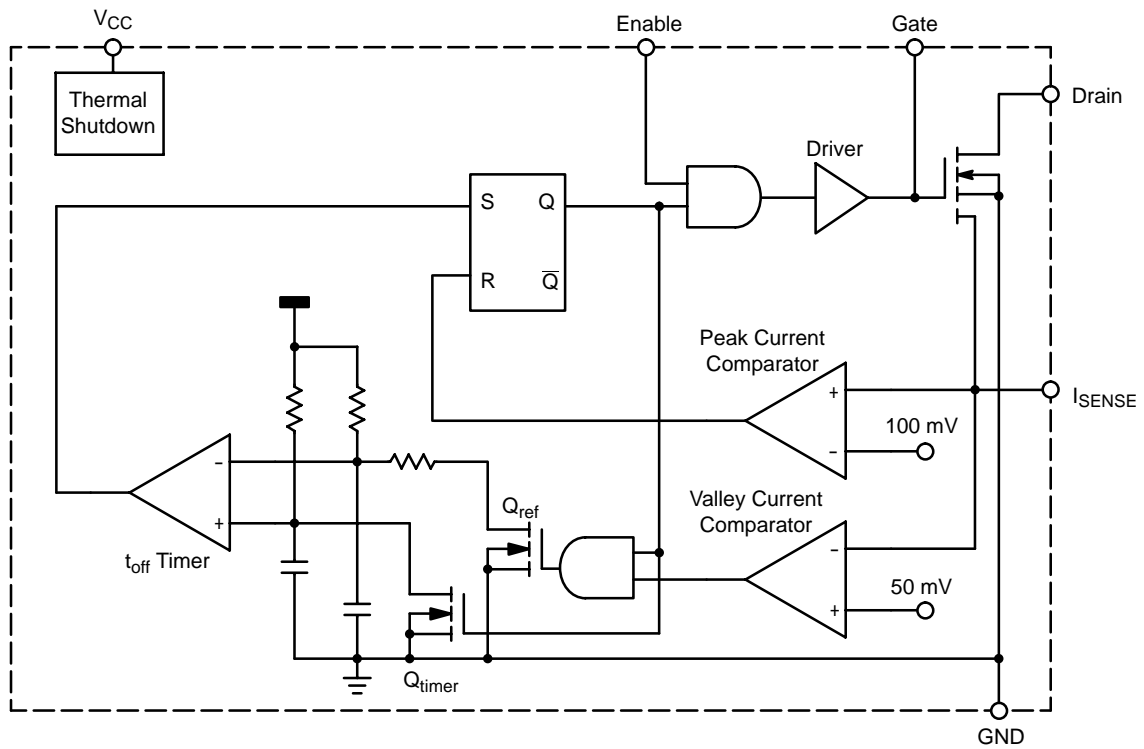


Figure 2. Simplified Block Diagram

Load Dump Pulse Not Suppressed:

$V_r = 13.5 \text{ V Nominal } \pm 10\%$
 $V_s = 60 \text{ V Nominal } \pm 10\%$
 $T = 300 \text{ ms Nominal } \pm 10\%$
 $t_r = 1 - 10 \text{ ms } \pm 10\%$

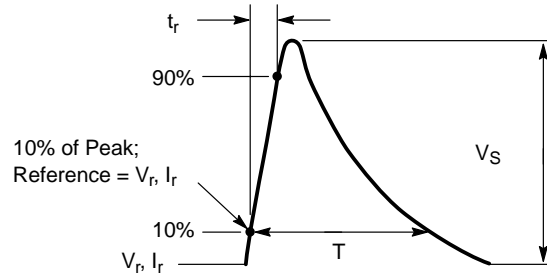


Figure 3. Load Dump Waveform Definition

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TYPICAL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise specified)

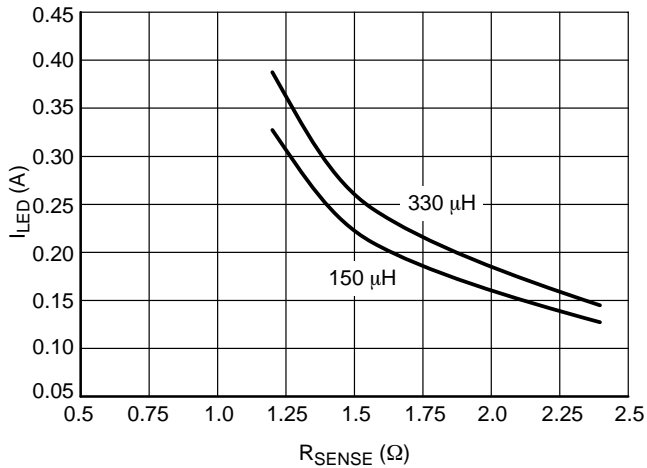


Figure 4. NUD4021, LED Current Adjustment
($V_{CC} = 12\text{ V}$, $V_{LED} = 3.5\text{ V}$, $R_{pullup} = 1.1\text{ k}\Omega$, $C_{in} = 100\text{ }\mu\text{F}$)

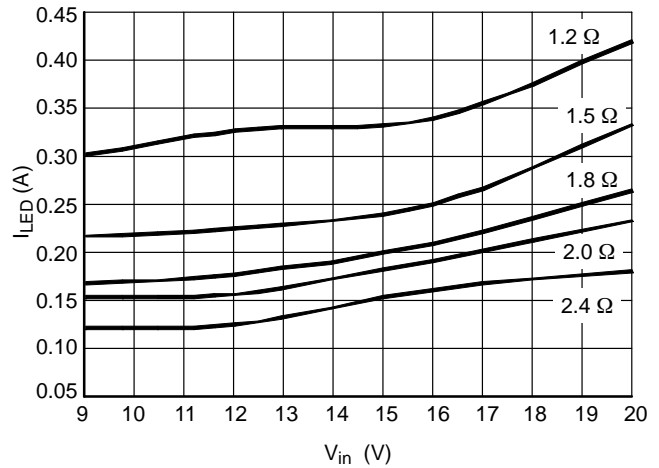


Figure 5. NUD4021, Line Regulation for different LED Currents
($V_{LED} = 3.5\text{ V}$, $R_{pullup} = 1.1\text{ k}\Omega$, $C_{in} = 100\text{ }\mu\text{F}$, $L = 150\text{ }\mu\text{H}$)

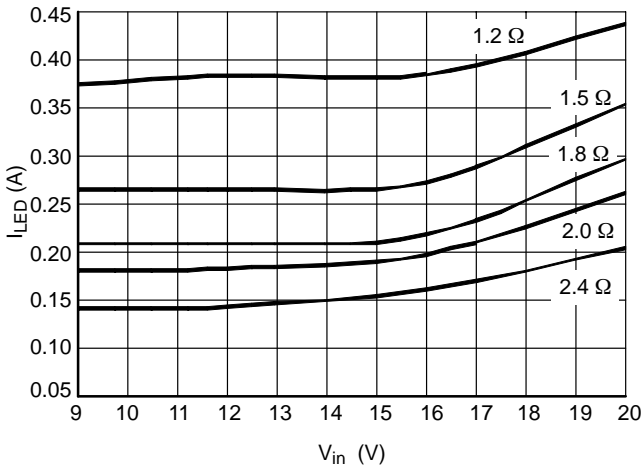


Figure 6. NUD4021, Line Regulation for different LED Currents
($V_{LED} = 3.5\text{ V}$, $R_{pullup} = 1.1\text{ k}\Omega$, $C_{in} = 100\text{ }\mu\text{F}$, $L = 330\text{ }\mu\text{H}$)

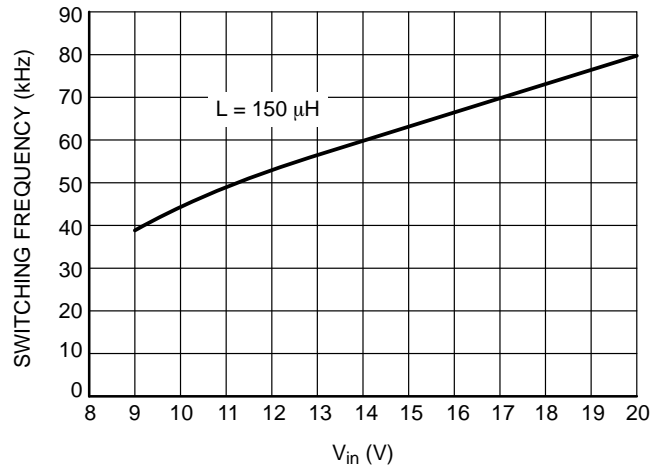


Figure 7. NUD4021, Switching Frequency Variation versus Input Voltage
($V_{LED} = 3.5\text{ V}$, $R_{sense} = 1.2\text{ }\Omega$, $R_{pullup} = 1.1\text{ k}\Omega$, $C_{in} = 100\text{ }\mu\text{F}$)

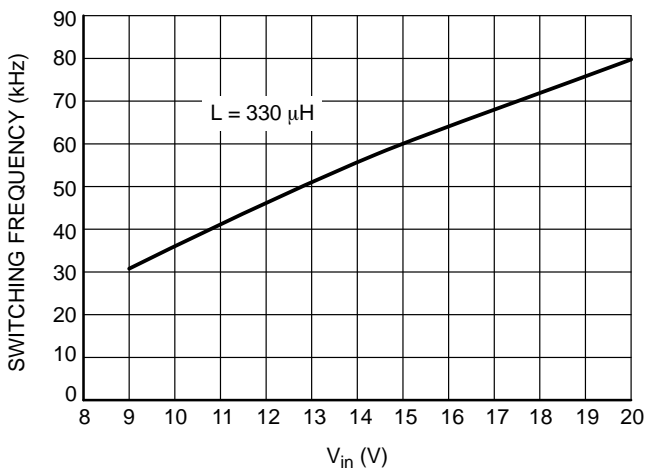


Figure 8. NUD4021, Switching Frequency Variation versus Input Voltage
($V_{LED} = 3.5\text{ V}$, $R_{sense} = 1.2\text{ }\Omega$, $R_{pullup} = 1.1\text{ k}\Omega$, $C_{in} = 100\text{ }\mu\text{F}$)

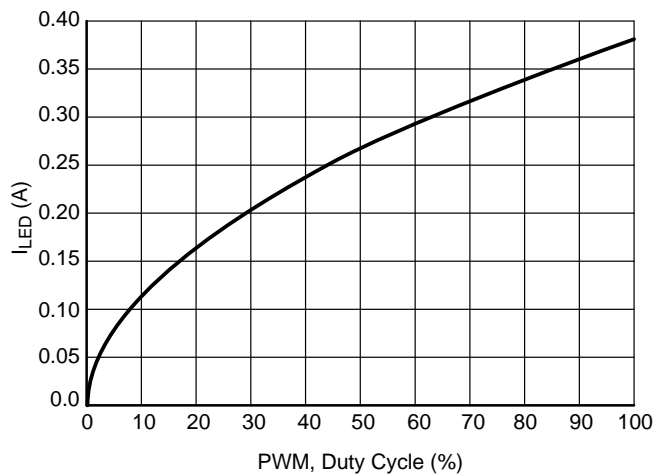


Figure 9. NUD4021, Dimming Performance
($V_{LED} = 3.5\text{ V}$, $R_{sense} = 1.2\text{ }\Omega$, $R_{pullup} = 1.1\text{ k}\Omega$, $C_{in} = 100\text{ }\mu\text{F}$, $L = 330\text{ }\mu\text{H}$, $f_{PWM} = 100\text{ Hz}$)

TYPICAL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise specified)

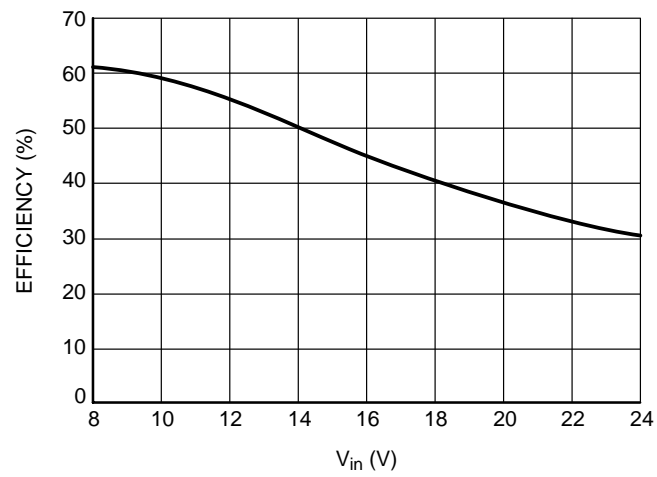


Figure 10. NUD4021, System Efficiency versus Input Voltage ($V_{LED} = 3.5\text{ V}$, $R_{sense} = 1.2\ \Omega$, $R_{pullup} = 1.1\text{ k}\Omega$, $C_{in} = 100\ \mu\text{F}$, $L = 330\ \mu\text{H}$, Diode MBRA160T3)

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TYPICAL APPLICATION CIRCUITS AND OPERATION WAVEFORMS

($T_J = 25^\circ\text{C}$ unless otherwise specified)

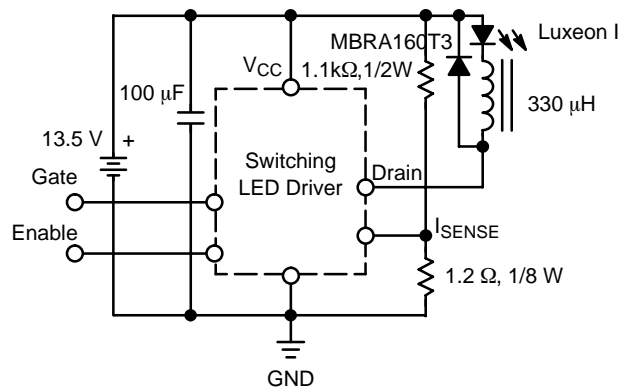


Figure 11. NUD4021, Typical Application Circuit to Drive one LED (Luxeon I, $V_F = 3.5\text{ V}$, $I_F = 0.350\text{ mA}$)

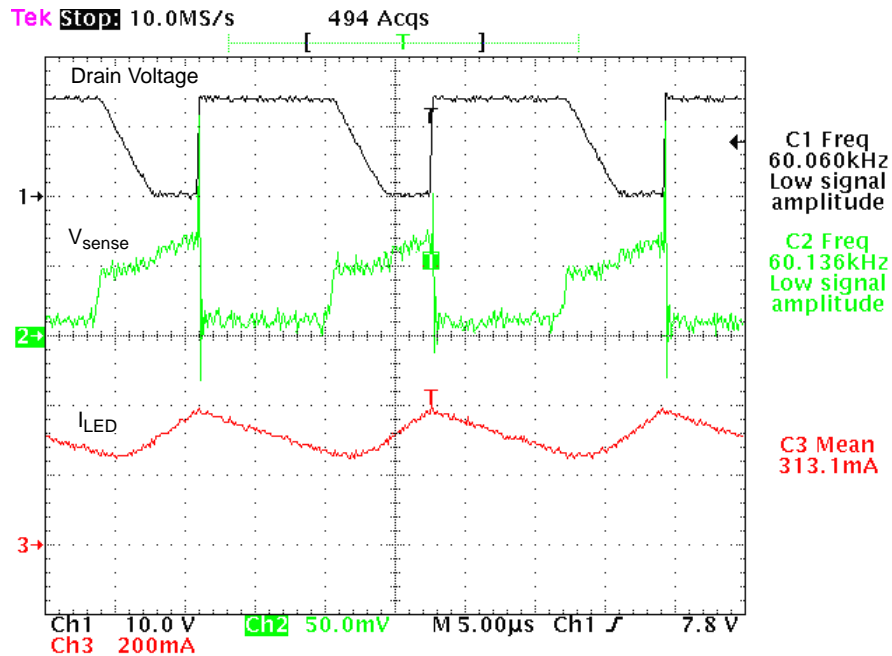


Figure 12. NUD4021, Typical Operation Waveforms ($V_{CC} = 13.5\text{ V}$, $V_{LED} = 3.5\text{ V}$, $R_{\text{sense}} = 1.2\ \Omega$, $R_{\text{pullup}} = 1.1\text{ k}\Omega$, $C_{in} = 100\ \mu\text{F}$, $L = 330\ \mu\text{H}$)

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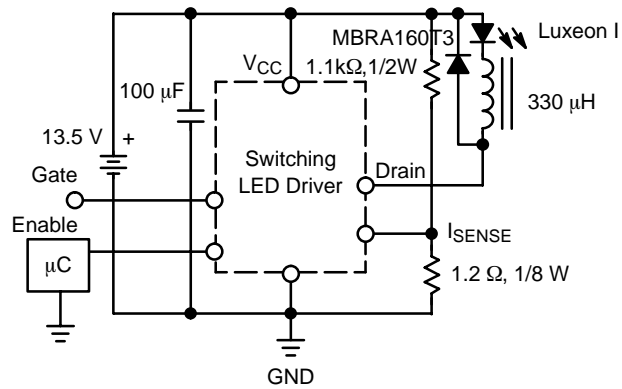


Figure 13. NUD4021, Typical Application Circuit for Dimming
(Load = One LED, V_F = 3.5 V, I_F = 0.350 mA)

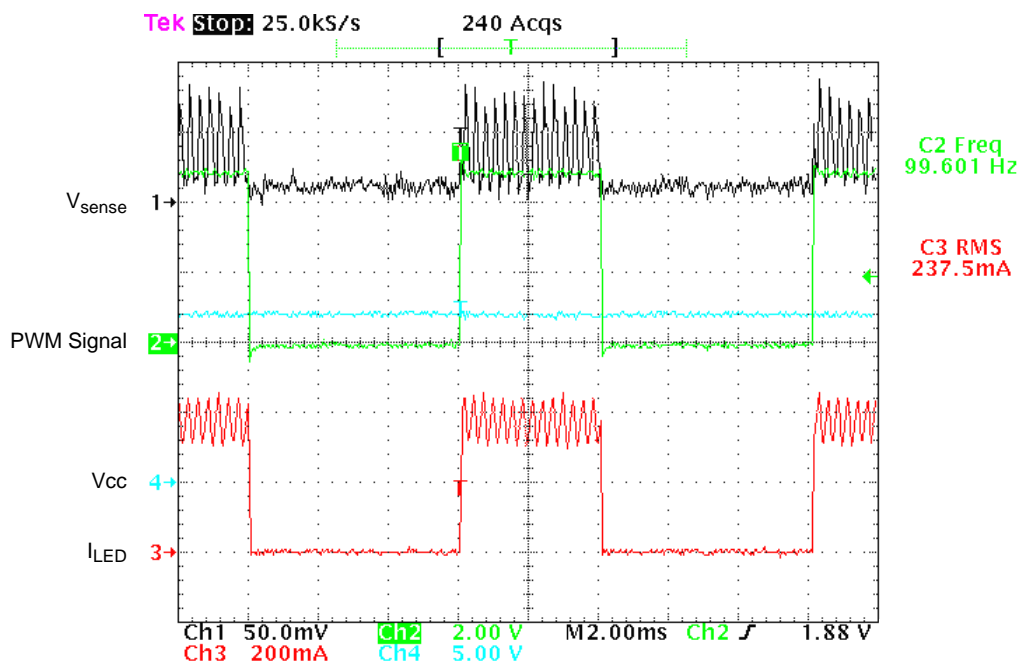


Figure 14. NUD4021, Typical Operation Waveforms
(V_{CC} = 13.5 V, V_{LED} = 3.5 V, R_{sense} = 1.2 Ω, R_{pullup} = 1.1 kΩ, C_{in} = 100 µF, L = 330 µH)

DEVICE THEORY

Theory of Operation

This switching power supply is comprised of an inverted buck regulator controlled by a current mode, hysteretic control circuit. The buck regulator operates exactly like a conventional buck regulator except the power device placement has been inverted to allow for a low side power FET.

Referring to Figure 1, when the SENSEFET is conducting, current flows through the inductor and the LED. When the SENSEFET shuts off, current continues to flow through the inductor and LED, but is diverted through the diode. This operation keeps the current in the LED continuous with a continuous current ramp that varies from the peak current level to 50% of the peak current level.

The control circuit hysteretically controls the current. Figure 2 illustrates the operation of this circuit. When the SENSEFET is conducting, the current in the inductor ramps up. This current is sensed by the sense resistor that is connected from I_{sense} to ground. The SENSEFET diverts a small fraction of its drain current through the I_{sense} terminal, so that a low power resistor is able to sense currents up to 2 amps.

When the voltage on the I_{sense} pin reaches 100 mV, the peak current comparator switches to its high state and sets the Q output of the flip-flop low, which turns off the power FET.

A conventional hysteretic controller would monitor the load current and turn the switch back on when the current reaches its minimum level; 50% in this case. Due to the topology and the fact that the current is being sensed by the FET, once the FET turns off, the current information is no longer available to the control circuit, so a proprietary timer circuit is used to determine the off time.

There are two RC networks in this timer. The one connected to the non-inverting input is a short time constant circuit (approx 10 μ s) that determines the off time of the switch. When the power switch is on, Qtimer is also conducting and keeps the timing capacitor discharged. When the switch turns off, Qtimer does also and the timing cap charges until it reaches the reference voltage at the inverting input.

The correct off time is essential to keep the valley current at 50% of the peak current. To achieve this, the valley current comparator sends a correction signal to the reference voltage circuit. This circuit uses a resistor and capacitor, similar to the timer circuit, but has a much slower time constant (approx 100 μ s).

Any time the switch is on and the valley current is less than 50% of the peak current (less than 50 mV on the input of the valley current comparator), the comparator will turn of Qref which will reduce the voltage on the reference capacitor. The resistor connected to the drain of Qref is much smaller than the one that charges the reference capacitor, so only a small pulse is required to reduce the reference voltage, but that voltage will increase very slowly when no pulse is present.

The reference signal will be adjusted to a level that keeps the valley current at 50% of the peak current, thereby minimizing the error pulses from the valley current comparator.

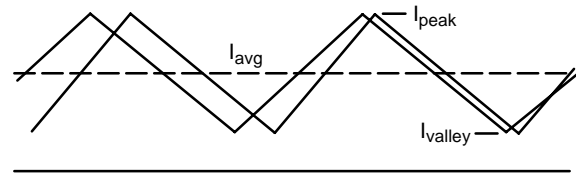


Figure 15. Typical Current Waveforms

The current waveshape is triangular, and the peak and valley currents are controlled. The average value for a triangular waveshape is halfway between the peak and valley, so even with changes in duty cycle due to input voltage variations or load changes, the average current will remain constant.

Inductor Calculation

These first engineering samples do not represent the final performance of the NUD4021 device since design changes are to be made. Therefore the inductor calculation is yet to be defined based on the new silicon. For suggested inductor values please refer to Figures 4, 5, 6 and 7 of the datasheet.

Pull-up Resistor

For these engineering samples, the 1.1 k Ω pull-up resistor connected from I_{sense} to V_{CC} is necessary to improve the LED current regulation. Its main purpose is to provide an offset to the current limit circuit so that the regulation is improved. This pull-up resistor may not be necessary for the next silicon design.

Enable

The device's enable can be used for two different functions: enable/disable and dimming. The enable circuit has an internal pull up resistor of 500 k Ω that is terminated to a 7.7V internal source. So if the enable pin is left open, the device will be enabled automatically. If logic gates are used, the device will be enabled when the voltage at the enable pin is higher than 1.5 V and will be disabled for voltages lower than 1.4 V. For dimming purposes, a PWM signal can be connected to the enable pin, and it is recommended that the frequency of the PWM signal is not higher than 500 Hz.

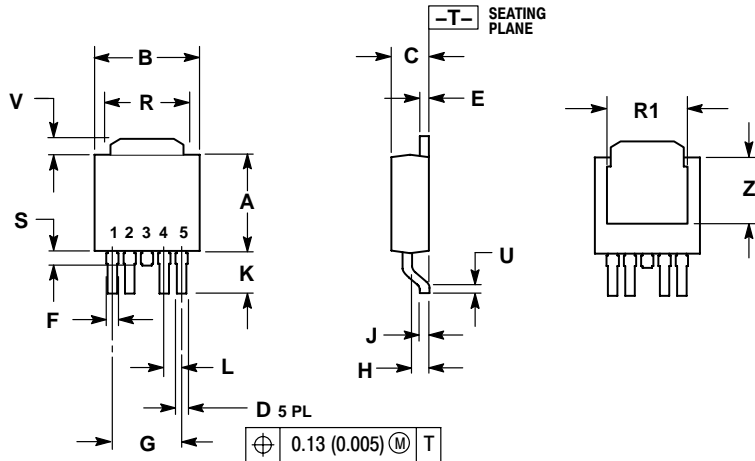
Cgate

The option for a gate capacitor (Cgate) is built in the NUD4021 device and was originally intended to slow down the switching speed of the internal SENSEFET to minimize EMI issues. However for these engineering samples, it is not necessary to use any gate capacitors because the turn-on time of the SENSEFET is already quite slow, and therefore the addition of a gate capacitor may cause malfunction on the device due to the slow switching speed.

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PACKAGE DIMENSIONS

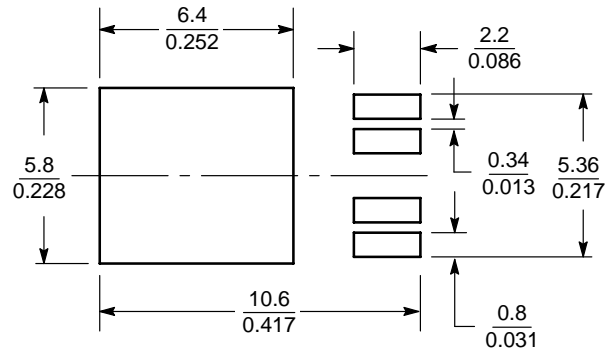
DPAK 5, CENTER LEAD CROP CASE 175AA-01 ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180	BSC	4.56	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045	BSC	1.14	BSC
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

SOLDERING FOOTPRINT*



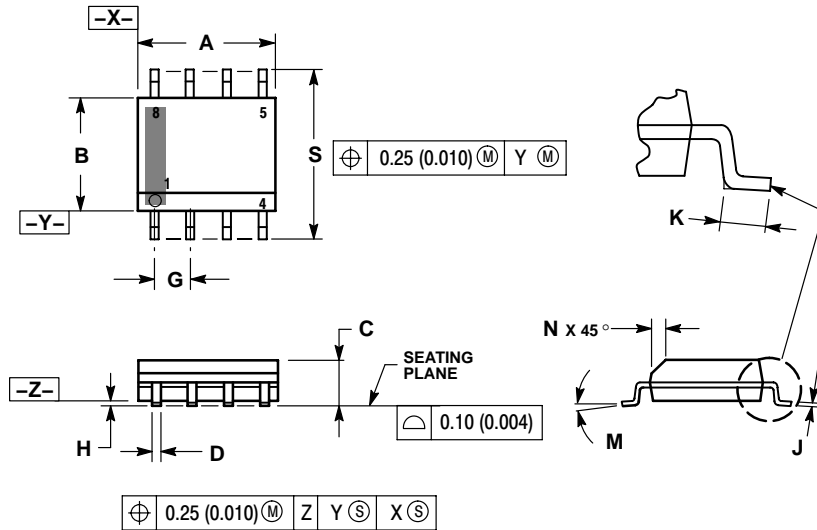
SCALE 4:1 $\left(\frac{\text{mm}}{\text{inches}} \right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NUD4021, NUD4022, NUD4023

PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AG

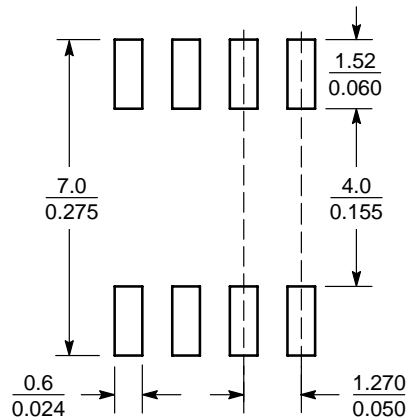


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244


SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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