INTEGRATED CIRCUITS
UNITRODE

UCC1889
UCC2889
UCC3889

Off-line Power Supply Controller

FEATURES

- Transformerless Off-line Applications
- Ideal Primary-side Bias Supply
- Efficient BiCMOS Design
- Wide Input Range
- Fixed or Adjustable Low Voltage Output
- Uses Low Cost SMD Inductors
- Short Circuit Protected
- Optional Isolation Capability

DESCRIPTION

The UCC1889 controller is optimized for use as an off-line, low power, low voltage, regulated bias supply. The unique circuit topology utilized in this device can be visualized as two cascaded flyback converters, each operating in the discontinuous mode, and both driven from a single external power switch. The significant benefit of this approach is the ability to achieve voltage conversion ratios of 400V to 12V with no transformer and low internal losses.

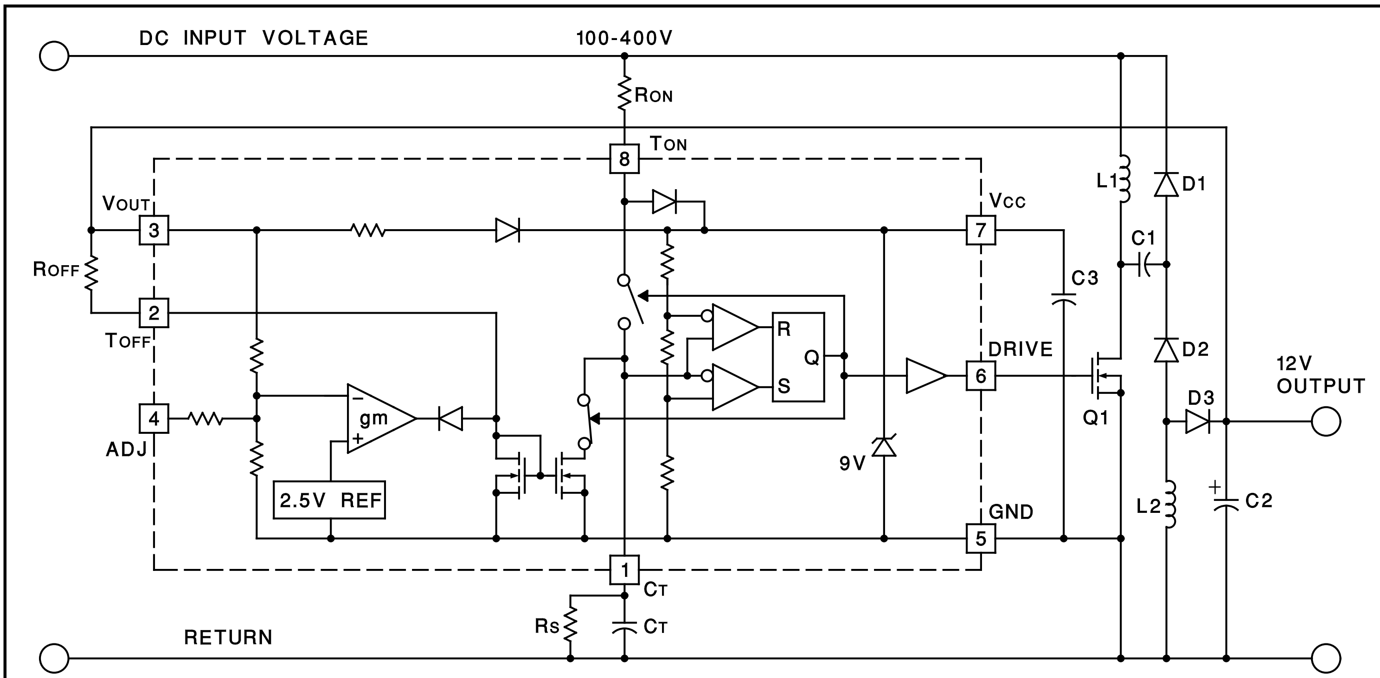
The control algorithm utilized by the UCC1889 is to force the switch on time to be inversely proportional to the input line voltage while the switch off time is made inversely proportional to the output voltage. This action is automatically controlled by an internal feedback loop and reference. The cascaded configuration allows a voltage conversion from 400V to 12V to be achieved with a switch duty cycle greater than 10%. This topology also offers inherent short circuit protection since as the output voltage falls to zero, the switch off time approaches infinity.

The output voltage can be easily set to 12V or 18V. Moreover, it can be programmed for other output voltages less than 18V with a few additional components. An isolated version can be achieved with this topology as described further in Unitrode Application Note U-149.

OPERATION

With reference to the application diagram below, when input voltage is first applied, the R_{ON} current into T_{ON} is directed to V_{CC} where it charges the external capacitor, C3, connected to V_{CC}. As voltage builds on V_{CC}, an internal undervoltage lockout holds the circuit off and the output at DRIVE low until V_{CC} reaches 8.4V. At this time, DRIVE goes high turning on the power switch, Q1, and redirecting the current into T_{ON} to the timing capacitor, C_T. C_T charges to a fixed threshold with a current $I_{CHG}=0.8 \bullet (V_{IN} - 4.5V)/R_{ON}$. Since DRIVE will only be high for as long as C_T charges, the power switch on time will be inversely proportional to line voltage. This provides a constant line voltage-switch on time product.

TYPICAL APPLICATION

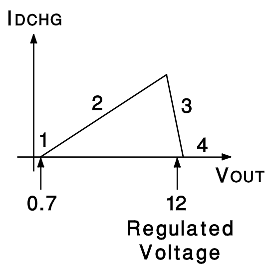


Note: This device incorporates patented technology used under license from Lambda Electronics, Inc. UDG-93060-1

OPERATION (cont.)

At the end of the on time, Q1 is turned off and the R_{ON} current into T_{ON} is again diverted to V_{CC}. Thus the current through R_{ON}, which charges C_T during the on time, contributes to supplying control power during the off time.

The power switch off time is controlled by the discharge of C_T which, in turn, is programmed by the regulated output voltage. The relationship between C_T discharge current, I_{DCHG}, and output voltage is illustrated as follows:



1. When V_{OUT} = 0, the off time is infinite. This feature provides inherent short circuit protection. However, to ensure output voltage startup when the output is not a short, a high value resistor, R_S, is placed in parallel with C_T to establish a minimum switching frequency.
2. As V_{OUT} rises above approximately 0.7V to its regulated value, I_{DCHG} is defined by R_{OFF}, and therefore is equal to:

$$I_{DCHG} = (V_{OUT} - 0.7V) / R_{OFF}$$

   As V_{OUT} increases, I_{DCHG} increases resulting in the reduction of off time. The frequency of operation increases and V_{OUT} rises quickly to its regulated value.
3. In this region, a transconductance amplifier reduces I_{DCHG} in order to maintain V_{OUT} in regulation.
4. If V_{OUT} should rise above its regulation range, I_{DCHG} falls to zero and the circuit returns to the minimum frequency established by R_S and C_T.

The range of switching frequencies is established by R_{ON}, R_{OFF}, R_S, and C_T as follows:

$$\text{Frequency} = 1/(T_{ON} + T_{OFF})$$

$$T_{ON} = R_{ON} \bullet C_T \bullet 4.6\,V/(V_{IN} - 4.5V)$$

$$T_{OFF}\,(\text{max}) = 1.4 \bullet R_S \bullet C_T$$

Regions 1 and 4

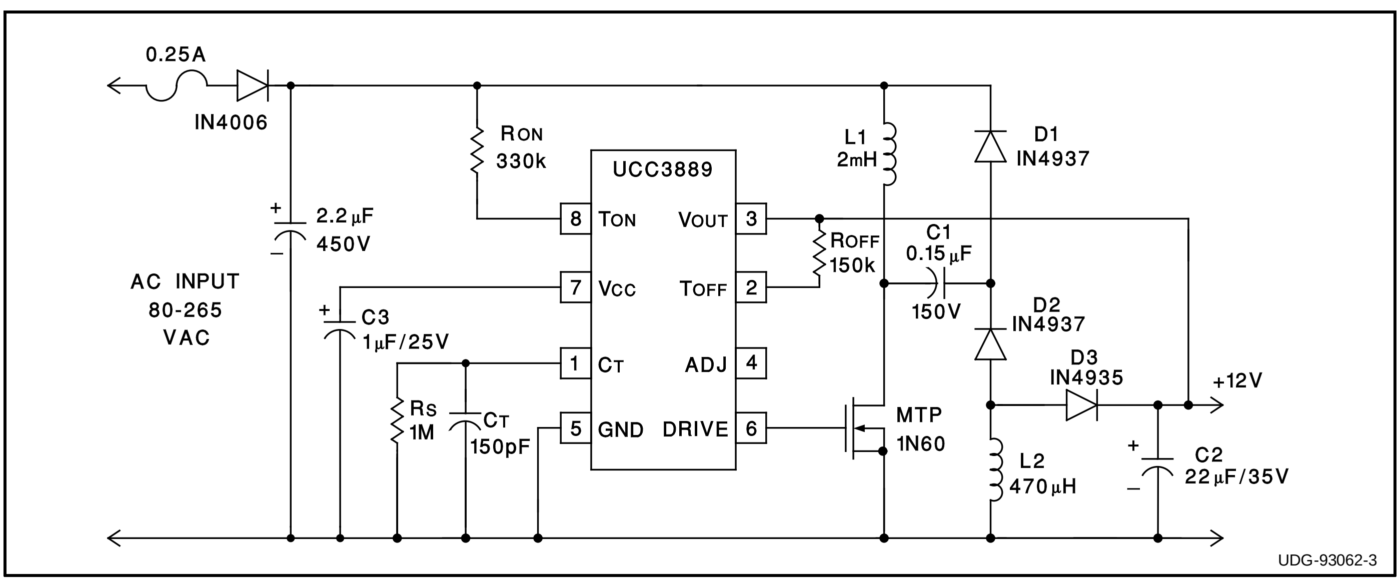
$$T_{OFF} = R_{OFF} \bullet C_T \bullet 3.7V\,/(V_{OUT} - 0.7V)$$

Region 2, excluding the effects of R_S which have a minimal impact on T_{OFF}.

The above equations assume that V_{CC} equals 9V. The voltage at T_{ON} increases from approximately 2.5V to 6.5V while C_T is charging. To take this into account, V_{IN} is adjusted by 4.5V in the calculation of T_{ON}. The voltage at T_{OFF} is approximately 0.7V.

DESIGN EXAMPLE

The UCC3889 regulates a 12 volt, 1 Watt nonisolated DC output from AC inputs between 80 and 265 volts. In this example, the IC is programmed to deliver a maximum on time gate drive pulse width of 2.4 microseconds which occurs at 80 VAC. The corresponding switching frequency is approximately 100kHz at low line, and overall efficiency is approximately 50%. Additional design information is available in Unitrode Application Note U-149.



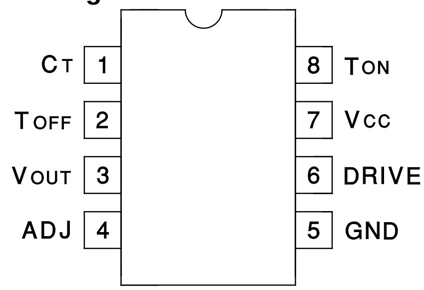
ABSOLUTE MAXIMUM RATINGS

I_{CC} 5mA
Current into T_{ON} Pin 1.5mA
Voltage on V_{OUT} Pin 20V
Current into T_{OFF} Pin 250µA
Storage Temperature . . . . -65°C to +150°C

Note: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N or J, D Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC3889, -40°C to +85°C for the UCC2889, and -55°C to +125°C for the UCC1889. No load at DRIVE pin (C_{LOAD}=0).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
General					
V_{CC} Zener Voltage	I_{CC} < 1.5mA	8.6	9.0	9.3	V
Startup Current	V_{OUT} = 0		150	250	µA
Operating Current I(V_{OUT})	V_{OUT} = 11V, F = 150kHz		1.2	2.5	mA
Under-Voltage-Lockout					
Start Threshold	V_{OUT} = 0	8.0	8.4	8.8	V
Minimum Operating Voltage after Start	V_{OUT} = 0	6.0	6.3	6.6	V
Hysteresis	V_{OUT} = 0	1.8			V
Oscillator					
Amplitude	V_{CC} = 9V	3.5	3.7	3.9	V
C_T to DRIVE high Propagation Delay	Overdrive = 0.2V		100	200	ns
C_T to DRIVE low Propagation Delay	Overdrive = 0.2V		50	100	ns
Driver					
VOL	I = 20mA, V_{CC} = 9V		0.15	0.4	V
	I = 100mA, V_{CC} = 9V		0.7	1.8	V
VOH	I = –20mA, V_{CC} = 9V	8.5	8.8		V
	I = –100mA, V_{CC} = 9V	6.1	7.8		V
Rise Time	C_{LOAD} = 1nF		35	70	ns
Fall Time	C_{LOAD} = 1nF		30	60	ns
Line Voltage Detection					
Charge Coefficient: I_{CHG} / I(T_{ON})	VCT = 3V, DRIVE = High, I(T_{ON}) = 1mA	0.73	0.79	0.85	
Minimum Line Voltage for Fault	R_{ON} = 330k	60	80	100	V
Minimum Current I(T_{ON}) for Fault	R_{ON} = 330k		220		µA
On Time During Fault	C_T = 150pF, V_{LINE} = Min – 1V		2		µs
Oscillator Restart Delay after Fault			0.5		ms
V_{OUT} Error Amp					
V_{OUT} Regulated 12V (ADJ Open)	V_{CC} = 9V, I_{DCHG} = I(T_{OFF})/2	11.2	11.9	12.8	V
V_{OUT} Regulated 18V (ADJ = 0V)	V_{CC} = 9V, I_{DCHG} = I(T_{OFF})/2	16.5	17.5	19.5	V
Discharge Ratio: I_{DCHG} / I(T_{OFF})	I(T_{OFF}) = 50µA	0.93	1.00	1.07	
Voltage at T_{OFF}	I(T_{OFF}) = 50µA	0.6	0.95	1.3	V
Regulation gm (Note 1)	Max I_{DCHG} = 50µA		1.0		mA/V
	Max I_{DCHG} = 125µA	0.8	1.7	2.9	mA/V

Note 1: gm is defined as $\frac{\Delta I_{DCHG}}{\Delta V_{OUT}}$ for the values of V_{OUT} when V_{OUT} is in regulation. The two points used to calculate gm are for I_{DCHG} at 65% and 35% of its maximum value.

PIN DESCRIPTIONS

ADJ: The ADJ pin is used to provide a 12V or an 18V regulated supply without additional external components. To select the 12V option, ADJ pin is left open. To select the 18V option, ADJ pin must be grounded. For other output voltages less than 18V, a resistor divider between VOUT, ADJ and GND is needed. Note, however, that for output voltages less than VCC, the device needs additional bootstrapping to VCC from an external source such as the line voltage. If so, precautions must be taken to ensure that total ICC does not exceed 5mA.

CT (timing capacitor): The signal voltage across CT has a peak-to-peak swing of 3.7V for 9V VCC. As the voltage on CT crosses the oscillator upper threshold, DRIVE goes low. As the voltage on CT crosses the oscillator lower threshold, DRIVE goes high.

DRIVE: This output is a CMOS stage capable of sinking 200mA peak and sourcing 150mA peak. The output voltage swing is 0 to VCC.

GND (chip ground): All voltages are measured with respect to GND.

TOFF (regulated output control): TOFF sets the discharge current of the timing capacitor through an external resistor connected between VOUT and TOFF.

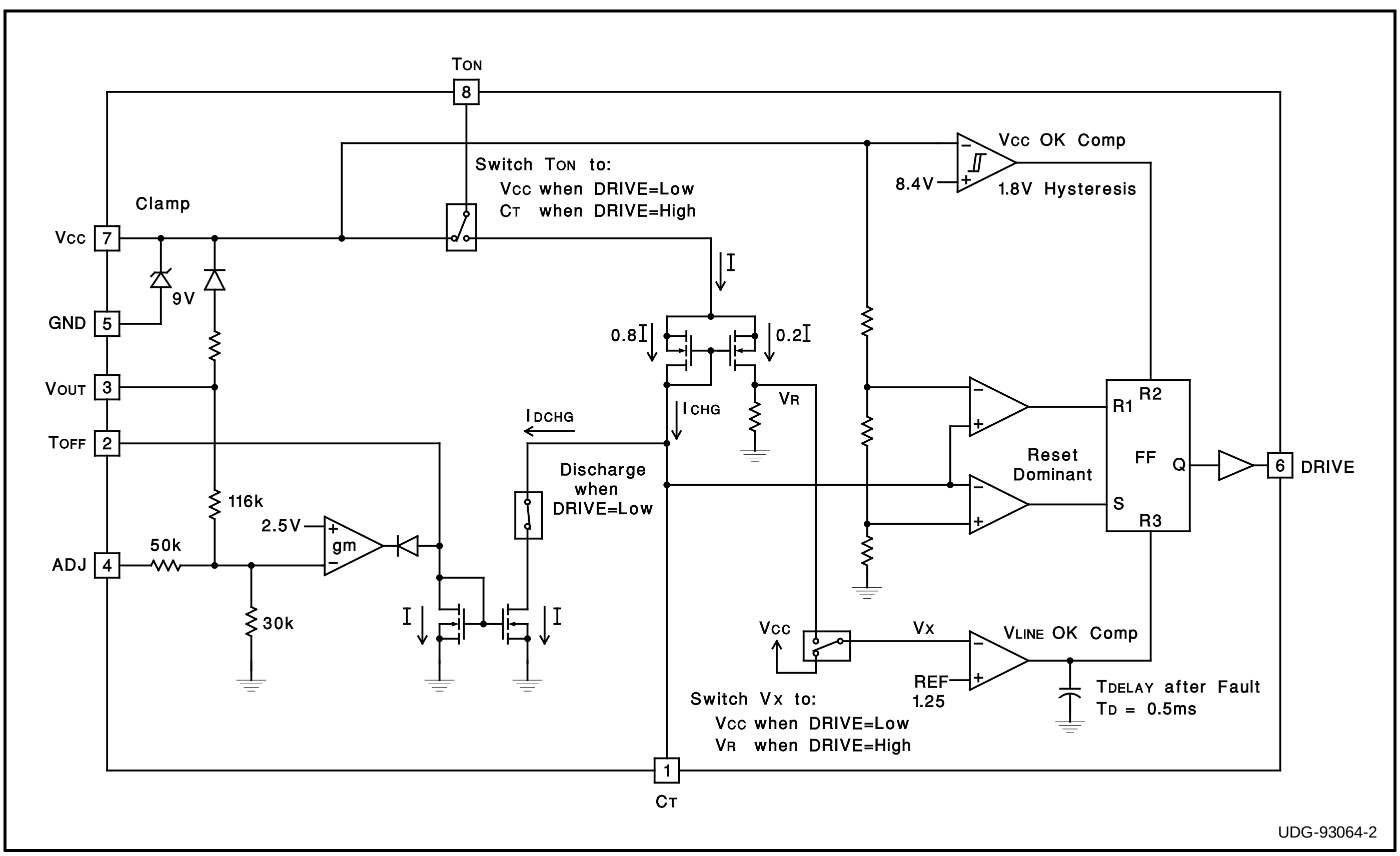
TON (line voltage control): TON serves three functions. When CT is discharging (off time), the current through TON is routed to VCC. When CT is charging (on time), the current through TON is split 80% to set the CT charge time and 20% to sense minimum line voltage which occurs for a TON current of 220µA. For a minimum line voltage of 80V, RON is 330kΩ.

The CT voltage slightly affects the value of the charge current during the on time. During this time, the voltage at the TON pin increases from approximately 2.5V to 6.5V.

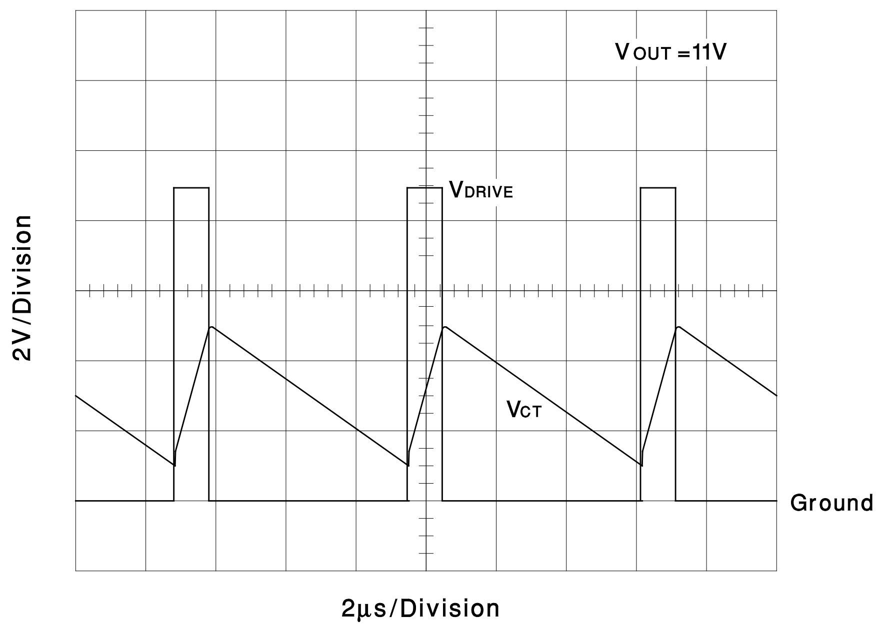
VCC (chip supply voltage): The supply voltage of the device at pin VCC is internally clamped at 9V. Normally, VCC is not directly powered from an external voltage source such as the line voltage. In the event that VCC is directly connected to a voltage source for additional bootstrapping, precautions must be taken to ensure that total ICC does not exceed 5mA.

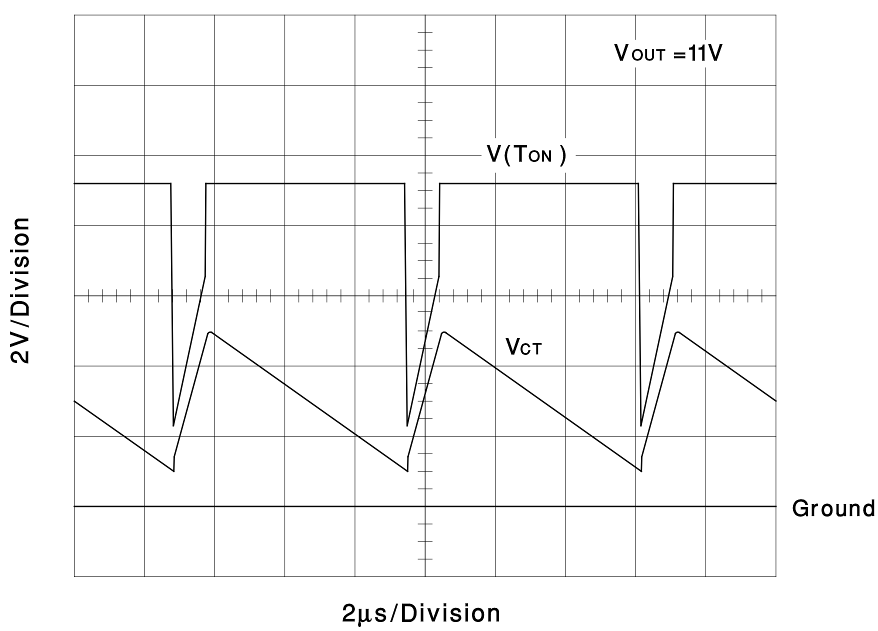
VOUT (regulated output): The VOUT pin is directly connected to the power supply output voltage. When VOUT is greater than VCC, VOUT bootstraps VCC.

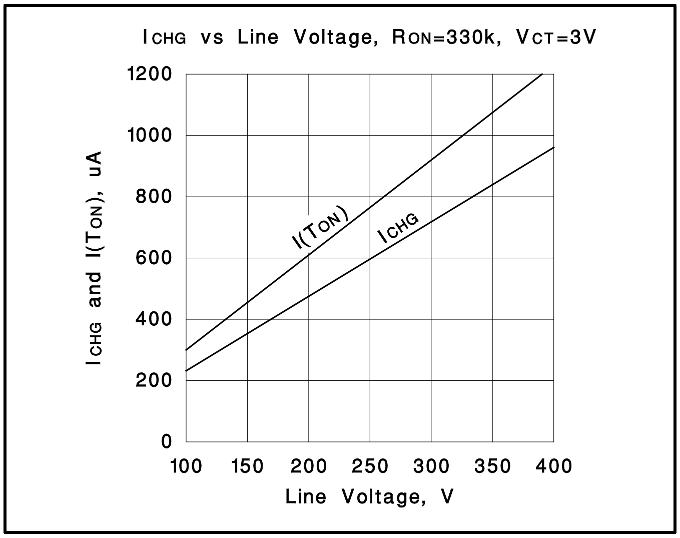
BLOCK DIAGRAM

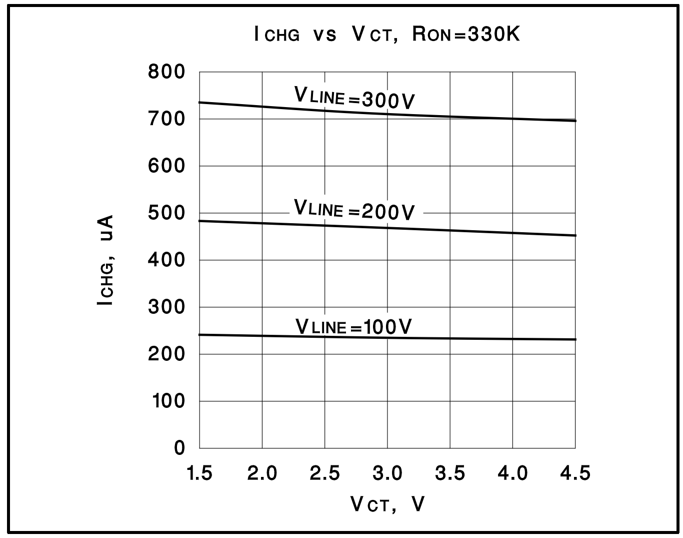


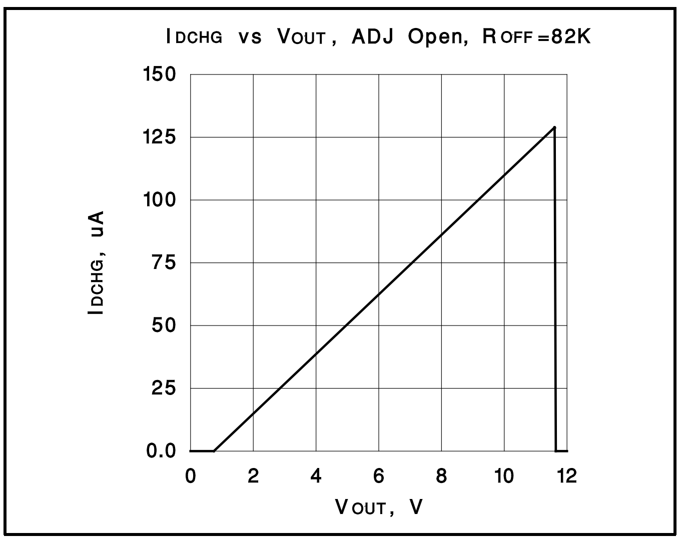
TYPICAL WAVEFORMS

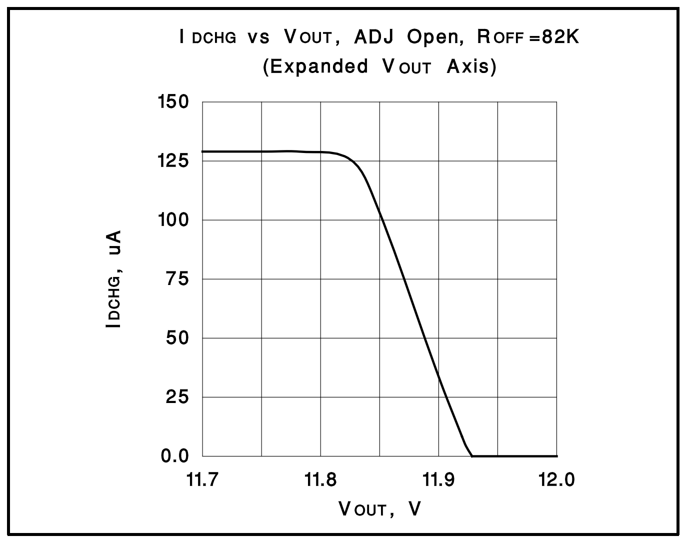


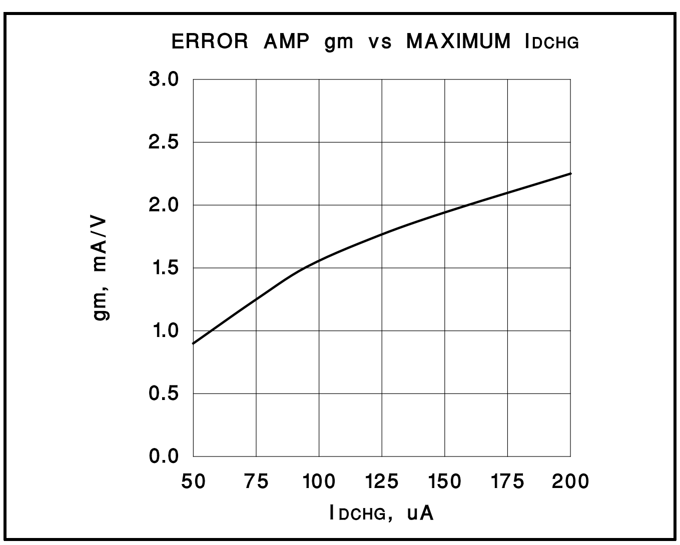


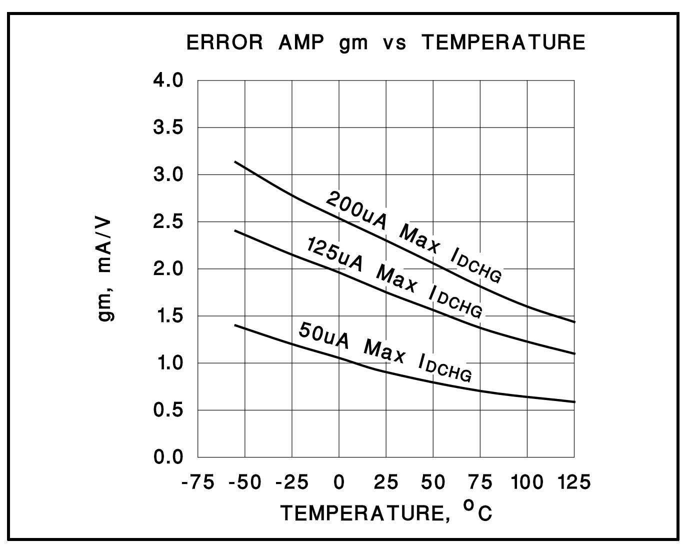












UNITRODE INTEGRATED CIRCUITS
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. 603-424-2410 • FAX 603-424-3460

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCC2889D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2889
UCC2889D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2889
UCC2889DTR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2889
UCC2889DTR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2889
UCC3889D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3889
UCC3889D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3889
UCC3889DG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3889
UCC3889DTR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3889
UCC3889DTR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3889

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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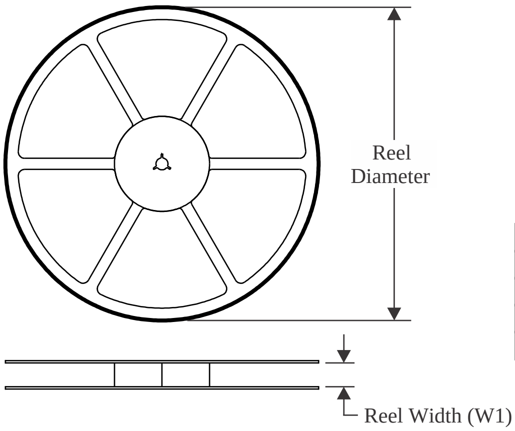
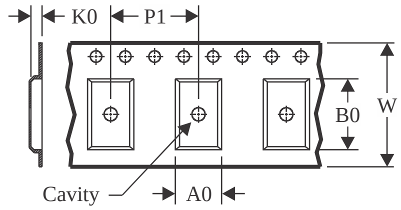
TAPE AND REEL INFORMATION

REEL DIMENSIONS

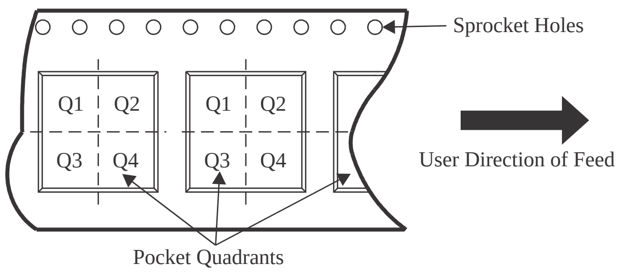


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

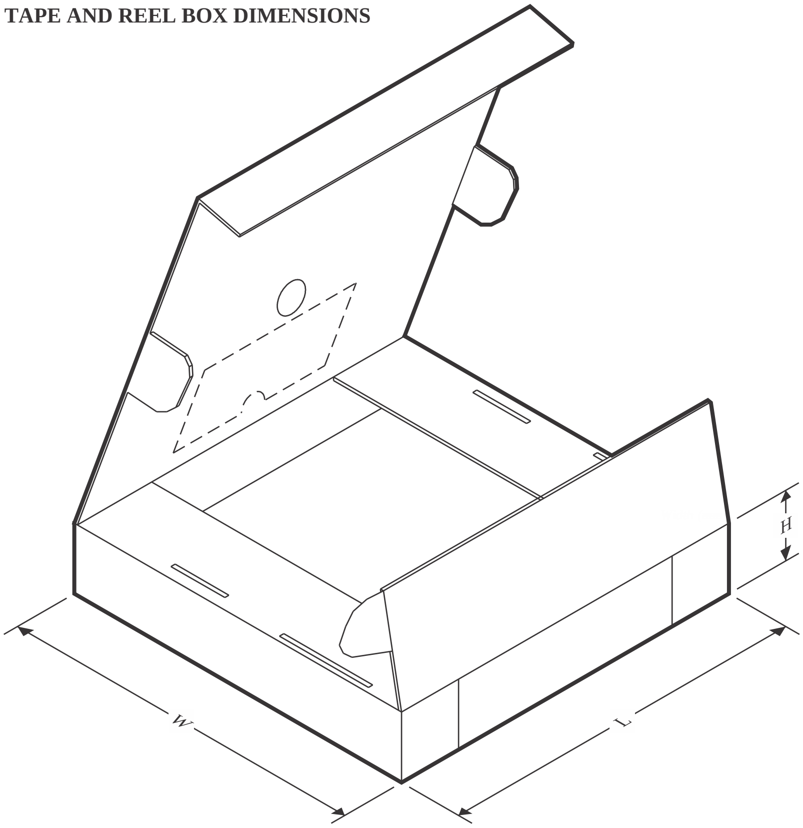
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2889DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3889DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

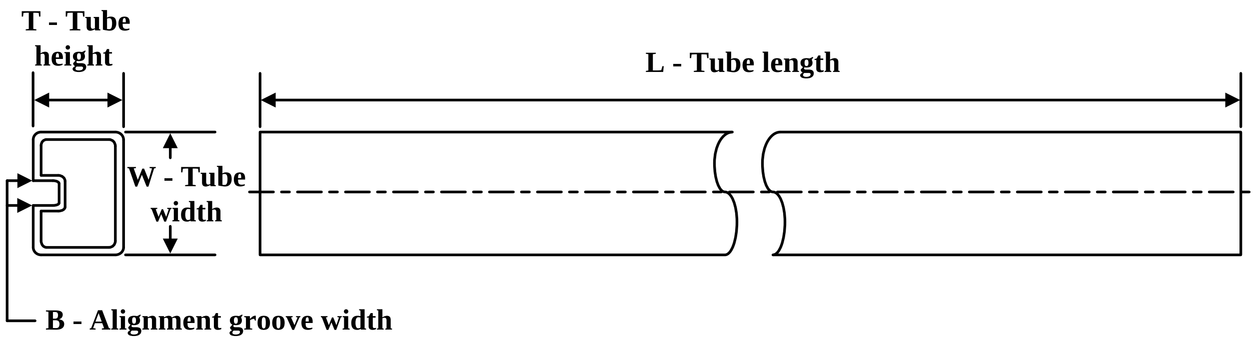
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

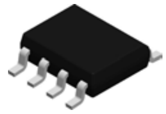
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2889DTR	SOIC	D	8	2500	353.0	353.0	32.0
UCC3889DTR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC2889D	D	SOIC	8	75	506.6	8	3940	4.32
UCC2889D.A	D	SOIC	8	75	506.6	8	3940	4.32
UCC3889D	D	SOIC	8	75	506.6	8	3940	4.32
UCC3889D.A	D	SOIC	8	75	506.6	8	3940	4.32
UCC3889DG4	D	SOIC	8	75	506.6	8	3940	4.32

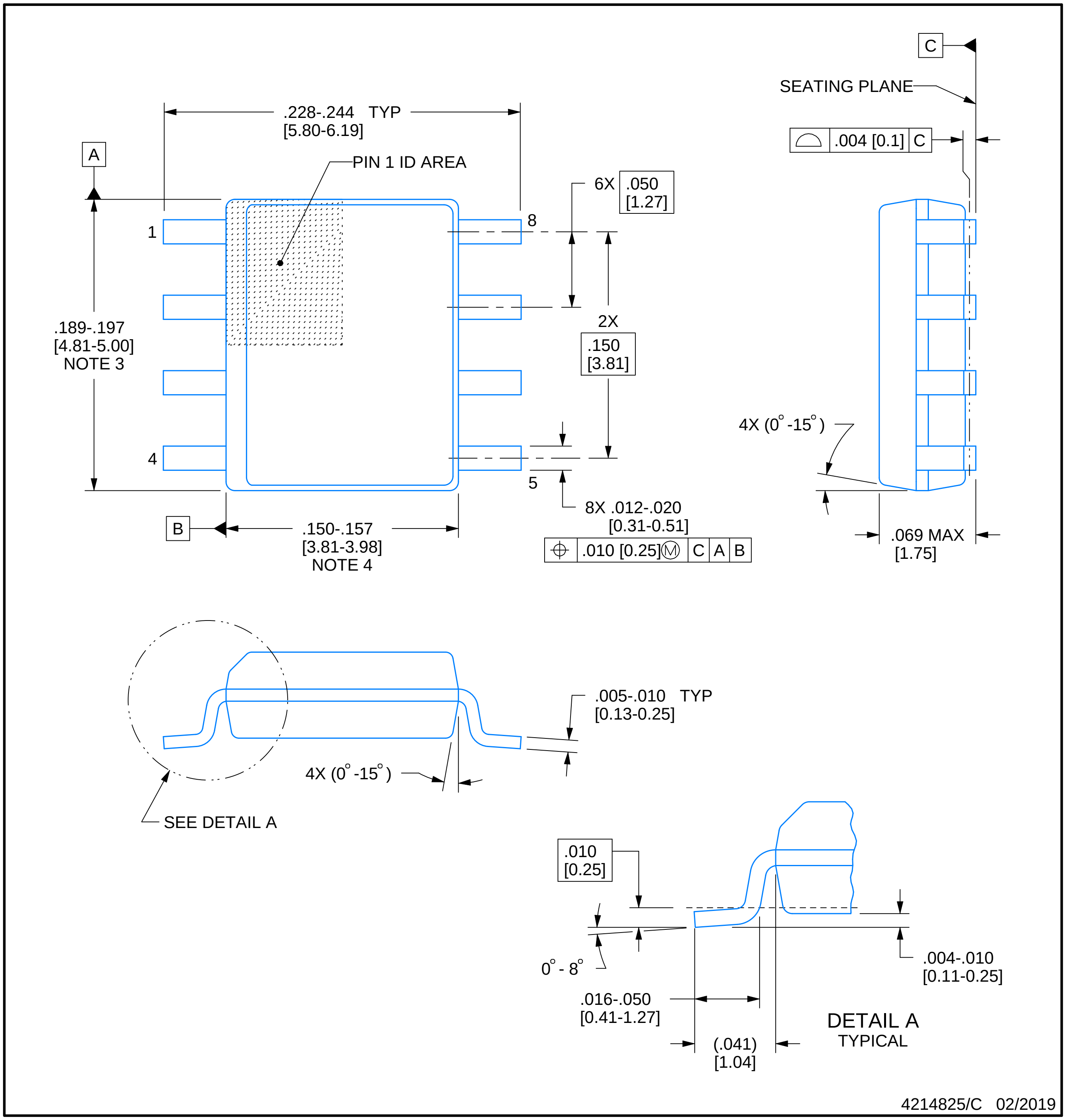


PACKAGE OUTLINE

D0008A

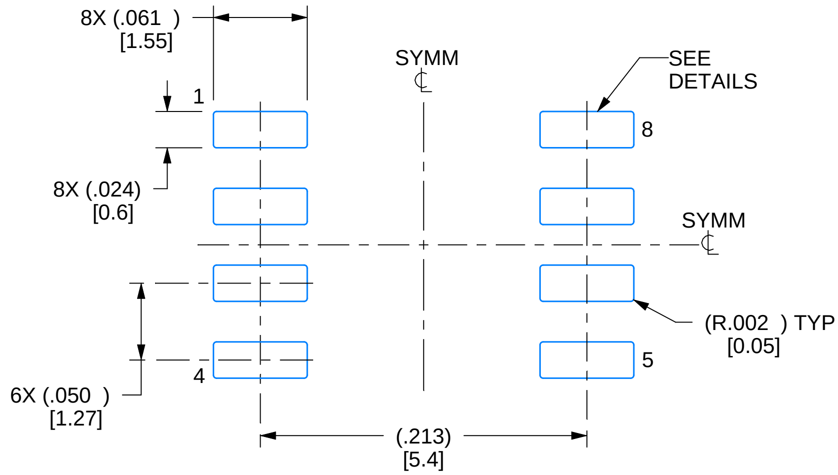
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

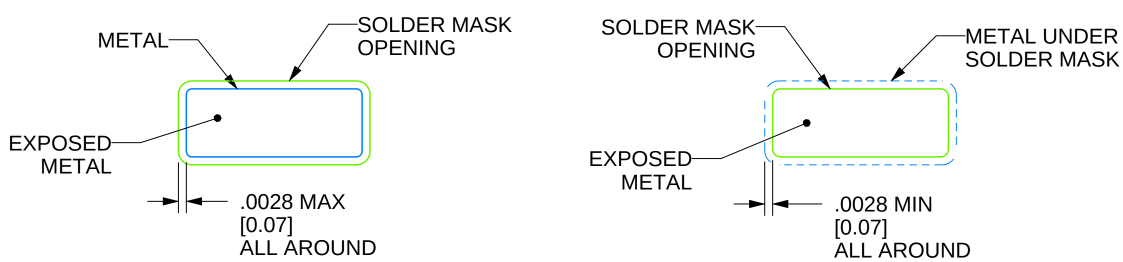


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

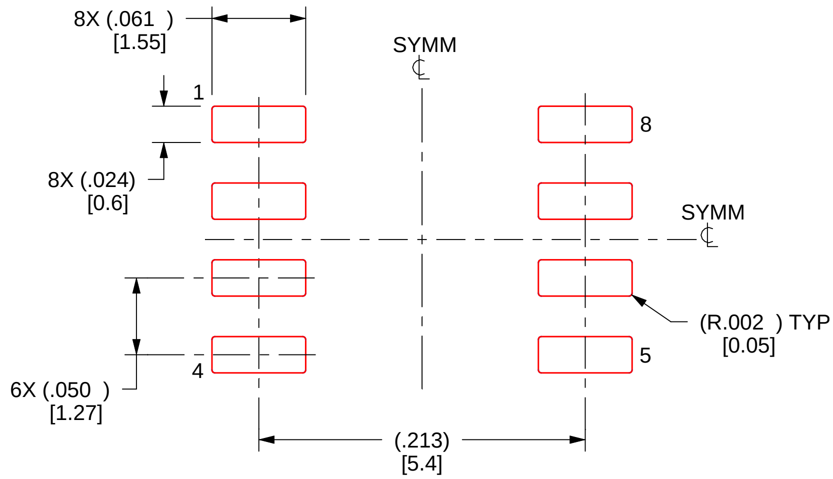
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265