
IGLOO2 and SmartFusion2 SoC FPGAs

Datasheet



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IGLOO2 and SmartFusion2 SoC FPGA AC/DC Electrical Characteristics

1. Introduction

Microsemi's mainstream SmartFusion[®]2 SoC and IGLOO[®]2 FPGA families integrate an industry standard 4-input look-up table-based (LUT) FPGA fabric with integrated mathblocks, multiple embedded memory blocks, and high-performance SERDES communications interfaces on a single chip. Both families benefit from low power flash technology and are the most secure and reliable FPGAs in the industry. These next generation devices offer up to 150K Logic Elements, up to five MB of embedded RAM, up to 16 SERDES lanes, and up to four PCI Express Gen 2 endpoints, as well as integrated hard DDR3 memory controllers with error correction.

SmartFusion2 devices integrate an entire low power real time Microcontroller Subsystem with a rich set of Industry standard peripherals including Ethernet, USB, and CAN, while IGLOO2 devices integrate a high performance memory subsystem with on-chip flash, 32 kbyte embedded SRAM, and multiple DMA controllers.

2. Device Status

Table 1 • IGLOO2 and SmartFusion2 SoC FPGAs Device Status

M2GL and M2S Devices	Status
005, 005S	Preliminary
010, 010S, 010T, 010TS	Preliminary
025, 025S, 025T, 025TS	Preliminary
050, 050T	Production*
090, 090S, 090T, 090TS	Advance
100, 100S, 100T, 100TS	Advance
150, 150S, 150T, 150TS	Advance
<i>Note: *Power numbers are Preliminary</i>	

3. Product Briefs and Pin Descriptions

The product brief and pin descriptions are published separately:

[IGLOO2 Product Brief](#)

[IGLOO2 Pin Descriptions](#)

[SmartFusion2 SoC FPGA Product Brief](#)

[SmartFusion2 Pin Descriptions](#)

4. General Specifications

4.1. Operating Conditions

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in [Table 2](#) is not implied.

Table 2 • Absolute Maximum Ratings

Symbol	Parameter	Limits		Units	Notes
		Min.	Max.		
VDD	DC core supply voltage. Must always power this pin.	−0.3	1.32	V	
VPP	Power supply for charge pumps (for normal operation and programming). Must always power this pin.	−0.3	3.63	V	
MSS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	−0.3	3.63	V	
HPMS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	−0.3	3.63	V	
FDDR_PLL_VDDA	Analog power pad for FDDR PLL	−0.3	3.63	V	
PLL0_PLL1_MSS_MDDR_VDDA	Analog power pad for MDDR PLL	−0.3	3.63	V	
PLL0_PLL1_HPMS_MDDR_VDDA	Analog power pad for MDDR PLL	−0.3	3.63	V	
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0–5	−0.3	3.63	V	
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	−0.3	3.63	V	
SERDES_[01]_L[0123]_VDDAPLL	Analog power for SERDES[01] PLL lane0 to lane3. This is a +2.5 V SERDES internal PLL supply.	−0.3	2.75	V	
SERDES_[01]_L[0123]_VDDAIO	Tx/Rx analog I/O voltage. Low voltage power for the lanes of SERDESIF0. This is a +1.2 V SERDES PMA supply.	−0.3	1.32	V	
SERDES_[01]_VDD	PCIe®/PCS power supply	−0.3	1.32	V	
VDDIx	DC FPGA I/O buffer supply voltage for MSIO I/O Bank	−0.3	3.63	V	
	DC FPGA I/O buffer supply voltage for MSIOD/DDRIO I/O Banks	−0.3	2.75	V	
VI	I/O Input voltage for MSIO I/O Bank	−0.3	3.63	V	
	I/O Input voltage for MSIOD/DDRIO I/O Bank	−0.3	2.75	V	
VPPNVM	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.	−0.3	3.63	V	
T _{STG}	Storage temperature	−65	150	°C	1
T _J	Junction temperature	–	125	°C	

Note:

1. For flash programming and retention maximum limits, refer to [Table 4 on page 13](#). For recommended operating conditions, refer to [Table 3 on page 12](#).

Table 3 • Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
T_J	Operating junction temperature	Commercial	0	25	85	°C	
		Industrial	–40	25	100	°C	
	Programming junction temperatures	Commercial	0	25	85	°C	
		Industrial	0	25	85	°C	
VDD	DC core supply voltage. Must always power this pin.		1.14	1.2	1.26	V	
VPP 005,010,025,050 devices	Power supply for charge pumps (for normal operation and programming)	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
VPP 090,100,150 devices	Power supply for charge pumps (for normal operation and programming)	3.3 V range	3.15	3.3	3.45	V	
MSS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
HPMS_MDDR_PLL_VDDA	Analog power pad for MDDR PLL	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
FDDR_PLL_VDDA	Analog power pad for FDDR PLL	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
PLL0_PLL1_MSS_MDDR_VDDA	Analog power pad for MDDR PLL	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
PLL0_PLL1_HPMS_MDDR_VDDA	Analog power pad for MDDR PLL	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
CCC_XX[01]_PLL_VDDA	Analog power pad for PLL0 to PLL5	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
SERDES_[01]_PLL_VDDA	High supply voltage for PLL SERDES[01]	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
SERDES_[01]_L[0123]_VDDAPLL	Analog power for SERDES[01] PLL Lane0 to Lane3. This is a +2.5 V SERDES internal PLL supply.		2.375	2.5	2.625	V	
SERDES_[01]_L[0123]_VDDAIO	Tx/Rx analog I/O voltage. Low voltage power for the lanes of SERDESIF0. This is a +1.2 V SERDES PMA supply.		1.14	1.2	1.26	V	
SERDES_[01]_VDD	PCIe/PCS power supply		1.14	1.2	1.26	V	
VDDIx	1.2 V DC supply voltage		1.14	1.2	1.26	V	
	1.5 V DC supply voltage		1.425	1.5	1.575	V	
	1.8 V DC supply voltage		1.71	1.8	1.89	V	
	2.5 V DC supply voltage		2.375	2.5	2.625	V	
	3.3 V DC supply voltage		3.15	3.3	3.45	V	
	LVDS differential I/O		2.375	2.5	3.45	V	
	B-LVDS, M-LVDS, Mini-LVDS, RSDS differential I/O		2.375	2.5	2.625	V	
	LVPECL differential I/O		3.15	3.3	3.45	V	

Table 3 • Recommended Operating Conditions (continued)

VREFx	Reference voltage supply for FDDR (bank 0) and MDDR (bank 5)		0.49 * VDDIx	0.5 * VDDIx	0.51 * VDDIx	V	
VPPNVM 005,010,025,050 devices	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	
VPPNVM 090,100,150 devices	Analog sense circuit supply of embedded nonvolatile memory (eNVM). Must be shorted to VPP.	2.5 V range	2.375	2.5	2.625	V	
		3.3 V range	3.15	3.3	3.45	V	

Note: Power supply ramps must all be strictly monotonic, without plateaus.

Table 4 • FPGA and Embedded Flash Programming, Storage, and Operating Limits

Product Grade	Storage Temperature	Programming Temperature	Element	Grade Programming Cycles	Retention
Commercial	Min. T _J = 0°C Max. T _J = 85°C	Min. T _J = 0°C Max. T _J = 85°C	FPGA	500	20 years
		Min. T _J = 0°C Max. T _J = 85°C	Embedded flash	< 1,000	20 years
				< 10,000	10 years
Industrial	Min. T _J = -40°C Max. T _J = 100°C	Min. T _J = 0°C Max. T _J = 85°C	FPGA	500	20 years
		Min. T _J = -40°C Max. T _J = 100°C	Embedded flash	< 1,000	20 years
				< 10,000	10 years

4.2. Overshoot/Undershoot Limits

For AC signals, the input signal may undershoot during transitions to -1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100mA.

For AC signals, the input signal may overshoot during transitions to VCCI + 1.0 V for no longer than 10% of the period. The current during the transition must not exceed 100mA.

Note: The above specification does not apply to the PCI standard. The IGLOO2 and SmartFusion2 PCI I/Os are compliant to the PCI standard including the PCI overshoot/undershoot specifications.

4.3. Thermal Characteristics

4.3.1. Introduction

The temperature variable in the Microsemi SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance

θ_{JB} = Junction-to-board thermal resistance

θ_{JC} = Junction-to-case thermal resistance

T_J = Junction temperature

T_A = Ambient temperature

T_B = Board temperature (measured 1.0 mm away from the package edge)

T_C = Case temperature

P = Total power dissipated by the device

Table 5 • Package Thermal Resistance

Product M2GL/M2S	θ_{JA}			θ_{JC}	θ_{JB}	Units
	Still Air	1.0 m/s	2.5 m/s			
005						
FG484	19.36	15.81	14.63	9.74	5.27	°C/W
VF400	20.19	16.94	15.41	8.86	4.95	°C/W
010						
FG484	18.22	14.83	13.62	8.83	4.92	°C/W
VF400	19.40	15.75	14.22	8.11	4.22	°C/W
025						
FG484	17.03	13.66	12.45	7.66	4.18	°C/W
VF400	18.36	14.89	13.36	7.12	3.41	°C/W
FCS325	29.17	24.87	23.12	14.44	2.31	°C/W
050						
FG484	15.29	12.19	10.99	6.27	3.24	°C/W
FG896	14.70	12.50	10.90	7.20	4.90	°C/W
VF400	17.53	14.17	12.63	3.32	2.81	°C/W
FCS325	27.38	23.18	21.41	12.47	1.59	°C/W
090						
FG484	14.64	11.37	10.16	5.43	2.77	°C/W
FG676	14.52	11.19	10.37	6.83	3.24	°C/W
100						
FC1152	9.08	6.81	5.87	2.56	0.38	°C/W
150						
FC1152	9.08	6.81	5.87	2.56	0.38	°C/W

4.3.2. Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution, but it is useful for comparing the thermal performance of one package to another.

The maximum power dissipation allowed is calculated using EQ 4.

$$\text{Maximum Power Allowed} = \frac{T_{J(\text{MAX})} - T_{A(\text{MAX})}}{\theta_{JA}}$$

EQ 4

The absolute maximum junction temperature is 100°C. EQ 5 shows a sample calculation of the absolute maximum power dissipation allowed for the M2GL050T-FG896 package at commercial temperature and in still air, where

$$\theta_{JA} = 14.7^{\circ}\text{C/W (taken from Table 5 on page 15).}$$

$$T_A = 85^{\circ}\text{C}$$

$$\text{Maximum Power Allowed} = \frac{100^{\circ}\text{C} - 85^{\circ}\text{C}}{14.7^{\circ}\text{C/W}} = 1.088 \text{ W}$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package.

If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

4.3.3. Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

4.3.4. Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

5. Calculating Power Dissipation

5.1. Quiescent Supply Current

Table 6 • Quiescent Supply Current Characteristics

Power Supplies/Blocks	Modes and Configurations		Notes
	Non-Flash*Freeze mode	Flash*Freeze mode	
FPGA Core	On	Off	
VDD / SERDES_[01]_VDD	On	On	1
VPP / VPPNVM	On	On	
HPMS_MDDR_PLL_VDDA / FDDR_PLL_VDDA/ CCC_XX[01]_PLL_VDDA / PLL0_PLL1_HPMS_MDDR_VDDA	0 V	0 V	
SERDES_[01]_PLL_VDDA	0 V	0 V	3
SERDES_[01]_L[0123]_VDDAPLL / VDD_2V5	On	On	3
SERDES_[01]_L[0123]_VDDAIO	On	On	3
VDDIx	On	On	2, 4
VREFx	On	On	
RAM	On	Sleep state	
System Controller	50 MHz	50 MHz	
50 MHz Oscillator (enable/disable)	Enabled	Disabled	
1 MHz Oscillator (enable/disable)	Disabled	Disabled	
Crystal Oscillator (enable/disable)	Disabled	Disabled	

Notes:

- SERDES_[01]_VDD Power Supply is shorted to VDD.
- VDDIx has been set to ON for test conditions as described. Banks on the east side should always be powered with the appropriate VDDI Bank supplies. For details on bank power supplies, refer to the "Recommendation for Unused Bank Supplies" table in the [SmartFusion2 Board Design Guidelines](#) and [IGLOO2 Board Design Guidelines](#) application notes.
- SERDES and DDR blocks to be unused.
- No Differential (i.e. LVDS) I/O's or ODT attributes to be used.

Table 7 • SmartFusion2 and IGLOO2 Quiescent Supply Current

Parameter	Modes	Conditions ¹	005	010	025	050	090	100	150	Units	
			Typical Process								
			VDD=1.2 V	VDD=1.2 V	VDD=1.2 V	VDD=1.2 V	VDD=1.2 V	VDD=1.2 V	VDD=1.2 V		
IDC1	Non-Flash*Freeze	Typical	5.4	6.6	8.6	11.4	15.0	21.7	21.7	mA	
		Commercial	17.4	25.0	36.4	52.3	72.8	112.2	112.2	mA	
		Industrial	25.1	36.6	54.0	78.1	109.4	169.4	169.4	mA	
IDC2	Flash*Freeze	Typical	1.6	2.2	2.8	3.2	4.2	5.2	5.2	mA	
		Commercial	10.8	15.2	19.6	21.8	29.0	35.6	35.6	mA	
		Industrial	16.6	23.4	30.1	33.6	44.7	54.8	54.8	mA	

Notes:

- Typical conditions are at 25°C, Commercial conditions are at 85°C, and Industrial conditions are at 100°C.
- The power numbers are preliminary.

6. Average Fabric Temperature and Voltage Derating Factors

Table 8 • Average Temperature and Voltage Derating Factors for Fabric Timing Delays
(normalized to $T_J = 85^\circ\text{C}$, worst-case $V_{DD} = 1.14\text{ V}$)

Array Voltage V_{DD} (V)	Junction Temperature ($^\circ\text{C}$)					
	-40°C	0°C	25°C	70°C	85°C	100°C
1.14	0.94	0.96	0.97	0.99	1.00	1.01
1.2	0.85	0.87	0.87	0.90	0.91	0.91
1.26	0.78	0.79	0.80	0.82	0.83	0.84

7. Timing Model

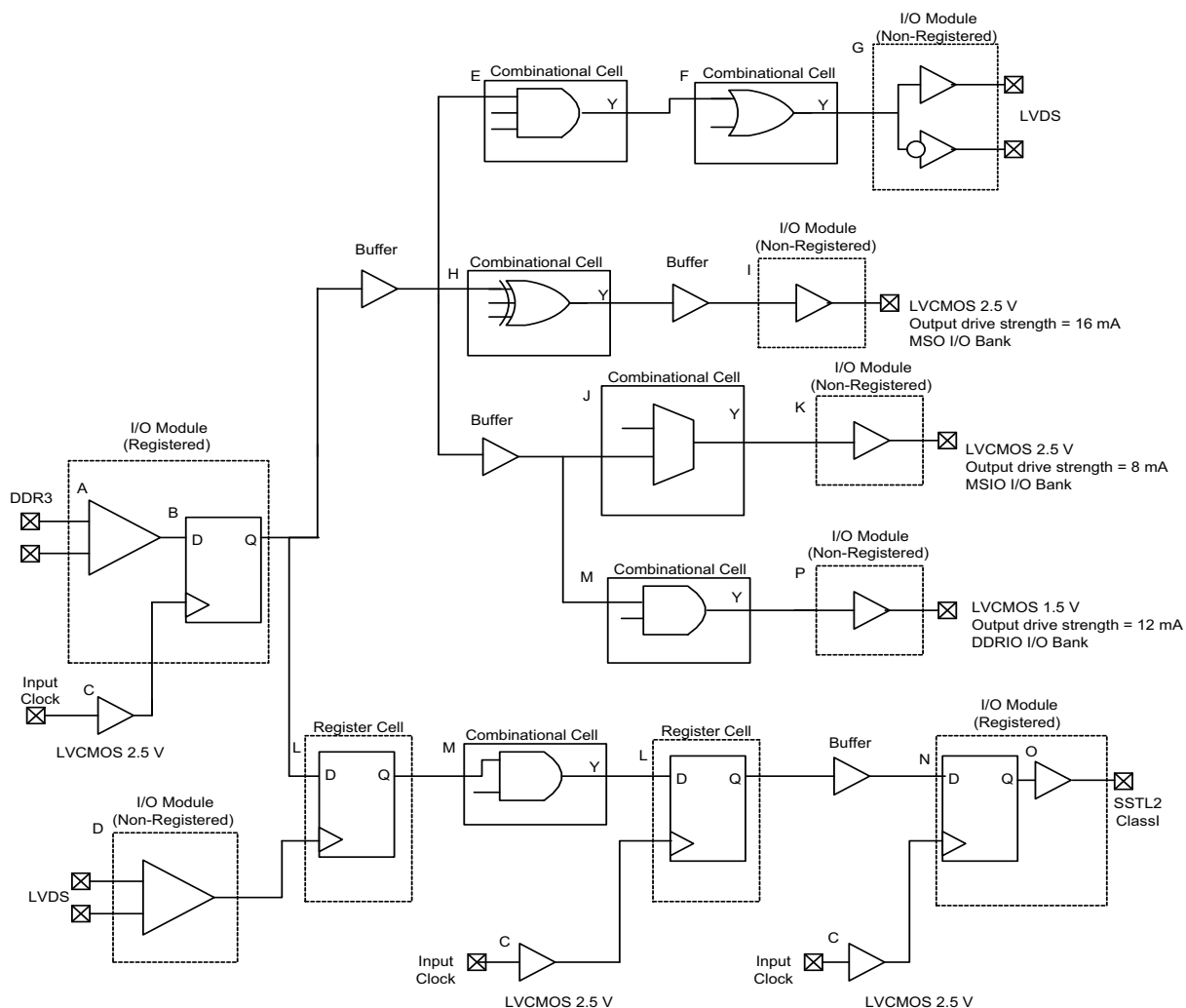


Figure 1 • Timing Model

Table 9 • Timing Model ParametersWorst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Index	Parameter	Description	-1	Units	For more information
A	t_{PY}	Propagation delay of DDR3 receiver	1.605	ns	Refer to page 55
B	t_{iCLKQ}	Clock-to-Q of the Input Data Register	0.16	ns	Refer to page 71
	t_{iSUD}	Setup Time of the Input Data Register	0.357	ns	Refer to page 71
C	t_{RCKH}	Input High Delay for Global Clock	0.897	ns	Refer to page 84
	t_{RCKL}	Input Low Delay for Global Clock	1.53	ns	Refer to page 84
D	t_{PY}	Input Propagation Delay of LVDS Receiver	2.774	ns	Refer to page 60
E	t_{DP}	Propagation Delay of a three-input AND Gate	0.198	ns	Refer to page 81
F	t_{DP}	Propagation Delay of an OR Gate	0.179	ns	Refer to page 81
G	t_{DP}	Propagation Delay of an LVDS Transmitter	2.136	ns	Refer to page 60
H	t_{DP}	Propagation Delay of a three-input XOR Gate	0.241	ns	Refer to page 81
I	t_{DP}	Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 16 mA on the MSIO Bank	2.412	ns	Refer to page 29
J	t_{DP}	Propagation Delay of a two-input NAND Gate	0.179	ns	Refer to page 81
K	t_{DP}	Propagation Delay of LVCMOS 2.5 V Transmitter, Drive strength of 8 mA on the MSIO Bank	2.309	ns	Refer to page 29
L	t_{CLKQ}	Clock-to-Q of the Data Register	0.108	ns	Refer to page 83
	t_{SUD}	Setup Time of the Data Register	0.254	ns	Refer to page 83
M	t_{DP}	Propagation Delay of a two-input AND Gate	0.179	ns	Refer to page 81
N	t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.263	ns	Refer to page 74
	t_{OSUD}	Setup Time of the Output Data Register	0.19	ns	Refer to page 74
O	t_{DP}	Propagation Delay of SSTL2, Class I Transmitter on the MSIO Bank	2.055	ns	Refer to page 49
P	t_{DP}	Propagation Delay of LVCMOS 1.5 V Transmitter, Drive strength of 12 mA, fast slew on the DDRIO Bank	3.316	ns	Refer to page 37

8. User I/O Characteristics

There are three types of I/Os supported in the IGLOO2 and SmartFusion2 FPGA Families: MSIO, MSIOD, and DDRIO I/O banks. The I/O standards supported by the different I/O banks is described in the "I/Os" section of the *IGLOO2 FPGA Fabric Architecture User Guide* or the *SmartFusion2 FPGA Fabric Architecture User Guide*.

8.1. Input Buffer and AC Loading

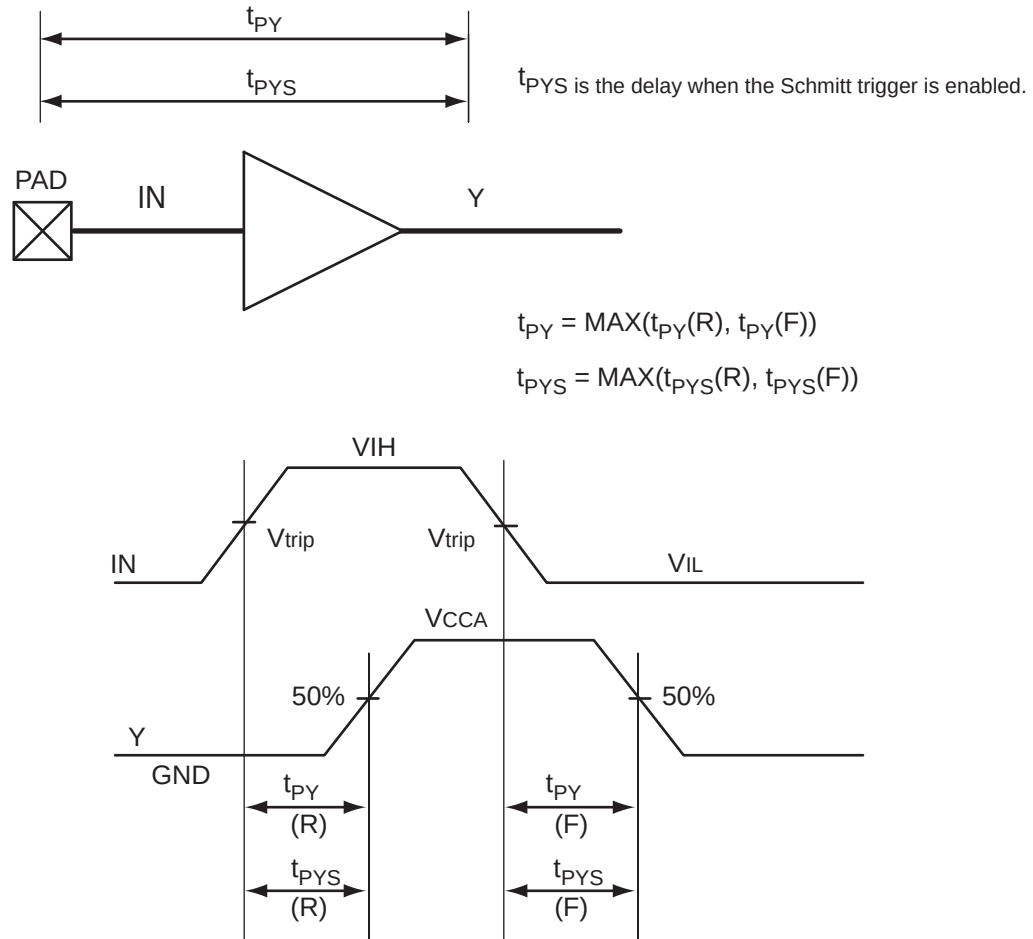


Figure 2 • Input Buffer AC Loading

8.2. Output Buffer and AC Loading

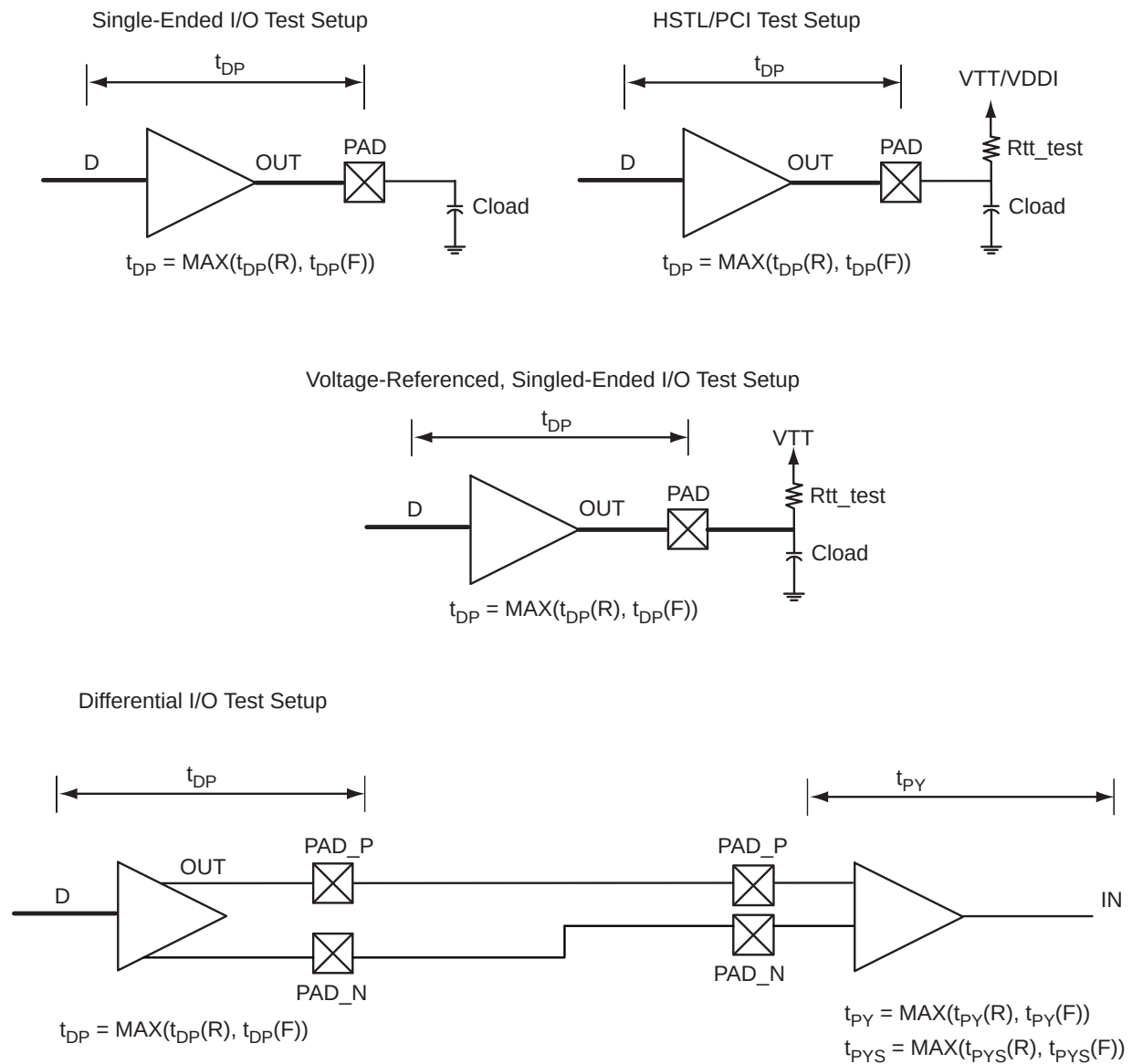


Figure 3 • Output Buffer AC Loading

8.3. Tristate Buffer and AC Loading

The tristate path for enable path loadings is described in the respective specifications. The methodology of characterization is illustrated by the enable path test point shown in Figure 4.

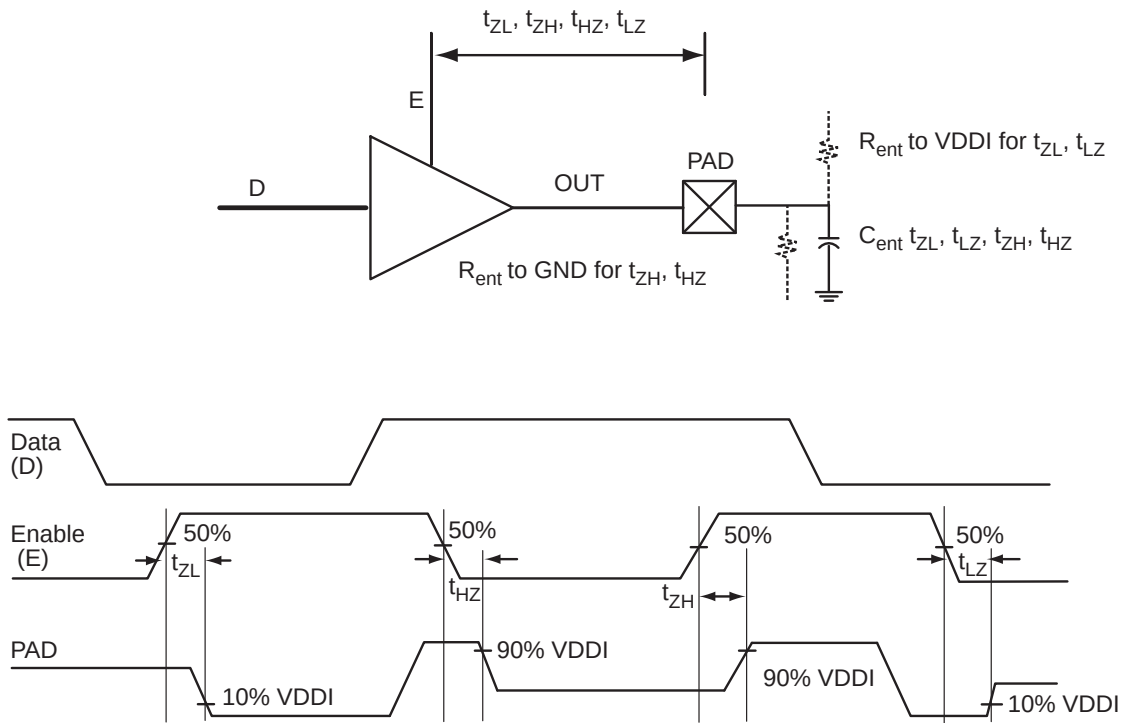


Figure 4 • Tristate Buffer for Enable Path Test Point

8.4. Detailed I/O Characteristics

Table 10 • Input Capacitance

Symbol	Definition	Minimum	Maximum	Units
C _{IN}	Input capacitance	–	10	pF

Table 11 • I/O Weak Pull-Up/Pull-Down Resistances for DDRIO I/O Bank
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level

VDDI Domain	DDRIO I/O Bank				Notes
	R(WEAK PULL-UP) at VOH (Ω)		R(WEAK PULL-DOWN) at VOL (Ω)		
	Min.	Max.	Min.	Max.	
3.3 V	N/A	N/A	N/A	N/A	—
2.5 V	10k	15.1k	9.98k	15.3k	1, 2
1.8 V	10.3k	16.2k	10.3k	16.6k	1, 2
1.5 V	10.6k	17.2k	10.6k	17.9k	1, 2
1.2 V	11.1k	19.3k	11.2k	20.9k	1, 2

Notes:

1. $R(\text{WEAK PULL-DOWN}) = (V_{OL\text{spec}}) / I(\text{WEAK PULL-DOWN MAX})$
2. $R(\text{WEAK PULL-UP}) = (V_{DDI\text{max}} - V_{OH\text{spec}}) / I(\text{WEAK PULL-UP MIN})$

Table 12 • I/O Weak Pull-Up/Pull-Down Resistances for MSIO I/O Bank
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level

VDDI Domain	MSIO I/O Bank				Notes
	R(WEAK PULL-UP) at VOH (Ω)		R(WEAK PULL-DOWN) at VOL (Ω)		
	Min.	Max.	Min.	Max.	
3.3 V	9.9k	14.5k	9.98k	14.9k	–
2.5 V	10k	15k	10.1k	15.6k	1, 2
1.8 V	10.4k	16.2k	10.4k	17.3k	1, 2
1.5 V	10.7k	17.3k	10.8k	18.9k	1, 2
1.2 V	11.3k	19.7k	11.5k	22.7k	1, 2

Notes:

1. $R(\text{WEAK PULL-DOWN}) = (V_{OL\text{spec}}) / I(\text{WEAK PULL-DOWN MAX})$
2. $R(\text{WEAK PULL-UP}) = (V_{DDI\text{max}} - V_{OH\text{spec}}) / I(\text{WEAK PULL-UP MIN})$

Table 13 • I/O Weak Pull-Up/Pull-Down Resistances for MSIOD I/O Bank
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values at VOH/VOL Level

VDDI Domain	MSIOD I/O Bank				Notes
	R(WEAK PULL-UP) at VOH (Ω)		R(WEAK PULL-DOWN) at VOL (Ω)		
	Min.	Max.	Min.	Max.	
3.3 V	N/A	N/A	N/A	N/A	—
2.5 V	9.6k	14.1k	9.5k	13.9k	1, 2
1.8 V	9.7k	14.7k	9.7k	14.5k	1, 2
1.5 V	9.9k	15.3k	9.8k	15k	1, 2
1.2 V	10.3k	16.7k	10k	16.2k	1, 2

Notes:

1. $R(\text{WEAK PULL-DOWN}) = (V_{OL\text{spec}}) / I(\text{WEAK PULL-DOWN MAX})$
2. $R(\text{WEAK PULL-UP}) = (V_{DDI\text{max}} - V_{OH\text{spec}}) / I(\text{WEAK PULL-UP MIN})$

Table 14 • Schmitt Trigger Input Hysteresis
Hysteresis Voltage Value for Schmitt Trigger Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typical, unless otherwise noted)
3.3 V LVTTTL / LVCMOS / PCI / PCI-X	$0.05 \times V_{DDI}$ (worst-case)
2.5 V LVCMOS	$0.05 \times V_{DDI}$ (worst-case)
1.8 V LVCMOS	$0.1 \times V_{DDI}$ (worst-case)
1.5 V LVCMOS	60 mV
1.2 V LVCMOS	20 mV

8.5. Single-Ended I/O Standards

8.5.1. Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)

LVCMOS is a widely used switching standard implemented in CMOS transistors. This standard is defined by JEDEC (JESD 8-5). The LVCMOS standards supported in IGLOO2 and SmartFusion2 SoC FPGAs are LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33.

8.5.2. 3.3 V LVCMOS/LVTTTL

LVCMOS 3.3 V or Low-Voltage Transistor-Transistor Logic (LVTTTL) is a general standard for 3.3 V applications.

8.5.2.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 15 • LVTTTL/LVCMOS 3.3 V DC Voltage Specification (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVTTTL/LVCMOS 3.3 V Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	
LVTTTL/LVCMOS 3.3 V DC Input Voltage Specification							
V _{IH} (DC)	DC input logic High		2.0	—	3.45	V	
V _{IL} (DC)	DC input logic Low		−0.3	—	0.8	V	
I _{IH} (DC)	Input current High		—	—	10	μA	

Note: 1. The VOH/VOL test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

Table 15 • LVTTL/LVCMOS 3.3 V DC Voltage Specification (Applicable to MSIO I/O Bank Only) (continued)

IIL (DC)	Input current Low	–	–	10	μA	
LVCMOS 3.3 V DC Output Voltage Specification						
VOH	DC output logic High	VDDI – 0.4	–	–	V	1
VOL	DC output logic Low	–	–	0.4	V	1
LVTTL 3.3 V DC Output Voltage Specification						
VOH	DC output logic High	2.4	–	–	V	
VOL	DC output logic Low	–	–	0.4	V	

Note: 1. The VOH/VOL test points selected ensure compliance with LVCMOS 3.3 V JESD8-B requirements.

Table 16 • LVTTL/LVCMOS 3.3 V AC Specifications (Applicable to MSIO I/O Bank Only)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVTTL/LVCMOS 3.3 V Maximum Switching Speed							
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	600	Mbps	
LVTTL/LVCMOS 3.3 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	1.4	–	V	
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

Table 17 • LVTTTL/LVCMOS 3.3 V Transmitter Drive Strength Specifications

Output Drive Selection	VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA	Notes
MSIO I/O Bank					
2 mA	VDDI – 0.4	0.4	2	2	
4 mA	VDDI – 0.4	0.4	4	4	
8 mA	VDDI – 0.4	0.4	8	8	
12 mA	VDDI – 0.4	0.4	12	12	
16 mA	VDDI – 0.4	0.4	16	16	
20 mA	VDDI – 0.4	0.4	20	20	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

8.5.2.2 AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, VDD = 1.14 V, VDDI = 3.0 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 18 • LVTTTL/LVCMOS 3.3 V Receiver Characteristics

Worst-Case Commercial Conditions: $T_J = 85^{\circ}\text{C}$, VDD = 1.14 V, Worst-Case VDDI

	On-Die Termination (ODT)	t_{PY}		t_{PYS}		Units
		–1	Std.	–1	Std.	
LVTTTL/LVCMOS 3.3 V (for MSIO I/O Bank)	None	2.262	2.663	2.289	2.695	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 19 • LVTTTL/LVCMOS 3.3 V Transmitter Characteristics

Worst-Case Commercial Conditions: $T_J = 85^{\circ}\text{C}$, VDD = 1.14 V, Worst-Case VDDI

Output Drive Selection	Slew Control	t _{DP} [*]		t _{ZL}		t _{ZH}		t _{HZ}		t _{LZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVTTTL/LVCMOS 3.3 V (for MSIO I/O Bank)												
2 mA	Slow	3.192	3.755	3.47	4.083	2.969	3.494	1.856	2.183	3.337	3.926	ns
4 mA	Slow	2.331	2.742	2.673	3.145	2.526	2.973	3.034	3.569	4.451	5.236	ns
8 mA	Slow	2.135	2.511	2.33	2.741	2.297	2.703	4.532	5.331	4.825	5.676	ns
12 mA	Slow	2.052	2.414	2.107	2.479	2.162	2.544	5.75	6.764	5.445	6.406	ns
16 mA	Slow	2.062	2.425	2.072	2.438	2.145	2.525	5.993	7.05	5.625	6.618	ns
20 mA	Slow	2.148	2.527	1.999	2.353	2.088	2.458	6.262	7.367	5.876	6.913	ns

Note: *: t_{DP} increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

8.5.3. LVCMOS 2.5 V

LVCMOS 2.5 V is a general standard for 2.5 V applications and is supported in IGLOO2 and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-5A.

8.5.3.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 20 • LVCMOS 2.5 V DC Voltage Specification

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 2.5 V Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
LVCMOS 2.5 V DC Input Voltage Specification							
VIH (DC)	DC input logic High (for MSIOD and DDRIO I/O banks)		1.7	–	2.625	V	
VIH (DC)	DC input logic High (for MSIO I/O Bank)		1.7	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	0.7	V	
IIH (DC)	Input current High		–	–	10	μA	
IIL (DC)	Input current Low		–	–	10	μA	
LVCMOS 2.5 V DC Output Voltage Specification							
VOH	DC output logic High	VDDI – 0.4	–	–	–	V	1
VOL	DC output logic Low		–	–	0.4	V	1

Note: 1. The VOH/VOL test points selected ensure compliance with LVCMOS 2.5 V JEDEC8-5A requirements.

Table 21 • LVCMOS 2.5 V AC Specifications

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 2.5 V Minimum and Maximum AC Switching Speed							
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	250	Mbps	
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	410	Mbps	
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	420	Mbps	
LVCMOS 2.5 V AC Calibrated Impedance Option							
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)			75, 60, 50, 33, 25, 20		Ohms	
LVCMOS 2.5 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path			1.2		V	
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})			2K		Ohms	
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})			5		pF	
Cload	Capacitive loading for data path (t_{DP})			5		pF	

Table 22 • LVCMOS 2.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA	Notes
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank (with Software Default Fixed Calibration Codes)	Min.	Max.			
2 mA	2 mA	2 mA	VDDI – 0.4	0.4	2	2	
4 mA	4 mA	4 mA	VDDI – 0.4	0.4	4	4	
6 mA	6 mA	6 mA	VDDI – 0.4	0.4	6	6	
8 mA	8 mA	8 mA	VDDI – 0.4	0.4	8	8	
12 mA	12 mA	12 mA	VDDI – 0.4	0.4	12	12	
16 mA	N/A	16 mA	VDDI – 0.4	0.4	16	16	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

8.5.3.2 AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 23 • LVCMOS 2.5 V Receiver Characteristics

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, VDD = 1.14 V, Worst-Case VDDI

	On-Die Termination (ODT)	t_{PY}		t_{PYS}		Units
		–1	Std.	–1	Std.	
LVCMOS 2.5 V (for DDRIO I/O Bank)	None	1.823	2.145	1.932	2.274	ns
LVCMOS 2.5 V (for MSIO I/O Bank)	None	2.486	2.925	2.495	2.935	ns
LVCMOS 2.5 V (for MSIOD I/O Bank)	None	2.29	2.694	2.305	2.712	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**Table 24 • LVCMOS 2.5 V Transmitter Characteristics**

Worst-Case Commercial Conditions: TJ = 85°C, VDD = 1.14 V, Worst-Case VDDI

Output Drive Selection	Slew Control	t _{DP} [*]		t _{ZL}		t _{ZH}		t _{HZ}		t _{LZ}		Units
		−1	Std.	−1	Std.	−1	Std.	−1	Std.	−1	Std.	
LVCMOS 2.5 V (for DDRIO I/O Bank with FIXED CODES)												
2 mA	Slow	3.657	4.302	3.393	3.991	3.675	4.323	3.894	4.582	3.552	4.18	ns
	Medium	3.374	3.97	3.139	3.693	3.396	3.995	3.635	4.277	3.253	3.828	ns
	Medium fast	3.239	3.811	3.036	3.572	3.261	3.836	3.519	4.141	3.128	3.681	ns
	Fast	3.224	3.793	3.029	3.563	3.246	3.818	3.512	4.132	3.119	3.67	ns
4 mA	Slow	3.095	3.641	2.705	3.182	3.088	3.633	4.738	5.575	4.348	5.116	ns
	Medium	2.825	3.324	2.488	2.927	2.823	3.321	4.492	5.285	4.063	4.781	ns
	Medium fast	2.701	3.178	2.384	2.804	2.698	3.173	4.364	5.135	3.945	4.642	ns
	Fast	2.69	3.165	2.377	2.796	2.687	3.161	4.359	5.129	3.94	4.636	ns
6 mA	Slow	2.919	3.434	2.491	2.93	2.902	3.414	5.085	5.983	4.674	5.5	ns
	Medium	2.65	3.118	2.279	2.681	2.642	3.108	4.845	5.701	4.375	5.148	ns
	Medium fast	2.529	2.975	2.176	2.56	2.521	2.965	4.724	5.558	4.259	5.011	ns
	Fast	2.516	2.96	2.168	2.551	2.508	2.95	4.717	5.55	4.251	5.002	ns
8 mA	Slow	2.863	3.368	2.427	2.855	2.844	3.346	5.196	6.114	4.769	5.612	ns
	Medium	2.599	3.058	2.217	2.608	2.59	3.047	4.952	5.827	4.471	5.261	ns
	Medium fast	2.483	2.921	2.114	2.487	2.473	2.91	4.832	5.685	4.364	5.134	ns
	Fast	2.467	2.902	2.106	2.478	2.457	2.89	4.826	5.678	4.348	5.116	ns
12 mA	Slow	2.747	3.232	2.296	2.701	2.724	3.204	5.39	6.342	4.938	5.81	ns
	Medium	2.493	2.934	2.102	2.473	2.483	2.921	5.166	6.078	4.65	5.471	ns
	Medium fast	2.382	2.803	2.006	2.36	2.371	2.789	5.067	5.962	4.546	5.349	ns
	Fast	2.369	2.787	1.999	2.352	2.357	2.773	5.063	5.958	4.538	5.339	ns
16 mA	Slow	2.677	3.149	2.213	2.604	2.649	3.116	5.575	6.56	5.08	5.977	ns
	Medium	2.432	2.862	2.028	2.386	2.421	2.848	5.372	6.32	4.801	5.649	ns
	Medium fast	2.324	2.734	1.937	2.278	2.311	2.718	5.297	6.233	4.7	5.531	ns
	Fast	2.313	2.721	1.929	2.269	2.3	2.706	5.296	6.231	4.699	5.529	ns
LVCMOS 2.5 V (for MSIO I/O Bank)												
2 mA	Slow	3.48	4.095	3.855	4.534	3.785	4.453	2.12	2.494	3.45	4.059	ns
4 mA	Slow	2.583	3.039	3.042	3.579	3.138	3.691	4.143	4.874	4.687	5.513	ns
6 mA	Slow	2.392	2.815	2.669	3.139	2.82	3.317	4.909	5.775	5.083	5.98	ns
8 mA	Slow	2.309	2.717	2.565	3.017	2.74	3.223	5.812	6.837	5.523	6.497	ns
12 mA	Slow	2.333	2.745	2.437	2.867	2.626	3.089	6.131	7.213	5.712	6.72	ns
16 mA	Slow	2.412	2.838	2.335	2.747	2.533	2.979	6.54	7.694	6.007	7.067	ns

Table 24 • LVCMOS 2.5 V Transmitter Characteristics

Worst-Case Commercial Conditions: TJ = 85°C, VDD = 1.14 V, Worst-Case VDDI (continued)

Output Drive Selection	Slew Control	t _{DP} [*]		t _{ZL}		t _{ZH}		t _{HZ}		t _{LZ}		Units
		−1	Std.	−1	Std.	−1	Std.	−1	Std.	−1	Std.	
LVCMOS 2.5 V (for MSIOD I/O Bank)												
2 mA	Slow	2.206	2.596	2.678	3.15	2.64	3.106	4.935	5.805	4.74	5.576	ns
4 mA	Slow	1.835	2.159	2.242	2.637	2.256	2.654	5.413	6.368	5.15	6.059	ns
6 mA	Slow	1.709	2.01	2.132	2.508	2.167	2.549	5.813	6.838	5.499	6.469	ns
8 mA	Slow	1.63	1.918	1.958	2.303	2.012	2.367	6.226	7.324	5.816	6.842	ns
12 mA	Slow	1.648	1.939	1.86	2.187	1.921	2.259	6.519	7.669	6.027	7.09	ns

Note: *TDP increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

8.5.4. 1.8 V LVCMOS

LVCMOS 1.8 is a general standard for 1.8 V applications and is supported in IGLOO2 and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-7A.

8.5.4.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 25 • LVCMOS 1.8 V DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 1.8 V Recommended DC Operating Conditions							
VDDI	Supply voltage		1.710	1.8	1.89	V	
LVCMOS 1.8 V DC Input Voltage Specification							
VIH (DC)	DC input logic High (for MSIOD and DDRIO I/O banks)	$0.65 * VDDI$	–	–	1.89	V	
VIH (DC)	DC input logic High (for MSIO I/O Bank)	$0.65 * VDDI$	–	–	3.45	V	
VIL (DC)	DC input logic Low	–0.3	–	–	$0.35 * VDDI$	V	
IIH (DC)	Input current High	–	–	–	10	μA	
IIL (DC)	Input current Low	–	–	–	10	μA	
LVCMOS 1.8 V DC Output Voltage Specification							
VOH	DC output logic High	$VDDI - 0.45$	–	–	–	V	
VOL	DC output logic Low	–	–	–	0.45	V	

Table 26 • LVCMOS 1.8 V AC Specifications

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 1.8 V Minimum and Maximum AC Switching Speed							
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	280	Mbps	
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	295	Mbps	
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	320	Mbps	
LVCMOS 1.8 V AC Calibrated Impedance Option							
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)			75, 60, 50, 33, 25, 20		Ohms	
LVCMOS 1.8 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	0.9	–	V	
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2k	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

Table 27 • LVCMOS 1.8 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA	Notes
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.			
2 mA	2 mA	2 mA	VDDI – 0.45	0.45	2	2	
4 mA	4 mA	4 mA	VDDI – 0.45	0.45	4	4	
6 mA	6 mA	6 mA	VDDI – 0.45	0.45	6	6	
8 mA	8 mA	8 mA	VDDI – 0.45	0.45	8	8	
10 mA	10 mA	10 mA	VDDI – 0.45	0.45	10	10	
12 mA	N/A	12 mA	VDDI – 0.45	0.45	12	12	
N/A	N/A	16 mA	VDDI – 0.45	0.45	16	16	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

8.5.4.2 AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, VDD = 1.14 V, VDDI = 1.71 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 28 • LVCMOS 1.8 V Receiver Characteristics

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, VDD = 1.14 V, Worst-Case VDDI

	On-Die Termination (ODT)	t_{PY}		t_{PYS}		Units
		–1	Std.	–1	Std.	
LVCMOS 1.8 V (for DDRIO I/O Bank)	None	1.968	2.315	2.099	2.47	ns
	50	1.992	2.343	2.229	2.622	ns
	75	1.979	2.327	2.179	2.564	ns
	150	1.978	2.327	2.136	2.512	ns
LVCMOS 1.8 V (for MSIO I/O Bank)	None	2.898	3.411	2.883	3.393	ns
	50	3.05	3.59	3.044	3.583	ns
	75	2.999	3.53	2.987	3.516	ns
	150	2.947	3.469	2.933	3.452	ns
LVCMOS 1.8 V (for MSIOD I/O Bank)	None	2.611	3.071	2.598	3.057	ns
	50	2.775	3.264	2.775	3.265	ns
	75	2.72	3.2	2.712	3.19	ns
	150	2.666	3.137	2.655	3.123	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**Table 29 • LVCMOS 1.8 V Transmitter Characteristics**

Worst-Case Commercial Conditions: TJ = 85°C, VDD = 1.14 V, Worst-Case VDDI

Output Drive Selection	Slew Control	t _{DP} [*]		t _{ZL}		t _{ZH}		t _{HZ}		t _{LZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 1.8 V (for DDRIO I/O Bank with FIXED CODES)												
2 mA	Slow	4.234	4.981	3.646	4.29	4.245	4.995	4.908	5.774	4.434	5.216	ns
	Medium	3.824	4.498	3.282	3.861	3.834	4.511	4.625	5.441	4.116	4.843	ns
	Medium fast	3.627	4.267	3.111	3.66	3.637	4.279	4.481	5.272	3.984	4.687	ns
	Fast	3.605	4.241	3.097	3.644	3.615	4.253	4.472	5.262	3.973	4.674	ns
4 mA	Slow	3.923	4.615	3.314	3.9	3.918	4.61	5.403	6.356	4.894	5.757	ns
	Medium	3.518	4.138	2.961	3.484	3.515	4.135	5.121	6.025	4.561	5.366	ns
	Medium fast	3.321	3.907	2.783	3.275	3.317	3.903	4.966	5.843	4.426	5.206	ns
	Fast	3.301	3.883	2.77	3.259	3.296	3.878	4.957	5.831	4.417	5.196	ns
6 mA	Slow	3.71	4.364	3.104	3.652	3.702	4.355	5.62	6.612	5.08	5.977	ns
	Medium	3.333	3.921	2.779	3.27	3.325	3.913	5.346	6.289	4.777	5.62	ns
	Medium fast	3.155	3.712	2.62	3.083	3.146	3.702	5.21	6.13	4.657	5.479	ns
	Fast	3.134	3.688	2.608	3.068	3.125	3.677	5.202	6.12	4.648	5.468	ns
8 mA	Slow	3.619	4.258	3.007	3.538	3.607	4.244	5.815	6.841	5.249	6.175	ns
	Medium	3.246	3.819	2.686	3.16	3.236	3.807	5.542	6.52	4.936	5.807	ns
	Medium fast	3.066	3.607	2.525	2.971	3.054	3.593	5.405	6.359	4.811	5.66	ns
	Fast	3.046	3.584	2.513	2.957	3.034	3.57	5.401	6.353	4.803	5.651	ns
10 mA	Slow	3.498	4.115	2.878	3.386	3.481	4.096	6.046	7.113	5.444	6.404	ns
	Medium	3.138	3.692	2.569	3.023	3.126	3.678	5.782	6.803	5.129	6.034	ns
	Medium fast	2.966	3.489	2.414	2.841	2.951	3.472	5.666	6.665	5.013	5.897	ns
	Fast	2.945	3.464	2.401	2.826	2.93	3.448	5.659	6.658	5.003	5.886	ns
12 mA	Slow	3.417	4.02	2.807	3.303	3.401	4.002	6.083	7.156	5.464	6.428	ns
	Medium	3.076	3.618	2.519	2.964	3.063	3.604	5.828	6.856	5.176	6.089	ns
	Medium fast	2.913	3.427	2.376	2.795	2.898	3.41	5.725	6.736	5.072	5.966	ns
	Fast	2.894	3.405	2.362	2.78	2.879	3.388	5.715	6.724	5.064	5.957	ns
16 mA	Slow	3.366	3.96	2.751	3.237	3.348	3.939	6.226	7.324	5.576	6.56	ns
	Medium	3.03	3.565	2.47	2.906	3.017	3.55	5.981	7.036	5.282	6.214	ns
	Medium fast	2.87	3.377	2.328	2.739	2.854	3.358	5.895	6.935	5.18	6.094	ns
	Fast	2.853	3.357	2.314	2.723	2.837	3.338	5.889	6.929	5.177	6.09	ns

Table 29 • LVC MOS 1.8 V Transmitter Characteristics

Worst-Case Commercial Conditions: TJ = 85°C, VDD = 1.14 V, Worst-Case VDDI (continued)

Output Drive Selection	Slew Control	t _{DP} [*]		t _{ZL}		t _{ZH}		t _{HZ}		t _{LZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 1.8 V (for MSIO I/O Bank)												
2 mA	Slow	3.441	4.047	4.165	4.9	4.413	5.192	4.891	5.755	5.138	6.044	ns
4 mA	Slow	3.218	3.786	3.642	4.284	3.941	4.636	5.665	6.665	5.568	6.551	ns
6 mA	Slow	3.141	3.694	3.501	4.118	3.823	4.498	6.587	7.75	6.032	7.096	ns
8 mA	Slow	3.165	3.723	3.319	3.904	3.654	4.298	6.898	8.115	6.216	7.313	ns
10 mA	Slow	3.202	3.767	3.278	3.857	3.616	4.254	7.25	8.529	6.435	7.571	ns
12 mA	Slow	3.277	3.855	3.175	3.736	3.519	4.139	7.392	8.697	6.538	7.692	ns
LVCMOS 1.8 V (for MSIOD I/O Bank)												
2 mA	Slow	2.725	3.206	3.316	3.901	3.484	4.099	5.204	6.123	4.997	5.88	ns
4 mA	Slow	2.242	2.638	2.777	3.267	2.947	3.466	5.729	6.74	5.448	6.41	ns
6 mA	Slow	1.995	2.347	2.466	2.901	2.63	3.094	6.372	7.496	5.987	7.043	ns
8 mA	Slow	2.001	2.354	2.44	2.87	2.6	3.058	6.633	7.804	6.193	7.286	ns
10 mA	Slow	2.025	2.382	2.312	2.719	2.47	2.906	6.94	8.165	6.412	7.544	ns

Note: *TDP increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

8.5.5. 1.5 V LVCMOS

LVCMOS 1.5 is a general standard for 1.5 V applications and is supported in IGLOO2 and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-11A.

8.5.5.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 30 • LVCMOS 1.5 V DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 1.5 V Recommended DC Operating Conditions							
VDDI	Supply voltage		1.425	1.5	1.575	V	
LVCMOS 1.5 V DC Input Voltage Specification							
VIH (DC)	DC input logic High for (MSIOD and DDRIO I/O banks)		$0.65 * VDDI$	–	1.575	V	
VIH (DC)	DC input logic High (for MSIO I/O Bank)		$0.65 * VDDI$	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	$0.35 * VDDI$	V	
IIH (DC)	Input current High		–	–	10	μA	
IIL (DC)	Input current Low		–	–	10	μA	
LVCMOS 1.5 V DC Output Voltage Specification							
VOH	DC output logic High		$VDDI * 0.75$	–	–	V	
VOL	DC output logic Low		–	–	$VDDI * 0.25$	V	

Table 31 • LVCMOS 1.5 V AC Specifications

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 1.5 V Minimum and Maximum AC Switching Speed							
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	235	Mbps	
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	160	Mbps	
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	220	Mbps	
LVCMOS 1.5 V AC Calibrated Impedance Option							
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)			75, 60, 50, 40		Ohms	
LVCMOS 1.5 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point		–	0.75	–	V	
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

Table 32 • LVCMOS 1.5 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA	Notes
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.			
2 mA	2 mA	2 mA	VDDI * 0.75	VDDI * 0.25	2	2	
4 mA	4 mA	4 mA	VDDI * 0.75	VDDI * 0.25	4	4	
6 mA	6 mA	6 mA	VDDI * 0.75	VDDI * 0.25	6	6	
8 mA	N/A	8 mA	VDDI * 0.75	VDDI * 0.25	8	8	
N/A	N/A	10 mA	VDDI * 0.75	VDDI * 0.25	10	10	
N/A	N/A	12 mA	VDDI * 0.75	VDDI * 0.25	12	12	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

8.5.5.2 AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, VDD = 1.14 V, VDDI = 1.425 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 33 • LVCMOS 1.5 V Receiver Characteristics

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, VDD = 1.14 V, Worst-Case VDDI

	On-Die Termination (ODT)	t_{PY}		t_{PYS}		Units
		-1	Std.	-1	Std.	
LVCMOS 1.5 V (for DDRIO I/O Bank)	None	2.051	2.413	2.086	2.455	ns
	50	2.118	2.492	2.273	2.674	ns
	75	2.099	2.47	2.198	2.586	ns
	150	2.083	2.451	2.133	2.51	ns
LVCMOS 1.5 V (for MSIO I/O Bank)	None	3.311	3.896	3.285	3.865	ns
	50	3.654	4.299	3.623	4.263	ns
	75	3.533	4.156	3.501	4.119	ns
	150	3.415	4.018	3.388	3.986	ns
LVCMOS 1.5 V (for MSIOD I/O Bank)	None	2.959	3.481	2.93	3.447	ns
	50	3.298	3.88	3.268	3.845	ns
	75	3.162	3.719	3.128	3.68	ns
	150	3.053	3.592	3.021	3.554	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**Table 34 • LVCMOS 1.5 V Transmitter Characteristics**

Worst-Case Commercial Conditions: TJ = 85°C, VDD = 1.14 V, Worst-Case VDDI

Output Drive Selection	Slew Control	t _{DP} [*]		t _{ZL}		t _{ZH}		t _{HZ}		t _{LZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 1.5 V (for DDRIO I/O Bank)												
2 mA	Slow	5.122	6.026	4.31	5.07	5.145	6.052	5.258	6.186	4.672	5.496	ns
	Medium	4.58	5.389	3.86	4.54	4.6	5.411	4.977	5.855	4.357	5.126	ns
	Medium fast	4.323	5.086	3.629	4.269	4.341	5.107	4.804	5.652	4.228	4.974	ns
	Fast	4.296	5.054	3.609	4.245	4.314	5.075	4.791	5.636	4.219	4.963	ns
4 mA	Slow	4.449	5.235	3.707	4.361	4.443	5.227	6.058	7.127	5.458	6.421	ns
	Medium	3.961	4.66	3.264	3.839	3.954	4.651	5.778	6.797	5.116	6.018	ns
	Medium fast	3.729	4.387	3.043	3.579	3.72	4.376	5.63	6.624	4.981	5.86	ns
	Fast	3.704	4.358	3.027	3.56	3.695	4.347	5.624	6.617	4.973	5.851	ns
6 mA	Slow	4.244	4.993	3.465	4.076	4.233	4.979	6.39	7.518	5.736	6.748	ns
	Medium	3.774	4.44	3.05	3.587	3.762	4.426	6.114	7.193	5.397	6.35	ns
	Medium fast	3.544	4.17	2.839	3.339	3.529	4.152	5.978	7.033	5.27	6.2	ns
	Fast	3.519	4.14	2.82	3.317	3.504	4.122	5.965	7.017	5.259	6.187	ns
8 mA	Slow	4.099	4.823	3.311	3.894	4.087	4.807	6.584	7.746	5.854	6.888	ns
	Medium	3.656	4.301	2.927	3.443	3.642	4.284	6.311	7.425	5.553	6.533	ns
	Medium fast	3.437	4.044	2.731	3.213	3.42	4.023	6.182	7.273	5.435	6.394	ns
	Fast	3.41	4.012	2.715	3.193	3.393	3.991	6.178	7.269	5.425	6.383	ns
10 mA	Slow	4.029	4.74	3.238	3.809	4.015	4.723	6.732	7.921	5.965	7.018	ns
	Medium	3.601	4.237	2.867	3.372	3.586	4.218	6.473	7.615	5.669	6.669	ns
	Medium fast	3.384	3.981	2.672	3.143	3.365	3.958	6.351	7.471	5.55	6.529	ns
	Fast	3.357	3.949	2.655	3.123	3.338	3.927	6.345	7.464	5.54	6.518	ns
12 mA	Slow	3.974	4.675	3.196	3.759	3.958	4.656	6.842	8.049	6.068	7.139	ns
	Medium	3.55	4.176	2.827	3.326	3.534	4.157	6.584	7.746	5.751	6.766	ns
	Medium fast	3.345	3.935	2.638	3.103	3.325	3.911	6.488	7.633	5.641	6.637	ns
	Fast	3.316	3.902	2.621	3.083	3.297	3.878	6.486	7.63	5.626	6.619	ns
LVCMOS 1.5 V (for MSIO I/O Bank)												
2 mA	Slow	4.423	5.203	5.397	6.35	5.686	6.69	5.609	6.599	5.561	6.542	ns
4 mA	Slow	4.05	4.765	4.503	5.298	4.92	5.788	7.358	8.657	6.525	7.677	ns
6 mA	Slow	4.081	4.801	4.259	5.012	4.699	5.528	7.659	9.011	6.709	7.893	ns
8 mA	Slow	4.234	4.98	4.068	4.786	4.521	5.319	8.218	9.668	7.05	8.294	ns

Table 34 • LVCMOS 1.5 V Transmitter Characteristics
Worst-Case Commercial Conditions: TJ = 85°C, VDD = 1.14 V, Worst-Case VDDI (continued)

Output Drive Selection	Slew Control	t _{DP} [*]		t _{ZL}		t _{ZH}		t _{HZ}		t _{LZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 1.5 V (for MSIOD I/O Bank)												
2 mA	Slow	2.735	3.218	3.371	3.966	3.618	4.257	6.03	7.095	5.705	6.712	ns
4 mA	Slow	2.426	2.854	2.992	3.521	3.221	3.79	6.738	7.927	6.298	7.41	ns
6 mA	Slow	2.433	2.862	2.81	3.306	3.031	3.566	7.123	8.38	6.596	7.76	ns

Note: *TDP increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

8.5.6. 1.2 V LVCMOS

LVCMOS 1.2 is a general standard for 1.2 V applications and is supported in IGLOO2 and SmartFusion2 SoC FPGAs in compliance to the JEDEC specification JESD8-12A.

8.5.6.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 35 • LVCMOS 1.2 V DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 1.2 V DC Recommended DC Operating Conditions							
VDDI	Supply voltage		1.140	1.2	1.26	V	
LVCMOS 1.2 V DC Input Voltage Specification							
VIH (DC)	DC input logic High (for MSIOD and DDRIO I/O banks)		$0.65 * VDDI$	–	1.26	V	
VIH (DC)	DC input logic High (for MSIO I/O Bank)		$0.65 * VDDI$	–	3.45	V	
VIL (DC)	DC input logic Low		–0.3	–	$0.35 * VDDI$	V	
IIH (DC)	Input current High		–	–	10	μA	
IIL (DC)	Input current Low		–	–	10	μA	
LVCMOS 1.2 V DC Output Voltage Specification							
VOH	DC output logic High		$VDDI * 0.75$	–	–	V	
VOL	DC output logic Low		–	–	$VDDI * 0.25$	V	

Table 36 • LVCMOS 1.2 V AC Specifications

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVCMOS 1.2 V Minimum and Maximum AC Switching Speed							
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	200	Mbps	
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	120	Mbps	
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 17 pF load, maximum drive/slew	–	–	160	Mbps	
LVCMOS 1.2 V AC Calibrated Impedance Option							
Rodt_cal	Supported output driver calibrated impedance (for DDRIO I/O Bank)			75, 60, 50, 40		Ohms	
LVCMOS 1.2 V AC Test Parameters Specifications							
Vtrip	Measuring/trip point		–	0.6	–	V	
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	pF	

Table 37 • LVCMOS 1.2 V Transmitter Drive Strength Specifications

Output Drive Selection			VOH (V)	VOL (V)	IOH (at VOH) mA	IOL (at VOL) mA	Notes
MSIO I/O Bank	MSIOD I/O Bank	DDRIO I/O Bank	Min.	Max.			
2 mA	2 mA	2 mA	VDDI * 0.75	VDDI * 0.25	2	2	
4 mA	4 mA	4 mA	VDDI * 0.75	VDDI * 0.25	4	4	
N/A	N/A	6 mA	VDDI * 0.75	VDDI * 0.25	6	6	

Note: For a detailed I/V curve, use the corresponding IBIS models: www.microsemi.com/soc/download/ibis/default.aspx.

8.5.6.2 AC Switching Characteristics

Worst Commercial-Case Conditions: $T_j = 85^\circ\text{C}$, VDD = 1.14 V, VDDI = 1.14 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 38 • LVCMOS 1.2 V Receiver Characteristics

Worst-Case Commercial Conditions: $T_j = 85^\circ\text{C}$, VDD = 1.14 V, Worst-Case VDDI

	On-Die Termination (ODT)	t_{py}		t_{pys}		Units
		-1	Std.	-1	Std.	
LVCMOS 1.2 V (for DDRIO I/O Bank)	None	2.448	2.88	2.466	2.901	ns
	50	2.578	3.033	2.823	3.321	ns
	75	2.49	2.929	2.68	3.153	ns
	150	2.419	2.846	2.56	3.012	ns
LVCMOS 1.2 V (for MSIO I/O Bank)	None	4.714	5.545	4.675	5.5	ns
	50	6.668	7.845	6.579	7.74	ns
	75	5.832	6.862	5.76	6.777	ns
	150	5.162	6.073	5.111	6.014	ns
LVCMOS 1.2 V (for MSIOD I/O Bank)	None	4.154	4.887	4.114	4.84	ns
	50	6.918	8.139	6.806	8.008	ns
	75	5.613	6.603	5.533	6.509	ns
	150	4.716	5.549	4.657	5.479	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**Table 39 • LVCMOS 1.2 V Transmitter Characteristics**

Worst-Case Commercial Conditions: TJ = 85°C, VDD = 1.14 V, Worst-Case VDDI

Output Drive Selection	Slew Control	t _{DP} [*]		t _{ZL}		t _{ZH}		t _{HZ}		t _{LZ}		Units
		–1	Std.	–1	Std.	–1	Std.	–1	Std.	–1	Std.	
LVCMOS 1.2 V (for DDRIO I/O Bank)												
2 mA	Slow	6.713	7.897	5.362	6.308	6.723	7.909	7.233	8.51	6.375	7.499	ns
	Medium	5.912	6.955	4.616	5.43	5.915	6.959	6.887	8.102	6.009	7.069	ns
	Medium fast	5.5	6.469	4.231	4.978	5.5	6.471	6.672	7.849	5.835	6.865	ns
	Fast	5.462	6.426	4.194	4.935	5.463	6.427	6.646	7.819	5.828	6.857	ns
4 mA	Slow	6.109	7.186	4.708	5.539	6.098	7.174	8.005	9.418	7.033	8.274	ns
	Medium	5.355	6.299	4.034	4.746	5.338	6.28	7.637	8.985	6.672	7.849	ns
	Medium fast	4.953	5.826	3.685	4.336	4.932	5.802	7.44	8.752	6.499	7.646	ns
	Fast	4.911	5.777	3.658	4.303	4.89	5.754	7.427	8.737	6.488	7.632	ns
6 mA	Slow	5.89	6.929	4.506	5.301	5.874	6.911	8.337	9.808	7.315	8.605	ns
	Medium	5.176	6.089	3.862	4.543	5.155	6.065	7.986	9.394	6.943	8.168	ns
	Medium fast	4.792	5.637	3.523	4.145	4.765	5.606	7.808	9.186	6.775	7.97	ns
	Fast	4.754	5.593	3.486	4.101	4.728	5.563	7.777	9.149	6.769	7.963	ns
LVCMOS 1.2 V (for MSIO I/O Bank)												
2 mA	Slow	6.746	7.937	7.458	8.774	8.172	9.614	9.867	11.608	8.393	9.874	ns
4 mA	Slow	7.068	8.315	6.678	7.857	7.474	8.793	10.986	12.924	9.043	10.638	ns
LVCMOS 1.2 V (for MSIOD I/O Bank)												
2 mA	Slow	3.883	4.568	4.868	5.726	5.329	6.269	7.994	9.404	7.527	8.855	ns
4 mA	Slow	3.774	4.44	4.188	4.926	4.613	5.426	8.972	10.555	8.315	9.782	ns

Note: * TDP increases with drive strength are inherent to built-in slew control circuitry for simultaneous switching output (SSO) management.

8.5.7. 3.3 V PCI/PCIX

Peripheral Component Interface (PCI) for 3.3 V standards specify support for 33 MHz and 66 MHz PCI bus applications.

8.5.7.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 40 • PCI/PCI-X DC Voltage Specification – Applicable to MSIO Bank Only

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
PCI/PCIX Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	
PCI/PCIX DC Input Voltage Specification							
VI	DC input voltage		0	–	3.45	V	
IIH(DC)	Input current High		–	–	10	μA	
IIL(DC)	Input current Low		–	–	10	μA	
PCI/PCIX DC Output Voltage Specification							
VOH	DC output logic High		Per PCI Specification			V	
VOL	DC output logic Low		Per PCI Specification			V	

Table 41 • PCI/PCI-X AC Specifications (Applicable to MSIO Bank Only)

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
PCI/PCI-X Minimum and Maximum AC Switching Speed							
Dmax	Maximum data rate (MSIO I/O Bank)	AC Loading: per JEDEC specifications	–	–	630	Mbps	
PCI/PCI-X AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path (falling edge)		–	$0.615 * VDDI$	–	V	
Vtrip	Measuring/trip point for data path (rising edge)		–	$0.285 * VDDI$	–	V	
Rtt_test	Resistance for data test path		–	25	–	Ohms	
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF	

8.5.7.2. AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 3.0\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 42 • AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	On-Die Termination (ODT)	t_{PY}		t_{PYS}		Units
		-1	Std.	-1	Std.	
PCI/PCIX (for MSIO I/O Bank)	None	2.229	2.623	2.238	2.633	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 43 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	t _{DP}		t _{ZL}		t _{ZH}		t _{HZ}		t _{LZ}		Units
	-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
PCI/PCIX (for MSIO I/O Bank)											
	2.146	2.525	2.043	2.404	2.084	2.452	6.095	7.171	5.558	6.539	ns

8.6. Memory Interface and Voltage Referenced I/O Standards

8.6.1. High-Speed Transceiver Logic (HSTL)

The High-Speed Transceiver Logic (HSTL) standard is a general purpose high-speed bus standard sponsored by IBM (EIA/JESD8-6). IGLOO2 and SmartFusion2 SoC FPGA devices support two classes of the 1.5 V HSTL. These differential versions of the standard require a differential amplifier input buffer and a push-pull output buffer.

8.6.1.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 44 • HSTL DC Voltage Specification(Applicable to DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
HSTL Recommended DC Operating Conditions							
VDDI	Supply voltage		1.425	1.5	1.575	V	
VTT	Termination voltage		0.698	0.750	0.803	V	
VREF	Input reference voltage		0.698	0.750	0.803	V	
HSTL DC Input Voltage Specification							
VIH (DC)	DC input logic High		VREF + 0.1	–	1.575	V	
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.1	V	
IIH (DC)	Input current High		–	–	10	μA	
IIL (DC)	Input current Low		–	–	10	μA	
HSTL DC Output Voltage Specification							
HSTL Class I							
VOH	DC output logic High		VDDI – 0.4	–	–	V	
VOL	DC output logic Low		–	–	0.4	V	
IOH at VOH	Output minimum source DC current (MSIO and DDRIO I/O banks)		–8.0	–	–	mA	
IOL at VOL	Output minimum sink current (MSIO and DDRIO I/O banks)		8.0	–	–	mA	
HSTL Class II (Applicable to DDRIO I/O Bank Only)							
VOH	DC output logic High		VDDI – 0.4	–	–	V	
VOL	DC output logic Low		–	–	0.4	V	
IOH at VOH	Output minimum source DC current		–16.0	–	–	mA	
IOL at VOL	Output minimum sink current		16.0	–	–	mA	
HSTL DC Differential Voltage Specifications							
VID (DC)	DC input differential voltage		0.2	–	–	V	

Table 45 • HSTL AC Specifications (Applicable to DDRIO Bank Only)

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
HSTL AC Differential Voltage Specifications							
V _{DIFF}	AC input differential voltage		0.4	–	–	V	
V _x	AC differential cross point voltage		0.68	–	0.9	V	
HSTL Minimum and Maximum AC Switching Speed							
D _{max}	Maximum data rate	AC loading: per JEDEC specifications	–	–	400	Mbps	
HSTL Impedance Specification							
R _{ref}	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistance = 191 Ohms	–	25.5, 47.8	–	Ohms	
R _{TT}	Effective impedance value (ODT for DDRIO I/O Bank only)	Reference resistance = 191 Ohms	–	47.8	–	Ohms	
HSTL AC Test Parameters Specification							
V _{trip}	Measuring/trip point for data path		–	0.75	–	V	
R _{ent}	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2K	–	Ohms	
C _{ent}	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF	
R _{tt_test}	Reference resistance for data test path for HSTL15 Class I (t _{DP})			50		Ohms	
R _{tt_test}	Reference resistance for data test path for HSTL15 Class II (t _{DP})		–	25	–	Ohms	
C _{load}	Capacitive loading for data path (t _{DP})		–	5	–	pF	

8.6.1.2. AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 46 • HSTL Receiver Characteristics

Worst-Case Commercial Conditions: $T_J = 85^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case VDDI

	On-Die Termination (ODT)	t _{PY}		Units
		-1	Std.	
HSTL (for DDRIO I/O Bank)				
Pseudo differential	None	1.605	1.888	ns
	47.8	1.614	1.898	ns
True differential	None	1.622	1.909	ns
	47.8	1.628	1.916	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 47 • HSTL Transmitter Characteristics

Worst-Case Commercial Conditions: $T_J = 85^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case VDDI

	t _{DP}		t _{ZL}		t _{ZH}		t _{HZ}		t _{LZ}		Units
	−1	Std.	−1	Std.	−1	Std.	−1	Std.	−1	Std.	
HSTL Class I											
For DDRIO I/O Bank											
Single-ended	2.6	3.059	2.514	2.958	2.514	2.958	2.431	2.86	2.431	2.86	ns
Differential	2.621	3.083	2.648	3.115	2.647	3.113	2.925	3.442	2.923	3.44	ns
HSTL Class II											
For DDRIO I/O Bank											
Single-ended	2.511	2.954	2.488	2.927	2.49	2.93	2.409	2.833	2.411	2.836	ns
Differential	2.528	2.974	2.552	3.003	2.551	3.001	2.897	3.409	2.896	3.408	ns

8.6.2. Stub-Series Terminated Logic

Stub-Series Terminated Logic (SSTL) for 2.5 V (SSTL2), 1.8 V (SSTL18), and 1.5 V (SSTL15) is supported in IGLOO2 and SmartFusion2 SoC FPGAs. SSTL2 is defined by JEDEC standard JESD8-9B and SSTL18 is defined by JEDEC standard JESD8-15. IGLOO2 SSTL I/O configurations are designed to meet double data rate standards DDR/2/3 for general purpose memory buses. Double data rate standards are designed to meet their JEDEC specifications as defined by JEDEC standard JESD79F for DDR, JEDEC standard JESD79-2F for DDR, JEDEC standard JESD79-3D for DDR3, and JEDEC standard JESD209A for LPDDR.

8.6.3. Stub-Series Terminated Logic 2.5 V (SSTL2)

SSTL2 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs and also comply with reduced and full drive of double data rate (DDR) standards. IGLOO2 and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL2. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.6.3.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 48 • DDR1/SSTL2 DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
VTT	Termination voltage		1.164	1.250	1.339	V	
VREF	Input reference voltage		1.164	1.250	1.339	V	
DDR/SSTL2 DC Input Voltage Specification							
VIH (DC)	DC input logic High	VREF + 0.15	–	–	2.625	V	
VIL (DC)	DC input logic Low	–0.3	–	–	VREF – 0.15	V	
IIH (DC)	Input current High	–	–	–	10	μA	
IIL (DC)	Input current Lo	–	–	–	10	μA	
DDR/SSTL2 DC Output Voltage Specification							
SSTL2 Class I (DDR Reduced Drive)							
VOH	DC output logic High	VTT + 0.608	–	–	–	V	
VOL	DC output logic Low	–	–	–	VTT – 0.608	V	
IOH at VOH	Output minimum source DC current	8.1	–	–	–	mA	
IOL at VOL	Output minimum sink current	–8.1	–	–	–	mA	
SSTL2 Class II (DDR Full Drive) – Applicable to MSIO and DDRIO I/O Banks Only							
VOH	DC output logic High	VTT + 0.81	–	–	–	V	
VOL	DC output logic Low	–	–	–	VTT – 0.81	V	
IOH at VOH	Output minimum source DC current	16.2	–	–	–	mA	
IOL at VOL	Output minimum sink current	–16.2	–	–	–	mA	
SSTL2 DC Differential Voltage Specification							
VID (DC)	DC input differential voltage	0.3	–	–	–	V	

Table 49 • DDR1/SSTL2 AC Specifications

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
SSTL2 AC Differential Voltage Specification							
VDIFF (AC)	AC input differential voltage		0.7	–	–	V	
Vx (AC)	AC differential cross point voltage		0.5 * VDDI – 0.2	–	0.5 * VDDI + 0.2	V	
SSTL2 Minimum and Maximum AC Switching Speeds							
Dmax	Maximum data rate (for DDRIO I/O Bank)	AC loading: per JEDEC specifications	–	–	400	Mbps	
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 17pF load	–	–	575	Mbps	
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 3 pF / 50 Ohm load	–	–	700	Mbps	
		AC loading: 17pF load	–	–	510	Mbps	
SSTL2 Impedance Specifications							
	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistor = 150 Ohms	–	20, 42	–	Ohms	
AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	1.25	–	V	
Rent	Resistance for enable path (tZH, tZL, tHZ, tLZ)		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (tZH, tZL, tHZ, tLZ)		–	5	–	pF	
Rs	Series resistance for data test path (tDP)		–	25	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL2 Class I (tDP)		–	50	–	Ohms	
Rtt_test	Reference resistance for data test path for SSTL2 Class II (tDP)		–	25	–	Ohms	
Cload	Capacitive loading for data path (tDP)		–	5	–	pF	

8.6.3.2. AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 50 • DDR1/SSTL2 Receiver Characteristics

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	On-Die Termination (ODT)	t _{py}		Units
		–1	Std.	
SSTL2 (for DDRIO I/O Bank)				
Pseudo differential	None	1.549	1.821	ns
True differential	None	1.589	1.87	ns
SSTL2 (for MSIO I/O Bank)				
Pseudo differential	None	2.798	3.293	ns
True differential	None	2.733	3.215	ns
SSTL2 (for MSIOD I/O Bank)				
Pseudo differential	None	2.476	2.913	ns
True differential	None	2.475	2.911	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 51 • DDR1/SSTL2 Transmitter Characteristics

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	t _{DP}		t _{ZL}		t _{ZH}		t _{HZ}		t _{LZ}		Units	
	-1	STD	-1	STD	-1	STD	-1	STD	-1	STD		
SSTL2 Class I												
For DDRIO I/O Bank												
Single-ended	2.26	2.66	1.99	2.341	1.985	2.335	2.135	2.512	2.13	2.505	ns	
Differential	2.26	2.658	2.202	2.591	2.201	2.589	2.393	2.815	2.392	2.814	ns	
For MSIO I/O Bank												
Single-ended	2.055	2.417	2.037	2.396	2.03	2.388	2.068	2.433	2.061	2.425	ns	
Differential	2.192	2.58	2.434	2.864	2.425	2.852	2.164	2.545	2.156	2.536	ns	
For MSIOD I/O Bank												
Single-ended	1.512	1.779	1.462	1.72	1.462	1.72	1.676	1.972	1.676	1.971	ns	
Differential	1.676	1.971	1.774	2.087	1.766	2.077	1.854	2.181	1.845	2.171	ns	
SSTL2 Class II												
For DDRIO I/O Bank												
Single-ended	2.122	2.497	1.906	2.243	1.902	2.237	2.061	2.424	2.056	2.418	ns	
Differential	2.127	2.501	2.042	2.402	2.043	2.403	2.363	2.78	2.365	2.781	ns	
For MSIO I/O Bank												
Single-ended	2.29	2.693	1.988	2.338	1.978	2.326	1.989	2.34	1.979	2.328	ns	
Differential	2.418	2.846	2.304	2.711	2.297	2.702	2.131	2.506	2.124	2.499	ns	

8.6.4. Stub-Series Terminated Logic 1.8 V (SSTL18)

SSTL18 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR2) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os support both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.6.4.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 52 • SSTL18 DC Minimum and Maximum DC Input and Output Levels

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.71	1.8	1.89	V	
VTT	Termination voltage		0.838	0.900	0.964	V	
VREF	Input reference voltage		0.838	0.900	0.964	V	
SSTL18 DC Input Voltage Specification							
VIH (DC)	DC input logic High		VREF + 0.125	–	1.89	V	
VIL (DC)	DC input logic Low		–0.3	–	VREF – 0.125	V	
IIH (DC)	Input current High		–	–	10	μA	
IIL (DC)	Input current Low		–	–	10	μA	
SSTL18 DC Output Voltage Specification							
SSTL18 Class I (DDR2 Reduced Drive)							
VOH	DC output logic High		VTT + 0.603	–	–	V	
VOL	DC output logic Low		–	–	VTT – 0.603	V	
IOH at VOH	Output minimum source DC current (DDRIO I/O Bank only)		6.5	–	–	mA	
IOL at VOL	Output minimum sink current (DDRIO I/O Bank only)		–6.5	–	–	mA	
STL18 Class II (DDR2 Full Drive)							1
VOH	DC output logic High		VTT + 0.603	–	–	V	
VOL	DC output logic Low		–	–	VTT – 0.603	V	
IOH at VOH	Output minimum source DC current (DDRIO I/O Bank only)		13.4	–	–	mA	
IOL at VOL	Output minimum sink current (DDRIO I/O Bank only)		–13.4	–	–	mA	
SSTL18 DC Differential Voltage Specification							
VID (DC)	DC input differential voltage		0.3	–	–	V	

Note: To meet JEDEC Electrical Compliance, use DDR2 Full Drive Transmitter.

Table 53 • SSTL18 AC Specifications (Applicable to DDRIO Bank Only)

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
SSTL18 AC Differential Voltage Specification							
V _{DIFF} (AC)	AC input differential voltage		0.7	–	–	V	
V _x (AC)	AC differential cross point voltage		$0.5 * V_{DDI} - 0.175$	–	$0.5 * V_{DDI} + 0.175$	V	
SSTL18 Minimum and Maximum AC Switching Speed							
D _{max}	Maximum data rate (for DDRIO I/O Bank)	AC loading: per JEDEC specification	–	–	667	Mbps	
SSTL18 Impedance Specifications							
R _{ref}	Supported output driver calibrated impedance (for DDRIO I/O Bank)	Reference resistor = 150 Ohms	–	20, 42	–	Ohms	
R _{TT}	Effective impedance value (ODT)	Reference resistor = 150 Ohms	–	50, 75, 150	–	Ohms	
SSTL18 AC Test Parameters Specifications							
V _{trip}	Measuring/trip point for data path		–	0.9	–	V	
R _{ent}	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2K	–	Ohms	
C _{ent}	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF	
R _s	Series resistance for data test path (t_{DP})		–	25	–	Ohms	
R _{tt_test}	Reference resistance for data test path for SSTL18 Class I (t_{DP})		–	50	–	Ohms	
R _{tt_test}	Reference resistance for data test path for SSTL18 Class II (t_{DP})		–	25	–	Ohms	
C _{load}	Capacitive loading for data path (t_{DP})		–	5	–	pF	

8.6.4.2. AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.71\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 54 • DDR2/SSTL18 Receiver Characteristics

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	On-Die Termination (ODT)	t _{py}		Units
		−1	STD	
SSTL18 (for DDRIO I/O Bank)				
Pseudo differential	None	1.567	1.844	ns
	50	1.573	1.851	ns
	75	1.571	1.849	ns
	150	1.569	1.846	ns
True differential	None	1.588	1.869	ns
	50	1.593	1.875	ns
	75	1.589	1.871	ns
	150	1.585	1.866	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 55 • DDR2/SSTL18 Transmitter Characteristics

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	t _{DP}		t _{ZL}		t _{ZH}		t _{HZ}		t _{LZ}		Units	
	−1	STD	−1	STD	−1	STD	−1	STD	−1	STD		
SSTL18 Class I												
For DDRIO I/O Bank												
Single-ended	2.383	2.804	2.23	2.623	2.229	2.622	2.202	2.591	2.201	2.59	ns	
Differential	2.413	2.84	2.797	3.29	2.797	3.29	2.282	2.685	2.282	2.685	ns	
SSTL18 Class II												
For DDRIO I/O Bank												
Single-ended	2.281	2.683	2.196	2.584	2.195	2.583	2.171	2.555	2.17	2.554	ns	
Differential	2.315	2.724	2.698	3.173	2.698	3.173	2.242	2.639	2.242	2.639	ns	

8.6.5. Stub-Series Terminated Logic 1.5 V (SSTL15)

SSTL15 Class I and Class II are supported in IGLOO2 and SmartFusion2 SoC FPGAs, and also comply with the reduced and full drive double data rate (DDR3) standard. IGLOO2 and SmartFusion2 SoC FPGA I/Os supports both standards for single-ended signaling and differential signaling for SSTL18. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.6.5.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 56 • SSTL15 DC Voltage Specification (for DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.425	1.5	1.575	V	
VTT	Termination voltage		0.698	0.750	0.803	V	
VREF	Input reference voltage		0.698	0.750	0.803	V	
SSTL15 DC Input Voltage Specification							
VIH(DC)	DC input logic High	VREF + 0.1	–	–	1.575	V	
VIL(DC)	DC input logic Low	–0.3	–	–	VREF – 0.1	V	
IIH (DC)	Input current High	–	–	–	10	μA	
IIL (DC)	Input current Low	–	–	–	10	μA	
SSTL15 DC Output Voltage Specification							
DDR3/SSTL15 Class I (DDR3 Reduced Drive)							
VOH	DC output logic High	0.8 * VDDI	–	–	–	V	
VOL	DC output logic Low	–	–	–	0.2 * VDDI	V	
IOH at VOH	Output minimum source DC current	6.5	–	–	–	mA	
IOL at VOL	Output minimum sink current	–6.5	–	–	–	mA	
SSTL15 Class II (DDR3 Full Drive)							1
VOH	DC output logic High	0.8 * VDDI	–	–	–	V	
VOL	DC output logic Low	–	–	–	0.2 * VDDI	V	
IOH at VOH	Output minimum source DC current	7.6	–	–	–	mA	
IOL at VOL	Output minimum sink current	–7.6	–	–	–	mA	
SSTL15 Differential Voltage Specification							
VID	DC input differential voltage	0.2	–	–	–	V	

Note: *To meet JEDEC Electrical Compliance, use DDR3 Full Drive Transmitter.

Table 57 • SSTL15 AC Specifications (for DDRIO I/O Bank Only)

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
SSTL15 Differential Voltage Specification							
V _{DIFF} (AC)	AC input differential voltage		0.7	–	–	V	
V _x (AC)	AC differential cross point voltage		0.5 * V _{DDI} – 0.150	–	0.5 * V _{DDI} + 0.150	V	
SSTL15 Minimum and Maximum AC Switching Speed (for DDRIO I/O Banks only)							
D _{max}	Maximum data rate	AC loading: per JEDEC specifications			667	Mbps	
SSTL15 AC Calibrated Impedance Option							
R _{ref}	Supported output driver calibrated impedance	Reference resistor = 240 Ohms		34, 40		Ohms	
R _{TT}	Effective impedance value (ODT)	Reference resistor = 240 Ohms		20, 30, 40, 60, 120		Ohms	
SSTL15 AC Test Parameters Specifications							
V _{trip}	Measuring/trip point for data path		–	0.75	–	V	
R _{ent}	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2K	–	Ohms	
C _{ent}	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF	
R _s	Series resistance for data test path (t _{DP})		–	25	–	Ohms	
R _{tt_test}	Reference resistance for data test path for SSTL15 Class I (t _{DP})		–	50	–	Ohms	
R _{tt_test}	Reference resistance for data test path for SSTL15 Class II (t _{DP})		–	25	–	Ohms	
C _{load}	Capacitive loading for data path (t _{DP})		–	5	–	pF	

8.6.5.2. AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 1.425\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 58 • DDR3/SSTL15 Receiver Characteristics

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	On-Die Termination (ODT)	t _{py}		Units
		–1	Std.	
DDR3/SSTL15 (for DDRIO I/O Bank)				
Pseudo differential	None	1.605	1.888	ns
	20	1.616	1.901	ns
	30	1.613	1.897	ns
	40	1.611	1.895	ns
	60	1.609	1.893	ns
	120	1.607	1.89	ns
True differential	None	1.623	1.91	ns
	20	1.637	1.926	ns
	30	1.63	1.918	ns
	40	1.626	1.914	ns
	60	1.622	1.91	ns
	120	1.619	1.905	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 59 • DDR3/SSTL15 Transmitter Characteristics

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	t _{DP}		t _{ZL}		t _{ZH}		t _{HZ}		t _{LZ}		Units	
	−1	STD	−1	STD	−1	STD	−1	STD	−1	STD		
DDR3 Reduced Drive/SSTL15 Class I												
For DDRIO I/O Bank												
Single-ended	2.533	2.98	2.522	2.967	2.523	2.968	2.427	2.855	2.428	2.856	ns	
Differential	2.555	3.005	3.073	3.615	3.073	3.615	2.416	2.843	2.416	2.843	ns	
DDR3 Full DriveSSTL15 Class II												
For DDRIO I/O Bank												
Single-ended	2.53	2.977	2.514	2.958	2.516	2.96	2.422	2.849	2.425	2.852	ns	
Differential	2.552	3.002	2.591	3.048	2.59	3.047	2.882	3.391	2.881	3.39	ns	

8.6.6. Low Power Double Data Rate (LPDDR)

LPDDR reduced and full drive low power double data rate standards are supported in IGLOO2 and SmartFusion2 SoC FPGA I/Os. This standard requires a differential amplifier input buffer and a push-pull output buffer.

8.6.6.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 60 • LPDDR DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		1.71	1.8	1.89	V	
VTT	Termination voltage		0.838	0.900	0.964	V	
VREF	Input reference voltage		0.838	0.900	0.964	V	
LPDDR DC Input Voltage Specification							
VIH (DC)	DC input logic High		0.7 * VDDI	–	1.89	V	
VIL (DC)	DC input logic Low		–0.3	–	0.3 * VDDI	V	
IIH (DC)	Input current High		–	–	10	μA	
IIL (DC)	Input current Low		–	–	10	μA	
LPDDR DC Output Voltage Specification							
LPDDR reduced drive							
VOH	DC output logic High		0.9 * VDDI	–	–	V	
VOL	DC output logic Low		–	–	0.1 * VDDI	V	
IOH at VOH	Output minimum source DC current		0.1	–	–	mA	
IOL at VOL	Output minimum sink current		–0.1	–	–	mA	
LPDDR full drive							1
VOH	DC output logic High		0.9 * VDDI	–	–	V	
VOL	DC output logic Low		–	–	0.1 * VDDI	V	
IOH at VOH	Output minimum source DC current		0.1	–	–	mA	
IOL at VOL	Output minimum sink current		–0.1	–	–	mA	
LPDDR Differential Voltage Specification							
VID (DC)	DC input differential voltage		0.4 * VDDI	–	–	V	

Note: *To meet JEDEC Electrical Compliance, use LPDDR Full Drive Transmitter.

Table 61 • LPDDR AC Specifications (for DDRIO I/O banks only)

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LPDDR AC Differential Voltage Specification							
VDIFF	AC input differential voltage		$0.6 * VDDI$	–	–	V	
Vx	AC differential cross point voltage		$0.4 * VDDI$	–	$0.6 * VDDI$	V	
LPDDR AC Specifications							
Dmax	Maximum data rate	AC loading: per JEDEC specifications	–		400	Mbps	
LPDDR AC Calibrated Impedance Option							
Rref	Supported output driver calibrated impedance	Reference resistor = 150 Ohms	–	20, 42	–	Ohms	
Rtt	Effective impedance value (ODT)	Reference resistor = 150 Ohms	–	50, 70, 150	–	Ohms	
LPDDR AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	0.9	–	V	
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF	
Rs	Series resistance for data test path (t_{DP})		–	25	–	Ohms	
Rtt_test	Reference resistance for data test path for LPDDR (t_{DP})		–	50	–	Ohms	
Cload	Capacitive loading for data path (t_{DP})		–	5	–	Ohms	

8.6.6.2 AC Switching Characteristics

Table 62 • LPDDR Receiver CharacteristicsWorst-Case Commercial Conditions: $T_J = 85^{\circ}\text{C}$, $VDD = 1.14\text{ V}$, Worst-Case VDDI

	On-Die Termination (ODT)	t _{PY}		Units
		–1	Std.	
LPDDR (for DDRIO I/O Bank)				
Pseudo differential	None	1.568	1.845	ns
	50	1.574	1.852	ns
	75	1.572	1.85	ns
	150	1.57	1.847	ns
True differential	None	1.588	1.869	ns
	50	1.593	1.875	ns
	75	1.589	1.871	ns
	150	1.585	1.866	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)**Table 63 • LPDDR Transmitter Characteristics**Worst-Case Commercial Conditions: $T_J = 85^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case VDDI

	t _{DP}		t _{ZL}		t _{ZH}		t _{HZ}		t _{LZ}		Units	
	−1	Std.	−1	Std.	−1	Std.	−1	Std.	−1	Std.		
LPDDR Reduced Drive												
For DDRIO I/O Bank												
Single-ended	2.383	2.804	2.23	2.623	2.229	2.622	2.202	2.591	2.201	2.59	ns	
Differential	2.396	2.819	2.764	3.252	2.764	3.252	2.255	2.653	2.255	2.653	ns	
LPDDR Full Drive												
For DDRIO I/O Bank												
Single-ended	2.281	2.683	2.196	2.584	2.195	2.583	2.171	2.555	2.17	2.554	ns	
Differential	2.298	2.703	2.288	2.692	2.288	2.692	2.593	3.051	2.593	3.051	ns	

8.7. Differential I/O Standards

Configuration of the I/O modules as a differential pair is handled by Microsemi SoC Products Group Libero software when the user instantiates a differential I/O macro in the design. Differential I/Os can also be used in conjunction with the embedded Input register (InReg), Output register (OutReg), Enable register (EnReg), and Double Data Rate registers (DDR).

8.7.1. LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard.

8.7.1.1 Minimum and Maximum Input and Output Levels

Table 64 • LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVDS Recommended DC Operating Conditions							
VDDI	Supply voltage	2.5 V range	2.375	2.5	2.625	V	
VDDI	Supply voltage	3.3 V range	3.15	3.3	3.45	V	
LVDS DC Input Voltage Specification							
VI	DC Input voltage	2.5 V range	0	–	2.925	V	
VI	DC input voltage	3.3 V range	0	–	3.45	V	
IIH (DC)	Input current High		–	–	10	μA	
IIL (DC)	Input current Low		–	–	10	μA	
LVDS DC Output Voltage Specification							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
LVDS Differential Voltage Specification							
VOD	Differential output voltage swing		250	350	450	mV	
VOCM	Output common mode voltage		1.125	1.25	1.375	V	
VICM	Input common mode voltage		0.05	1.25	2.35	V	
VID	Input differential voltage		100	350	600	mV	

Table 65 • LVDS AC Specifications

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVDS Minimum and Maximum AC Switching Speed							
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 12 pF / 100 Ohm differential load	–	–	535	Mbps	
Dmax	Maximum data rate (for MSIOD I/O Bank) – no pre-emphasis	AC loading: 10 pF / 100 Ohm differential load	–	–	620	Mbps	
		AC loading: 2 pF / 100 Ohm differential load	–	–	700	Mbps	
LVDS Impedance Specification							
Rt	Termination resistance		–	100	–	Ohms	
LVDS AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t _{ZH} , t _{ZL} , t _{HZ} , t _{LZ})		–	5	–	pF	

8.7.1.2. LVDS25 AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 66 • LVDS25 Receiver Characteristics

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	On-Die Termination (ODT)	t_{py}		Units
		-1	Std.	
LVDS (for MSIO I/O Bank)	None	2.774	3.263	ns
	100	2.775	3.264	ns
LVDS (for MSIOD I/O Bank)	None	2.554	3.004	ns
	100	2.549	2.999	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 67 • LVDS25 Transmitter Characteristics

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		Units
	-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
LVDS (for MSIO I/O Bank)	2.136	2.513	2.416	2.842	2.402	2.825	2.423	2.85	2.409	2.833	ns
LVDS (for MSIOD I/O Bank)											
No pre-emphasis	1.61	1.893	1.844	2.169	1.813	2.133	1.897	2.231	1.866	2.195	ns
Min. pre-emphasis	1.527	1.796	1.852	2.179	1.823	2.145	1.905	2.241	1.876	2.207	ns
Med. pre-emphasis	1.496	1.76	1.861	2.19	1.831	2.154	1.914	2.252	1.884	2.216	ns

LVDS33 AC Switching Characteristics

AC Switching Characteristics for Receiver (Input Buffers)

Table 68 • LVDS33 Receiver Characteristics

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	On Die Termination (ODT)	t_{py}		Units
		-1	Std.	
LVDS33 (for MSIO I/O Bank)	None	2.572	3.025	ns
	100	2.569	3.023	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 69 • LVDS33 Transmitter Characteristics

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		Units
	-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
LVDS33 (for MSIO I/O Bank)	1.942	2.284	1.98	2.33	1.97	2.318	1.953	2.298	1.96	2.307	ns

8.7.2. B-LVDS

Bus LVDS (B-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

8.7.2.1 Minimum and Maximum DC/AC Input and Output Levels Specification

Table 70 • B-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
Bus-LVDS DC Input Voltage Specification							
VI	DC input voltage		0	–	2.925	V	
IIH (DC)	Input current High		–	–	10	μA	
IIL (DC)	Input current Low		–	–	10	μA	
Bus-LVDS DC Output Voltage Specification (for MSIO I/O bank Only)							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
Bus-LVDS Differential Voltage Specification							
VOD	Differential output voltage swing (for MSIO I/O Bank Only)		65	–	460	mV	
VOCM	Output common mode voltage (for MSIO I/O Bank Only)		1.1	–	1.5	V	
VICM	Input common mode voltage		0.05	–	2.4	V	
VID	Input differential voltage		100	–	VDDI	mV	

Table 71 • B-LVDS AC Specifications

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Bus-LVDS Minimum and Maximum AC Switching Speed							
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	500	Mbps	
Bus-LVDS Impedance Specifications							
Rt	Termination resistance		–	27	–	Ohms	
Bus-LVDS AC Test Parameters Specifications							
Vtrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF	

8.7.2.2. AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 72 • AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	On-Die Termination (ODT)	t_{PY}		Units
		-1	Std.	
Bus-LVDS (for MSIO I/O Bank)	None	2.738	3.221	ns
	100	2.735	3.218	ns
Bus-LVDS (for MSIOD I/O Bank)	None	2.495	2.934	ns
	100	2.495	2.935	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 73 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		Units
	-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
Bus-LVDS (for MSIO I/O Bank)	2.258	2.656	2.343	2.756	2.329	2.74	2.12	2.494	2.123	2.497	ns

8.7.3. M-LVDS

M-LVDS specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers.

8.7.3.1 Minimum and Maximum Input and Output Levels

Table 74 • M-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
M-LVDS Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	1
M-LVDS DC Input Voltage Specification							
VI	DC input voltage		0	–	2.925	V	
IIH (DC)	Input current High		–	–	10	μA	
IIL (DC)	Input current Low		–	–	10	μA	
M-LVDS DC Output Voltage Specification (for MSIO I/O Bank Only)							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
M-LVDS Differential Voltage Specification							
VOD	Differential output voltage Swing (for MSIO I/O Bank Only)		300	–	650	mV	
VOCM	Output common mode voltage (for MSIO I/O Bank Only)		0.3	–	2.1	V	
VICM	Input common mode voltage		0.3	–	1.2	V	
VID	Input differential voltage		50	–	2400	mV	
<i>Note: Only M-LVDS TYPE I is supported</i>							

Table 75 • M-LVDS AC Specifications

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
M-LVDS Minimum and Maximum AC Switching Speed							
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	500	Mbps	
M-LVDS Impedance Specification							
Rt	Termination resistance		–	50	–	Ohms	
M-LVDS AC Test Parameters Specifications							
VTrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF	

8.7.3.2. AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 76 • AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	On-Die Termination (ODT)	t_{PY}		Units
		-1	Std.	
M-LVDS (for MSIO I/O Bank)	None	2.738	3.221	ns
	100	2.735	3.218	ns
M-LVDS (for MSIOD I/O Bank)	None	2.495	2.934	ns
	100	2.495	2.935	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 77 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		Units
	-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
M-LVDS (for MSIO I/O Bank)	2.258	2.656	2.348	2.762	2.334	2.746	2.123	2.497	2.125	2.5	ns

8.7.4. Mini-LVDS

Mini-LVDS is an unidirectional interface from the timing controller to the column drivers and is designed to the Texas Instruments Standard SLDA007A.

8.7.4.1 Mini-LVDS Minimum and Maximum Input and Output Levels

Table 78 • Mini-LVDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
Mini-LVDS DC Input Voltage Specification							
VI	DC Input voltage		0	–	2.925	V	
Mini-LVDS DC Output Voltage Specification							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
Mini-LVDS Differential Voltage Specification							
VOD	Differential output voltage swing		300	–	600	mV	
VOCM	Output common mode voltage		1	–	1.4	V	
VICM	Input common mode voltage		0.3	–	1.2	V	
VID	Input differential voltage		100	–	600	mV	

Table 79 • Mini-LVDS AC Specifications

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Mini-LVDS Minimum and Maximum AC Switching Speed							
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	520	Mbps	
Dmax	Maximum data rate (for MSIOD I/O Bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	700	Mbps	
Mini-LVDS Impedance Specification							
Rt	Termination resistance		–	100	–	Ohms	
Mini-LVDS AC Test Parameters Specifications							
VTrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF	

8.7.4.2. AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 80 • AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	On-Die Termination (ODT)	t_{py}		Units
		-1	Std.	
Mini-LVDS (for MSIO I/O Bank)	None	2.855	3.359	ns
	100	2.85	3.353	ns
Mini-LVDS (for MSIOD I/O Bank)	None	2.602	3.061	ns
	100	2.597	3.055	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 81 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		Units
	-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
Mini-LVDS (for MSIO I/O Bank)	2.097	2.467	2.308	2.715	2.296	2.701	1.964	2.31	1.949	2.293	ns
Mini-LVDS (for MSIOD I/O Bank)											
No pre-emphasis	1.614	1.899	1.562	1.837	1.553	1.826	1.593	1.874	1.578	1.856	ns
Min. pre-emphasis	1.604	1.887	1.745	2.053	1.731	2.036	1.892	2.225	1.861	2.189	ns
Med. pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max. pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

8.7.5. RSDS

Reduced Swing Differential Signaling (RSDS) is similar to an LVDS high-speed interface using differential signaling. RSDS has a similar implementation to LVDS devices and is only intended for point-to-point applications.

8.7.5.1 Minimum and Maximum Input and Output Levels

Table 82 • RSDS DC Voltage Specification

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		2.375	2.5	2.625	V	
RSDS DC Input Voltage Specification							
VI	DC input voltage		0	–	2.925	V	
RSDS DC Output Voltage Specification							
VOH	DC output logic High		1.25	1.425	1.6	V	
VOL	DC output logic Low		0.9	1.075	1.25	V	
RSDS Differential Voltage Specification							
VOD	Differential output voltage swing		100	–	600	mV	
VOCM	Output common mode voltage		0.5	–	1.5	V	
VICM	Input common mode voltage		0.3	–	1.5	V	
VID	Input differential voltage		100	–	600	mV	

Table 83 • RSDS AC Specifications

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
RSDS Minimum and Maximum AC Switching Speed							
Dmax	Maximum data rate (for MSIO I/O Bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	520	Mbps	
Dmax	Maximum data Rate (for MSIOD I/O Bank)	AC loading: 2 pF / 100 Ohm differential load	–	–	700	Mbps	
RSDS Impedance Specification							
Rt	Termination resistance			100		Ohms	
RSDS AC Test Parameters Specifications							
VTrip	Measuring/trip point for data path		–	Cross point	–	V	
Rent	Resistance for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	2K	–	Ohms	
Cent	Capacitive loading for enable path (t_{ZH} , t_{ZL} , t_{HZ} , t_{LZ})		–	5	–	pF	

8.7.5.2. AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, $V_{DDI} = 2.375\text{ V}$

AC Switching Characteristics for Receiver (Input Buffers)

Table 84 • AC Switching Characteristics for Receiver (Input Buffers)

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	On-Die Termination (ODT)	t_{PY}		Units
		-1	Std.	
RSDS (for MSIO I/O Bank)	None	2.855	3.359	ns
	100	2.85	3.353	ns
RSDS (for MSIOD I/O Bank)	None	2.602	3.061	ns
	100	2.597	3.055	ns

AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Table 85 • AC Switching Characteristics for Transmitter (Output and Tristate Buffers)

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$, Worst-Case V_{DDI}

	t_{DP}		t_{ZL}		t_{ZH}		t_{HZ}		t_{LZ}		Units
	-1	Std.	-1	Std.	-1	Std.	-1	Std.	-1	Std.	
RSDS (for MSIO I/O Bank)	2.097	2.467	2.303	2.709	2.291	2.695	1.961	2.307	1.947	2.29	ns
RSDS (for MSIOD I/O Bank)											
No pre-emphasis	1.614	1.899	1.559	1.834	1.55	1.823	1.59	1.87	1.575	1.852	ns
Min. pre-emphasis	1.604	1.887	1.742	2.05	1.728	2.032	1.889	2.222	1.858	2.185	ns
Med. pre-emphasis	1.521	1.79	1.753	2.062	1.737	2.043	1.9	2.235	1.868	2.197	ns
Max. pre-emphasis	1.492	1.754	1.762	2.073	1.745	2.052	1.91	2.247	1.876	2.206	ns

8.7.6. LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Similar to LVDS, two pins are needed. It also requires external resistor termination. IGLOO2 and SmartFusion2 SoC FPGAs support only LVPECL receivers and do not support LVPECL transmitters.

8.7.6.1 Minimum and Maximum Input and Output Levels

Table 86 • LVPECL DC Voltage Specification (Applicable to MSIO I/O Banks Only)

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
Recommended DC Operating Conditions							
VDDI	Supply voltage		3.15	3.3	3.45	V	
LVPECL DC Input Voltage Specification							
VI	DC input voltage		0	–	3.45	V	
LVPECL Differential Voltage Specification							
VICM	Input common mode voltage		0.3		2.8	V	
VIDIFF	Input differential voltage		100	300	1,000	mV	

Table 87 • LVPECL Minimum and Maximum AC Switching Speeds (Applicable to MSIO I/O Banks ONLY)

Symbols	Parameters	Conditions	Min.	Typ.	Max.	Units	Notes
LVPECL AC Specifications							
Dmax	Maximum data rate (for MSIO I/O Bank)		–	–	900	Mbps	

8.7.6.2 AC Switching Characteristics

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, VDD = 1.14 V, VDDI = 2.375 V

AC Switching Characteristics for Receiver (Input Buffers)

Table 88 • LVPECL Receiver Characteristics

Worst-Case Commercial Conditions: $T_J = 85^\circ\text{C}$, VDD = 1.14 V, Worst-Case VDDI

	On-Die Termination (ODT)	t_{py}		Units
		–1	Std.	
LVPECL (for MSIO I/O Bank)	None	2.572	3.025	ns
	100	2.569	3.023	ns

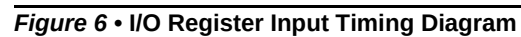
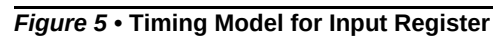


Table 89 • Input Data Register Propagation Delays
Worst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Measuring Nodes (from, to)*	-1	Std.	Units
t_{IBYP}	Bypass Delay of the Input Register	F, G	0.353	0.415	ns
t_{CLKQ}	Clock-to-Q of the Input Register	E, G	0.16	0.188	ns
t_{ISUD}	Data Setup Time for the Input Register	A, E	0.357	0.421	ns
t_{IHD}	Data Hold Time for the Input Register	A, E	0	0	ns
t_{ISUE}	Enable Setup Time for the Input Register	B, E	0.46	0.542	ns
t_{IHE}	Enable Hold Time for the Input Register	B, E	0	0	ns
t_{ISUSL}	Synchronous Load Setup Time for the Input Register	D, E	0.46	0.542	ns
t_{IHSL}	Synchronous Load Hold Time for the Input Register	D, E	0	0	ns
t_{IALn2Q}	Asynchronous Clear-to-Q of the Input Register ($\text{ADn}=1$)	C, G	0.625	0.735	ns
	Asynchronous Preset-to-Q of the Input Register ($\text{ADn}=0$)	C, G	0.587	0.69	ns
t_{IREMALn}	Asynchronous Load Removal Time for the Input Register	C, E	0	0	ns
t_{IRECALn}	Asynchronous Load Recovery Time for the Input Register	C, E	0.074	0.087	ns
t_{IWALn}	Asynchronous Load Minimum Pulse Width for the Input Register	C, C	0.304	0.357	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Input Register	E, E	0.075	0.088	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Input Register	E, E	0.159	0.187	ns

Note: *For the derating values at specific junction temperature and voltage supply levels, refer to [Table 8 on page 18](#) for derating values.

8.8.2. Output/Enable Register

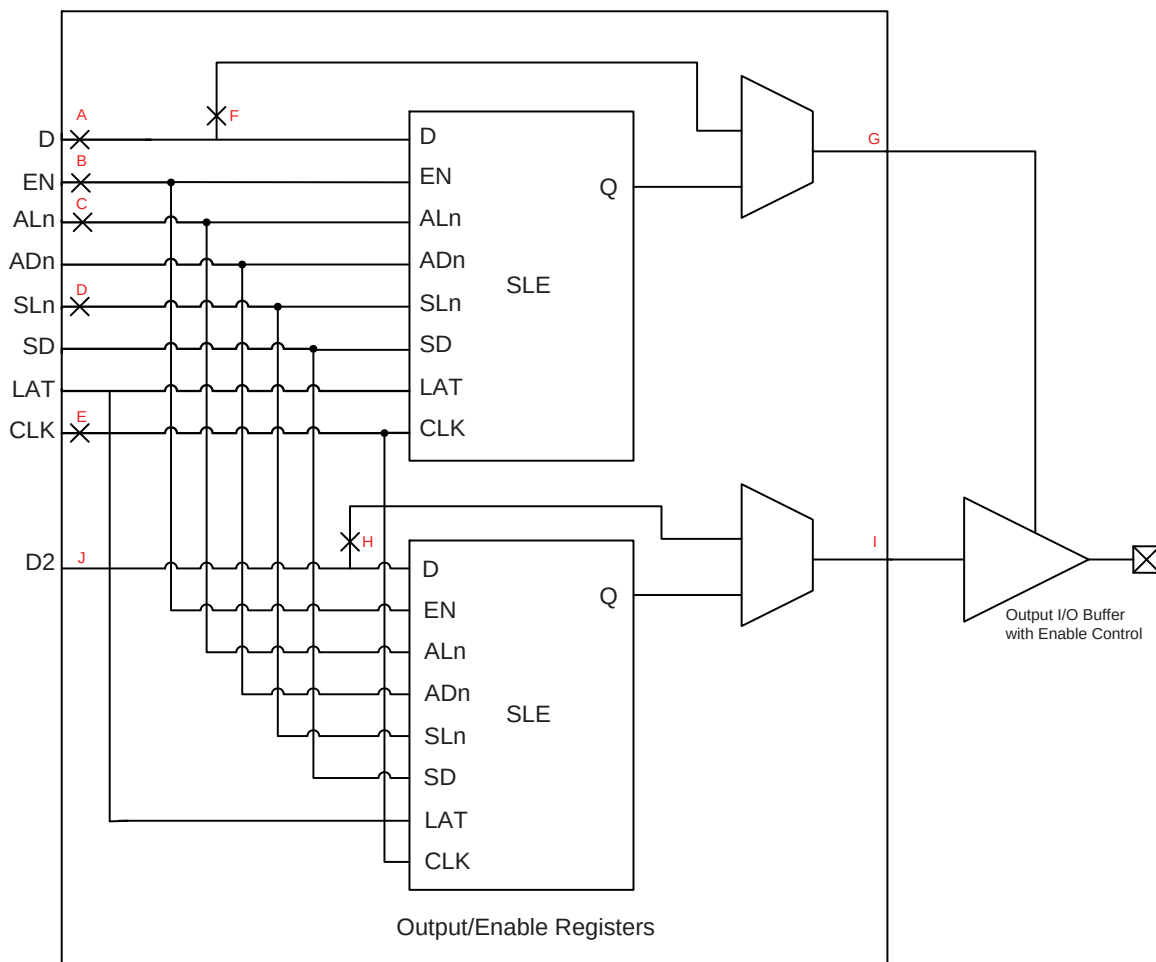


Figure 7 • Timing Model for Output/Enable Register

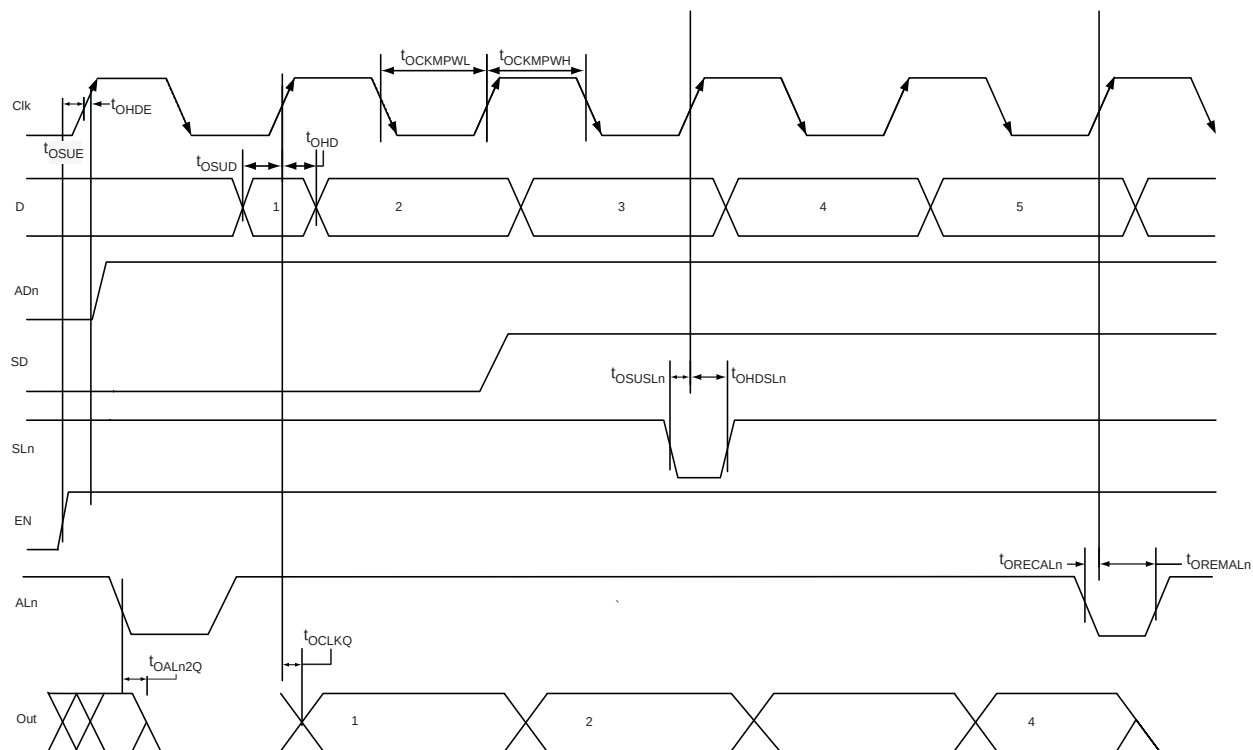
**Figure 8 • I/O Register Output Timing Diagram**

Table 90 • Output/Enable Data Register Propagation Delays
Worst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Measuring Nodes (from, to)*	-1	Std.	Units
t_{OBYP}	Bypass Delay of the Output/Enable Register	F, G or H, I	0.353	0.415	ns
t_{OCLKQ}	Clock-to-Q of the Output/Enable Register	E, G or E, I	0.263	0.309	ns
t_{OSUD}	Data Setup Time for the Output/Enable Register	A, E or J, E	0.19	0.223	ns
t_{OHD}	Data Hold Time for the Output/Enable Register	A, E or J, E	0	0	ns
t_{OSUE}	Enable Setup Time for the Output/Enable Register	B, E	0.419	0.493	ns
t_{OHE}	Enable Hold Time for the Output/Enable Register	B, E	0	0	ns
t_{OSUSL}	Synchronous Load Setup Time for the Output/Enable Register	D, E	0.196	0.231	ns
t_{OHSL}	Synchronous Load Hold Time for the Output/Enable Register	D, E	0	0	ns
t_{OALn2Q}	Asynchronous Clear-to-Q of the Output/Enable Register ($ADn = 1$)	C, G or C, I	0.505	0.594	ns
	Asynchronous Preset-to-Q of the Output/Enable Register ($ADn = 0$)	C, G or C, I	0.528	0.621	ns
$t_{OREMALn}$	Asynchronous Load Removal Time for the Output/Enable Register	C, E	0	0	ns
$t_{ORECALn}$	Asynchronous Load Recovery Time for the Output/Enable Register	C, E	0.034	0.04	ns
t_{OWALn}	Asynchronous Load Minimum Pulse Width for the Output/Enable Register	C, C	0.304	0.357	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output/Enable Register	E, E	0.075	0.088	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output/Enable Register	E, E	0.159	0.187	ns

Note: *For the derating values at specific junction temperature and voltage supply levels, refer to [Table 8 on page 18](#) for derating values.

8.9. DDR Module Specification

8.9.1. Input DDR Module

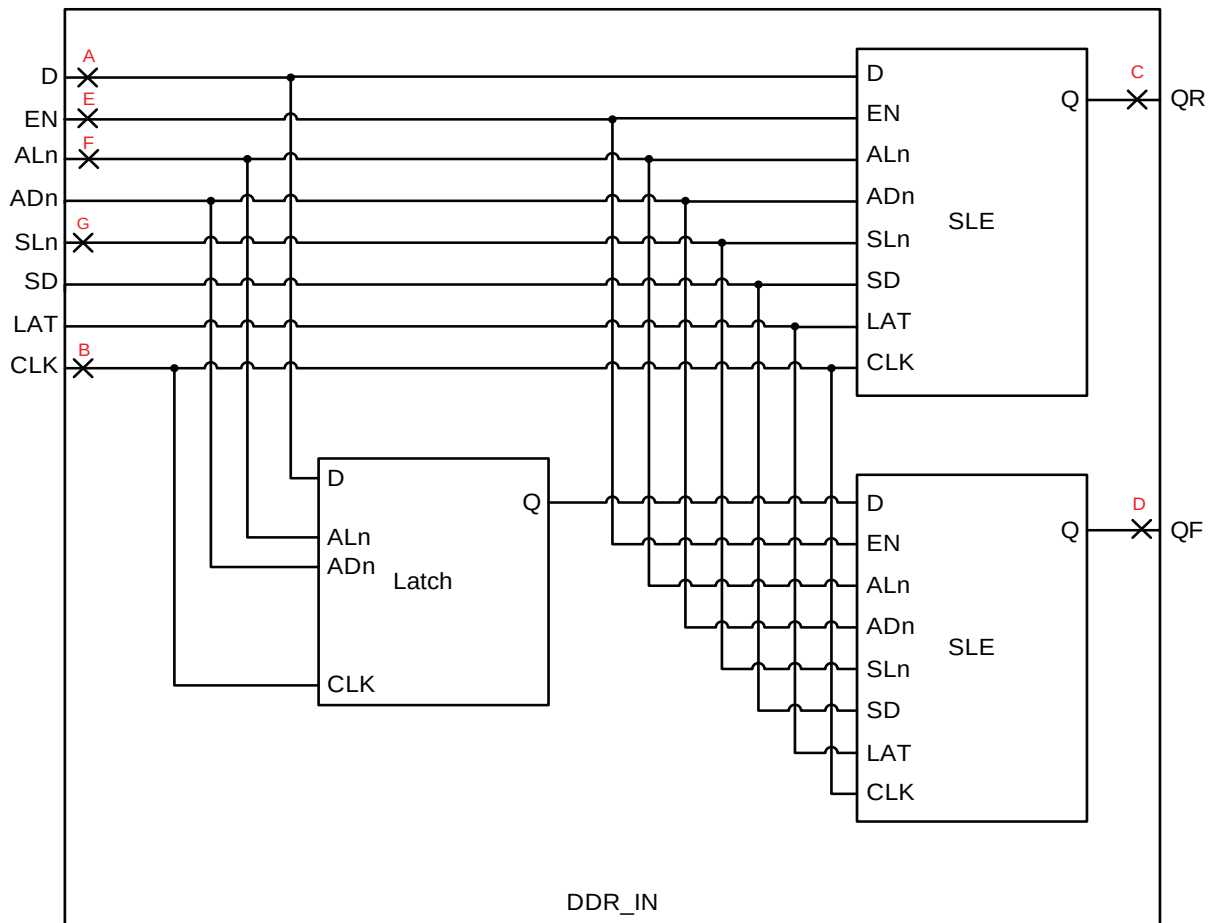


Figure 9 • Input DDR Module

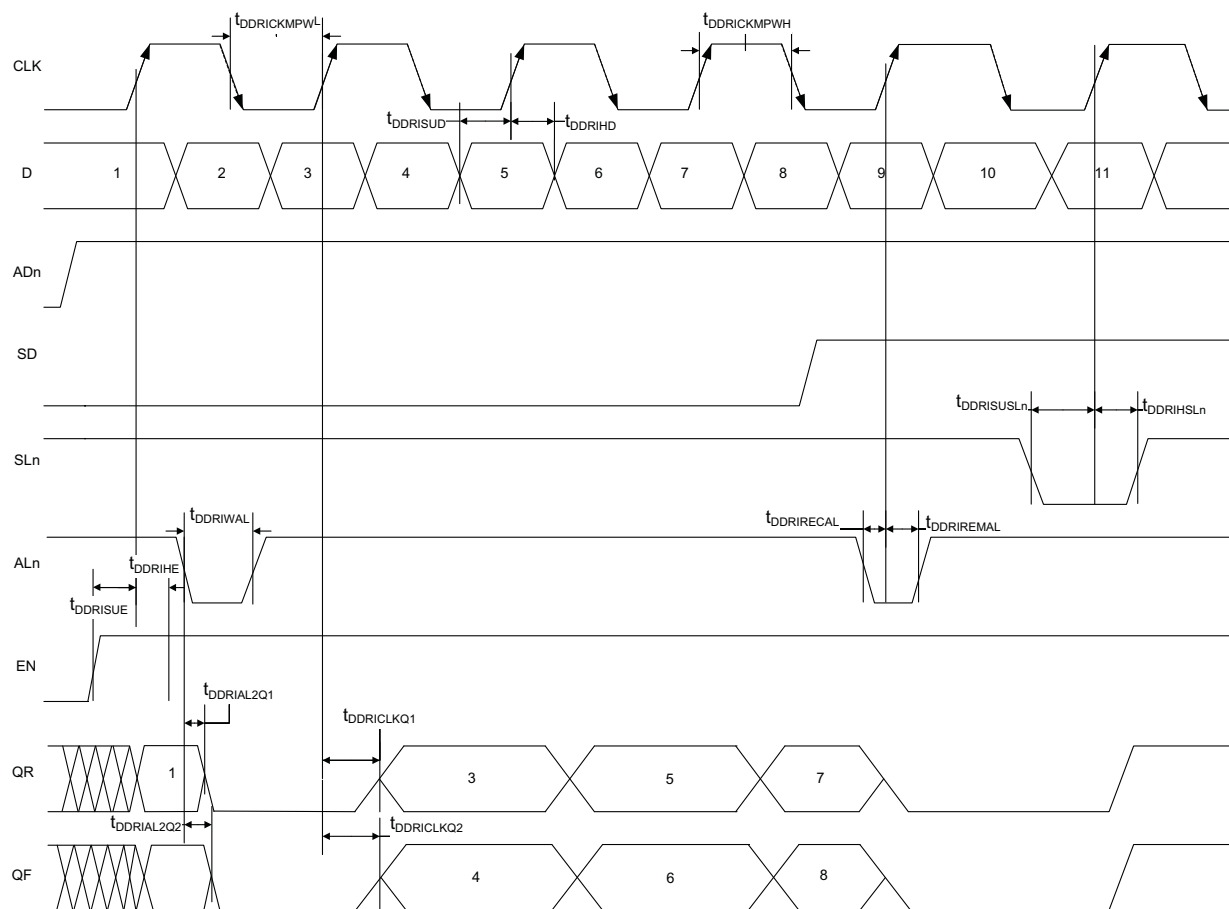


Figure 10 • Input DDR Timing Diagram

8.9.3. Timing Characteristics

Table 91 • Input DDR Propagation Delays
Worst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Measuring Nodes (from, to)	-1	Std.	Units
t_{DDRICKQ1}	Clock-to-Out Out_QR for Input DDR	B,C	0.16	0.188	ns
t_{DDRICKQ2}	Clock-to-Out Out_QF for Input DDR	B,D	0.166	0.195	ns
t_{DDRISUD}	Data Setup for Input DDR	A,B	0.357	0.421	ns
t_{DDRIHD}	Data Hold for Input DDR	A,B	0	0	ns
t_{DDRISUE}	Enable Setup for Input DDR	E,B	0.46	0.542	ns
t_{DDRIHE}	Enable Hold for Input DDR	E,B	0	0	ns
$t_{\text{DDRISUSLn}}$	Synchronous Load Setup for Input DDR	G,B	0.46	0.542	ns
t_{DDRIHSLn}	Synchronous Load Hold for Input DDR	G,B	0	0	ns
$t_{\text{DDRIAL2Q1}}$	Asynchronous Load-to-Out QR for Input DDR	F,C	0.587	0.69	ns
$t_{\text{DDRIAL2Q2}}$	Asynchronous Load-to-Out QF for Input DDR	F,D	0.541	0.636	ns
$t_{\text{DDRIREMAL}}$	Asynchronous Load Removal time for Input DDR	F,B	0	0	ns
$t_{\text{DDRIRECAL}}$	Asynchronous Load Recovery time for Input DDR	F,B	0.074	0.087	ns
t_{DDRIWAL}	Asynchronous Load Minimum Pulse Width for Input DDR	F,F	0.304	0.357	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width High for Input DDR	B,B	0.075	0.088	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width Low for Input DDR	B,B	0.159	0.187	ns

8.9.4. Output DDR Module

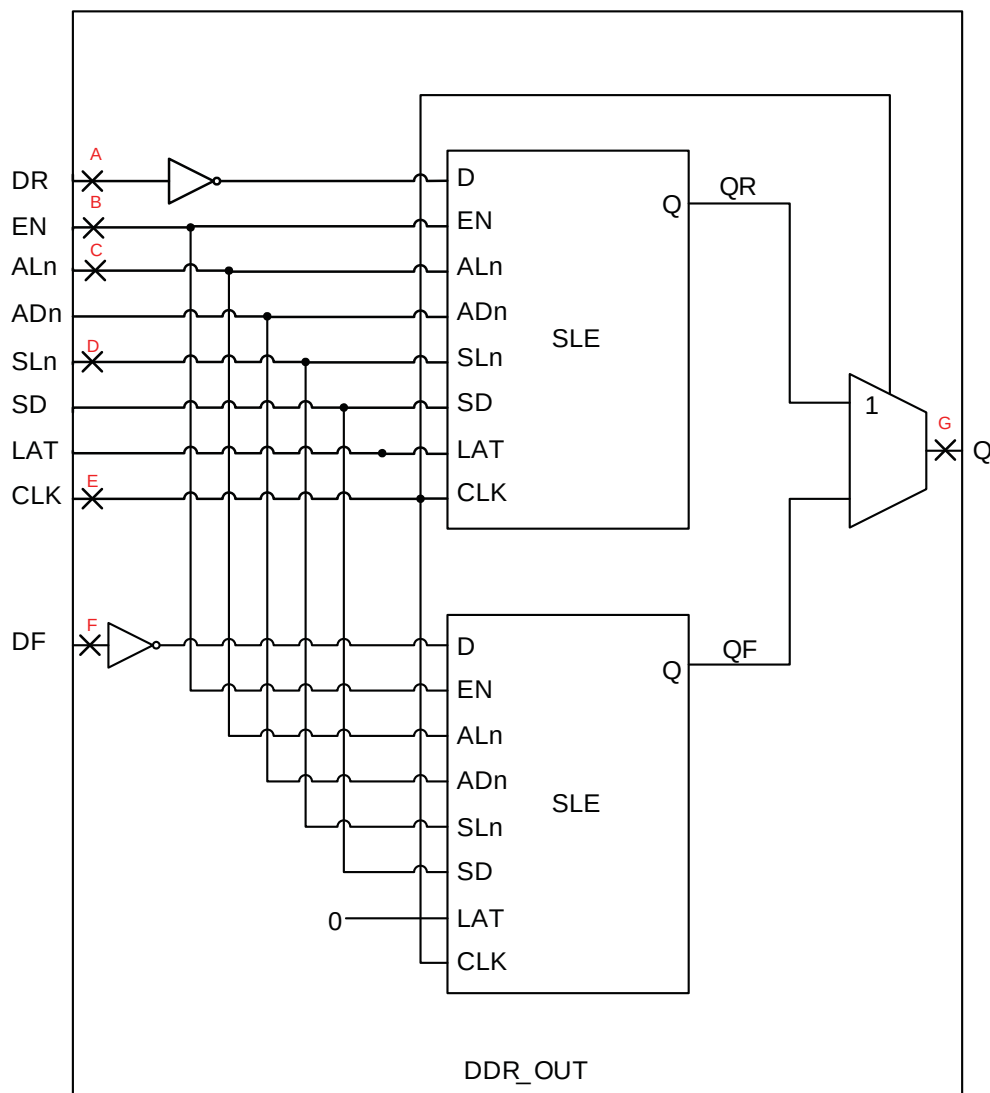
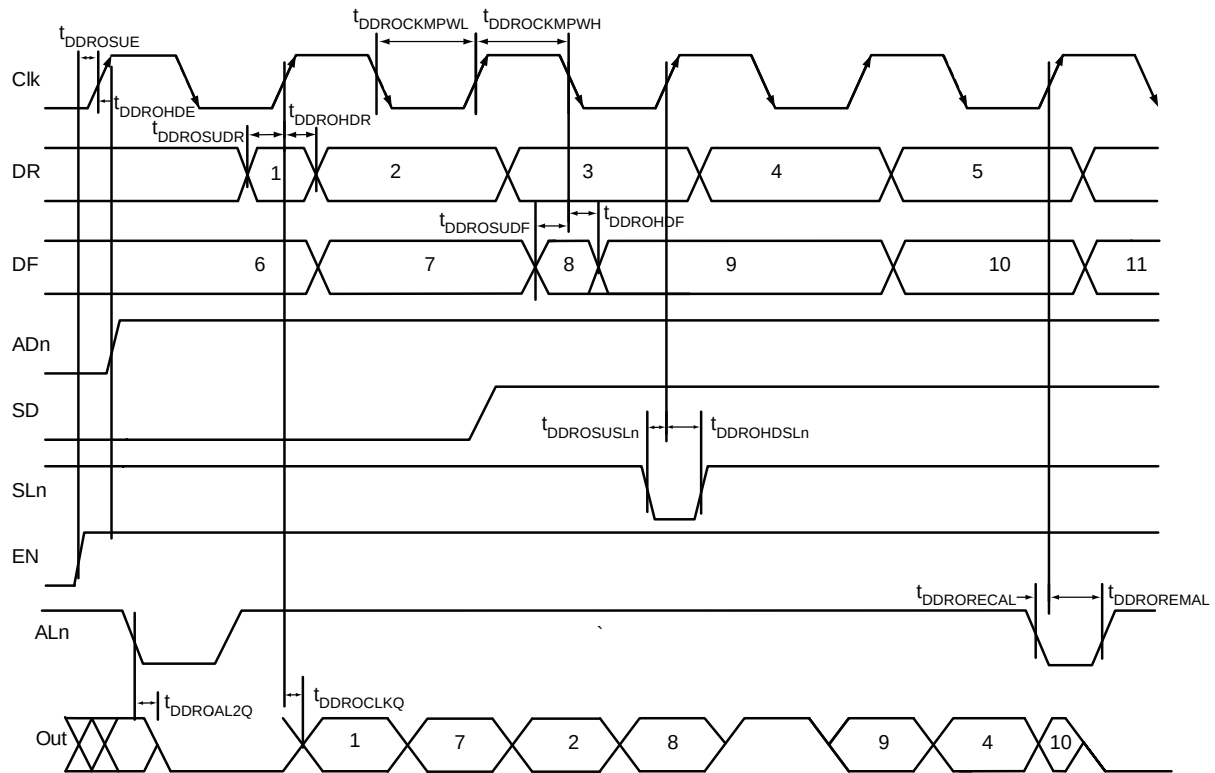


Figure 11 • Output DDR Module


Figure 12 • Output DDR Timing Diagram

8.9.5. Timing Characteristics

Table 92 • Output DDR Propagation Delays
Worst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Measuring Nodes (from, to)	-1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	E,G	0.263	0.309	ns
$t_{DDROSUDF}$	Data_F Data Setup for Output DDR	F,E	0.143	0.168	ns
$t_{DDROSUDR}$	Data_R Data Setup for Output DDR	A,E	0.19	0.223	ns
$t_{DDROHDF}$	Data_F Data Hold for Output DDR	F,E	0	0	ns
$t_{DDROHDR}$	Data_R Data Hold for Output DDR	A,E	0	0	ns
$t_{DDROSUE}$	Enable Setup for Input DDR	B,E	0.419	0.493	ns
t_{DDROHE}	Enable Hold for Input DDR	B,E	0	0	ns
$t_{DDROSUSLn}$	Synchronous Load Setup for Input DDR	D,E	0.196	0.231	ns
$t_{DDROHSLn}$	Synchronous Load Hold for Input DDR	D,E	0	0	ns
$t_{DDROAL2Q}$	Asynchronous Load-to-Out for Output DDR	C,G	0.528	0.621	ns
$t_{DDROREMA}$	Asynchronous Load Removal time for Output DDR	C,E	0	0	ns
$t_{DDRORECA}$	Asynchronous Load Recovery time for Output DDR	C,E	0.034	0.04	ns
$t_{DDROWAL}$	Asynchronous Load Minimum Pulse Width for Output DDR	C,C	0.304	0.357	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	E,E	0.075	0.088	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	E,E	0.159	0.187	ns

9. Logic Element Specifications

9.1. 4-input LUT (LUT-4)

The IGLOO2 and SmartFusion2 SoC FPGAs offer a fully permutable 4-input LUT. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the [IGLOO2 Macro Library Guide](#) or the [SmartFusion2 Macro Library Guide](#).

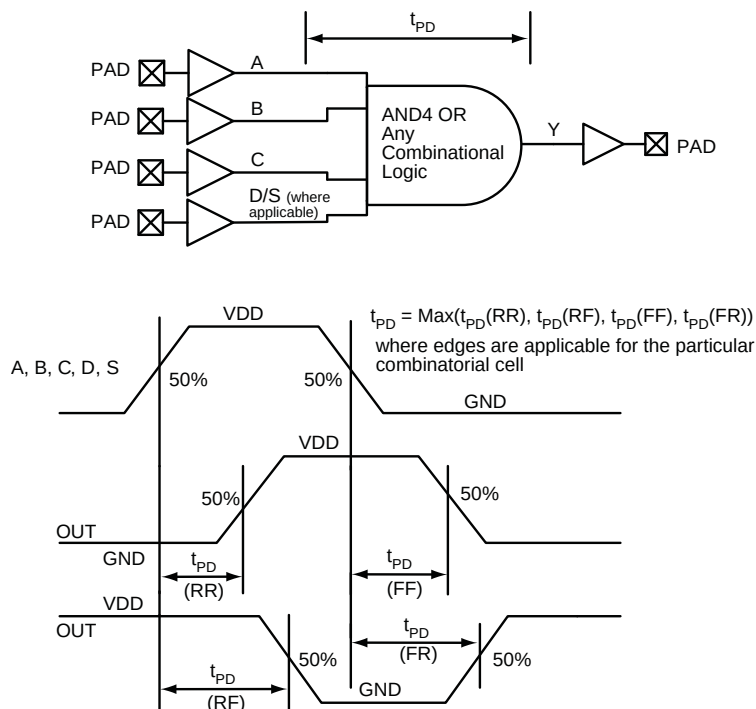


Figure 13 • LUT-4

Timing Characteristics

Table 93 • Combinatorial Cell Propagation Delays

Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Combinatorial Cell	Equation	Parameter	-1	Std.	Units	Notes
INV	$Y = !A$	t_{PD}	0.102	0.12	ns	
AND2	$Y = A \cdot B$	t_{PD}	0.179	0.211	ns	
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.144	0.169	ns	
OR2	$Y = A + B$	t_{PD}	0.179	0.211	ns	
NOR2	$Y = !(A + B)$	t_{PD}	0.144	0.169	ns	
XOR2	$Y = A \oplus B$	t_{PD}	0.179	0.211	ns	
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	0.241	0.283	ns	
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.198	0.233	ns	
AND4	$Y = A \cdot B \cdot C \cdot D$	t_{PD}	0.371	0.436	ns	

9.2. Sequential Module

IGLOO2 and SmartFusion2 SoC FPGAs offer a separate flip-flop which can be used independently from the LUT. The flip-flop can be configured as a register or a latch and has a data input and optional enable, synchronous load (clear or preset), and asynchronous load (clear or preset).

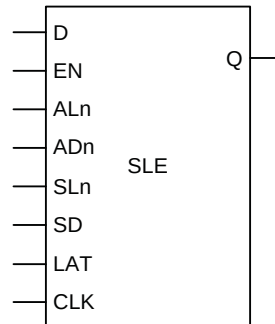


Figure 14 • Sequential Module

Figure 15 shows a configuration with $SD = 1$ (synchronous preset) and $ADn = 1$ (asynchronous clear) for a flip-flop ($LAT = 0$).

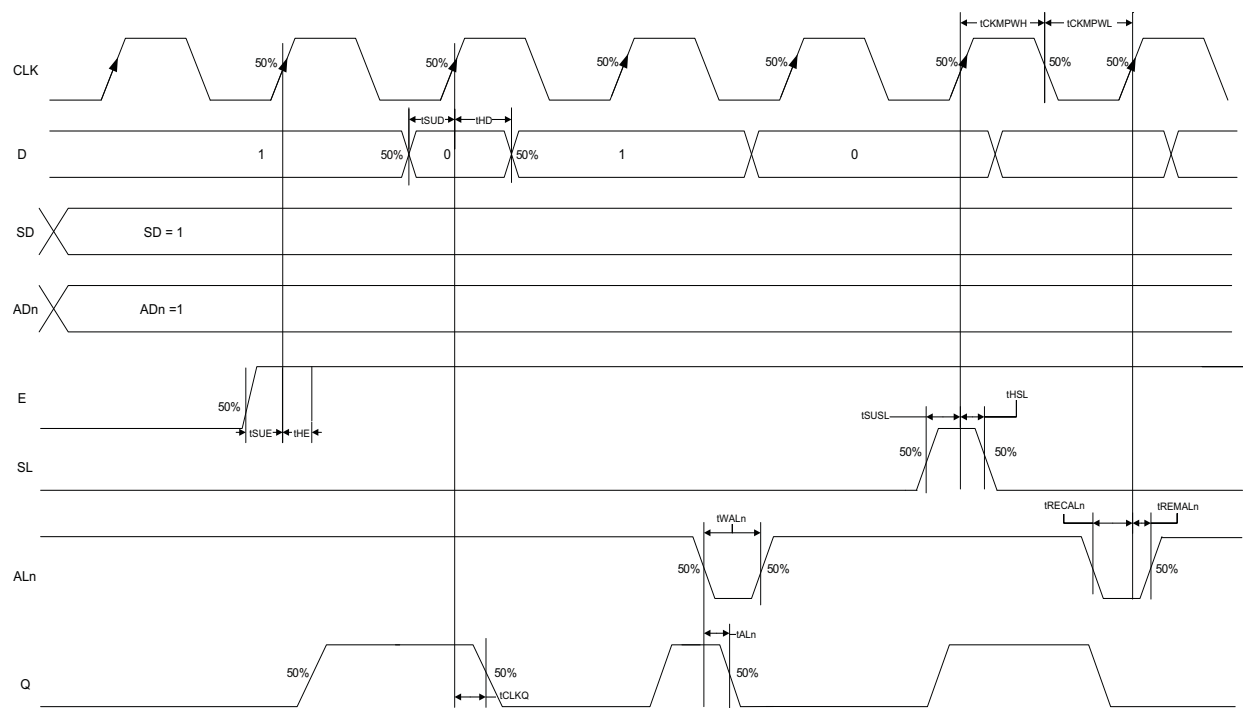


Figure 15 • Timing Diagram

9.2.1. Timing Characteristics

Table 94 • Register Delays

Worst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	–1	Std.	Units	Notes
t_{CLKQ}	Clock-to-Q of the Core register	0.108	0.127	ns	
t_{SUD}	Data Setup Time for the Core register	0.254	0.298	ns	
t_{HD}	Data Hold Time for the Core register	0	0	ns	
t_{SUE}	Enable Setup Time for the Core register	0.335	0.394	ns	
t_{HE}	Enable Hold Time for the Core register	0	0	ns	
t_{SUSL}	Synchronous Load Setup Time for the Core register	0.335	0.394	ns	
t_{HSL}	Synchronous Load Hold Time for the Core register	0	0	ns	
t_{ALn2Q}	Asynchronous Clear-to-Q of the Core register ($ADn = 1$)	0.473	0.556	ns	
	Asynchronous Preset-to-Q of the Core register ($ADn = 0$)	0.451	0.531	ns	
t_{REMAIn}	Asynchronous Load Removal Time for the Core register	0	0	ns	
t_{RECAIn}	Asynchronous Load Recovery Time for the Core register	0.353	0.415	ns	
t_{WALn}	Asynchronous Load Minimum Pulse Width for the Core register	0.304	0.357	ns	
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core register	0.075	0.088	ns	
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core register	0.159	0.187	ns	

10. Global Resource Characteristics

The IGLOO2 and SmartFusion2 SoC FPGA devices offer a powerful, low skew global routing network which provides an effective clock distribution throughout the FPGA fabric. Refer to the [IGLOO2 FPGA Fabric User Guide](#) or the [SmartFusion2 FPGA Fabric Architecture User Guide](#) for the positions of various global routing resources.

Table 95 • 150 Device Global Resource
Worst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	-1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RCKL}	Input Low Delay for Global Clock	0.83	0.911	0.831	0.913	ns	
t_{RCKH}	Input High Delay for Global Clock	1.457	1.588	1.715	1.869	ns	
t_{RCKSW}	Maximum Skew for Global Clock		0.131		0.154	ns	

Table 96 • 100 Device Global Resource
Worst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	-1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RCKL}	Input Low Delay for Global Clock	0.83	0.911	0.831	0.913	ns	
t_{RCKH}	Input High Delay for Global Clock	1.457	1.588	1.715	1.869	ns	
t_{RCKSW}	Maximum Skew for Global Clock		0.131		0.154	ns	

Table 97 • 090 Device Global Resource
Worst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	-1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RCKL}	Input Low Delay for Global Clock	0.835	0.888	0.833	0.886	ns	
t_{RCKH}	Input High Delay for Global Clock	1.405	1.489	1.654	1.752	ns	
t_{RCKSW}	Maximum Skew for Global Clock		0.084		0.098	ns	

Table 98 • 050 Device Global Resource
Worst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	-1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RCKL}	Input Low Delay for Global Clock	0.827	0.897	0.826	0.896	ns	
t_{RCKH}	Input High Delay for Global Clock	1.419	1.53	1.671	1.8	ns	
t_{RCKSW}	Maximum Skew for Global Clock		0.111		0.129	ns	

Table 99 • 025 Device Global ResourceWorst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	–1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RCKL}	Input Low Delay for Global Clock	0.747	0.799	0.745	0.797	ns	
t_{RCKH}	Input High Delay for Global Clock	1.294	1.378	1.522	1.621	ns	
t_{RCKSW}	Maximum Skew for Global Clock		0.084		0.099	ns	

Table 100 • 010 Device Global ResourceWorst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	–1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RCKL}	Input Low Delay for Global Clock	0.626	0.669	0.627	0.668	ns	
t_{RCKH}	Input High Delay for Global Clock	1.112	1.182	1.308	1.393	ns	
t_{RCKSW}	Maximum Skew for Global Clock		0.07		0.085	ns	

Table 101 • 005 Device Global ResourceWorst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	–1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RCKL}	Input Low Delay for Global Clock	0.625	0.66	0.628	0.66	ns	
t_{RCKH}	Input High Delay for Global Clock	1.126	1.187	1.325	1.397	ns	
t_{RCKSW}	Maximum Skew for Global Clock		0.061		0.072	ns	

11. FPGA Fabric SRAM

Refer to the [IGLOO2 FPGA Fabric User Guide](#) or the [SmartFusion2 FPGA Fabric User Guide](#) for more information.

11.1. FPGA Fabric Large SRAM (LSRAM)

Table 102 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 1K × 18
Worst Commercial-Case Conditions: $T_J = 85^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{CY}	Clock period	2.5	–	2.941	–	ns
$t_{CLKMPWH}$	Clock minimum pulse width High	1.125	–	1.323	–	ns
$t_{CLKMPWL}$	Clock minimum pulse width Low	1.125	–	1.323	–	ns
t_{PLCY}	Pipelined clock period	2.5	–	2.941	–	ns
$t_{PLCLKMPWH}$	Pipelined clock minimum pulse width High	1.125	–	1.323	–	ns
$t_{PLCLKMPWL}$	Pipelined clock minimum pulse width Low	1.125	–	1.323	–	ns
t_{CLK2Q}	Read access time with pipeline register	–	0.334	–	0.393	ns
	Read access time without pipeline register	–	2.273	–	2.674	ns
	Access time with feed-through write timing	–	1.529	–	1.799	ns
t_{ADDRSU}	Address setup time	0.441	–	0.519	–	ns
t_{ADDRHD}	Address hold time	0.274	–	0.322	–	ns
t_{DSU}	Data setup time	0.341	–	0.401	–	ns
t_{DHD}	Data hold time	0.107	–	0.126	–	ns
t_{BLKSU}	Block select setup time (with pipelined register enabled)	0.207	–	0.244	–	ns
t_{BLKHD}	Block select hold time (with pipelined register enabled)	0.216	–	0.254	–	ns
t_{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	1.529	–	1.799	ns
t_{BLKMPW}	Block select minimum pulse width	0.186	–	0.219	–	ns
t_{RDESU}	Read enable setup time (A_WEN , $B_WEN = 0$)	0.449	–	0.528	–	ns
t_{RDEHD}	Read enable hold time (A_WEN , $B_WEN = 0$)	0.167	–	0.197	–	ns
$t_{RDPLESU}$	Pipelined read enable setup time (A_DOUT_EN , B_DOUT_EN)	0.248	–	0.291	–	ns
$t_{RDPLEHD}$	Pipelined read enable hold time (A_DOUT_EN , B_DOUT_EN)	0.102	–	0.12	–	ns
t_{R2Q}	Asynchronous reset to output propagation delay	–	1.506	–	1.772	ns
t_{RSTREM}	Asynchronous reset removal time	0.506	–	0.595	–	ns
t_{RSTREC}	Asynchronous reset recovery time	0.004	–	0.005	–	ns
t_{RSTMPW}	Asynchronous reset minimum pulse width	0.301	–	0.354	–	ns
$t_{PLRSTREM}$	Pipelined register asynchronous reset removal time	-0.279	–	-0.328	–	ns
$t_{PLRSTREC}$	Pipelined register asynchronous reset recovery time	0.327	–	0.385	–	ns
$t_{PLRSTMPW}$	Pipelined register asynchronous reset minimum pulse width	0.282	–	0.332	–	ns
t_{SRSTSU}	Synchronous reset setup time	0.226	–	0.265	–	ns
t_{SRSTHD}	Synchronous reset hold time	0.036	–	0.043	–	ns
t_{WESU}	Write enable setup time (A_WEN , $B_WEN = 1$)	0.39	–	0.458	–	ns
t_{WEHD}	Write enable hold time (A_WEN , $B_WEN = 1$)	0.242	–	0.285	–	ns
f_{MAX}	Maximum frequency	–	400	–	340	Mhz

Table 103 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 2K × 9**Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Clock period	2.5	–	2.941	–	ns
t _{CLKMPWH}	Clock minimum pulse width High	1.125	–	1.323	–	ns
t _{CLKMPWL}	Clock minimum pulse width Low	1.125	–	1.323	–	ns
t _{PLCY}	Pipelined clock period	2.5	–	2.941	–	ns
t _{PLCLKMPWH}	Pipelined clock minimum pulse width High	1.125	–	1.323	–	ns
t _{PLCLKMPWL}	Pipelined clock minimum pulse width Low	1.125	–	1.323	–	ns
t _{CLK2Q}	Read access time with pipeline register	–	0.334	–	0.393	ns
	Read access time without pipeline register	–	2.273	–	2.674	ns
	Access time with feed-through write timing	–	1.529	–	1.799	ns
t _{ADDRSU}	Address setup time	0.475	–	0.559	–	ns
t _{ADDRHD}	Address hold time	0.274	–	0.322	–	ns
t _{DSU}	Data setup time	0.336	–	0.395	–	ns
t _{DHD}	Data hold time	0.082	–	0.096	–	ns
t _{BLKSU}	Block select setup time	0.207	–	0.244	–	ns
t _{BLKHD}	Block select hold time	0.216	–	0.254	–	ns
t _{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	1.529	–	1.799	ns
t _{BLKMPW}	Block select minimum pulse width	0.186	–	0.219	–	ns
t _{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.485	–	0.57	–	ns
t _{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.071	–	0.083	–	ns
t _{RDPLESU}	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.248	–	0.291	–	ns
t _{RDPLEHD}	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	0.102	–	0.12	–	ns
t _{R2Q}	Asynchronous reset to output propagation delay	–	1.514	–	1.781	ns
t _{RSTREM}	Asynchronous reset removal time	0.506	–	0.595	–	ns
t _{RSTREC}	Asynchronous reset recovery time	0.004	–	0.005	–	ns
t _{RSTMPW}	Asynchronous reset minimum pulse width	0.301	–	0.354	–	ns
t _{PLRSTREM}	Pipelined register asynchronous reset removal time	-0.279	–	-0.328	–	ns
t _{PLRSTREC}	Pipelined register asynchronous reset recovery time	0.327	–	0.385	–	ns
t _{PLRSTMPW}	Pipelined register asynchronous reset minimum pulse width	0.282	–	0.332	–	ns
t _{SRSTSU}	Synchronous reset setup time	0.226	–	0.265	–	ns
t _{SRSTHD}	Synchronous reset hold time	0.036	–	0.043	–	ns
t _{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.415	–	0.488	–	ns
t _{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.048	–	0.057	–	ns
f _{MAX}	Maximum frequency	–	400	–	340	Mhz

Table 104 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 4K × 4**Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Clock period	2.5	–	2.941	–	ns
t _{CLKMPWH}	Clock minimum pulse width High	1.125	–	1.323	–	ns
t _{CLKMPWL}	Clock minimum pulse width Low	1.125	–	1.323	–	ns
t _{PLCY}	Pipelined clock period	2.5	–	2.941	–	ns
t _{PLCLKMPWH}	Pipelined clock minimum pulse width High	1.125	–	1.323	–	ns
t _{PLCLKMPWL}	Pipelined clock minimum pulse width Low	1.125	–	1.323	–	ns
t _{CLK2Q}	Read access time with pipeline register	–	0.323	–	0.38	ns
	Read access time without pipeline register	–	2.273	–	2.673	ns
	Access time with feed-through write timing	–	1.511	–	1.778	ns
t _{ADDRSU}	Address setup time	0.543	–	0.638	–	ns
t _{ADDRHD}	Address hold time	0.274	–	0.322	–	ns
t _{DSU}	Data setup time	0.334	–	0.393	–	ns
t _{DHD}	Data hold time	0.082	–	0.096	–	ns
t _{BLKSU}	Block select setup time	0.207	–	0.244	–	ns
t _{BLKHD}	Block select hold time	0.216	–	0.254	–	ns
t _{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	1.511	–	1.778	ns
t _{BLKMPW}	Block select minimum pulse width	0.186	–	0.219	–	ns
t _{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.516	–	0.607	–	ns
t _{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.071	–	0.083	–	ns
t _{RDPLESU}	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.248	–	0.291	–	ns
t _{RDPLEHD}	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	0.102	–	0.12	–	ns
t _{R2Q}	Asynchronous reset to output propagation delay	–	1.507	–	1.773	ns
t _{RSTREM}	Asynchronous reset removal time	0.506	–	0.595	–	ns
t _{RSTREC}	Asynchronous reset recovery time	0.004	–	0.005	–	ns
t _{RSTMPW}	Asynchronous reset minimum pulse width	0.301	–	0.354	–	ns
t _{PLRSTREM}	Pipelined register asynchronous reset removal time	-0.279	–	-0.328	–	ns
t _{PLRSTREC}	Pipelined register asynchronous reset recovery time	0.327	–	0.385	–	ns
t _{PLRSTMPW}	Pipelined register asynchronous reset minimum pulse width	0.282	–	0.332	–	ns
t _{SRSTSU}	Synchronous reset setup time	0.226	–	0.265	–	ns
t _{SRSTHD}	Synchronous reset hold time	0.036	–	0.043	–	ns
t _{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.458	–	0.539	–	ns
t _{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.048	–	0.057	–	ns
f _{MAX}	Maximum frequency	–	400	–	340	Mhz

Table 105 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 8K × 2**Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V**

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Clock period	2.5	–	2.941	–	ns
t _{CLKMPWH}	Clock minimum pulse width High	1.125	–	1.323	–	ns
t _{CLKMPWL}	Clock minimum pulse width Low	1.125	–	1.323	–	ns
t _{PLCY}	Pipelined clock period	2.5	–	2.941	–	ns
t _{PLCLKMPWH}	Pipelined clock minimum pulse width High	1.125	–	1.323	–	ns
t _{PLCLKMPWL}	Pipelined clock minimum pulse width Low	1.125	–	1.323	–	ns
t _{CLK2Q}	Read access time with pipeline register	–	0.32	–	0.377	ns
	Read access time without pipeline register	–	2.272	–	2.673	ns
	Access time with feed-through write timing	–	1.511	–	1.778	ns
t _{ADDRSU}	Address setup time	0.612	–	0.72	–	ns
t _{ADDRHD}	Address hold time	0.274	–	0.322	–	ns
t _{DSU}	Data setup time	0.33	–	0.388	–	ns
t _{DHD}	Data hold time	0.082	–	0.096	–	ns
t _{BLKSU}	Block select setup time	0.207	–	0.244	–	ns
t _{BLKHD}	Block select hold time	0.216	–	0.254	–	ns
t _{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	1.511	–	1.778	ns
t _{BLKMPW}	Block select minimum pulse width	0.186	–	0.219	–	ns
t _{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.529	–	0.622	–	ns
t _{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.071	–	0.083	–	ns
t _{RDPLESU}	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.248	–	0.291	–	ns
t _{RDPLEHD}	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	0.102	–	0.12	–	ns
t _{R2Q}	Asynchronous reset to output propagation delay	–	1.528	–	1.797	ns
t _{RSTREM}	Asynchronous reset removal time	0.506	–	0.595	–	ns
t _{RSTREC}	Asynchronous reset recovery time	0.004	–	0.005	–	ns
t _{RSTMPW}	Asynchronous reset minimum pulse width	0.301	–	0.354	–	ns
t _{PLRSTREM}	Pipelined register asynchronous reset removal time	-0.279	–	-0.328	–	ns
t _{PLRSTREC}	Pipelined register asynchronous reset recovery time	0.327	–	0.385	–	ns
t _{PLRSTMPW}	Pipelined register asynchronous reset minimum pulse width	0.282	–	0.332	–	ns
t _{SRSTSU}	Synchronous reset setup time	0.226	–	0.265	–	ns
t _{SRSTHD}	Synchronous reset hold time	0.036	–	0.043	–	ns
t _{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.488	–	0.574	–	ns
t _{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.048	–	0.057	–	ns
f _{MAX}	Maximum frequency	–	400	–	340	Mhz

Table 106 • RAM1K18 – Dual-Port Mode for Depth × Width Configuration 16K × 1
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	–1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Clock period	2.5	–	2.941	–	ns
t _{CLKMPWH}	Clock minimum pulse width High	1.125	–	1.323	–	ns
t _{CLKMPWL}	Clock minimum pulse width Low	1.125	–	1.323	–	ns
t _{PLCY}	Pipelined clock period	2.5	–	2.941	–	ns
t _{PLCLKMPWH}	Pipelined clock minimum pulse width High	1.125	–	1.323	–	ns
t _{PLCLKMPWL}	Pipelined clock minimum pulse width Low	1.125	–	1.323	–	ns
t _{CLK2Q}	Read access time with pipeline register	–	0.32	–	0.377	ns
	Read access time without pipeline register	–	2.269	–	2.669	ns
	Access time with feed-through write timing	–	1.51	–	1.777	ns
t _{ADDRSU}	Address setup time	0.626	–	0.737	–	ns
t _{ADDRHD}	Address hold time	0.274	–	0.322	–	ns
t _{DSU}	Data setup time	0.322	–	0.378	–	ns
t _{DHD}	Data hold time	0.082	–	0.096	–	ns
t _{BLKSU}	Block select setup time	0.207	–	0.244	–	ns
t _{BLKHD}	Block select hold time	0.216	–	0.254	–	ns
t _{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	1.51	–	1.777	ns
t _{BLKMPW}	Block select minimum pulse width	0.186	–	0.219	–	ns
t _{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.53	–	0.624	–	ns
t _{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.071	–	0.083	–	ns
t _{RDPLESU}	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.248	–	0.291	–	ns
t _{RDPLEHD}	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	0.102	–	0.12	–	ns
t _{R2Q}	Asynchronous reset to output propagation delay	–	1.547	–	1.82	ns
t _{RSTREM}	Asynchronous reset removal time	0.506	–	0.595	–	ns
t _{RSTREC}	Asynchronous reset recovery time	0.004	–	0.005	–	ns
t _{RSTMPW}	Asynchronous reset minimum pulse width	0.301	–	0.354	–	ns
t _{PLRSTREM}	Pipelined register asynchronous reset removal time	-0.279	–	-0.328	–	ns
t _{PLRSTREC}	Pipelined register asynchronous reset recovery time	0.327	–	0.385	–	ns
t _{PLRSTMPW}	Pipelined register asynchronous reset minimum pulse width	0.282	–	0.332	–	ns
t _{SRSTSU}	Synchronous reset setup time	0.226	–	0.265	–	ns
t _{SRSTHD}	Synchronous reset hold time	0.036	–	0.043	–	ns
t _{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.454	–	0.534	–	ns
t _{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.048	–	0.057	–	ns
f _{MAX}	Maximum frequency	–	400	–	340	Mhz

Table 107 • RAM1K18 – Two-Port Mode for Depth × Width Configuration 512 × 36
Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Clock period	2.5	–	2.941	–	ns
t _{CLKMPWH}	Clock minimum pulse width High	1.125	–	1.323	–	ns
t _{CLKMPWL}	Clock minimum pulse width Low	1.125	–	1.323	–	ns
t _{PLCY}	Pipelined clock period	2.5	–	2.941	–	ns
t _{PLCLKMPWH}	Pipelined clock minimum pulse width High	1.125	–	1.323	–	ns
t _{PLCLKMPWL}	Pipelined clock minimum pulse width Low	1.125	–	1.323	–	ns
t _{CLK2Q}	Read access time with pipeline register	–	0.334	–	0.393	ns
	Read access time without pipeline register	–	2.25	–	2.647	ns
t _{ADDRSU}	Address setup time	0.313	–	0.368	–	ns
t _{ADDRHD}	Address hold time	0.274	–	0.322	–	ns
t _{DSU}	Data setup time	0.337	–	0.396	–	ns
t _{DHD}	Data hold time	0.111	–	0.13	–	ns
t _{BLKSU}	Block select setup time	0.207	–	0.244	–	ns
t _{BLKHD}	Block select hold time	0.201	–	0.237	–	ns
t _{BLK2Q}	Block select to out disable time (when pipelined register is disabled)	–	2.25	–	2.647	ns
t _{BLKMPW}	Block select minimum pulse width	0.186	–	0.219	–	ns
t _{RDESU}	Read enable setup time (A_WEN, B_WEN = 0)	0.449	–	0.528	–	ns
t _{RDEHD}	Read enable hold time (A_WEN, B_WEN = 0)	0.167	–	0.197	–	ns
t _{RDPLESU}	Pipelined read enable setup time (A_DOUT_EN, B_DOUT_EN)	0.248	–	0.291	–	ns
t _{RDPLEHD}	Pipelined read enable hold time (A_DOUT_EN, B_DOUT_EN)	0.102	–	0.12	–	ns
t _{R2Q}	Asynchronous reset to output propagation delay	–	1.506	–	1.772	ns
t _{RSTREM}	Asynchronous reset removal time	0.506	–	0.595	–	ns
t _{RSTREC}	Asynchronous reset recovery time	0.004	–	0.005	–	ns
t _{RSTMPW}	Asynchronous reset minimum pulse width	0.301	–	0.354	–	ns
t _{PLRSTREM}	Pipelined register asynchronous reset removal time	-0.279	–	-0.328	–	ns
t _{PLRSTREC}	Pipelined register asynchronous reset recovery time	0.327	–	0.385	–	ns
t _{PLRSTMPW}	Pipelined register asynchronous reset minimum pulse width	0.282	–	0.332	–	ns
t _{SRSTSU}	Synchronous reset setup time	0.226	–	0.265	–	ns
t _{SRSTHD}	Synchronous reset hold time	0.036	–	0.043	–	ns
t _{WESU}	Write enable setup time (A_WEN, B_WEN = 1)	0.39	–	0.458	–	ns
t _{WEHD}	Write enable hold time (A_WEN, B_WEN = 1)	0.242	–	0.285	–	ns
f _{MAX}	Maximum frequency	–	400	–	340	Mhz

11.2. FPGA Fabric Micro SRAM (uSRAM)

Table 108 • uSRAM (RAM64x18) in 64x18 Mode

Worst Commercial-Case Conditions: TJ = 85°C, VDD = 1.14 V

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Read clock period	4		4		ns
t _{CLKMPWH}	Read clock minimum pulse width High	1.8		1.8		ns
t _{CLKMPWL}	Read clock minimum pulse width Low	1.8		1.8		ns
t _{PLCY}	Read pipeline clock period	4		4		ns
t _{PLCLKMPWH}	Read pipeline clock minimum pulse width High	1.8		1.8		ns
t _{PLCLKMPWL}	Read pipeline clock minimum pulse width Low	1.8		1.8		ns
t _{CLK2Q}	Read access time with pipeline register		0.266		0.313	ns
	Read access time without pipeline register		1.677		1.973	ns
t _{ADDRSU}	Read address setup time in synchronous mode	0.301		0.354		ns
	Read address setup time in asynchronous mode	1.856		2.184		ns
t _{ADDRHD}	Read address hold time in synchronous mode	0.091		0.107		ns
	Read address hold time in asynchronous mode	-0.778		-0.915		ns
t _{RDENSU}	Read enable setup time	0.278		0.327		ns
t _{RDENHD}	Read enable hold time	0.057		0.067		ns
t _{BLKSU}	Read block select setup time (with pipeline register enabled)	1.839		2.163		ns
t _{BLKHD}	Read block select hold time (with pipelined register enabled)	-0.65		-0.765		ns
t _{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)		2.036		2.396	ns
t _{RSTREM}	Read asynchronous reset removal time (pipelined clock)	-0.023		-0.027		ns
	Read asynchronous reset removal time (non-pipelined clock)	0.046		0.054		ns
t _{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.507		0.597		ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.236		0.278		ns
t _{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)		0.839		0.987	ns
t _{SRSTSU}	Read synchronous reset setup time	0.271		0.319		ns
t _{SRSTHD}	Read synchronous reset hold time	0.061		0.071		ns
t _{CCY}	Write clock period	4		4.705		ns
t _{CCLKMPWH}	Write clock minimum pulse width High	1.8		2.117		ns
t _{CCLKMPWL}	Write clock minimum pulse width Low	1.8		2.117		ns
t _{BLKCSU}	Write block setup time	0.404		0.476		ns
t _{BLKCHD}	Write block hold time	0.007		0.008		ns
t _{DINCSU}	Write input data setup time	0.115		0.135		ns
t _{DINCHD}	Write input data hold time	0.15		0.177		ns
t _{ADDRCSU}	Write address setup time	0.088		0.104		ns
t _{ADDRCHD}	Write address hold time	0.128		0.15		ns
t _{WECSU}	Write enable setup time	0.397		0.467		ns

Table 108 • uSRAM (RAM64x18) in 64x18 Mode**Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V (continued)**

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{WECHD}	Write enable hold time	-0.026		-0.03		ns
f _{MAX}	Maximum frequency		250		250	MHz

Table 109 • uSRAM (RAM64x16) in 64x16 Mode**Worst Commercial-Case Conditions: TJ = 85°C, VDD = 1.14 V**

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Read clock period	4		4		ns
t _{CLKMPWH}	Read clock minimum pulse width High	1.8		1.8		ns
t _{CLKMPWL}	Read clock minimum pulse width Low	1.8		1.8		ns
t _{PLCY}	Read pipeline clock period	4		4		ns
t _{PLCLKMPWH}	Read pipeline clock minimum pulse width High	1.8		1.8		ns
t _{PLCLKMPWL}	Read pipeline clock minimum pulse width Low	1.8		1.8		ns
t _{CLK2Q}	Read access time with pipeline register		0.266		0.313	ns
	Read access time without pipeline register		1.677		1.973	ns
t _{ADDRSU}	Read address setup time in synchronous mode	0.301		0.354		ns
	Read address setup time in asynchronous mode	1.856		2.184		ns
t _{ADDRHD}	Read address hold time in synchronous mode	0.091		0.107		ns
	Read address hold time in asynchronous mode	-0.778		-0.915		ns
t _{RDENSU}	Read enable setup time	0.278		0.327		ns
t _{RDENHD}	Read enable hold time	0.057		0.067		ns
t _{BLKSU}	Read block select setup time (with pipeline register enabled)	1.839		2.163		ns
t _{BLKHD}	Read block select hold time (with pipelined register enabled)	-0.65		-0.765		ns
t _{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)		2.036		2.396	ns
t _{RSTREM}	Read asynchronous reset removal time (pipelined clock)	-0.023		-0.027		ns
	Read asynchronous reset removal time (non-pipelined clock)	0.046		0.054		ns
t _{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.507		0.597		ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.236		0.278		ns
t _{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)		0.839		0.987	ns
t _{SRSTSU}	Read synchronous reset setup time	0.271		0.319		ns
t _{SRSTHD}	Read synchronous reset hold time	0.061		0.071		ns
t _{CCY}	Write clock period	4		4.705		ns
t _{CCLKMPWH}	Write clock minimum pulse width High	1.8		2.117		ns
t _{CCLKMPWL}	Write clock minimum pulse width Low	1.8		2.117		ns
t _{BLKCSU}	Write block setup time	0.404		0.476		ns
t _{BLKCHD}	Write block hold time	0.007		0.008		ns
t _{DINCSU}	Write input data setup time	0.115		0.135		ns
t _{DINCHD}	Write input data hold time	0.15		0.177		ns
t _{ADDRCSU}	Write address setup time	0.088		0.104		ns
t _{ADDRCHD}	Write address hold time	0.128		0.15		ns
t _{WECSU}	Write enable setup time	0.397		0.467		ns

Table 109 • uSRAM (RAM64x16) in 64x16 Mode**Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V (continued)**

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{WECHD}	Write enable hold time	-0.026		-0.03		ns
f _{MAX}	Maximum frequency		250		250	MHz

Table 110 • uSRAM (RAM128x9) in 128x9 Mode**Worst Commercial-Case Conditions: TJ = 85°C, VDD = 1.14 V**

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Read clock period	4		4		ns
t _{CLKMPWH}	Read clock minimum pulse width High	1.8		1.8		ns
t _{CLKMPWL}	Read clock minimum pulse width Low	1.8		1.8		ns
t _{PLCY}	Read pipeline clock period	4		4		ns
t _{PLCLKMPWH}	Read pipeline clock minimum pulse width High	1.8		1.8		ns
t _{PLCLKMPWL}	Read pipeline clock minimum pulse width Low	1.8		1.8		ns
t _{CLK2Q}	Read access time with pipeline register		0.266		0.313	ns
	Read access time without pipeline register		1.677		1.973	ns
t _{ADDRSU}	Read address setup time in synchronous mode	0.301		0.354		ns
	Read address setup time in asynchronous mode	1.856		2.184		ns
t _{ADDRHD}	Read address hold time in synchronous mode	0.091		0.107		ns
	Read address hold time in asynchronous mode	-0.778		-0.915		ns
t _{RDENSU}	Read enable setup time	0.278		0.327		ns
t _{RDENHD}	Read enable hold time	0.057		0.067		ns
t _{BLKSU}	Read block select setup time (with pipeline register enabled)	1.839		2.163		ns
t _{BLKHD}	Read block select hold time (with pipelined register enabled)	-0.65		-0.765		ns
t _{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)		2.036		2.396	ns
t _{RSTREM}	Read asynchronous reset removal time (pipelined clock)	-0.023		-0.027		ns
	Read asynchronous reset removal time (non-pipelined clock)	0.046		0.054		ns
t _{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.507		0.597		ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.236		0.278		ns
t _{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)		0.839		0.987	ns
t _{SRSTSU}	Read synchronous reset setup time	0.271		0.319		ns
t _{SRSTHD}	Read synchronous reset hold time	0.061		0.071		ns
t _{CCY}	Write clock period	4		4.705		ns
t _{CCLKMPWH}	Write clock minimum pulse width High	1.8		2.117		ns
t _{CCLKMPWL}	Write clock minimum pulse width Low	1.8		2.117		ns
t _{BLKCSU}	Write block setup time	0.404		0.476		ns
t _{BLKCHD}	Write block hold time	0.007		0.008		ns
t _{DINCSU}	Write input data setup time	0.115		0.135		ns
t _{DINCHD}	Write input data hold time	0.15		0.177		ns
t _{ADDRCSU}	Write address setup time	0.088		0.104		ns
t _{ADDRCHD}	Write address hold time	0.128		0.15		ns
t _{WECSU}	Write enable setup time	0.397		0.467		ns

Table 110 • uSRAM (RAM128x9) in 128x9 Mode**Worst Commercial-Case Conditions: T_J = 85°C, V_{DD} = 1.14 V (continued)**

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{WECHD}	Write enable hold time	-0.026		-0.03		ns
f _{MAX}	Maximum frequency		250		250	MHz

Table 111 • uSRAM (RAM128x8) in 128x8 Mode
Worst Commercial-Case Conditions: TJ = 85°C, VDD = 1.14 V

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Read clock period	4		4		ns
t _{CLKMPWH}	Read clock minimum pulse width High	1.8		1.8		ns
t _{CLKMPWL}	Read clock minimum pulse width Low	1.8		1.8		ns
t _{PLCY}	Read pipeline clock period	4		4		ns
t _{PLCLKMPWH}	Read pipeline clock minimum pulse width High	1.8		1.8		ns
t _{PLCLKMPWL}	Read pipeline clock minimum pulse width Low	1.8		1.8		ns
t _{CLK2Q}	Read access time with pipeline register		0.266		0.313	ns
	Read access time without pipeline register		1.677		1.973	ns
t _{ADDRSU}	Read address setup time in synchronous mode	0.301		0.354		ns
	Read address setup time in asynchronous mode	1.856		2.184		ns
t _{ADDRHD}	Read address hold time in synchronous mode	0.091		0.107		ns
	Read address hold time in asynchronous mode	-0.778		-0.915		ns
t _{RDENSU}	Read enable setup time	0.278		0.327		ns
t _{RDENHD}	Read enable hold time	0.057		0.067		ns
t _{BLKSU}	Read block select setup time (with pipeline register enabled)	1.839		2.163		ns
t _{BLKHD}	Read block select hold time (with pipelined register enabled)	-0.65		-0.765		ns
t _{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)		2.036		2.396	ns
t _{RSTREM}	Read asynchronous reset removal time (pipelined clock)	-0.023		-0.027		ns
	Read asynchronous reset removal time (non-pipelined clock)	0.046		0.054		ns
t _{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.507		0.597		ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.236		0.278		ns
t _{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)		0.839		0.987	ns
t _{SRSTSU}	Read synchronous reset setup time	0.271		0.319		ns
t _{SRSTHD}	Read synchronous reset hold time	0.061		0.071		ns
t _{CCY}	Write clock period	4		4.705		ns
t _{CCLKMPWH}	Write clock minimum pulse width High	1.8		2.117		ns
t _{CCLKMPWL}	Write clock minimum pulse width Low	1.8		2.117		ns
t _{BLKCSU}	Write block setup time	0.404		0.476		ns
t _{BLKCHD}	Write block hold time	0.007		0.008		ns
t _{DINCSU}	Write input data setup time	0.115		0.135		ns
t _{DINCHD}	Write input data hold time	0.15		0.177		ns
t _{ADDRCSU}	Write address setup time	0.088		0.104		ns
t _{ADDRCHD}	Write address hold time	0.128		0.15		ns
t _{WECSU}	Write enable setup time	0.397		0.467		ns

Table 111 • uSRAM (RAM128x8) in 128x8 Mode**Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V (continued)**

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{WECHD}	Write enable hold time	-0.026		-0.03		ns
f _{MAX}	Maximum frequency		250		250	MHz

Table 112 • uSRAM (RAM256x4) in 256x4 Mode
Worst Commercial-Case Conditions: TJ = 85°C, VDD = 1.14 V

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Read clock period	4		4		ns
t _{CLKMPWH}	Read clock minimum pulse width High	1.8		1.8		ns
t _{CLKMPWL}	Read clock minimum pulse width Low	1.8		1.8		ns
t _{PLCY}	Read pipeline clock period	4		4		ns
t _{PLCLKMPWH}	Read pipeline clock minimum pulse width High	1.8		1.8		ns
t _{PLCLKMPWL}	Read pipeline clock minimum pulse width Low	1.8		1.8		ns
t _{CLK2Q}	Read access time with pipeline register		0.27		0.31	ns
	Read access time without pipeline register		1.75		2.06	ns
t _{ADDRSU}	Read address setup time in synchronous mode	0.301		0.354		ns
	Read address setup time in asynchronous mode	1.931		2.272		ns
t _{ADDRHD}	Read address hold time in synchronous mode	0.121		0.142		ns
	Read address hold time in asynchronous mode	-0.65		-0.76		ns
t _{RDENSU}	Read enable setup time	0.278		0.327		ns
t _{RDENHD}	Read enable hold time	0.057		0.067		ns
t _{BLKSU}	Read block select setup time (with pipeline register enabled)	1.839		2.163		ns
t _{BLKHD}	Read block select hold time (with pipelined register enabled)	-0.65		-0.77		ns
t _{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)		2.09		2.46	ns
t _{RSTREM}	Read asynchronous reset removal time (pipelined clock)	-0.02		-0.03		ns
	Read asynchronous reset removal time (non-pipelined clock)	0.046		0.054		ns
t _{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.507		0.597		ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.236		0.278		ns
t _{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)		0.83		0.98	ns
t _{SRSTSU}	Read synchronous reset setup time	0.271		0.319		ns
t _{SRSTHD}	Read synchronous reset hold time	0.061		0.071		ns
t _{CCY}	Write clock period	4		4.705		ns
t _{CCLKMPWH}	Write clock minimum pulse width High	1.8		2.117		ns
t _{CCLKMPWL}	Write clock minimum pulse width Low	1.8		2.117		ns
t _{BLKCSU}	Write block setup time	0.404		0.476		ns
t _{BLKCHD}	Write block hold time	0.007		0.008		ns
t _{DINCSU}	Write input data setup time	0.101		0.118		ns
t _{DINCHD}	Write input data hold time	0.137		0.161		ns
t _{ADDRCSU}	Write address setup time	0.088		0.104		ns
t _{ADDRCHD}	Write address hold time	0.245		0.288		ns
t _{WECSU}	Write enable setup time	0.397		0.467		ns

Table 112 • uSRAM (RAM256x4) in 256x4 Mode**Worst Commercial-Case Conditions: T_J = 85°C, V_{DD} = 1.14 V (continued)**

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{WECHD}	Write enable hold time	-0.03		-0.03		ns
f _{MAX}	Maximum frequency		250		250	MHz

Table 113 • uSRAM (RAM512x2) in 512x2 Mode**Worst Commercial-Case Conditions: TJ = 85°C, VDD = 1.14 V**

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Read clock period	4		4		ns
t _{CLKMPWH}	Read clock minimum pulse width High	1.8		1.8		ns
t _{CLKMPWL}	Read clock minimum pulse width Low	1.8		1.8		ns
t _{PLCY}	Read pipeline clock period	4		4		ns
t _{PLCLKMPWH}	Read pipeline clock minimum pulse width High	1.8		1.8		ns
t _{PLCLKMPWL}	Read pipeline clock minimum pulse width Low	1.8		1.8		ns
t _{CLK2Q}	Read access time with pipeline register		0.27		0.31	ns
	Read access time without pipeline register		1.76		2.08	ns
t _{ADDRSU}	Read address setup time in synchronous mode	0.301		0.354		ns
	Read address setup time in asynchronous mode	1.96		2.306		ns
t _{ADDRHD}	Read address hold time in synchronous mode	0.137		0.161		ns
	Read address hold time in asynchronous mode	-0.58		-0.68		ns
t _{RDENSU}	Read enable setup time	0.278		0.327		ns
t _{RDENHD}	Read enable hold time	0.057		0.067		ns
t _{BLKSU}	Read block select setup time (with pipeline register enabled)	1.839		2.163		ns
t _{BLKHD}	Read block select hold time (with pipelined register enabled)	-0.65		-0.77		ns
t _{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)		2.14		2.52	ns
t _{RSTREM}	Read asynchronous reset removal time (pipelined clock)	-0.02		-0.03		ns
	Read asynchronous reset removal time (non-pipelined clock)	0.046		0.054		ns
t _{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.507		0.597		ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.236		0.278		ns
t _{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)		0.83		0.98	ns
t _{SRSTSU}	Read synchronous reset setup time	0.271		0.319		ns
t _{SRSTHD}	Read synchronous reset hold time	0.061		0.071		ns
t _{CCY}	Write clock period	4		4.705		ns
t _{CCLKMPWH}	Write clock minimum pulse width High	1.8		2.117		ns
t _{CCLKMPWL}	Write clock minimum pulse width Low	1.8		2.117		ns
t _{BLKCSU}	Write block setup time	0.404		0.476		ns
t _{BLKCHD}	Write block hold time	0.007		0.008		ns
t _{DINCSU}	Write input data setup time	0.101		0.118		ns
t _{DINCHD}	Write input data hold time	0.137		0.161		ns
t _{ADDRCSU}	Write address setup time	0.088		0.104		ns
t _{ADDRCHD}	Write address hold time	0.247		0.29		ns
t _{WECSU}	Write enable setup time	0.397		0.467		ns

Table 113 • uSRAM (RAM512x2) in 512x2 Mode**Worst Commercial-Case Conditions: T_J = 85°C, VDD = 1.14 V (continued)**

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{WECHD}	Write enable hold time	-0.03		-0.03		ns
f _{MAX}	Maximum frequency		250		250	MHz

Table 114 • uSRAM (RAM1024x1) in 1024x1 Mode**Worst Commercial-Case Conditions: TJ = 85°C, VDD = 1.14 V**

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t _{CY}	Read clock period	4		4		ns
t _{CLKMPWH}	Read clock minimum pulse width High	1.8		1.8		ns
t _{CLKMPWL}	Read clock minimum pulse width Low	1.8		1.8		ns
t _{PLCY}	Read pipeline clock period	4		4		ns
t _{PLCLKMPWH}	Read pipeline clock minimum pulse width High	1.8		1.8		ns
t _{PLCLKMPWL}	Read pipeline clock minimum pulse width Low	1.8		1.8		ns
t _{CLK2Q}	Read access time with pipeline register		0.27		0.31	ns
	Read access time without pipeline register		1.78		2.1	ns
t _{ADDRSU}	Read address setup time in synchronous mode	0.301		0.354		ns
	Read address setup time in asynchronous mode	1.978		2.327		ns
t _{ADDRHD}	Read address hold time in synchronous mode	0.137		0.161		ns
	Read address hold time in asynchronous mode	-0.6		-0.71		ns
t _{RDENSU}	Read enable setup time	0.278		0.327		ns
t _{RDENHD}	Read enable hold time	0.057		0.067		ns
t _{BLKSU}	Read block select setup time (with pipeline register enabled)	1.839		2.163		ns
t _{BLKHD}	Read block select hold time (with pipelined register enabled)	-0.65		-0.77		ns
t _{BLK2Q}	Read block select to out disable time (when pipelined register is disabled)		2.16		2.54	ns
t _{RSTREM}	Read asynchronous reset removal time (pipelined clock)	-0.02		-0.03		ns
	Read asynchronous reset removal time (non-pipelined clock)	0.046		0.054		ns
t _{RSTREC}	Read asynchronous reset recovery time (pipelined clock)	0.507		0.597		ns
	Read asynchronous reset recovery time (non-pipelined clock)	0.236		0.278		ns
t _{R2Q}	Read asynchronous reset to output propagation delay (with pipelined register enabled)		0.83		0.98	ns
t _{SRSTSU}	Read synchronous reset setup time	0.271		0.319		ns
t _{SRSTHD}	Read synchronous reset hold time	0.061		0.071		ns
t _{CCY}	Write clock period	4		4.705		ns
t _{CCLKMPWH}	Write clock minimum pulse width High	1.8		2.117		ns
t _{CCLKMPWL}	Write clock minimum pulse width Low	1.8		2.117		ns
t _{BLKCSU}	Write block setup time	0.404		0.476		ns
t _{BLKCHD}	Write block hold time	0.007		0.008		ns
t _{DINCSU}	Write input data setup time	0.003		0.004		ns
t _{DINCHD}	Write input data hold time	0.137		0.161		ns
t _{ADDRCSU}	Write address setup time	0.088		0.104		ns
t _{ADDRCHD}	Write address hold time	0.247		0.29		ns
t _{WECSU}	Write enable setup time	0.397		0.467		ns

Table 114 • uSRAM (RAM1024x1) in 1024x1 ModeWorst Commercial-Case Conditions: $T_J = 85^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

Parameter	Description	-1		Std.		Units
		Min.	Max.	Min.	Max.	
t_{WECHD}	Write enable hold time	-0.03		-0.03		ns
f_{MAX}	Maximum frequency		250		250	MHz

12. On-Chip Oscillators

Table 115 through Table 117 on page 106 describe the electrical characteristics of the available on-chip oscillators in the IGLOO2 and SmartFusion2 SoC FPGAs.

Table 115 • Electrical Characteristics of the Crystal OscillatorWorst-Case Industrial Conditions: $T_J = 100^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Condition	Min.	Typ.	Max.	Units	Notes
FXTAL	Operating frequency	—	—	32	—	KHz	
ACCXTAL	Accuracy	High Gain Mode (20 MHz)			0.0047	%	
		Medium Gain Mode (2 MHz)			0.00105	%	
		Low Gain Mode (32 KHz)			0.000429	%	
CYCXTAL	Output duty cycle	High Gain Mode (20 MHz)		1	3	%	
		Medium Gain Mode (2 MHz)		1	3	%	
		Low Gain Mode (32 KHz)		1	3	%	
JITPERXTAL	Output Period Jitter (peak-to-peak)	High Gain Mode (20 MHz)		200	300	ps	
		Medium Gain Mode (2 MHz)		1	5	ns	
		Low Gain Mode (32 KHz)		150	300	ns	
JITCYCXTAL	Output Cycle-to-Cycle Jitter (peak-to-peak)	High Gain Mode (20 MHz)		200	300	ps	
		Medium Gain Mode (2 MHz)		1	5	ns	
		Low Gain Mode (32 KHz)		150	300	ns	
IDYNXTAL	Operating current	High Gain Mode (20 MHz)			1.5	mA	
		Medium Gain Mode (2 MHz)			0.3	mA	
		Low Gain Mode (32 KHz)			0.044	mA	
VIHXTAL	Input logic level High		$0.9 \times V_{PP}$			V	
VILXTAL	Input logic level Low				$0.1 \times V_{PP}$	V	
SUXTAL	Startup time (w.r.t. stable oscillator output)	High Gain Mode (20 MHz)			0.8	μs	
		Medium Gain Mode (2 MHz)			4.5	μs	
		Low Gain Mode (32 KHz)			115	μs	

Table 116 • Electrical Characteristics of the 50 MHz RC OscillatorWorst-Case Industrial Conditions: $T_J = 100^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Condition	Min.	Typ.	Max.	Units	Notes
F50RC	Operating frequency		–	50	–	MHz	
ACC50RC	Accuracy			1	4	%	
CYC50RC	Output duty cycle			1	3	%	
JIT50RC	Output jitter	Period jitter		200	300	ps	
		Cycle-to-cycle jitter		200	300	ps	
IDYN50RC	Operating current			6.5		mA	

Table 117 • Electrical Characteristics of the 1 MHz RC OscillatorWorst-Case Industrial Conditions: $T_J = 100^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Condition	Min.	Typ.	Max.	Units	Notes
F1RC	Operating frequency		–	1	–	MHz	
ACC1RC	Accuracy			1	3	%	
CYC1RC	Output duty cycle			1	3	%	
JIT1RC	Output jitter	Period jitter		10	20	ns	
		Cycle-to-cycle jitter		10	20	ns	
IDYN1RC	Operating current			0.1		mA	
SU1RC	Startup time				17	μs	

13. Clock Conditioning Circuits (CCC)

Table 118 • IGLOO2 and SmartFusion2 SoC FPGAs CCC/PLL Specification

Worst-Case Industrial Conditions: $T_J = 100^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter			Minimum	Typical	Maximum	Units	Notes
Clock conditioning circuitry input frequency $f_{\text{IN_CCC}}$			1		200	MHz	
Clock conditioning circuitry output frequency $f_{\text{OUT_CCC}}$			20		400	MHz	
Delay increments in programmable delay blocks				75	100	ps	
Number of programmable values in each programmable delay block					64		
Acquisition time				70	100	μs	
Output duty cycle			48		52	%	
Spread Spectrum Characteristics							
Modulation frequency range			25	35	50	kHz	
Modulation depth range			0		1.5	%	
Modulation depth control				0.5		%	
Maximum peak-to-peak period jitter							
Parameter	Conditions/Package Combinations					Units	Notes
CCC output peak-to-peak period jitter $F_{\text{CCC_OUT}}$							
	SSO = 0	$0 < \text{SSO} \leq 2$	$\text{SSO} \leq 4$	$\text{SSO} \leq 8$	$\text{SSO} \leq 16$		*
20 MHz to 100 MHz	$110 \text{ ps} < \text{jitter} < \pm 1\% f_{\text{OUT_CCC}}$	$150 \text{ ps} < \text{jitter} < \pm 1\% f_{\text{OUT_CCC}}$				ps	
100 MHz to 400 MHz	$120 \text{ ps} < \text{jitter} < \pm 1\% f_{\text{OUT_CCC}}$	$150 \text{ ps} < \text{jitter} < \pm 1\% f_{\text{OUT_CCC}}$		$170 \text{ ps} < \text{jitter} < \pm 1\% f_{\text{OUT_CCC}}$		ps	
<i>Note:</i> * SSO Data is based on LVCMOS 2.5 V MSIOD Bank I/Os on the M2GL050/M2S050 FG896 Package.							

14. JTAG

Table 119 • JTAG 1532

Worst-Case Industrial Conditions: $T_J = 100^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	-1	Std.	Units	Notes
t_{DISU}	Test data input setup time	-0.3	-0.26	ns	
t_{DIHD}	Test data input hold time	2.08	2.45	ns	
t_{TMSSU}	Test mode select setup time	0.29	0.35	ns	
t_{TMDHD}	Test mode select hold time	0.17	0.2	ns	
t_{TCK2Q}	Clock to Q (data out)	7.86	9.25	ns	
t_{RSTB2Q}	Reset to Q (data out)	8.87	10.44	ns	
F_{TCKMAX}	TCK maximum frequency	25	21.25	MHz	

Note: For specific junction temperature and voltage supply levels, refer to [Table 8 on page 18](#) for derating values.

15. System Controller SPI Characteristics

Table 120 • System Controller SPI Characteristics

Worst-Case Industrial Conditions: $T_J = 100^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Symbol	Description	Conditions	All Devices/Speed Grades			Units	Notes
			Min	Type	Max		
sp1	SC_SPI_SCK minimum period		-	-	20	ns	
sp2	SC_SPI_SCK minimum pulse width high		-	-	10	ns	
sp3	SC_SPI_SCK minimum pulse width low		-	-	10	ns	
sp4	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS rise time (10%-90%) 1	IO Configuration: LVTTTL 3.3 V- 20 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25°C	-	1.239	-	ns	1
sp5	SC_SPI_SCK, SC_SPI_SDO, SC_SPI_SS fall time (10%-90%) 1	IO Configuration: LVTTTL 3.3 V- 20 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25°C	-	1.245	-	ns	1
sp6	Data from master (SC_SPI_SDO) setup time		-	-	160	ns	
sp7	Data from master (SC_SPI_SDO) hold time		-	-	160	ns	
sp8	SC_SPI_SDI setup time		-	-	20	ns	
sp9	SC_SPI_SDI hold time		-	-	20	ns	

Notes:

- For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website:
<http://www.microsemi.com/soc/download/ibis/default.aspx>. Please use the supported I/O Configurations for System Controller SPI on [Table 121 • Supported I/O Configurations for System Controller SPI \(MSIO Bank Only\)](#).

Table 121 • Supported I/O Configurations for System Controller SPI (MSIO Bank Only)

Voltage Supply	I/O Drive Configuration	Units	Notes
3.3V	20	mA	
2.5V	16	mA	
1.8V	12	mA	
1.5V	8	mA	
1.2V	4	mA	

16. Mathblock Timing Characteristics

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. Each IGLOO2 and SmartFusion2 SoC mathblock supports 18x18 signed multiplication, dot product, and built-in addition, subtraction, and accumulation units to combine multiplication results efficiently.

Table 122 • Mathblocks with All Registers Used

Parameter	Description	-1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t _{MISU}	Input, control register setup time	0.149		0.176		ns	
t _{MIHD}	Input, control register hold time	1.68		1.976		ns	
t _{MOCDINSU}	CDIN input setup time	0.185		0.218		ns	
t _{MOCDINHD}	CDIN input hold time	0.08		0.094		ns	
t _{MSRSTENSU}	Synchronous reset/enable setup time	-0.419		-0.493		ns	
t _{MSRSTENHD}	Synchronous reset/enable hold time	0.011		0.013		ns	
t _{MARSTREM}	Asynchronous reset removal time	0		0		ns	
t _{MARSTREC}	Asynchronous reset recovery time	0.088		0.104		ns	
t _{MOCQ}	Output register clock to out delay		0.232		0.273	ns	
t _{MCLKMP}	CLK minimum period	2.245		2.641		ns	

Table 123 • Mathblock with Input Bypassed and Output Registers Used

Parameter	Description	-1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t _{MOSU}	Output register setup time	2.294		2.699		ns	
t _{MOHD}	Output register hold time	1.68		1.976		ns	
t _{MOCDINSU}	CDIN input setup time	0.115		0.136		ns	
t _{MOCDINHD}	CDIN input hold time	-0.444		-0.522		ns	
t _{MSRSTENSU}	Synchronous reset/enable setup time	-0.419		-0.493		ns	
t _{MSRSTENHD}	Synchronous reset/enable hold time	0.011		0.013		ns	
t _{MARSTREM}	Asynchronous reset removal time	0		0		ns	
t _{MARSTREC}	Asynchronous reset recovery time	0.014		0.017		ns	

Table 123 • Mathblock with Input Bypassed and Output Registers Used (continued)

t_{MOCQ}	Output register clock to out delay		0.232		0.273	ns	
t_{MCLKMP}	CLK minimum period	2.179		2.563		ns	

Table 124 • Mathblock with Input Register Used and Output in Bypass Mode

Parameter	Description	-1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{MISU}	Input register setup time	0.149		0.176		ns	
t_{MIHD}	Input register hold time	0.185		0.218		ns	
$t_{MSRSTENSU}$	Synchronous reset/enable setup time	0.08		0.094		ns	
$t_{MSRSTENHD}$	Synchronous reset/enable hold time	-0.012		-0.014		ns	
$t_{MARSTREM}$	Asynchronous reset removal time	-0.005		-0.005		ns	
$t_{MARSTREC}$	Asynchronous reset recovery time	0.088		0.104		ns	
t_{MICQ}	Input register clock to output delay		2.52		2.964	ns	
$t_{MCDIN2Q}$	CDIN to output delay		1.951		2.295	ns	

Table 125 • Mathblock with Input and Output in Bypass Mode

Parameter	Description	-1		Std.		Units	Notes
		Min.	Max.	Min.	Max.		
t_{MIQ}	Input to output delay	–	2.568	–	3.022	ns	
$t_{MCDIN2Q}$	CDIN to output delay	–	1.951	–	2.295	ns	

Table 126 • Flash*Freeze Entry and Exit TimesWorst-Case Industrial Conditions: $T_J = 100^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Symbols	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
TFF_ENTRY	Entry Time	eNVM and HPMS PLL=ON	–	–	150	us	
		eNVM and HPMS PLL=OFF	–	–	200	us	
TFF_EXIT	Exit Time with respect to HPMS PLL Lock	eNVM and HPMS PLL=ON during F*F	–	–	100	us	
		eNVM=ON and HPMS PLL=OFF during F*F and HPMS PLL turned back on at exit	–	–	120	us	
		eNVM and HPMS PLL=OFF during F*F and both are turned back on at exit	–	–	200	us	
		eNVM=OFF and HPMS PLL=ON during F*F and eNVM turned back on at exit	–	–	200	us	
	Exit Time with respect to Fabric PLL Lock	eNVM and HPMS PLL=ON during F*F	–	–	1.5	μs	
		eNVM and HPMS PLL=OFF during F*F and both are turned back on at exit	–	–	1.5	μs	
	Exit Time with respect to Fabric buffer output	eNVM and HPMS PLL=ON during F*F	–	–	15	us	
		eNVM and HPMS PLL=OFF during F*F and both are turned back on at exit	–	–	55	us	

17. PCIe Electrical and Timing AC and DC Characteristics

PCIe® is a high speed, packet-based, point-to-point, low pin count, serial interconnect bus. The IGLOO2 and SmartFusion2 SoC FPGAs has up to four hard high-speed serial interface blocks. Each SERDES block contains a PCIe system block. The PCIe system is connected to the SERDES block.

Table 127 • Transmitter Parameters

Worst-Case Industrial Conditions: $T_J = 100^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Min.	Typ.	Max.	Units	Notes
VTX-DIFF-PP	Differential swing PCIe Gen 1 and 2	0.8	–	1.2	V	
VTX-CM-AC-P	Output common mode voltage PCIe Gen 1	–	–	20	mV	
VTX-CM-AC-PP	Output common mode voltage PCIe Gen 2	–	–	100	mV	
VTX-RISE-FALL	Rise and fall time (20% to 80%) PCIe Gen 1	0.125	–	–	UI	
	Rise and fall time (20% to 80%) PCIe Gen 2	0.15	–	–	UI	
ZTX-DIFF-DC	Output impedance – differential	80	–	120	ohm	
LTX-SKEW	Lane-to-lane TX skew within a SERDES block PCIe Gen 1	–	–	500 ps + 2 UI	ps	
	Lane-to-lane TX skew within a SERDES block PCIe Gen 2	–	–	500 ps +4 UI	ps	
RLTX-DIFF	Return loss differential mode PCIe Gen 1	–10	–	–	dB	
	Return loss differential mode PCIe Gen 2	–10 (min.) 0.05 – 1.25 GHz – 8 (min.) 1.25 – 2.5 GHz			dB	
RLTX-CM	Return loss common mode PCIe Gen 1 and 2	–6	–	–	dB	
	Transmit PLL lock time from reset	–	–	10	μs	

Table 128 • Receiver Parameters

Worst-Case Industrial Conditions: $T_J = 100^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Description	Min	Typ	Max	Units	Notes
VRX-DIFF-PP-CC	Input levels PCIe Gen 1	0.175	–	1.2	V	
	Input levels PCIe Gen 2	0.12	–	1.2	V	
VRX-CM-DC-P	Input common mode range (DC coupled) Note: PCIe standard mandates AC coupling	NA	NA	NA	-	
VRX-CM-AC-P	Input common mode range (AC coupled)	–	–	150	mV	
VRX-DIFF-PP-CC	Differential input sensitivity PCIe Gen 1	0.175	–	–	mV	
	Differential input sensitivity PCIe Gen 2	0.12	–	–	mV	
ZRX-DIFF-DC	Differential input termination	80	100	120	Ohms	
REXT	External calibration resistor	1,188	1,200	1,212	Ohms	
	CDR relock time from reset	–	–	15	μs	
RLRX-DIFF	Return loss differential mode PCIe Gen 1	–10	–	–	dB	
	Return loss differential mode PCIe Gen 2	–10 (min.) 0.05 – 1.25 GHz – 8 (min.) 1.25 – 2.5 GHz			dB	
RLRX-CM	Return loss common mode PCIe Gen 1 and 2	–6	–	–	dB	
	CID limit (set by 8B/10B coding, not the receiver PLL)	–	–	4	UI	
VRX-IDLE-DET-DIFF-PP	Signal detect limit	65	–	175	mV	

Table 129 • SERDES Reference Clock AC Specifications
Worst-Case Industrial Conditions: $T_J = 100^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Symbols	Description	Conditions	Min.	Typ.	Max.	Units	Notes
FREFCLK	Reference Clock Frequency		100		160	MHz	
TRISE	Reference Clock Rise Time		0.6		4	V/ns	
TFALL	Reference Clock Fall Time		0.6		4	V/ns	
TCYC	Reference Clock Duty Cycle		40		60	%	
Mmrefclk	Reference Clock Mismatch		-300		300	ppm	
SSCref	Reference Spread Spectrum Clock		0		5000	ppm	

18. SmartFusion2 Specifications

18.1. SmartFusion2 Inter-Integrated Circuit (I²C) Characteristics

This section describes the DC and switching of the I²C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, refer to Figure 16 on page 114.

Table 130 • I²C Characteristics

Worst-Case Industrial Conditions: T_J = 100°C, VDD = 1.14 V

Parameter	Definition	Conditions	Min.	Typ.	Max.	Units	Notes
VIL	Input low voltage	Refer to the "Single-Ended I/O Standards" section on page 24 for more information. I/O standard used for illustration: MSIO bank – LVTTTL 8 mA low drive.	–0.3	–	0.8	V	
VIH	Input high voltage	Refer to the "Single-Ended I/O Standards" section on page 24 for more information. I/O standard used for illustration: MSIO bank – LVTTTL 8 mA low drive.	2	–	3.45	V	
VHYS	Hysteresis of Schmitt triggered inputs for VDDI > 2 V	Refer to Table 14 on page 24 for more information.	0.05 * VDDI	–	–	V	
IIL	Input current high	Refer to the "Single-Ended I/O Standards" section on page 24 for more information.	–	–	10	μA	
IIH	Input current low	Refer to the "Single-Ended I/O Standards" section on page 24 for more information.	–	–	10	μA	
VOL	Maximum output voltage low (open drain) at 3 mA sink current for VDDI > 2 V	Refer to the "Single-Ended I/O Standards" section on page 24 for more information. I/O standard used for illustration: MSIO bank – LVTTTL 8 mA low drive.	–	–	0.4	V	
Cin	Pin capacitance	VIN = 0, f = 1.0 MHz	–	–	10	pF	
t _{OF}	Output fall time from VIHmin to VILMax	VIHmin to VILMax, Cload = 400 pF	–	21.04	–	ns	1
		VIHmin to VILMax, Cload = 100 pF	–	5.556	–	ns	
t _{OR}	Output rise time from VILMax to VIHmin	VILMax to VIHmin, Cload = 400pF	–	19.887	–	ns	1
		VILMax to VIHmin, Cload = 100pF	–	5.218	–	ns	
Rpull-up	Output buffer maximum pull-down resistance		–	–	50	Ohms	2, 3

Notes:

1. These values are provided for MSIO Bank - LVTTTL 8 mA Low Drive at 25°C, typical conditions. For Board Design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. These maximum values are provided for information only. Minimum output buffer resistance values depend on VDDIx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
3. $R(\text{PULL-DOWN-MAX}) = (V_{OL\text{spec}}) / I_{OL\text{spec}}$
4. $R(\text{PULL-UP-MAX}) = (V_{DDI\text{max}} - V_{OH\text{spec}}) / I_{OH\text{spec}}$

Table 130 • I2C CharacteristicsWorst-Case Industrial Conditions: $T_J = 100^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)

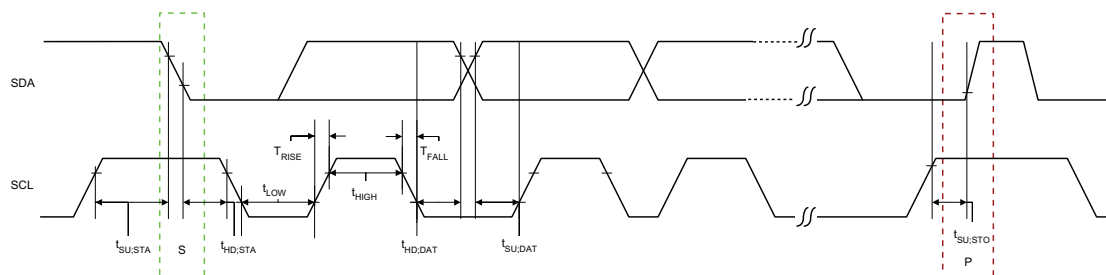
Parameter	Definition	Conditions	Min.	Typ.	Max.	Units	Notes
Rpull-down	Output buffer maximum pull-up resistance		–	–	131.25	Ohms	2, 4
Dmax	Maximum data rate	Fast mode	–	–	400	Kbps	
		Standard mode	–	–	100	Kbps	
t _{FILT}	Pulse width of spikes which must be suppressed by the input filter	Fast mode	–	50	–	ns	

Notes:

1. These values are provided for MSIO Bank - LVTTTL 8 mA Low Drive at 25°C , typical conditions. For Board Design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. These maximum values are provided for information only. Minimum output buffer resistance values depend on V_{DDIx} , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website: <http://www.microsemi.com/soc/download/ibis/default.aspx>.
3. $R(\text{PULL-DOWN-MAX}) = (V_{OLspec}) / I_{OLspec}$
4. $R(\text{PULL-UP-MAX}) = (V_{DDImax} - V_{OHspec}) / I_{OHspec}$

Table 131 • I2C Switching CharacteristicsWorst-Case Industrial Conditions: $T_J = 100^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$

Parameter	Definition	Conditions	–1		Std.		Units	Notes
			Min.	Max.	Min.	Max.		
t _{LOW}	Low period of I2C_x_SCL	–	1	–	1	–	pclk cycles	
t _{HIGH}	High period of I2C_x_SCL	–	1	–	1	–	pclk cycles	
t _{HD;STA}	START hold time	–	1	–	1	–	pclk cycles	
t _{SU;STA}	START setup time	–	1	–	1	–	pclk cycles	
t _{HD;DAT}	DATA hold time	–	1	–	1	–	pclk cycles	
t _{SU;DAT}	DATA setup time	–	1	–	1	–	pclk cycles	
t _{SU;STO}	STOP setup time	–	1	–	1	–	pclk cycles	

**Figure 16 • I²C Timing Parameter Definition**

18.2. Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to [Figure 17 on page 116](#).

Table 132 • SPI Characteristics

Worst-Case Industrial Conditions: $T_J = 100^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Symbol	Description	Conditions	All Devices/Speed Grades			Units	Notes
			Min	Type	Max		
sp1	SPI_[0 1]_CLK minimum period						
	SPI_[0 1]_CLK = PCLK/2		-	-	12	ns	
	SPI_[0 1]_CLK = PCLK/4		-	-	24.1	ns	
	SPI_[0 1]_CLK = PCLK/8		-	-	48.2	ns	
	SPI_[0 1]_CLK = PCLK/16		-	-	0.1	µs	
	SPI_[0 1]_CLK = PCLK/32		-	-	0.19	µs	
	SPI_[0 1]_CLK = PCLK/64		-	-	0.39	µs	
	SPI_[0 1]_CLK = PCLK/128		-	-	0.77	µs	
sp2	SPI_[0 1]_CLK minimum pulse width high						
	SPI_[0 1]_CLK = PCLK/2		-	-	6	ns	
	SPI_[0 1]_CLK = PCLK/4		-	-	12.05	ns	
	SPI_[0 1]_CLK = PCLK/8		-	-	24.1	ns	
	SPI_[0 1]_CLK = PCLK/16		-	-	0.05	µs	
	SPI_[0 1]_CLK = PCLK/32		-	-	0.095	µs	
	SPI_[0 1]_CLK = PCLK/64		-	-	0.195	µs	
	SPI_[0 1]_CLK = PCLK/128		-	-	0.385	µs	
sp3	SPI_[0 1]_CLK minimum pulse width low						
	SPI_[0 1]_CLK = PCLK/2		-	-	6	ns	
	SPI_[0 1]_CLK = PCLK/4		-	-	12.05	ns	
	SPI_[0 1]_CLK = PCLK/8		-	-	24.1	ns	
	SPI_[0 1]_CLK = PCLK/16		-	-	0.05	µs	
	SPI_[0 1]_CLK = PCLK/32		-	-	0.095	µs	
	SPI_[0 1]_CLK = PCLK/64		-	-	0.195	µs	
	SPI_[0 1]_CLK = PCLK/128		-	-	0.385	µs	
sp4	SPI_[0 1]_CLK, SPI_[0 1]_DO, SPI_[0 1]_SS rise time (10%-90%) 1	I/O Configuration: LVCMOS 2.5 V- 8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25°C	-	2.77	-	ns	1

Notes:

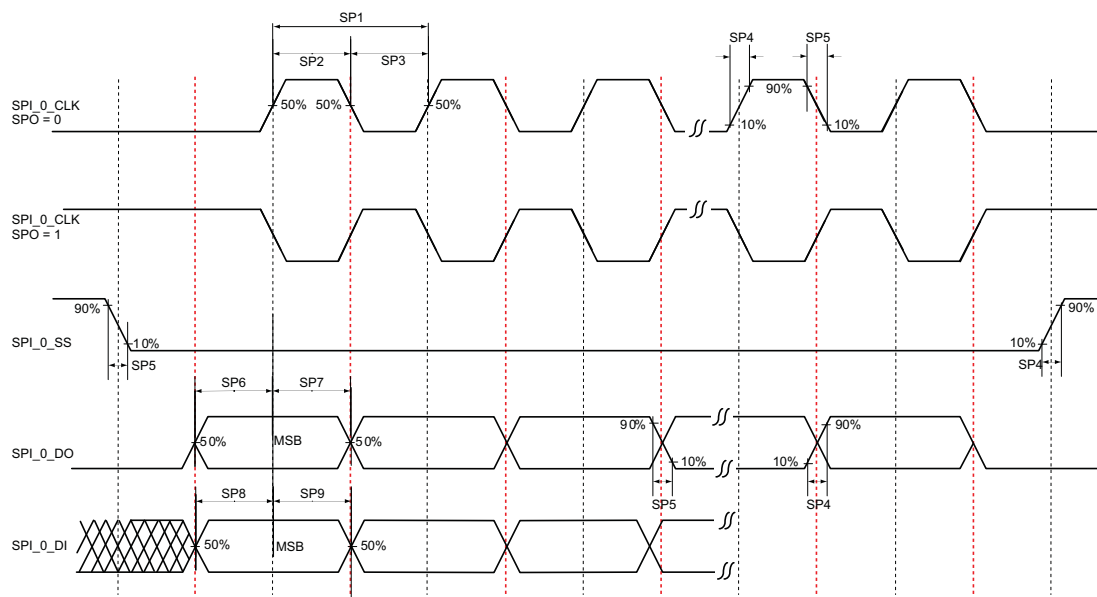
- For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website:
<http://www.microsemi.com/soc/download/ibis/default.aspx>.
- For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the [SmartFusion2 Microcontroller Subsystem User Guide](#).

Table 132 • SPI Characteristics**Worst-Case Industrial Conditions: $T_J = 100^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued) (continued)**

Symbol	Description	Conditions	All Devices/Speed Grades			Units	Notes
			Min	Type	Max		
sp5	SPI_[0]1_CLK, SPI_[0]1_DO, SPI_[0]1_SS fall time (10%-90%) 1	I/O Configuration: LVCMOS 2.5 V- 8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25°C	-	2.906	-	ns	1
sp6	Data from master (SPI_[0]1_DO) setup time		-	-	1	pclk cycles	2
sp7	Data from master (SPI_[0]1_DO) hold time		-	-	1	pclk cycles	2
sp8	SPI_[0]1_DI setup time		-	-	1	pclk cycles	2
sp9	SPI_[0]1_DI hold time		-	-	1	pclk cycles	2

Notes:

1. For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website:
<http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the [SmartFusion2 Microcontroller Subsystem User Guide](#).

**Figure 17 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**

19. IGLOO2 Specifications

19.1. IGLOO2 Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given are for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_0_CLK. For timing parameter definitions, refer to [Figure 18 on page 119](#).

Table 133 • SPI Characteristics

Worst-Case Industrial Conditions: $T_J = 100^{\circ}\text{C}$, $V_{DD} = 1.14\text{ V}$

Symbol	Description	Conditions	All Devices/Speed Grades			Units	Notes
			Min	Type	Max		
sp1	SPI_0_CLK minimum period						
	SPI_0_CLK = PCLK/2		-	-	12	ns	
	SPI_0_CLK = PCLK/4		-	-	24.1	ns	
	SPI_0_CLK = PCLK/8		-	-	48.2	ns	
	SPI_0_CLK = PCLK/16		-	-	0.1	μs	
	SPI_0_CLK = PCLK/32		-	-	0.19	μs	
	SPI_0_CLK = PCLK/64		-	-	0.39	μs	
	SPI_0_CLK = PCLK/128		-	-	0.77	μs	
sp2	SPI_0_CLK minimum pulse width high						
	SPI_0_CLK = PCLK/2		-	-	6	ns	
	SPI_0_CLK = PCLK/4		-	-	12.05	ns	
	SPI_0_CLK = PCLK/8		-	-	24.1	ns	
	SPI_0_CLK = PCLK/16		-	-	0.05	μs	
	SPI_0_CLK = PCLK/32		-	-	0.095	μs	
	SPI_0_CLK = PCLK/64		-	-	0.195	μs	
	SPI_0_CLK = PCLK/128		-	-	0.385	μs	
sp3	SPI_0_CLK minimum pulse width low						
	SPI_0_CLK = PCLK/2		-	-	6	ns	
	SPI_0_CLK = PCLK/4		-	-	12.05	ns	
	SPI_0_CLK = PCLK/8		-	-	24.1	ns	
	SPI_0_CLK = PCLK/16		-	-	0.05	μs	
	SPI_0_CLK = PCLK/32		-	-	0.095	μs	
	SPI_0_CLK = PCLK/64		-	-	0.195	μs	
	SPI_0_CLK = PCLK/128		-	-	0.385	μs	

Notes:

- For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website:
<http://www.microsemi.com/soc/download/ibis/default.aspx>.
- For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the *IGLOO2 FPGA High Performance Memory Subsystem User Guide*.

Table 133 • SPI Characteristics**Worst-Case Industrial Conditions: $T_J = 100^\circ\text{C}$, $V_{DD} = 1.14\text{ V}$ (continued)**

Symbol	Description	Conditions	All Devices/Speed Grades			Units	Notes
			Min	Type	Max		
sp4	SPI_0_CLK, SPI_0_DO, SPI_0_SS rise time (10%-90%) 1	I/O Configuration: LVCMOS 2.5 V- 8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25°C	-	2.77	-	ns	1
sp5	SPI_0_CLK, SPI_0_DO, SPI_0_SS fall time (10%-90%) 1	I/O Configuration: LVCMOS 2.5 V- 8 mA AC Loading: 35 pF Test Conditions: Typical Voltage, 25°C	-	2.906	-	ns	1
sp6	Data from master (SPI_0_DO) setup time		-	-	1	pclk cycles	2
sp7	Data from master (SPI_0_DO) hold time		-	-	1	pclk cycles	2
sp8	SPI_0_DI setup time		-	-	1	pclk cycles	2
sp9	SPI_0_DI hold time		-	-	1	pclk cycles	2

Notes:

1. For specific Rise/Fall Times, board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website:
<http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the *IGLOO2 FPGA High Performance Memory Subsystem User Guide*.

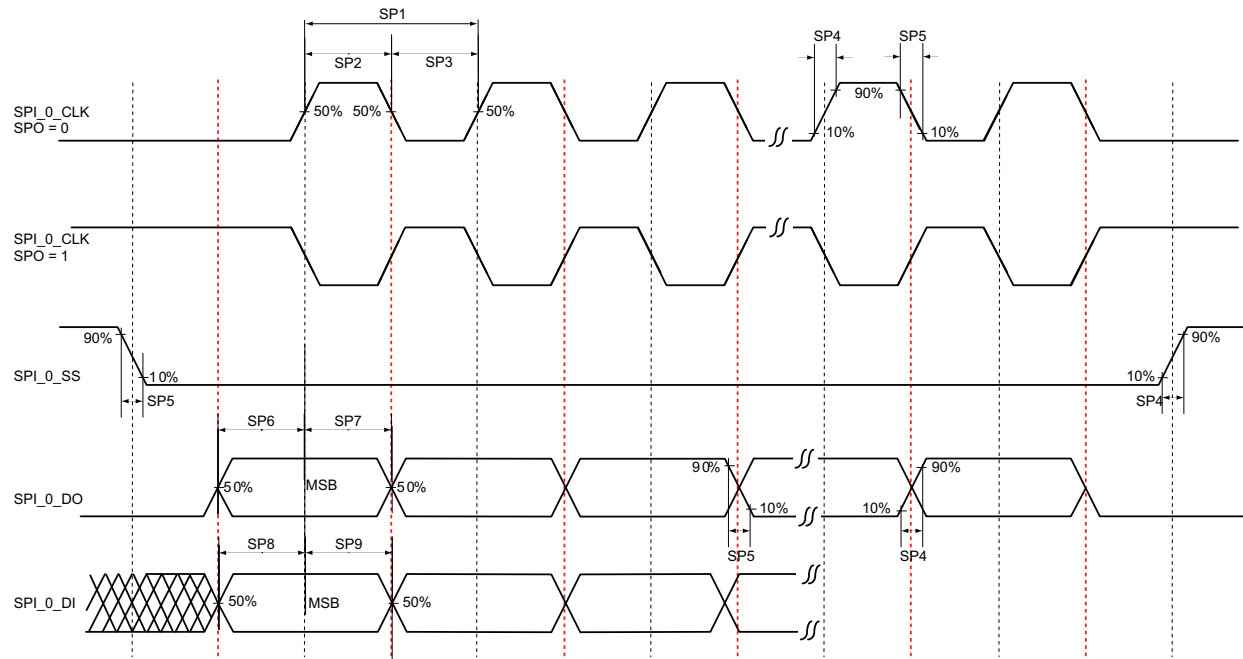


Figure 18 • SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)

Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the datasheet.

Revision	Changes	Page
Revision 1 (May 2014)	The IGLOO2 v2 and the SmartFusion2 v5 datasheets are combined into this single product family datasheet.	N/A

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in [Table 1 on page 10](#) is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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