OCTAL BUFFER/ LINE DRIVER WITH 3 STATE OUTPUTS

NEW PRODUCT

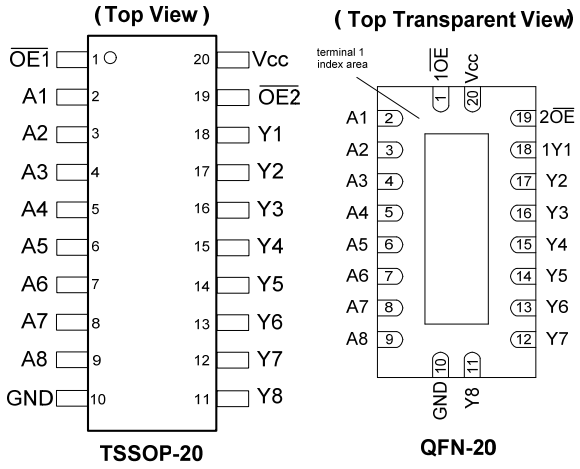
Description

The 74LVC540A is an octal inverting buffer/driver is designed for driving bus lines or buffer memory address registers. The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all eight outputs are in the high-impedance state..These devices feature inputs and outputs on opposite sides of the package that facilitate printed circuit board layout.

The device is designed for operation with a power supply range of 1.65V to 3.6V.

The inputs are tolerant to 5.5V allowing this device to be used in a mixed voltage environment. The device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output preventing damaging current backflow when the device is powered down.

Pin Assignments



Features

- Supply Voltage Range from 1.65V to 3.6V
- Sinks or Sources 24mA at V_{CC} = 3V
- CMOS Low Power Consumption
- I_{OFF} Supports Partial Power Down Operation
- Inputs or Outputs Accept Up to 5.5V
- Inputs Can Be Driven by 3.3V or 5V Allowing for Mixed Voltage Applications
- Schmitt Trigger Action at All Inputs
- Typical V_{OLP} (Quiet Output Ground Bounce) Less Than 0.8V with V_{CC} = 3.3V and T_A = +25°C
- Typical V_{OHV} (Quiet Output dynamic VOH) Greater than 2.0V with V_{CC} = 3.3V and T_A = +25°C
- ESD Protection Tested per JESD 22
  - Exceeds 200-V Machine Model (A115)
  - Exceeds 2000-V Human Body Model (A114)
  - Exceeds 1000-V Charged Device Model (C101)
- Latch-Up Exceeds 250mA per JESD 78, Class I
- All devices are:
  - **Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)**
  - **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

- General Purpose Logic
- Bus Driving
- Power Down Signal Isolation
- Wide array of products such as:
  - PCs, Notebooks, Netbooks, Ultrabooks
  - Networking Computer Peripherals, Hard Drives, CD/DVD ROM
  - TV, DVD, DVR, Set Top Box

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen and Antimony free, "Green" and Lead-Free.
3. Halogen and Antimony free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

NEW PRODUCT

Ordering Information

74 LVC 540A xxx -13

Logic Device	Function	Package	Packing
74 : Logic Prefix	540 : Octal Buffer/Line Driver with 3 State Outputs	T20 : TSSOP-20 Q20 : QFN-20	**-13 : 13" Tape & Reel**

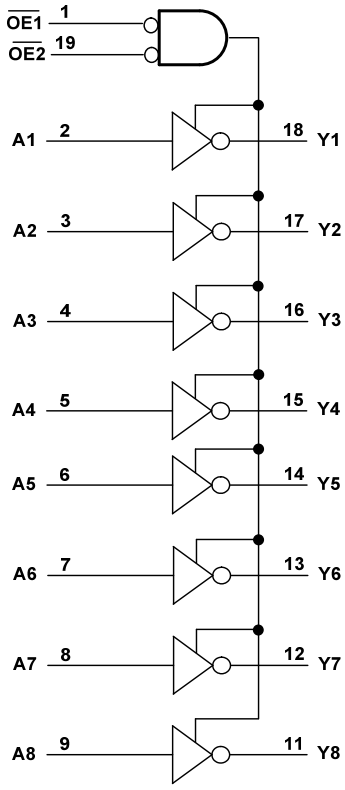
Part Number	Package Code	Package (Note 4 & 5)	Package Size	13" Tape and Reel	
				Quantity	Part Number Suffix
74LVC540AT20-13	T20	TSSOP-20	6.4mm X 6.5mm X 1.2mm 0.65 mm lead pitch	2500/Tape & Reel	-13
74LVC540AQ20-13	Q20	V-QFN4525-20	2.5mm X 4.5mm X 0.95mm 0.50 mm lead pitch	2500/Tape & Reel	-13

Notes: 4. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.
5. V-QFN4525-20 is a JEDEC recognized naming convention that specifies the package thickness category as V and the number 4525 describes the package as 4.5mm X 2.5mm.

Pin Descriptions

Pin Number	Pin Name	Description
1	$\overline{OE1}$	Output Enable 1
2	A1	Data Input
3	A2	Data Input
4	A3	Data Input
5	A4	Data Input
6	A5	Data Input
7	A6	Data Input
8	A7	Data Input
9	A8	Data Input
10	GND	Ground
11	B8	Data Output
12	B7	Data Output
13	B6	Data Output
14	B5	Data Output
15	B4	Data Output
16	B3	Data Output
17	B2	Data Output
18	B1	Data Output
19	$\overline{OE2}$	Output Enable 2
20	V_{CC}	Supply Voltage

Logic Diagram



Function Table

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Q
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

NEW PRODUCT

Absolute Maximum Ratings (Notes 6 & 7)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	kV
ESD CDM	Charged Device Model ESD Protection	1	kV
ESD MM	Machine Model ESD Protection	200	V
V_{CC}	Supply Voltage Range	-0.5 to +7.0	V
V_I	Input Voltage Range	-0.5 to +7.0	V
I_{IK}	Input Clamp Current V_I< 0V	-20	mA
I_{OK}	Output Clamp Current V_O< 0V	-50	mA
I_O	Continuous Output Current -0.5V < V_O V_{CC} +0.5V	±50	mA
I_{CC}	Continuous Current Through V_{CC}	100	mA
I_{GND}	Continuous Current Through GND	-100	mA
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_{TOT}	Total Power Dissipation	500	mW

Notes: 6. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.
7. Forcing the maximum allowed voltage could cause a condition exceeding the maximum current or conversely forcing the maximum current could cause a condition exceeding the maximum voltage. The ratings of both current and voltage must be maintained within the controlled range.

Recommended Operating Conditions (Note 8)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Operating	1.65	3.6	V
		Data Retention Only	1.5	—	V
V_I	Input Voltage	—	0	5.5	V
V_O	Output Voltage	—	0	V_{CC}	V
I_{OH}	High-Level Output Current	V_{CC} = 1.65V	—	-4	mA
		V_{CC} = 2.3V	—	-8	
		V_{CC} = 2.7V	—	-12	
		V_{CC} = 3.0V	—	-24	
I_{OL}	Low-Level Output Current	V_{CC} = 1.65V	—	4	mA
		V_{CC} = 2.3V	—	8	
		V_{CC} = 2.7V	—	12	
		V_{CC} = 3.0V	—	24	
Δt/ΔV	Input Transition Rise or Fall Rate		—	10	ns/V
T_A	Operating Free-Air Temperature		-40	+125	ºC

Note: 8. Unused inputs should be held at V_{CC} or ground.

NEW PRODUCT

Electrical Characteristics

Symbol	Parameter	Test Conditions	V_{CC}	T_A = -40°C to +85°C		T_A = +85°C to +125°C		Unit
				Min	Max	Min	Max	
V_{IH}	High-Level Input Voltage		1.65V to 1.95V	V_{CC} X 0.65	—	V_{CC} X 0.65	—	V
			2.3V to 2.7V	1.7	—	1.7	—	
			3.0V to 3.6V	2	—	2	—	
V_{IL}	Low-Level Input voltage		1.65V to 1.95V	—	V_{CC} X 0.35	—	V_{CC} X 0.35	V
			2.3V to 2.7V	—	0.7	—	0.7	
			3.0V to 3.6V	—	0.8	—	0.8	
V_{OH}	High-Level Output Voltage	I_{OH} = -50µA	1.65V to 3.6V	V_{CC} -0.2	—	V_{CC} -0.3	—	
		I_{OH} = -4mA	1.65V	1.2	—	1.05	—	
		I_{OH} = -8mA	2.3V	1.7	—	1.65	—	V
		I_{OH} = -12mA	2.7V	2.2	—	2.05	—	
			3.0V	2.4	—	2.48	—	
		I_{OH} = -24mA	3.0V	2.3	—	2.0	—	
V_{OL}	Low-Level Output Voltage	I_{OL} = 100µA	1.65V to 3.6V	—	0.2	—	0.3	V
		I_{OL} = 4mA	1.65V	—	0.45	—	0.65	
		I_{OL} = 8mA	2.3V	—	0.60	—	0.80	
		I_{OL} = 12mA	2.7V	—	0.40	—	0.60	
		I_{OL} = 24mA	3.0V	—	0.55	—	0.80	
I_{OFF}	Power Down Leakage Current	V_I or V_O = 0 or 5.5V	0V	—	±10	—	±20	µA
I_I	Input Current Control Pins	V_I =GND or 5.5V	0 to 3.6V	—	±5	—	±20	µA
I_{OZ}	Z-state Current Including Input Current I/O Pins	V_I =GND or 5.5V V_O = 0 to 5.5V	3.6V	—	±5	—	±20	µA
I_{CC}	Supply Current	V_I = GND or V_{CC}, I_O = 0	3.6V	—	10	—	40	µA
ΔI_{CC}	Additional Supply Current	One input at V_{CC} -0.6V Io = 0A	2.7V to 3.6V	—	500	—	5000	µA
C_i	Input Capacitance	Control Pins, V_I = GND or V_{CC}	0V to 3.6V	4.0 typical		4.0 typical		pF
		I/O Pins, V_I = GND or V_{CC}		5.5 typical		5.5 typical		

Switching Characteristics

Symbol	Parameter	Test Conditions	V_{CC}	T_A = +25°C			-40°C to +85°C		+85°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PD}	Propagation Delay A_N to Y_N	Figure 1	1.8V ± 0.15V	1	6.0	12.2	1	16.4	1	17.9	ns
			2.5V ± 0.3V	1	3.9	7.6	1	8.6	1	9.7	
			2.7V	1	4.2	7.2	1	7.8	1	8.9	
			3.3V ± 0.3V	1.5	3.8	6.5	1.5	6.9	1.5	7.8	
t_{EN}	Enable Time $\overline{OE}$ to Y_N	Figure 1	1.8V ± 0.15V	1	7	14.8	1	16.5	1	18.5	ns
			2.5V ± 0.3V	1	4.5	10	1	10.5	1	12.4	
			2.7V	1	5.4	8.3	1	9.0	1	11.5	
			3.3V ± 0.3V	1.5	4.4	6.4	1.5	6.6	1.5	8.0	
t_{DIS}	Disable Time $\overline{OE}$ to Y_N	Figure 1	1.8V ± 0.15V	1	7.8	15.5	1	16.4	1	18.2	ns
			2.5 V ± 0.3V	1	5	8.7	1	9.0	1	9.6	
			2.7V	1	4.4	8.0	1	8.2	1	10.0	
			3.3V ± 0.3V	1.7	4.1	7.1	1.7	7.4	1.7	9.0	
$t_{sk(0)}$	Output Skew Time		3.3V ± 0.3V			1.0				1.5	ns

NEW PRODUCT

Operating Characteristics

T_A = +25°C

Symbol	Parameter	Test Conditions	V_{CC}	Typ	Unit
C_{pd}	Power dissipation capacitance per gate	F= 10 MHz Outputs Enabled	1.8V ± 0.15V	9.9	pF
			2.5V ± 0.3V	10.2	
			3.3V ± 0.3V	10.6	

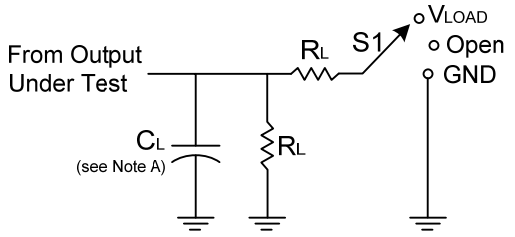
Package Characteristics

Symbol	Parameter	Package	Test Conditions	Min	Typ	Max	Unit
θ_{JA}	Thermal Resistance Junction-to-Ambient	TSSOP-20	(Note 9)	—	74	—	°C/W
θ_{JC}	Thermal Resistance Junction-to-Case	TSSOP-20	(Note 9)	—	15	—	°C/W
θ_{JA}	Thermal Resistance Junction-to-Ambient	V-QFN4525-20	(Note 9)	—	67	—	°C/W
θ_{JC}	Thermal Resistance Junction-to-Case	V-QFN4525-20	(Note 9)	—	20	—	°C/W

Note: 9. Test conditions for TSSOP-20 and V-QFN4525-20: Devices mounted on 4 layer FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout per JESD 51-7.

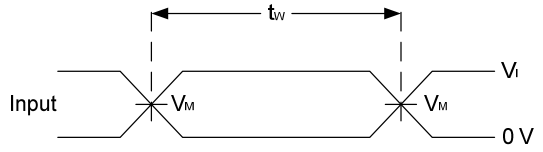
NEW PRODUCT

Parameter Measurement Information

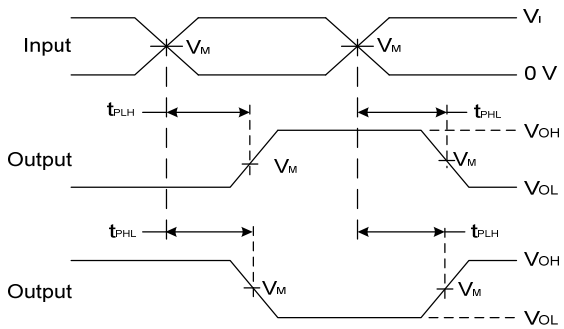


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	Vload
t_{PHZ}/t_{PZH}	GND

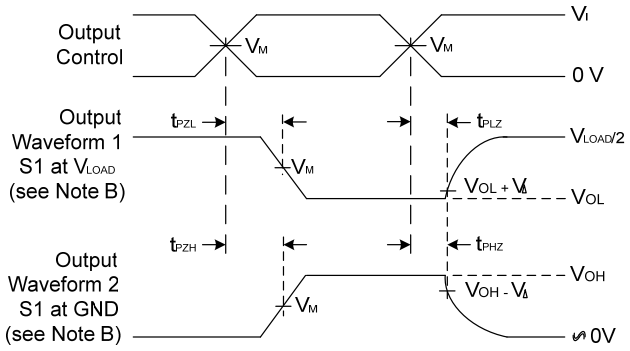
V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	$V\Delta$
	V_I	t_r/t_f					
1.8V ± 0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	30pF	1KΩ	0.15V
2.5V ± 0.2V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	30pF	500Ω	0.15V
2.7V	2.7V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
3.3V ± 0.3V	2.7V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V



Voltage Waveform Pulse Duration



Voltage Waveform Propagation Delay Times
Inverting and Non Inverting Outputs



Voltage Waveform Enable and Disable Times
Low and High Level Enabling

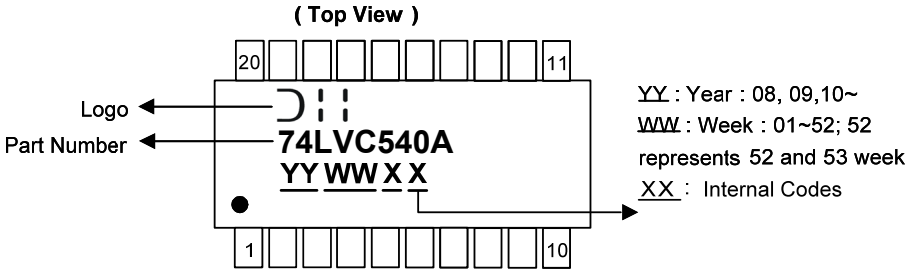
Notes:
A. Includes test lead and test apparatus capacitance.
B. All pulses are supplied at pulse repetition rate ≤ 10 MHz.
C. Inputs are measured separately one transition per measurement.
D. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
E. t_{PZL} and t_{PZH} are the same as t_{EN0}
F. t_{PLH} and t_{PHL} are the same as t_{PD}.

Figure 1 Load Circuit and Voltage Waveforms

NEW PRODUCT

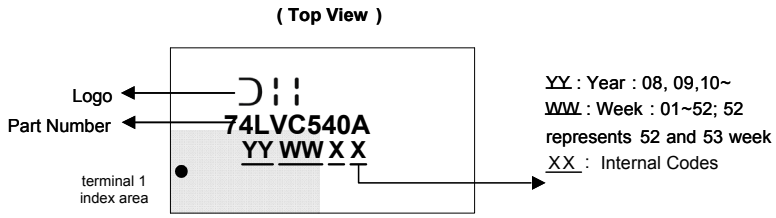
Marking Information

(1) TSSOP20



Part Number	Package
74LVC540AT20	TSSOP-20

(2) QFN-20 (V-QFN4525-20)



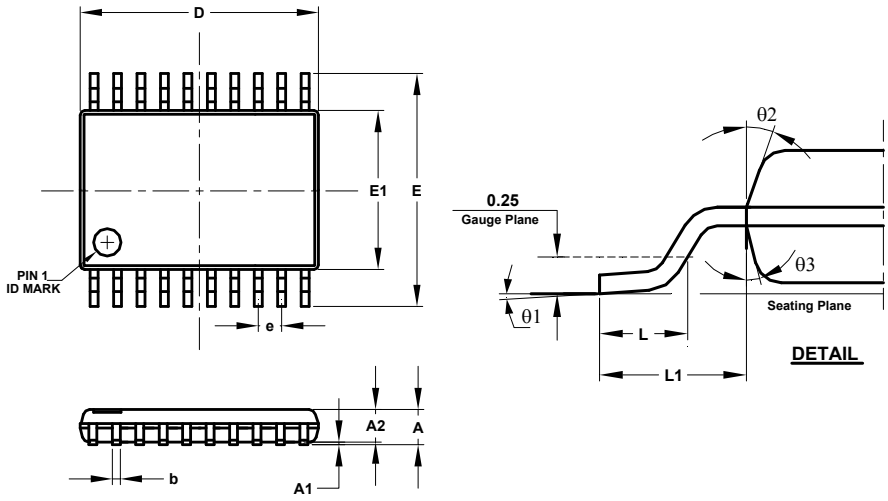
Part Number	Package
74LVC540AQ20	V-QFN4525-20

NEW PRODUCT

Package Outline Dimensions (All Dimensions in mm)

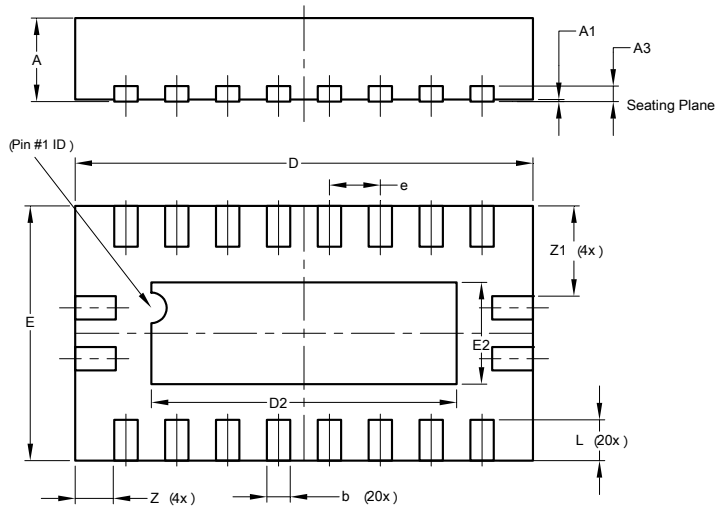
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.

(1) TSSOP-20



TSSOP-20			
Dim	Min	Max	Typ
A	-	1.20	-
A1	0.05	0.15	-
A2	0.80	1.05	-
b	0.19	0.30	-
c	0.09	0.20	-
D	6.40	6.60	6.50
E	6.20	6.60	6.40
E1	4.30	4.50	4.40
e	0.65 BSC		
L	0.45	0.75	0.60
L1	1.0 REF		
θ1	0°	8°	-
θ2	10°	14°	12°
θ3	10°	14°	12°
All Dimensions in mm			

(2) QFN-20 (V-QFN4525-20)



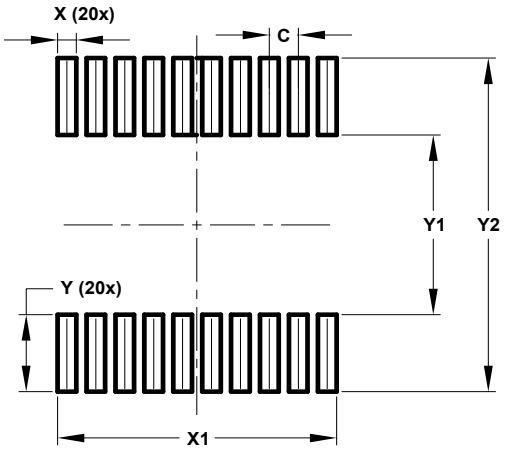
V-QFN4525-20			
Dim	Min	Max	Typ
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	-	-	0.15
b	0.18	0.30	0.23
D	4.45	4.55	4.50
D2	2.85	3.15	3.00
E	2.45	2.55	2.50
E2	0.85	1.15	1.00
e	0.50BSC		
L	0.30	0.50	0.40
Z	-	-	0.385
Z1	-	-	0.885
All Dimensions in mm			

NEW PRODUCT

Suggested Pad Layout

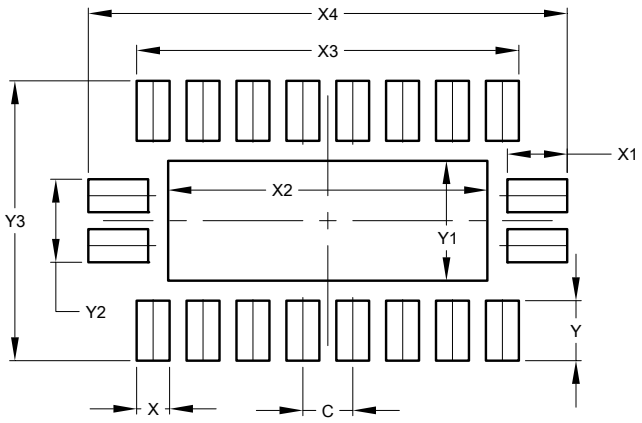
Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.

(1) TSSOP-20



Dimensions	Value (in mm)
C	0.650
X	0.420
X1	6.270
Y	1.789
Y1	4.160
Y2	7.720

(2) QFN-20 (V-QFN4525-20)



Dimensions	Value (in mm)
C	0.500
X	0.330
X1	0.600
X2	3.200
X3	3.830
X4	4.800
Y	0.600
Y1	1.200
Y2	0.830
Y3	2.800

NEW PRODUCT

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