512Kx8 Monolithic SRAM, SMD 5962-95600

FEATURES

- Access Times of 15, 17, 20, 25, 35, 45, 55ns
- Data Retention Function (LPA version)
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks
- Organized as 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 32 lead JEDEC Approved Evolutionary Pinout
  - Ceramic Sidebrazed 600 mil DIP (Package 9)
  - Ceramic Sidebrazed 400 mil DIP (Package 326)
  - Ceramic 32 pin Flatpack (Package 344)
  - Ceramic Thin Flatpack (Package 321)
  - Ceramic SOJ (Package 140)
- 36 lead JEDEC Approved Revolutionary Pinout
  - Ceramic Flatpack (Package 316)
  - Ceramic SOJ (Package 327)
  - Ceramic LCC (Package 502)
- Single +5V (±10%) Supply Operation

The EDI88512CA is a 4 megabit Monolithic CMOS Static RAM.

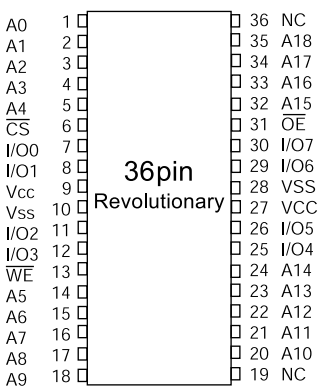
The 32 pin DIP pinout adheres to the JEDEC evolutionary standard for the four megabit device. All 32 pin packages are pin for pin upgrades for the single chip enable 128K x 8, the EDI88128CS. Pins 1 and 30 become the higher order addresses.

The 36 pin revolutionary pinout also adheres to the JEDEC standard for the four megabit device. The center pin power and ground pins help to reduce noise in high performance systems. The 36 pin pinout also allows the user an upgrade path to the future 2Mx8.

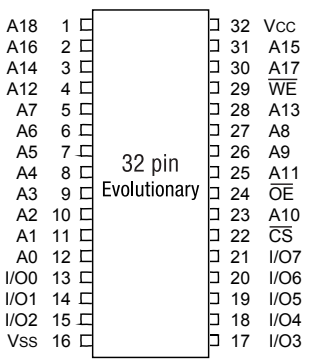
A Low Power version with Data Retention (EDI88512LPA) is also available for battery backed applications. Military product is available compliant to Appendix A of MIL-PRF-38535.

FIG. 1 PIN CONFIGURATION

36 PIN TOP VIEW



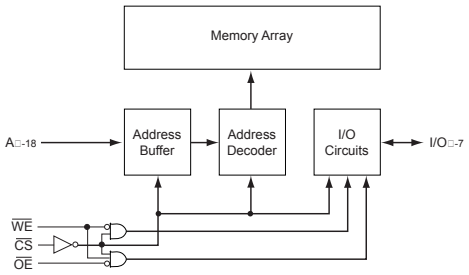
32 PIN TOP VIEW



PIN DESCRIPTION

I/O0-7	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{WE}$	Write Enables
$\overline{CS}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power (+5V ±10%)
Vss	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on any pin relative to Vss	-0.5 to 7.0	V
Operating Temperature T_A (Ambient)		
Commercial	0 to +70	°C
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Plastic	-65 to +150	°C
Power Dissipation	1.5	W
Output Current	20	mA
Junction Temperature, T_J	175	°C

NOTE:
Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

$\overline{OE}$	$\overline{CS}$	$\overline{WE}$	Mode	Output	Power
X	H	X	Standby	High Z	I_{CC2}, I_{CC3}
H	L	H	Output Deselect	High Z	I_{CC1}
L	L	H	Read	Data Out	I_{CC1}
X	L	L	Write	Data In	I_{CC1}

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	3.0	V
Input Low Voltage	V_{IL}	-0.3	—	+0.8	V

CAPACITANCE
(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Address Lines	C_I	V_{IN} = Vcc or Vss, f = 1.0MHz	12	pF
Data Lines	C_O	V_{OUT} = Vcc or Vss, f = 1.0MHz	14	pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS
(V_{CC} = 5V, T_A = -55°C TO +125°C)

Parameter	Symbol	Conditions		Min	Max	Units
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}		-10	10	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = 0V to V_{CC}		-10	10	µA
Operating Power Supply Current	I_{CC1}	$\overline{WE}$, $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA, Min Cycle	(17ns)	—	250	mA
			(20 -55ns)	—	225	mA
Standby (TTL) Power Supply Current	I_{CC2}	$\overline{CS}$ ≥ V_{IH}, V_{IN} ≤ V_{IL}, V_{IN} ≥ V_{IH}		—	60	mA
Full Standby Power Supply Current	I_{CC3}	$\overline{CS}$ ≥ V_{CC} -0.2V	CA	—	25	mA
		V_{IN} ≥ Vcc -0.2V or V_{IN} ≤ 0.2V	LPA	—	20	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0mA		—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	—	V

NOTE: DC test conditions: V_{IL} = 0.3V, V_{IH} = Vcc -0.3V

AC TEST CONDITIONS

Figure 1

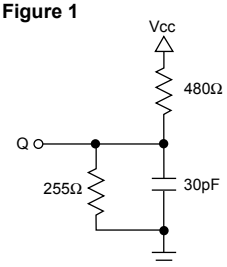
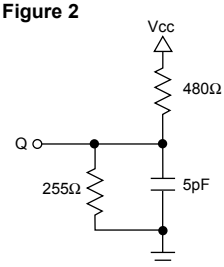


Figure 2



Input Pulse Levels	Vss to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, CL = 5pF Figure 2)

AC CHARACTERISTICS – READ CYCLE
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol JEDEC	Symbol Alt.	15ns Min	15ns Max	17ns Min	17ns Max	20ns Min	20ns Max	25ns Min	25ns Max	35ns Min	35ns Max	45ns Min	45ns Max	55ns Min	55ns Max	Units
Read Cycle Time	t_{AVAV}	t_{RC}	15		17		20		25		35		45		55		ns
Address Access Time	t_{AVQV}	t_{AA}		15		17		20		25		35		45		55	ns
Chip Enable Access Time	t_{ELQV}	t_{ACS}		15		17		20		25		35		45		55	ns
Chip Enable to Output in Low Z (1)	t_{ELQX}	t_{CLZ}	2		3		3		3		3		3		3		ns
Chip Disable to Output in High Z (1)	t_{EHQZ}	t_{CHZ}	0	7	0	7	0	8	0	10	0	15	0	20	0	20	ns
Output Hold from Address Change	t_{AVQX}	t_{OH}	0		0		0		0		0		0		0		ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		8		8		10		12		15		25		30	ns
Output Enable to Output in Low Z (1)	t_{GLQX}	t_{OLZ}	0		0		0		0		0		0		0		ns
Output Disable to Output in High Z(1)	t_{GHQZ}	t_{OHZ}	0	7	0	7	0	8	0	10	0	15	0	20	0	20	ns

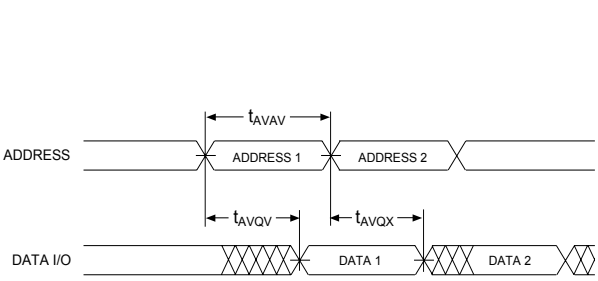
1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – WRITE CYCLE
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO +125°C)

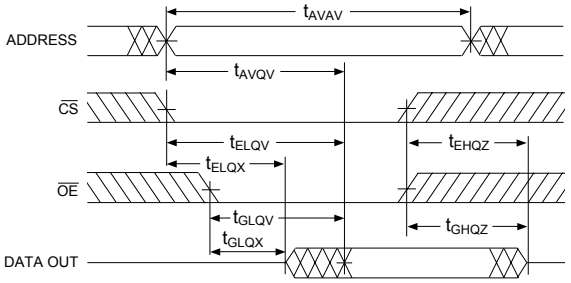
Parameter	Symbol JEDEC	Symbol Alt.	15ns Min	15ns Max	17ns Min	17ns Max	20ns Min	20ns Max	25ns Min	25ns Max	35ns Min	35ns Max	45ns Min	45ns Max	55ns Min	55ns Max	Units
Write Cycle Time	t_{AVAV}	t_{WC}	15		17		20		25		35		45		55		ns
Chip Enable to End of Write	t_{ELWH}	t_{CW}	13		14		15		17		25		30		50		ns
	t_{ELEH}	t_{CW}	13		14		15		17		25		30		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		0		0		0		0		ns
	t_{AVEL}	t_{AS}	0		0		0		0		0		0		0		ns
Address Valid to End of Write	t_{AVWH}	t_{AW}	13		14		15		17		25		30		50		ns
	t_{AVEH}	t_{AW}	13		14		15		17		25		30		50		ns
Write Pulse Width	t_{WLWH}	t_{WP}	13		14		15		17		25		30		45		ns
	t_{WLEH}	t_{WP}	13		14		15		17		25		30		45		ns
Write Recovery Time	t_{WHAX}	t_{WR}	0		0		0		0		0		0		0		ns
	t_{EHAX}	t_{WR}	0		0		0		0		0		0		0		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		0		0		0		0		ns
	t_{EHDX}	t_{DH}	0		0		0		0		0		0		0		ns
Write to Output in High Z (1)	t_{WLQZ}	t_{WHZ}	0	8	0	8	0	8	0	10	0	25	0	30	0	30	ns
Data to Write Time	t_{DVWH}	t_{DW}	8		8		10		12		20		25		40		ns
	t_{DVEH}	t_{DW}	8		8		10		12		20		25		30		ns
Output Active from End of Write (1)	t_{WHQX}	t_{WLZ}	0		0		0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 2 TIMING WAVEFORM - READ CYCLE

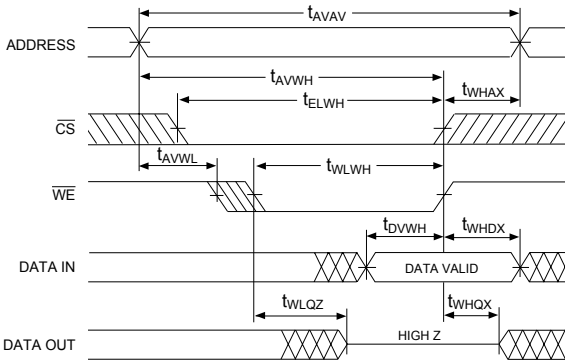


READ CYCLE 1 ($\overline{WE}$ HIGH; $\overline{OE}$, $\overline{CS}$ LOW)



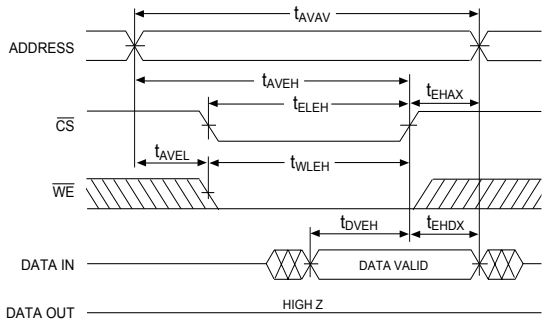
READ CYCLE 2 ($\overline{WE}$ HIGH)

FIG. 3 WRITE CYCLE - $\overline{WE}$ CONTROLLED



WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

FIG. 4 WRITE CYCLE - $\overline{CS}$ CONTROLLED

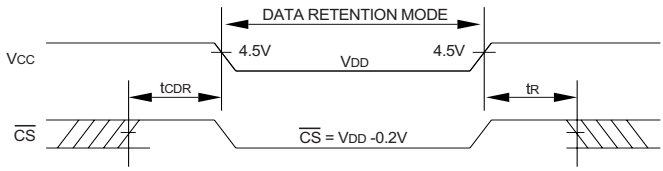


WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

DATA RETENTION CHARACTERISTICS (EDI88512LPA ONLY)
(T_A = -55°C TO +125°C)

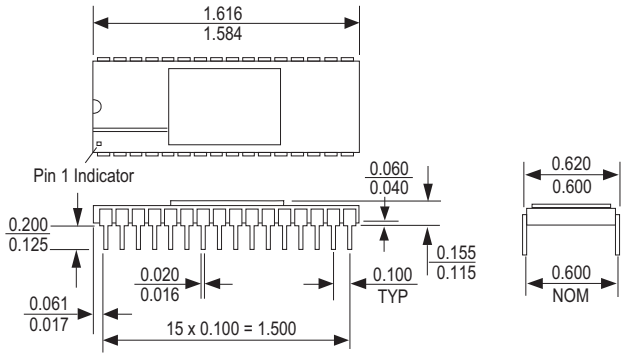
Characteristic Low Power Version only	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V_{DD}	V_{DD} = 2.0V	2	–	–	V
Data Retention Quiescent Current	I_{CCDR}	$\overline{CS} \geq V_{DD}$ -0.2V	–	–	2	mA
Chip Disable to Data Retention Time	T_{CDR}	$V_{IN} \geq V_{DD}$ -0.2V	0	–	–	ns
Operation Recovery Time	T_R	or $V_{IN} \leq$ 0.2V	T_{AVAV}	–	–	ns

FIG. 5 DATA RETENTION - $\overline{CS}$ CONTROLLED



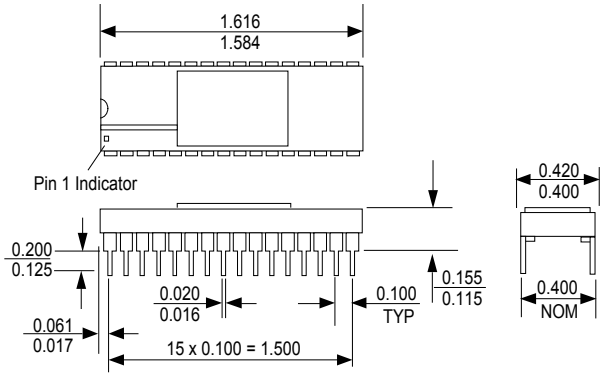
DATA RETENTION, $\overline{CS}$ CONTROLLED

PACKAGE 9: 32 LEAD SIDEBRAZED CERAMIC DIP, SMD 5962-95600XXMXA



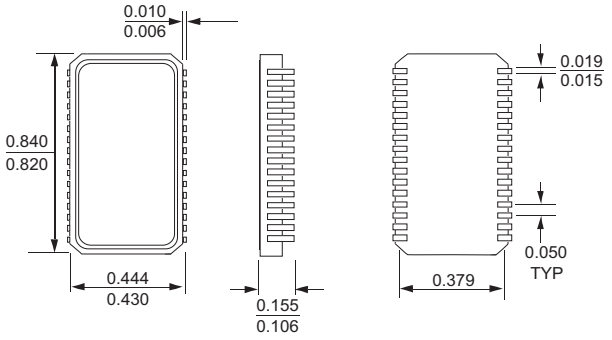
ALL DIMENSIONS ARE IN INCHES

PACKAGE 326: 32 LEAD SIDEBRAZED CERAMIC DIP



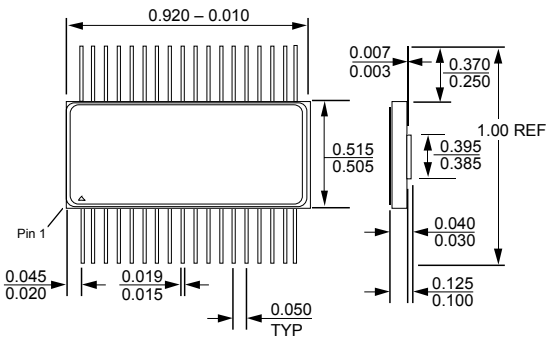
ALL DIMENSIONS ARE IN INCHES

PACKAGE 140: 32 LEAD CERAMIC SOJ, SMD 5962-95600XXMUA



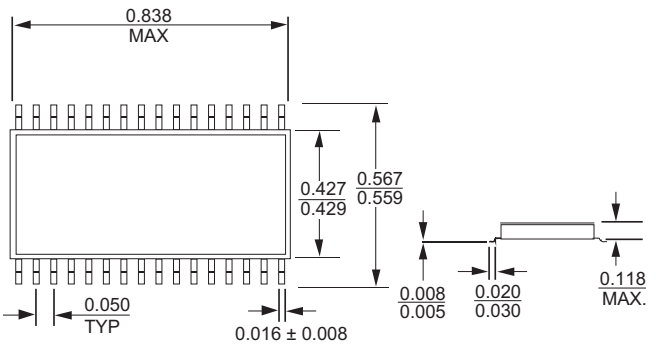
ALL DIMENSIONS ARE IN INCHES

PACKAGE 316: 36 PIN CERAMIC FLATPACK, SMD 5962-95600XXMTA



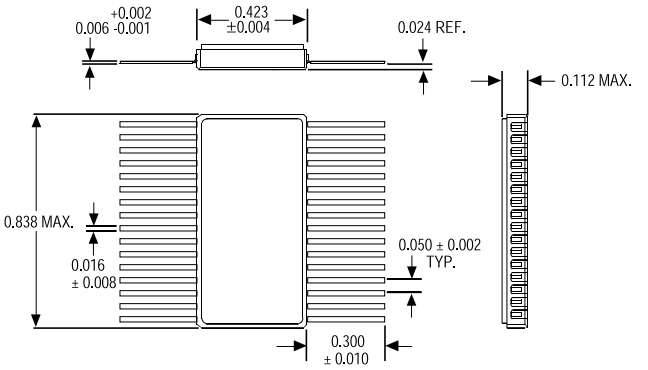
ALL DIMENSIONS ARE IN INCHES

PACKAGE 321: 32 PIN THINPACK™ FLATPACK, SMD 5962-95600XXMYA



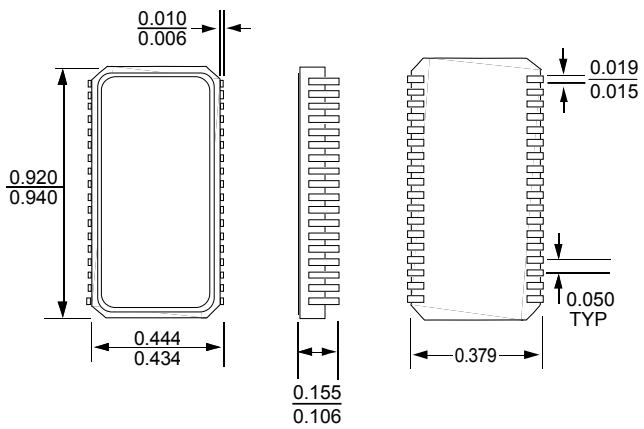
ALL DIMENSIONS ARE IN INCHES

PACKAGE 344: 32 PIN CERAMIC FLATPACK, SMD 5962-95600XXM9A



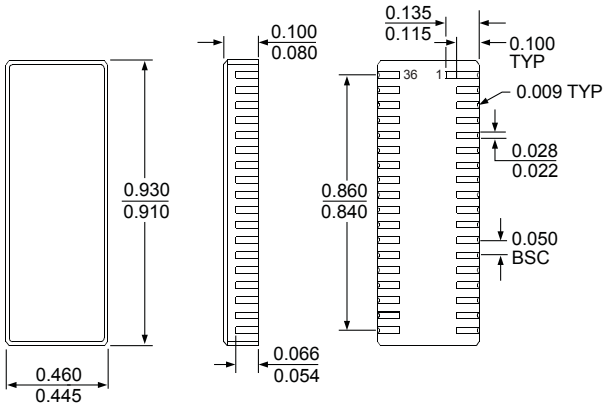
ALL DIMENSIONS ARE IN INCHES

PACKAGE 327: 36 LEAD CERAMIC SOJ, SMD 5962-95600XXMMA



ALL DIMENSIONS ARE IN INCHES

PACKAGE 502: 36 LEAD CERAMIC LCC, SMD 5962-95600XXMNA *(Pending)*



ALL DIMENSIONS ARE IN INCHES

ORDERING INFORMATION

EDI 8 8 512 CA X X X

WHITE ELECTRONIC DESIGNS

SRAM

ORGANIZATION, 512Kx8

TECHNOLOGY:
- CA = CMOS Standard Power
- LPA = Low Power

ACCESS TIME (ns)

PACKAGE TYPE:
- C = 32 lead Sidebrazed DIP, 600 mil (Package 9)
- K = 36 lead Ceramic LCC (Package 502)
- N = 32 lead Ceramic SOJ (Package 140)
- T = 32 lead Sidebrazed DIP, 400 mil (Package 326)
- B32 = 32 pin Ceramic Thinpack™ Flatpack (Package 321)
- F32 = 32 pin Ceramic Flatpack (Package 344)
- F36 = 36 pin Ceramic Flatpack (Package 316)
- N36 = 36 lead Ceramic SOJ (Package 327)

DEVICE GRADE:

B = MIL-STD-883 Compliant	
M = Military Screened	-55°C to +125°C
I = Industrial	-40°C to +85°C
C = Commercial	0°C to +70°C