

Octal inverting buffer (3-State)

74ABT240

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +64mA/–32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Power-up 3-State
- Live insertion/extraction permitted

DESCRIPTION

The 74ABT240 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT240 device is an octal inverting buffer that is ideal for driving bus lines. The device features two Output Enables (1OE, 2OE), each controlling four of the 3-State outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T _{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t _{PLH} t _{PHL}	Propagation delay nAx to nYx	C _L = 50pF; V _{CC} = 5V	3.1	ns
C _{IN}	Input capacitance	V _I = 0V or V _{CC}	4	pF
C _{OUT}	Output capacitance	Outputs disabled; V _O = 0V or V _{CC}	7	pF
I _{CCZ}	Total supply current	Outputs disabled; V _{CC} =5.5V	50	μA

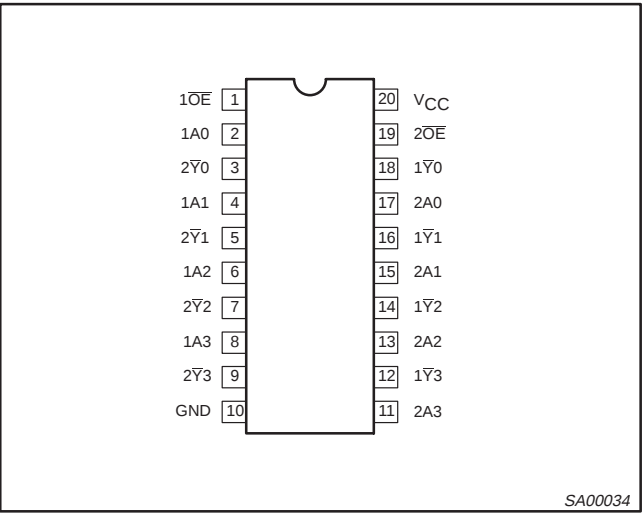
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	–40°C to +85°C	74ABT240 N	74ABT240 N	SOT146-1
20-Pin plastic SO	–40°C to +85°C	74ABT240 D	74ABT240 D	SOT163-1
20-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT240 DB	74ABT240 DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT240 PW	74ABT240PW DH	SOT360-1

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11, 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	1Y0 – 1Y3	Data outputs
9, 7, 5, 3	2Y0 – 2Y3	Data outputs
1, 19	1OE, 2OE	Output enables
10	GND	Ground (0V)
20	V _{CC}	Positive supply voltage

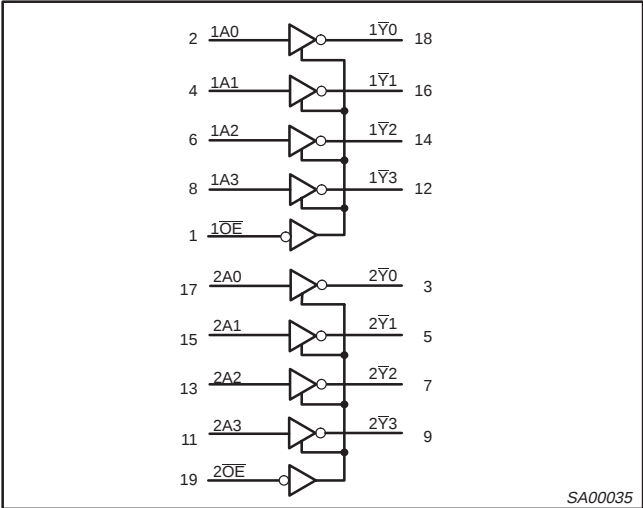
PIN CONFIGURATION



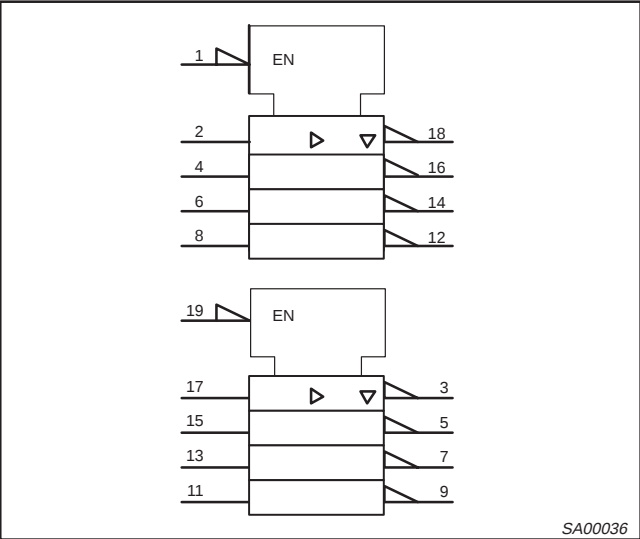
Octal inverting buffer (3-State)

74ABT240

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS				OUTPUTS	
1OE	1An	2OE	2An	1Yn	2Yn
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		−0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	−18	mA
V _I	DC input voltage ³		−1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	−50	mA
V _{OUT}	DC output voltage ³	output in Off or High state	−0.5 to +5.5	V
I _{OUT}	DC output current	output in Low state	128	mA
T _{stg}	Storage temperature range		−65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal inverting buffer (3-State)

74ABT240

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		-32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C			T _{amb} = −40°C to +85°C		
			Min	Typ	Max	Min	Max	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = −18mA		−0.9	−1.2		−1.2	V
V _{OH}	High-level output voltage	V _{CC} = 4.5V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V
		V _{CC} = 5.0V; I _{OH} = −3mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		V
		V _{CC} = 4.5V; I _{OH} = −32mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}		0.42	0.55		0.55	V
I _I	Input leakage current	V _{CC} = 5.5V; V _I = GND or 5.5V		±0.01	±1.0		±1.0	μA
I _{OFF}	Power-off leakage current	V _{CC} = 0.0V; V _I or V _O ≤ 4.5V;		±5.0	±100		±100	μA
I _{PU} /I _{PD}	Power-up/down 3-state output current ³	V _{CC} = 2.1V; V _O = 0.5V; V _I = GND or V _{CC} ; V _{OE} = Don't care		±5.0	±50		±50	μA
I _{OZH}	3-State output High current	V _{CC} = 5.5V; V _O = 2.7V; V _I = V _{IL} or V _{IH}		5.0	50		50	μA
I _{OZL}	3-State output Low current	V _{CC} = 5.5V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		−5.0	−50		−50	μA
I _{CEX}	Output High leakage current	V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}		5.0	50		50	μA
I _O	Output current ¹	V _{CC} = 5.5V; V _O = 2.5V	−50	−100	−180	−50	−180	mA
I _{CCH}	Quiescent supply current	V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		50	250		250	μA
I _{CCL}		V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}		24	30		30	mA
I _{CCZ}		V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}		50	250		250	μA
ΔI _{CC}	Additional supply current per input pin ²	Outputs 3-State, one input at 3.4V, other inputs at V _{CC} or GND; V _{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- This parameter is valid for any V_{CC} between 0V and 2.1V, with a transition time of up to 10msec. From $V_{CC} = 2.1\text{V}$ to $V_{CC} 5\text{V} \pm 10\%$ a transition time of up to 100 μsec is permitted.

Octal inverting buffer (3-State)

74ABT240

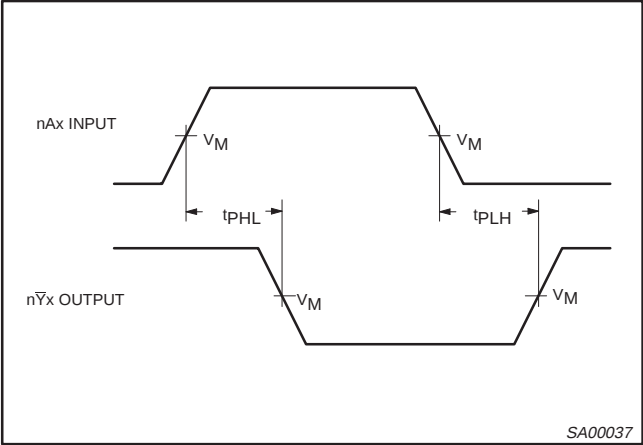
AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$, $R_L = 500\Omega$

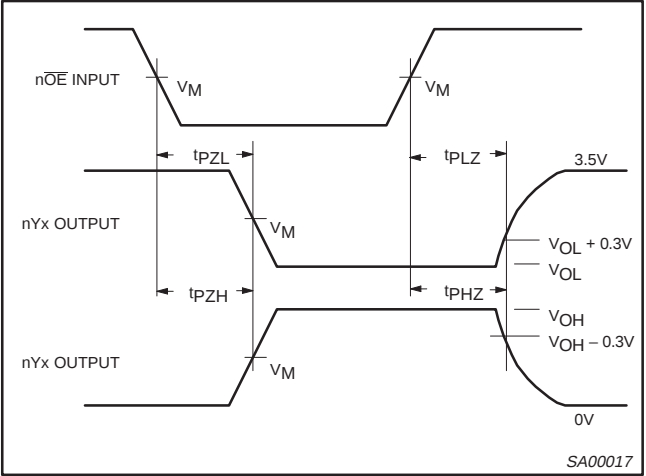
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = −40°C to +85°C V _{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay nAx to nYx	1	1.0 1.6	2.7 3.5	4.1 4.3	1.0 1.6	4.8 4.8	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.1 1.1	3.1 4.2	4.7 5.8	1.1 1.1	5.2 6.2	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	2	1.8 1.6	3.7 3.0	5.7 5.4	1.8 1.6	6.4 5.8	ns

AC WAVEFORMS

$V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



Waveform 1. Waveforms Showing the Input ($n\text{Ax}$) to Output ($n\bar{\text{Y}}\text{x}$) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

Octal inverting buffer (3-State)

74ABT240

TEST CIRCUIT AND WAVEFORMS

