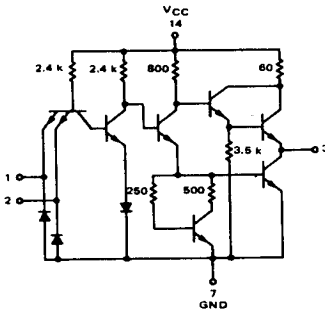


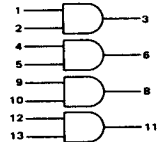
QUAD 2-INPUT "AND" GATE

MC3101F • MC3001F
MC3101L • MC3001L,P

1/4 OF CIRCUIT SHOWN



This device consists of four 2-input AND gates. This non-inverting function is useful for optimizing logic design, or for direct implementation of standard logic equations.

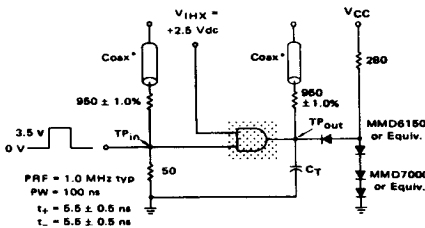


Positive Logic: $3 = 1 \cdot 2$
Negative Logic: $3 = 1 + 2$

Input Loading Factor = 1
Output Loading Factor = 10

Total Power Dissipation = 112 mW typ/pkg
Propagation Delay Time = 9.0 ns typ

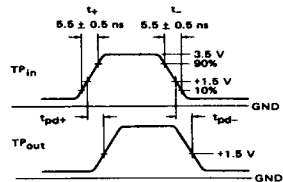
SWITCHING TIME TEST CIRCUIT



*The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50 ohm impedance. The 950 ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

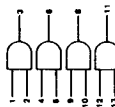
$C_T = 25 \text{ pF}$ = total parasitic capacitance, which includes probe, wiring, and load capacitances.

VOLTAGE WAVEFORMS AND DEFINITIONS



See General Information section for packaging.

Test procedures are shown for only one gate. The other gates are tested in the same manner. Further, test procedures are shown for only one input of the gate under test. To complete testing, sequence through remaining inputs.

[illegible]

Since this is a non-inverting gate, power drain is minimized by tying the inputs to gates not under test to V_{RH} .