

High Voltage Power Operational Amplifiers

FEATURES

- ◆ HIGH VOLTAGE — 400V ($\pm 200V$)
- ◆ LOW QUIESCENT CURRENT — 10mA
- ◆ HIGH OUTPUT CURRENT — 200mA
- ◆ PROGRAMMABLE CURRENT LIMIT
- ◆ HIGH SLEW RATE — 300V/ μ s

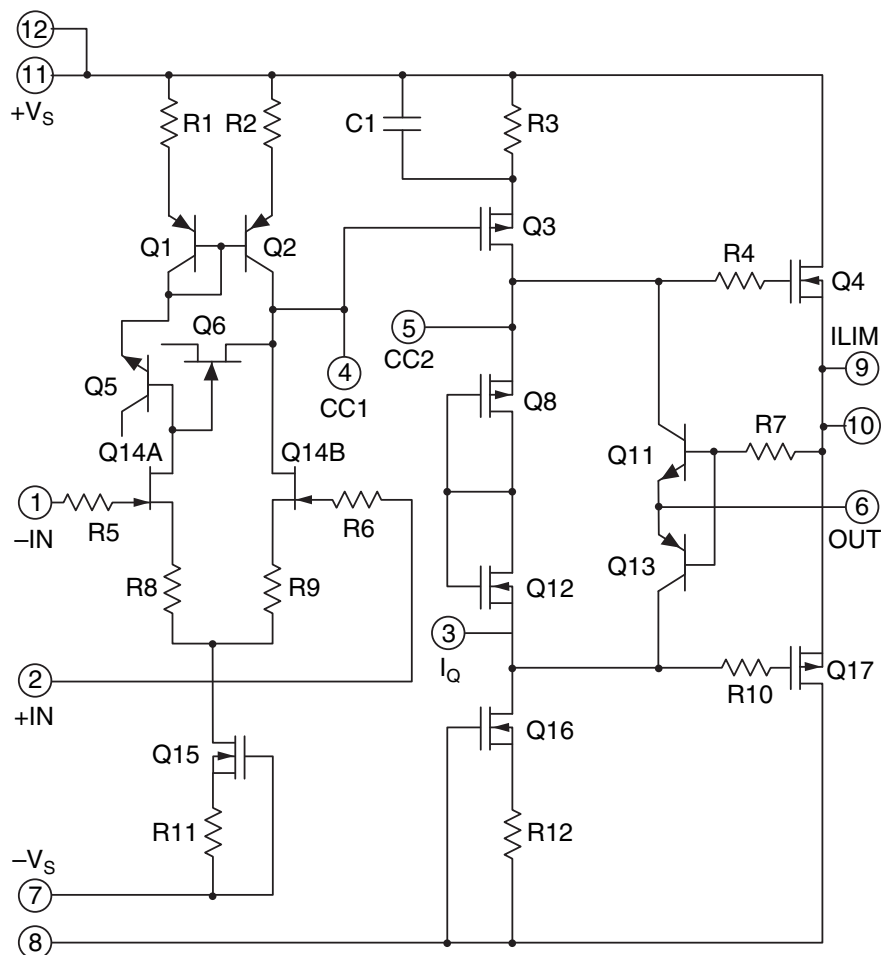
APPLICATIONS

- ◆ PIEZOELECTRIC POSITIONING
- ◆ HIGH VOLTAGE INSTRUMENTATION
- ◆ ELECTROSTATIC TRANSDUCERS
- ◆ PROGRAMMABLE POWER SUPPLIES UP TO 390V

DESCRIPTION

The PA90 is a high voltage, low quiescent current MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 200mA and pulse currents up to 350mA. The safe operating area (SOA) has no second breakdown limitations and can be observed for all type loads by choosing an appropriate current limiting resistor. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. Apex Microtechnology's Power SIP package uses a minimum of board space allowing for high density circuit boards. The 12-pin PowerSIP package is electrically isolated.

EQUIVALENT SCHEMATIC



1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
SUPPLY VOLTAGE, $+V_s$ to $-V_s$			400	V
OUTPUT CURRENT, source, sink, peak, within SOA			350	mA
POWER DISSIPATION, continuous @ $T_c = 25^\circ\text{C}$			30	W
INPUT VOLTAGE, differential		-20	20	V
INPUT VOLTAGE, common mode		$-V_s$	V_s	V
TEMPERATURE, pin solder, 10s max.			260	$^\circ\text{C}$
TEMPERATURE, junction (Note 2)			150	$^\circ\text{C}$
TEMPERATURE RANGE, storage		-55	125	$^\circ\text{C}$
OPERATING TEMPERATURE RANGE, case		-40	85	$^\circ\text{C}$

CAUTION The PA90 is constructed from MOSFET transistors. ESD handling procedures must be observed. The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

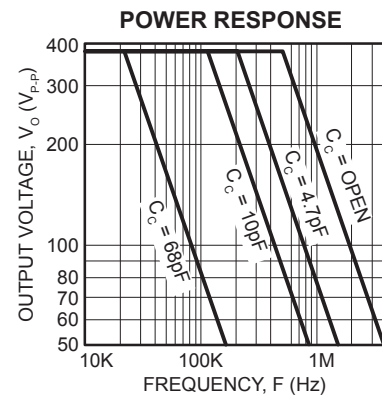
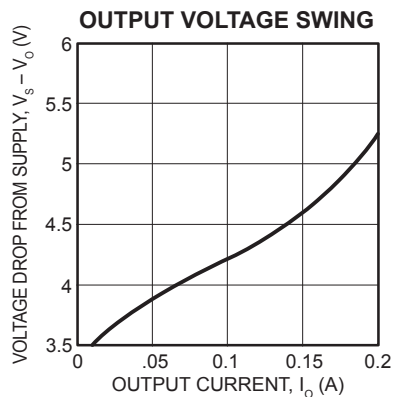
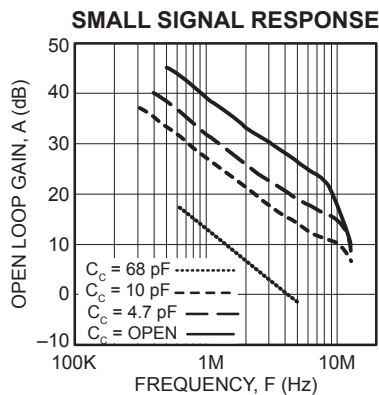
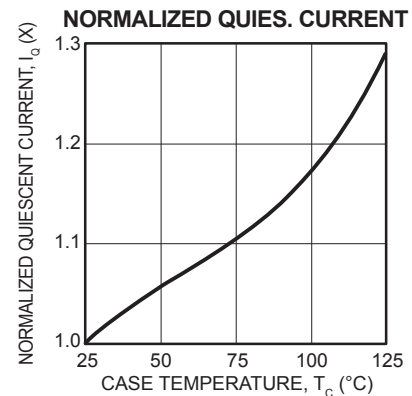
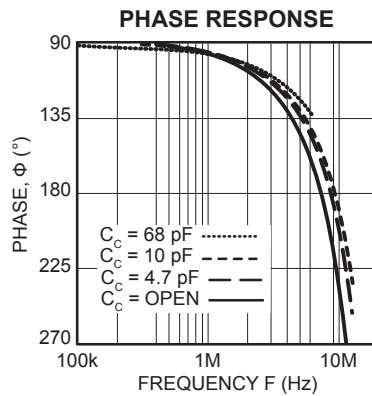
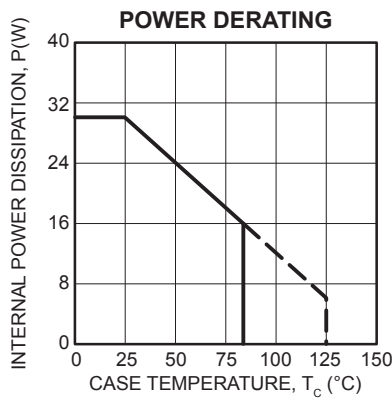
SPECIFICATIONS

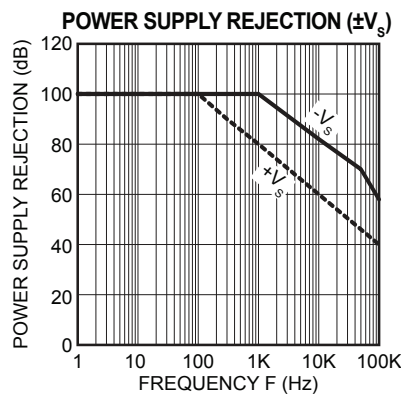
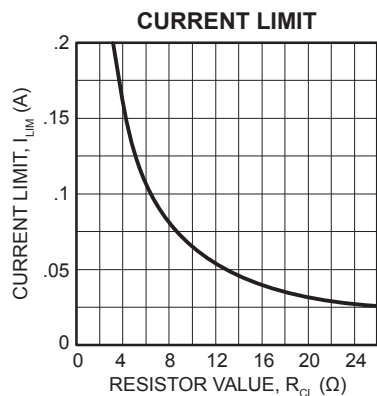
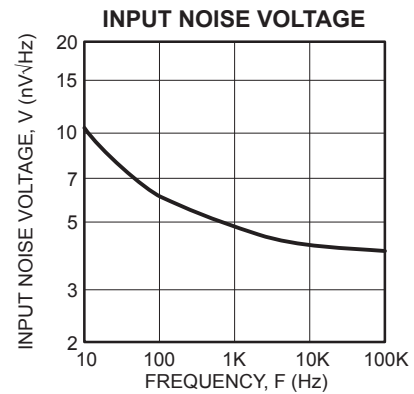
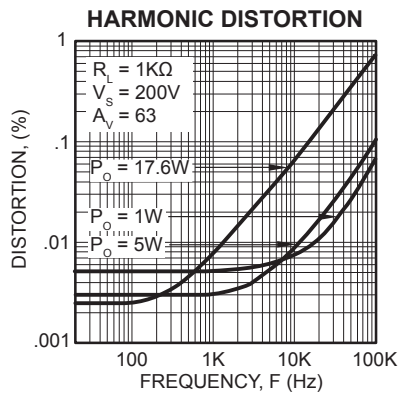
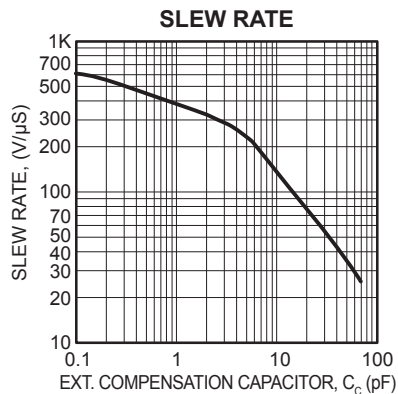
Parameter	Test Conditions ¹	Min	Typ	Max	Units
AMPLIFIER INPUT					
OFFSET VOLTAGE, initial			0.5	2	mV
OFFSET VOLTAGE vs. temperature	Full temperature range		15	50	$\mu\text{V}/^\circ\text{C}$
OFFSET VOLTAGE vs. supply			10	25	$\mu\text{V}/\text{V}$
OFFSET VOLTAGE vs. time			75		$\mu\text{V}/\text{kHz}$
BIAS CURRENT, initial			200	2000	pA
BIAS CURRENT vs. supply			4		pA/V
OFFSET CURRENT, initial			50	500	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE (Note 3)		$\pm V_s \mp 15$			V
COMMON MODE REJECTION, DC	$V_{CM} = \pm 90\text{V}$	80	98		dB
NOISE	100kHz bandwidth, $R_s = 1\text{K}\Omega$, $C_c = \text{OPEN}$		1		$\mu\text{V RMS}$
GAIN					
OPEN LOOP @ 15Hz	$R_L = 2\text{K}\Omega$, $C_c = \text{OPEN}$	94	111		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	$R_L = 2\text{K}\Omega$, $C_c = \text{OPEN}$		100		MHz
POWER BANDWIDTH	$R_L = 2\text{K}\Omega$, $C_c = \text{OPEN}$		470		kHz
PHASE MARGIN	Full temperature range		60		$^\circ$
OUTPUT					
VOLTAGE SWING (Note 3)	$I_o = 200\text{mA}$	$\pm V_s \mp 12$	$\pm V_s \mp 10$		V
CURRENT, continuous		200			mA
SLEW RATE, $A_v = 100$	$C_c = \text{OPEN}$	240	300		V/ μS
CAPACITIVE LOAD, $A_v = +1$	Full temperature range	470			pF

Parameter	Test Conditions ¹	Min	Typ	Max	Units
SETTLING TIME to 0.1%	$C_c = \text{OPEN}$, 2V step		1		μS
RESISTANCE, no load			50		Ω
POWER SUPPLY					
VOLTAGE (Note 5)		± 40	± 150	± 200	V
CURRENT, quiescent			10	14	mA
THERMAL					
RESISTANCE, AC, junction to case (Note 4)	Full temp range, $F > 60\text{Hz}$			2.5	$^{\circ}\text{C}/\text{W}$
RESISTANCE, DC, junction to case	Full temp range, $F < 60\text{Hz}$			4.2	$^{\circ}\text{C}/\text{W}$
RESISTANCE, junction to air	Full temp range		30		$^{\circ}\text{C}/\text{W}$
TEMPERATURE RANGE, case	Meets full range specifications	-25		+85	$^{\circ}\text{C}$

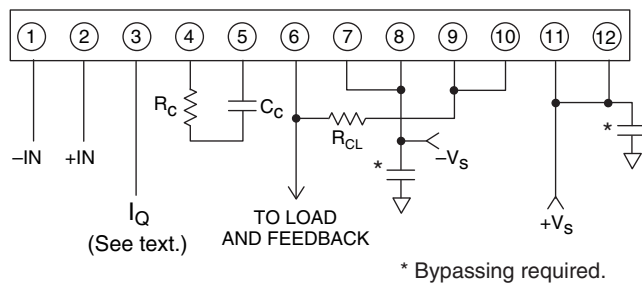
- NOTES: 1. (All Min/Max characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages and $T_c = 25^{\circ}\text{C}$).
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
3. $+V_s$ and $-V_s$ denote the positive and negative power supply rail respectively.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Derate max supply rating .625 V/ $^{\circ}\text{C}$ below 25°C case. No derating needed above 25°C case.

2. TYPICAL PERFORMANCE GRAPHS





EXTERNAL CONNECTIONS



**12-pin SIP
PACKAGE
STYLE DP**

Formed leads available
See package EE



PHASE COMPENSATION

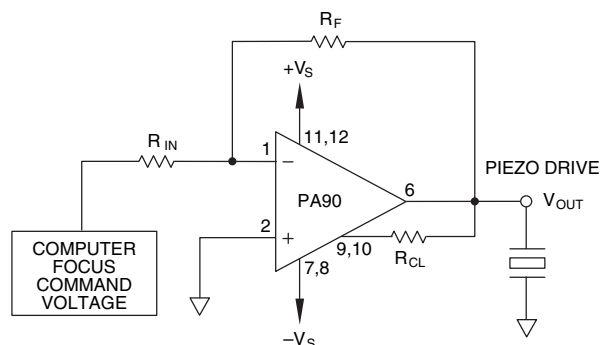
GAIN	C_c^*	R_c
≥ 1	68pF	100 Ω
≥ 5	10pF	100 Ω
≥ 10	4.7pF	0 Ω
≥ 30	NONE	0 Ω

* C_c To be rated for the full supply voltage $+V_s$ to $-V_s$. Use NPO ceramic (COG) type.

TYPICAL APPLICATION

LOW POWER, PIEZOELECTRIC POSITIONING

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA90 reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Microtechnology's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 32 ohms.

$$R_{CL} = \frac{.65}{I_{LIM}}$$

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

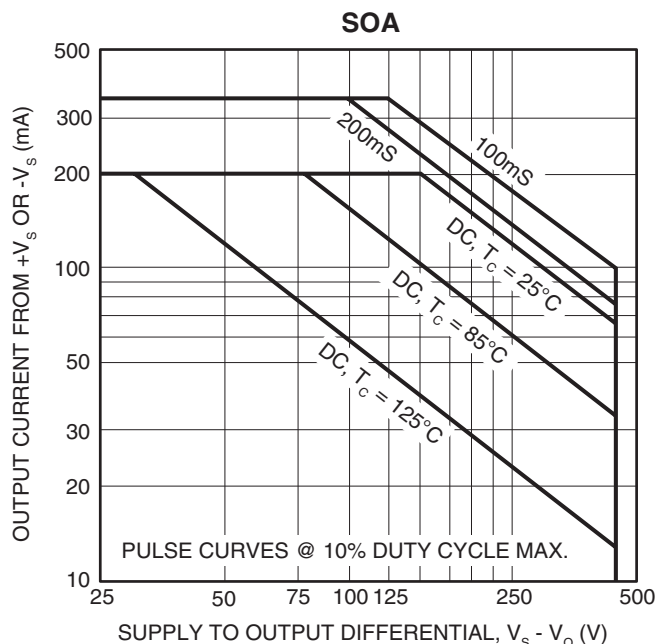
NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load.

INPUT PROTECTION

Although the PA90 can withstand differential voltages up to $\pm 20V$, additional external protection is recommended. Low leakage, low capacitance JFETs connected as diodes are recommended (e.g. 2N4416, Q1-Q4 in Figure 2). The differential input voltage will be clamped to $\pm 1.4V$. This is sufficient overdrive to produce maximum power bandwidth.



POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. See Figure 2. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail is known to induce input stage failure. Unidirectional transzors prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

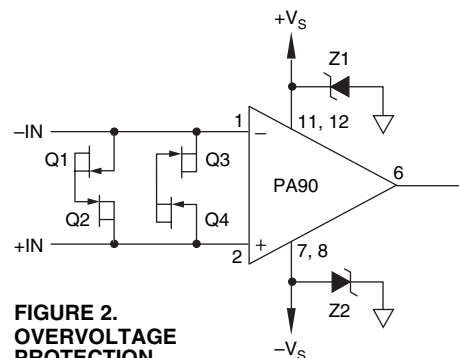


FIGURE 2.
OVERVOLTAGE
PROTECTION

STABILITY

The PA90 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_c must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network $C_c R_c$ must be mounted closely to the amplifier pins 4 and 5 to avoid spurious oscillation.

QUIESCENT CURRENT REDUCTION

When pin 3 (I_Q) is shorted to pin 5 (CC2) the AB biasing of the output stage is disabled. This raises distortion since the output stage is then class C biased, but reduces the quiescent current by 1mA for a power dissipation savings of 0.4W. Pin 3 may be left open if not used.

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