Data Sheet, DS1, Jan. 2003

# IPAC-X

## ISDN PC Adapter Circuit

## PSB/PSF 21150, V 1.4

Wired
Communications

Infineon technologies

Never stop thinking.

ABM®, ACE®, AOP®, ARCOFI®, ASM®, ASP®, DigiTape®, DuSLIC®, EPIC®, ELIC®, FALC®, GEMINAX®, IDEC®, INCA®, IOM®, IPAT®-2, ISAC®, ITAC®, IWE®, IWORX®, MUSAC®, MuSLIC®, OCTAT®, OptiPort®, POTSWIRE®, QUAT®, QuadFALC®, SCOUT®, SICAT®, SICOFI®, SIDEC®, SLICOFI®, SMINT®, SOCRATES®, VINETIC®, 10BaseV®, 10BaseVX® are registered trademarks of Infineon Technologies AG. 10BaseS™, EasyPort™, VDSLite™ are trademarks of Infineon Technologies AG. Microsoft® is a registered trademark of Microsoft Corporation. Linux® is a registered trademark of Linus Torvalds.

The information in this document is subject to change without notice.

**Edition 2003-01-30**

**Published by Infineon Technologies AG,**
**St.-Martin-Strasse 53,**
**81669 München, Germany**

**© Infineon Technologies AG 2003.**
**All Rights Reserved.**

**Attention please!**

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

**Information**

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (**www.infineon.com**).

**Warnings**

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

**Data Sheet**

**Revision History:** **2003-01-30** DS1

Previous Version: Data Sheet, DS1, V1.3, 2000-07-21

| Page | Subjects (major changes since last revision) |
|---|---|
| **Chapter 1** | Comparison IPAC/IPAC-X |
| **Chapter 3.3.7.2** | S- Transceiver Synchronization New |
| **Chapter 3.3.11** | Test Functions extended |
| **Chapter 3.7.1.1** | CDA Handler Description extended |
| **Chapter 3.7.5.1** | TIC Bus Access Control: Note added |
| **Chapter 5.6** | IOM-2 Interface Timing: Explanation added |
| **Chapter 5.7.2** | Parallel Microcontroller Interface Timing: Explanation added |
| **Chapter 5.10** | S-Transceiver |
| **Chapter 5.11** | Recommended Transformer Specificatio: Changed |
| **Chapter 5.12** | Line Overload Protection added |
| **Chapter 5.13** | EMC/ESD added |
| | |
| | |
| | |
| | |
| | |

**Table of Contents** **Page**


| | | |
|---|---|---|
| **1** | **Overview** | 13 |
| 1.1 | Features | 17 |
| 1.2 | Logic Symbol | 19 |
| 1.3 | Typical Applications | 20 |
| **2** | **Pin Configuration** | 24 |
| **3** | **Description of Functional Blocks** | 33 |
| 3.1 | General Functions and Device Architecture | 33 |
| 3.2 | Microcontroller Interfaces | 34 |
| 3.2.1 | Serial Control Interface (SCI) | 35 |
| 3.2.1.1 | Programming Sequences | 36 |
| 3.2.2 | Parallel Microcontroller Interface | 39 |
| 3.2.3 | Interrupt Structure | 41 |
| 3.2.4 | Reset Generation | 43 |
| 3.2.5 | Timer Modes | 45 |
| 3.2.6 | Activation Indication via Pin ACL | 47 |
| 3.3 | S/T-Interface | 48 |
| 3.3.1 | S/T-Interface Coding | 50 |
| 3.3.2 | S/T-Interface Multiframing | 52 |
| 3.3.3 | Multiframe Synchronization (M-Bit) | 54 |
| 3.3.4 | Data Transfer and Delay between IOM-2 and S/T | 57 |
| 3.3.5 | Transmitter Characteristics | 60 |
| 3.3.6 | Receiver Characteristics | 61 |
| 3.3.7 | S/T Interface Circuitry | 62 |
| 3.3.7.1 | External Protection Circuitry | 62 |
| 3.3.7.2 | S-Transceiver Synchronization | 65 |
| 3.3.8 | S/T Interface Delay Compensation (TE/LT-T Mode) | 65 |
| 3.3.9 | Level Detection Power Down | 65 |
| 3.3.10 | Transceiver Enable/Disable | 66 |
| 3.3.11 | Test Functions | 66 |
| 3.4 | Clock Generation | 68 |
| 3.4.1 | Description of the Receive PLL (DPLL) | 71 |
| 3.4.2 | Jitter | 71 |
| 3.4.3 | Oscillator Clock Output C768 | 72 |
| 3.5 | Control of Layer-1 | 73 |
| 3.5.1 | State Machine TE and LT-T Mode | 75 |
| 3.5.1.1 | State Transition Diagram (TE, LT-T) | 75 |
| 3.5.1.2 | States (TE, LT-T) | 77 |
| 3.5.1.3 | C/I Codes (TE, LT-T) | 79 |
| 3.5.1.4 | Infos on S/T (TE, LT-T) | 81 |
| 3.5.2 | State Machine LT-S Mode | 82 |
| 3.5.2.1 | State Transition Diagram (LT-S) | 82 |

**Table of Contents** **Page**

3.5.2.2 States (LT-S) . . . 83
3.5.2.3 C/I Codes (LT-S) . . . 84
3.5.2.4 Infos on S/T (LT-S) . . . 85
3.5.3 State Machine NT Mode . . . 86
3.5.3.1 State Transition Diagram (NT) . . . 86
3.5.3.2 States (NT) . . . 87
3.5.3.3 C/I Codes (NT) . . . 88
3.5.4 Command/Indicate Channel Codes (C/I0) - Overview . . . 90
3.6 Control Procedures . . . 91
3.6.1 Example of Activation/Deactivation . . . 91
3.6.2 Activation Initiated by the Terminal . . . 92
3.6.3 Activation initiated by the Network Termination NT . . . 93
3.7 IOM-2 Interface . . . 94
3.7.1 IOM-2 Handler . . . 97
3.7.1.1 Controller Data Access (CDA) . . . 99
3.7.1.2 IDSL Support . . . 109
3.7.2 Serial Data Strobe Signal and Strobed Data Clock . . . 112
3.7.2.1 Serial Data Strobe Signal . . . 112
3.7.2.2 Strobed IOM-2 Bit Clock . . . 114
3.7.3 IOM-2 Monitor Channel . . . 115
3.7.3.1 Handshake Procedure . . . 117
3.7.3.2 Error Treatment . . . 120
3.7.3.3 MONITOR Channel Programming as a Master Device . . . 122
3.7.3.4 MONITOR Channel Programming as a Slave Device . . . 123
3.7.3.5 Monitor Time-Out Procedure . . . 124
3.7.3.6 MONITOR Interrupt Logic . . . 125
3.7.4 C/I Channel Handling . . . 126
3.7.5 D-Channel Access Control . . . 128
3.7.5.1 TIC Bus D-Channel Access Control . . . 128
3.7.5.2 S-Bus Priority Mechanism for D-Channel . . . 130
3.7.5.3 S-Bus D-Channel Control in LT-T . . . 133
3.7.5.4 D-Channel Control in the Intelligent NT (TIC- and S-Bus) . . . 133
3.7.6 Activation/Deactivation of IOM-2 Interface . . . 137
3.8 Auxiliary Interface . . . 140
3.8.1 Mode Dependent Functions . . . 140
3.9 HDLC Controllers . . . 143
3.9.1 Message Transfer Modes . . . 144
3.9.2 Data Reception . . . 146
3.9.2.1 Structure and Control of the Receive FIFO . . . 146
3.9.2.2 Receive Frame Structure . . . 152
3.9.3 Data Transmission . . . 154
3.9.3.1 Structure and Control of the Transmit FIFO . . . 154

**Table of Contents** **Page**

3.9.3.2 Transmit Frame Structure . . . 159
3.9.4 Access to IOM-2 channels . . . 159
3.9.5 Extended Transparent Mode . . . 159
3.9.6 HDLC Controller Interrupts . . . 161
3.10 Test Functions . . . 162

**4 Detailed Register Description** . . . 164
4.1 D-channel HDLC Control and C/I Registers . . . 172
4.1.1 RFIFOD - Receive FIFO D-Channel . . . 172
4.1.2 XFIFOD - Transmit FIFO D-Channel . . . 172
4.1.3 ISTAD - Interrupt Status Register D-Channel . . . 172
4.1.4 MASKD - Mask Register D-Channel . . . 174
4.1.5 STARD - Status Register D-Channel . . . 174
4.1.6 CMDRD - Command Register D-Channel . . . 175
4.1.7 MODED - Mode Register . . . 176
4.1.8 EXMD1- Extended Mode Register D-channel 1 . . . 178
4.1.9 TIMR1 - Timer 1 Register . . . 179
4.1.10 SAP1 - SAPI1 Register . . . 180
4.1.11 SAP2 - SAPI2 Register . . . 180
4.1.12 RBCLD - Receive Frame Byte Count Low D-Channel . . . 181
4.1.13 RBCHD - Receive Frame Byte Count High D-Channel . . . 181
4.1.14 TEI1 - TEI1 Register 1 . . . 181
4.1.15 TEI2 - TEI2 Register . . . 182
4.1.16 RSTAD - Receive Status Register D-Channel . . . 182
4.1.17 TMD -Test Mode Register D-Channel . . . 184
4.1.18 CIR0 - Command/Indication Receive 0 . . . 185
4.1.19 CIX0 - Command/Indication Transmit 0 . . . 186
4.1.20 CIR1 - Command/Indication Receive 1 . . . 186
4.1.21 CIX1 - Command/Indication Transmit 1 . . . 187
4.2 Transceiver Registers . . . 188
4.2.1 TR_CONF0 - Transceiver Configuration Register 0 . . . 188
4.2.2 TR_CONF1 - Transceiver Configuration Register 1 . . . 189
4.2.3 TR_CONF2 - Transmitter Configuration Register 2 . . . 190
4.2.4 TR_STA - Transceiver Status Register . . . 191
4.2.5 TR_CMD - Transceiver Command Register . . . 192
4.2.6 SQRR1 - S/Q-Channel Receive Register 1 . . . 193
4.2.7 SQXR1- S/Q-Channel TX Register 1 . . . 194
4.2.8 SQRR2 - S/Q-Channel Receive Register 2 . . . 194
4.2.9 SQXR2 - S/Q-Channel TX Register 2 . . . 195
4.2.10 SQRR3 - S/Q-Channel Receive Register 3 . . . 195
4.2.11 SQXR3 - S/Q-Channel TX Register 3 . . . 195
4.2.12 ISTATR - Interrupt Status Register Transceiver . . . 196
4.2.13 MASKTR - Mask Transceiver Interrupt . . . 197

**Table of Contents** **Page**

4.2.14 TR_MODE - Transceiver Mode Register 1 . . . . . 197
4.3 Auxiliary Interface Registers . . . . . 198
4.3.1 ACFG1 - Auxiliary Configuration Register 1 . . . . . 198
4.3.2 ACFG2 - Auxiliary Configuration Register 2 . . . . . 198
4.3.3 AOE - Auxiliary Output Enable Register . . . . . 200
4.3.4 ARX - Auxiliary Interface Receive Register . . . . . 201
4.3.5 ATX - Auxiliary Interface Transmit Register . . . . . 201
4.4 IOM-2 and MONITOR Handler . . . . . 202
4.4.1 CDAxy - Controller Data Access Register xy . . . . . 202
4.4.2 XXX_TSDPxy - Time Slot and Data Port Selection for CHxy . . . . . 203
4.4.3 CDAx_CR - Control Register Controller Data Access CH1x . . . . . 204
4.4.4 TR_CR - Control Register Transceiver Data (IOM_CR.CI_CS=0) . . . 205
4.4.5 TRC_CR - Control Register Transceiver C/I0 (IOM_CR.CI_CS=1) . . . 206
4.4.6 BCHx_CR - Control Register B-Channel Controller Data . . . . . 206
4.4.7 DCI_CR - Control Register for D and CI1 Handler (IOM_CR.CI_CS=0) 207
4.4.8 DCIC_CR - Control Register for CI0 Handler (IOM_CR.CI_CS=1) . . . 208
4.4.9 MON_CR - Control Register Monitor Data . . . . . 209
4.4.10 SDSx_CR - Control Register Serial Data Strobe x . . . . . 210
4.4.11 IOM_CR - Control Register IOM Data . . . . . 211
4.4.12 STI - Synchronous Transfer Interrupt . . . . . 213
4.4.13 ASTI - Acknowledge Synchronous Transfer Interrupt . . . . . 214
4.4.14 MSTI - Mask Synchronous Transfer Interrupt . . . . . 214
4.4.15 SDS_CONF - Configuration Register for Serial Data Strobes . . . . . 215
4.4.16 MCDA - Monitoring CDA Bits . . . . . 215
4.4.17 MOR - MONITOR Receive Channel . . . . . 216
4.4.18 MOX - MONITOR Transmit Channel . . . . . 216
4.4.19 MOSR - MONITOR Interrupt Status Register . . . . . 216
4.4.20 MOCR - MONITOR Control Register . . . . . 217
4.4.21 MSTA - MONITOR Status Register . . . . . 218
4.4.22 MCONF - MONITOR Configuration Register . . . . . 218
4.5 Interrupt and General Configuration . . . . . 219
4.5.1 ISTA - Interrupt Status Register . . . . . 219
4.5.2 MASK - Mask Register . . . . . 220
4.5.3 AUXI - Auxiliary Interrupt Status Register . . . . . 220
4.5.4 AUXM - Auxiliary Mask Register . . . . . 221
4.5.5 MODE1 - Mode1 Register . . . . . 222
4.5.6 MODE2 - Mode2 Register . . . . . 223
4.5.7 ID - Identification Register . . . . . 224
4.5.8 SRES - Software Reset Register . . . . . 224
4.5.9 TIMR2 - Timer 2 Register . . . . . 225
4.6 B-Channel Registers . . . . . 226
4.6.1 ISTAB - Interrupt Status Register B-Channels . . . . . 226

**Table of Contents** **Page**

4.6.2 MASKB - Mask Register B-Channels . . . 227
4.6.3 STARB - Status Register B-Channels . . . 227
4.6.4 CMDRB - Command Register B-channels . . . 228
4.6.5 MODEB - Mode Register . . . 229
4.6.6 EXMB - Extended Mode Register B-Channels . . . 230
4.6.7 RAH1 - RAH1 Register . . . 232
4.6.8 RAH2 - RAH2 Register . . . 232
4.6.9 RBCLB - Receive Frame Byte Count Low B-Channels . . . 233
4.6.10 RBCHB - Receive Frame Byte Count High B-Channels . . . 233
4.6.11 RAL1 - RAL1 Register 1 . . . 233
4.6.12 RAL2 - RAL2 Register . . . 234
4.6.13 RSTAB - Receive Status Register B-Channels . . . 234
4.6.14 TMB -Test Mode Register B-Channels . . . 236
4.6.15 RFIFOB - Receive FIFO B-Channels . . . 236
4.6.16 XFIFOB - Transmit FIFO B-Channels . . . 236

**5 Electrical Characteristics** . . . 237
5.1 Absolute Maximum Ratings . . . 237
5.2 DC Characteristics . . . 238
5.3 Capacitances . . . 239
5.4 Oscillator Specification . . . 240
5.5 AC Characteristics . . . 241
5.6 IOM-2 Interface Timing . . . 242
5.7 Microcontroller Interface Timing . . . 245
5.7.1 Serial Control Interface (SCI) Timing . . . 245
5.7.2 Parallel Microcontroller Interface Timing . . . 246
5.8 Multiframe Synchronisation Timing . . . 250
5.9 Reset . . . 251
5.10 S-Transceiver . . . 252
5.11 Recommended Transformer Specification . . . 253
5.12 Line Overload Protection . . . 254
5.13 EMC / ESD Aspects . . . 255

**6 Package Outlines** . . . 256

**7 Appendix** . . . 258

**List of Figures** **Page**

Figure 1 Logic Symbol of the IPAC-X . . . . . 19
Figure 2 ISDN PC Adapter Card for S Interface . . . . . 20
Figure 3 ISDN PC Adapter Card for U or S Interface . . . . . 21
Figure 4 ISDN Voice/Data Terminal . . . . . 22
Figure 5 ISDN Stand-Alone Terminal with POTS Interface . . . . . 23
Figure 6 Pin Configuration of the IPAC-X . . . . . 24
Figure 7 Functional Block Diagram of the IPAC-X . . . . . 33
Figure 8 Serial Control Interface Timing . . . . . 35
Figure 9 Serial Control Interface Timing . . . . . 36
Figure 10 Direct/Indirect Register Address Mode . . . . . 40
Figure 11 Interrupt Status and Mask Registers . . . . . 41
Figure 12 Reset Generation . . . . . 43
Figure 13 Timer Interrupt Status Registers . . . . . 45
Figure 14 Timer 1 Register . . . . . 46
Figure 15 Timer 2 Register . . . . . 46
Figure 16 ACL Indication of Activated Layer 1 . . . . . 47
Figure 17 ACL Configuration . . . . . 47
Figure 18 Wiring Configurations in User Premises . . . . . 49
Figure 19 S/T -Interface Line Code . . . . . 50
Figure 20 Frame Structure at Reference Points S and T (ITU I.430) . . . . . 51
Figure 21 Multiframe Synchronization using the M-Bit . . . . . 54
Figure 22 Sampling Time in LT-S / NT Mode (M-Bit input) . . . . . 55
Figure 23 Frame Relationship in LT-S / NT Mode (M-Bit input) . . . . . 55
Figure 24 Frame Relationship in TE / LT-T Mode (M-Bit output) . . . . . 56
Figure 25 Data Delay Between IOM-2 and S/T Interface Transparent Mode (TE mode only) . . . . . 57
Figure 26 Data Delay Between IOM-2 and S/T Interface With S/G Bit Evaluation (TE mode only) . . . . . 58
Figure 27 Data Delay Between IOM-2 and S/T Interface With 8 IOM Channels (LT-S/NT mode only) . . . . . 59
Figure 28 Data Delay Between IOM-2 and S/T Interface With 3 IOM Channels a Maximum Receive Delay(LT-S/NT mode only) . . . . . 59
Figure 29 Equivalent Internal Circuit of the Transmitter Stage . . . . . 60
Figure 30 Equivalent Internal Circuit of the Receiver Stage . . . . . 61
Figure 31 Connection of Line Transformers and Power Supply to the IPAC-X . . 62
Figure 32 External Circuitry for Transmitter . . . . . 63
Figure 33 External Circuitry for Symmetrical Receivers . . . . . 64
Figure 34 External Circuitry for Symmetrical Receivers . . . . . 65
Figure 35 Disabling of S/T Transmitter . . . . . 66
Figure 36 External Loop at the S/T-Interface . . . . . 67
Figure 37 Clock System of the IPAC-X . . . . . 68
Figure 38 Phase Relationships of IPAC-X Clock Signals . . . . . 71

## List of Figures

Page

Figure 39 Buffered Oscillator Clock Output . . . 72
Figure 40 Layer-1 Control . . . 73
Figure 41 State Diagram Notation . . . 74
Figure 42 State Transition Diagram (TE, LT-T) . . . 76
Figure 43 State Transition Diagram of Unconditional Transitions (TE, LT-T) . . . 77
Figure 44 State Transition Diagram (LT-S) . . . 82
Figure 45 State Transition Diagram (NT) . . . 86
Figure 46 Example of Activation/Deactivation Initiated by the Terminal . . . 91
Figure 47 Example of Activation/Deactivation initiated by the Terminal (TE). Activation/Deactivation Completely Under Software Control . . . 92
Figure 48 Example of Activation/Deactivation Initiated by the Network Termination (NT). Activation/Deactivation Completely Under SoftwarControl . . . 93
Figure 49 IOM®-2 Frame Structure in Terminal Mode . . . 95
Figure 50 Multiplexed Frame Structure of the IOM-2 Interface in Non-TE Timing Mode . . . 96
Figure 51 Architecture of the IOM Handler (Example Configuration) . . . 98
Figure 52 Data Access via CDAx1 and CDAx2 Register Pairs . . . 100
Figure 53 Examples for Data Access via CDAxy Registers . . . 101
Figure 54 Data Access when Looping TSa from DU to DD . . . 102
Figure 55 Data Access When Shifting TSa to TSb on DU (DD) . . . 103
Figure 56 Example for Monitoring Data . . . 104
Figure 57 Interrupt Structure of the Synchronous Data Transfer . . . 106
Figure 58 Examples for the Synchronous Transfer Interrupt Control With One Enabled STIxy . . . 107
Figure 59 Timeslot Assignment on IOM-2 . . . 109
Figure 60 Examples for HDLC Controller Access . . . 110
Figure 61 Timeslot Assignment on S . . . 111
Figure 62 Mapping of Bits from IOM-2 to S . . . 111
Figure 63 Data Strobe Signal . . . 113
Figure 64 Strobed IOM-2 Bit Clock. Register SDS_CONF Programmed to 01H 114
Figure 65 Examples of MONITOR Channel Applications in IOM -2 TE Mode . . 115
Figure 66 MONITOR Channel Protocol (IOM-2) . . . 118
Figure 67 Monitor Channel, Transmission Abort Requested by the Receiver . . 121
Figure 68 Monitor Channel, Transmission Abort Requested by the Transmitter 121
Figure 69 Monitor Channel, Normal End of Transmission . . . 122
Figure 70 MONITOR Interrupt Structure . . . 125
Figure 71 CIC Interrupt Structure . . . 127
Figure 72 Applications of TIC Bus in IOM-2 Bus Configuration . . . 129
Figure 73 Structure of Last Octet of Ch2 on DU . . . 130
Figure 74 Structure of Last Octet of Ch2 on DD . . . 131
Figure 75 D-Channel Access Control on the S-Interface . . . 132

**List of Figures** **Page**

Figure 76 Data Flow for Collision Resolution Procedure in Intelligent NT . . . . . 136
Figure 77 Deactivation of the IOM-2 Interface . . . . . 137
Figure 78 Activation of the IOM-2 interface . . . . . 138
Figure 79 RFIFO Operation . . . . . 148
Figure 80 Data Reception Procedures . . . . . 150
Figure 81 Reception Sequence Example . . . . . 151
Figure 82 Receive Data Flow . . . . . 152
Figure 83 Data Transmission Procedure . . . . . 157
Figure 84 Transmission Sequence Example . . . . . 158
Figure 85 Transmit Data Flow . . . . . 159
Figure 86 Interrupt Status Registers of the HDLC Controllers . . . . . 161
Figure 87 Layer 2 Test Loops . . . . . 162
Figure 88 Register Mapping of the IPAC-X . . . . . 164
Figure 89 Oscillator Circuits . . . . . 240
Figure 90 Input/Output Waveform for AC Tests . . . . . 241
Figure 91 IOM-2 Timing (TE mode) . . . . . 242
Figure 92 IOM-2 Timing (LT-S, LT-T, NT mode) . . . . . 243
Figure 93 Definition of Clock Period and Width . . . . . 244
Figure 94 SCI Interface . . . . . 245
Figure 95 Microprocessor Read Cycle . . . . . 246
Figure 96 Microprocessor Write Cycle . . . . . 246
Figure 97 Multiplexed Address Timing . . . . . 247
Figure 98 Non-Multiplexed Address Timing . . . . . 247
Figure 99 Microprocessor Read Timing . . . . . 248
Figure 100 Microprocessor Write Cycle . . . . . 248
Figure 101 Non-Multiplexed Address Timing . . . . . 248
Figure 102 Sampling Time in LT-S/NT Mode (M-Bit Input) . . . . . 250
Figure 103 Reset Signal RES . . . . . 251
Figure 104 Maximum Line Input Current . . . . . 254
Figure 105 Transformer Circuitry . . . . . 255

## List of Tables

Page

Table 1 Comparison of the IPAC-X with the Previous Version IPAC: . . . . . 14
Table 2 IPAC-X Pin Definitions and Functions . . . . . 25
Table 3 Host Interface Selection . . . . . 34
Table 4 Header Byte Code . . . . . 36
Table 5 Bus Operation Modes . . . . . 39
Table 6 Reset Source Selection . . . . . 44
Table 7 IPAC-X Timers . . . . . 45
Table 8 S/Q-Bit Position Identification and Multi-Frame Structure . . . . . 52
Table 9 Clock Modes . . . . . 69
Table 10 Examples for Synchronous Transfer Interrupts . . . . . 105
Table 11 CDA Register Combinations with Correct Read/Write Access . . . . . 108
Table 12 Transmit Direction . . . . . 117
Table 13 Receive Direction . . . . . 117
Table 14 IPAC-X Configuration Settings in Intelligent NT Applications . . . . . 134
Table 15 AUX Pin Functions . . . . . 140
Table 16 IOM-2 Channel Selection . . . . . 141
Table 17 HDLC Controller Address Range . . . . . 143
Table 18 Receive Byte Count With RBC11...0 in the RBCHx/RBCLx Registers 147
Table 19 Receive Information at RME Interrupt . . . . . 153
Table 20 XPR Interrupt (Availability of XFIFOx) After XTF, XME Commands . 155

# 1 Overview

The ISDN PC Adapter Circuit Extended IPAC-X integrates all necessary functions for a host based ISDN access solution on a single chip. It is based on the IPAC PSB 2115, and provides enhanced features and functionality.

It includes the S-transceiver (Layer 1), an HDLC controller for the D-channel and two protocol controllers for each B-channel. They can be used for HDLC protocol or transparent access.

The system integration is simplified by several configurations of the parallel microcontroller interface selected via pin strapping. They include multiplexed and demultiplexed interface selection as well as the optional indirect register access mechanism which reduces the number of necessary registers in the address space to 2 locations. The IPAC-X also provides a serial control interface (SCI).

The FIFO size of the cyclic B-channel buffers is 128 bytes per channel and per direction, with programmable block size (threshold). Besides TE mode the S-transceiver supports other terminal relevant operation modes like line termination subscriber side (LT-S) and line termination trunk side (LT-T). A multi-line ISDN solution to support both S and U line coding is simplified as well as multi-line solution with up to 3 S-interfaces.

An auxiliary I/O port has been added with interrupt capabilities on two input lines. These programmable I/O lines may be used to connect peripheral components to the IPAC-X which need software control or have to forward status information to the host.

Three programmable LED outputs can be used to indicate certain status information, one of them is capable to indicate the activation status of the S-interface automatically.

The IPAC-X is produced in advanced CMOS technology.

**Table 1 Comparison of the IPAC-X with the Previous Version IPAC:**

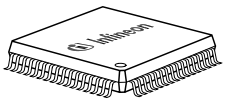
| | IPAC-X PSB 21150 | IPAC PSB 2115 |
|---|---|---|
| Operating modes | TE, LT-T, LT-S, NT, Int. NT | TE, LT-T, LT-S, Int. NT |
| Supply voltage | 3.3 V ± 5 % | 5 V ± 5 % |
| Technology | CMOS | CMOS |
| Package | P-MQFP-64 / P-TQFP-64 | P-MQFP-64 / P-TQFP-64 |
| Transceiver<br>Transformer ratio for the<br>transmitter<br>receiver | <br><br><br>1:1<br>1:1 | <br><br><br>2:1<br>2:1 |
| Test Functions | - Dig. loop via Layer 2 (TLP)<br>- Layer 1 disable (DIS_TR)<br>- Analog loop<br>(LP_A-bit, EXLP-bit, ARL) | - Dig. loop via Layer 2(TLP)<br>- Layer 1 disable (TEM)<br>- Analog loop (ARL) |
| Microcontroller Interface | Serial interface (SCI)<br><br>8-bit parallel interface:<br>Motorola Mux<br>Siemens/Intel Mux<br>Siemens/Intel Non-Mux<br>direct/ indirect Addressing | Not provided<br><br>8-bit parallel interface:<br>Motorola Mux<br>Siemens/Intel Mux<br>Siemens/Intel Non-Mux |
| Crystal | 7.68 MHz | 7.68 MHz |
| Buffered 7.68 MHz output | Provided | Provided |
| Controller data access to IOM-2 timeslots | All timeslots;<br>various possibilities of data access | Restricted access to<br>B- and IC-channel |
| Data control and manipulation | Various possibilities of data control and data manipulation (enable/ disable, shifting, looping, switching) | B- and IC-channel looping |
| IOM-2 | | |
| IOM-2 Interface | Double clock (DCL),<br>bit clock pin (BCL),<br>serial data strobe 1 (SDS1)<br>serial data strobe 2 (SDS2) | Double clock (DCL),<br>bit clock (BCL),<br>serial data strobe (SDS) |

| | IPAC-X PSB 21150 | IPAC PSB 2115 |
|---|---|---|
| Monitor channel programming | Provided (MON0, 1, 2, ..., 7) | Provided (MON0 or 1) |
| C/I channels | CI0 (4 bit), CI1 (4/6 bit) | CI0 (4 bit), CI1 (6 bit) |
| Layer 1 state machine | With changes for correspondence with the actual ITU specification | |
| Layer 1 state machine in software | Possible | Not possible |
| Support of IDSL (144kBit/s) | Provided (HDLC controller access, SDS1/2 signals active) | Not provided |
| D-channel HDLC support | D- and B-channel timeslots; non-auto mode, transparent mode 0-2, extended transparent mode | D-channel timeslot; auto mode, non-auto mode, transparent mode 1-3 |
| D-channel FIFO size | 64 bytes cyclic buffer per direction with programmable FIFO thresholds | 2x32 bytes buffer per direction |
| B-channel HDLC support | D- and B-channel timeslots; non-auto mode, transparent mode 0-2, extended transparent mode | D-channel timeslot; non-auto mode, transparent mode 0,1 extended transparent mode |
| B-channel FIFO size | 128 bytes cyclic buffer per direction for each channel with programmable FIFO thresholds | 2x64 bytes buffer per direction |
| Reset Sources | $\overline{\text{RES}}$ Input<br>Watchdog<br>C/I Code Change<br>$\overline{\text{EAW}}$ Pin<br>Software Reset | RST Input<br>Watchdog<br>C/I Code Change<br>EAW Pin |
| Interrupt Output Signals | $\overline{\text{INT}}$<br>low active (open drain) by default, reprogrammable to high active (push-pull) | Low active $\overline{\text{INT}}$ |

| | IPAC-X PSB 21150 | IPAC PSB 2115 |
|---|---|---|
| 8-bit Auxiliary Interface | Provided | Provided |
| PCM Interface | Not Provided | Provided |
| Functions FBOUT, $\overline{\text{INT0/1}}$ | Provided | Provided |
| Reset Signals | $\overline{\text{RES}}$ input signal<br>$\overline{\text{RSTO}}$ output signal | RES input/output signal |
| Pin SCLK | 1.536 MHz | 512 kHz |
| Timeslots of arbitrary lenght | not available | available (“Clock Mode 5”) |

**V 1.4**

## 1.1 Features



**P-MQFP-64-1**

**P-TQFP-64-1**

- Single chip host based ISDN solution
- Based on IPAC PSB 2115, integrating ISAC-S and HSCX-TE functionality
- 8-bit parallel microcontroller interface, Motorola and Siemens/Intel bus type multiplexed or non-multiplexed, direct-/indirect register addressing
- Serial control interface (SCI)
- Microcontroller access to all IOM-2 timeslots
- Various types of protocol support (Non-auto mode, transparent mode, extended transparent mode)
- B-channel HDLC controllers with 128 byte FIFOs
- Flexible access to 18-bit timeslots (2B+D) on IOM-2 for IDSL support
- D-channel HDLC controller with 64 byte FIFOs
- IOM-2 interface in TE, LT-T, LT-S and NT mode, single/double clocks and two strobe signals
- D-channel priority handler on IOM-2 for intelligent NT applications
- Monitor channel handler (master/slave)
- IOM-2 MONITOR and C/I-channel protocol to control peripheral devices
- Full duplex 2B+D S/T-interface transceiver according to ITU-T I.430
- Conversion of the frame structure between the S/T-interface and IOM-2
- Receive timing recovery
- D-channel access control
- Activation and deactivation procedures with automatic activation from power down state
- Access to S and Q bits of S/T-interface

| Type | Package |
|---|---|
| PSB/PSF 21150 H | P-MQFP-64-1 |
| PSB/PSF 21150 F | P-TQFP-64-1 |

- Adaptively switched receive thresholds
- Auxiliary Interface with general purpose I/O pins and LED drivers
- Two programmable timers
- Watchdog timer
- Test loops
- Sophisticated power management for restricted power mode
- Power supply 3.3 V
- 3.3 V output drivers, inputs are 5 V safe
- Advanced CMOS technology

## 1.2 Logic Symbol

The logic symbol gives an overview of the IPAC-X functions. It must be noted that not all functions are available simultaneously, but depend on the selected mode.

Pins which are marked with a " * " are multiplexed and not available in all modes.

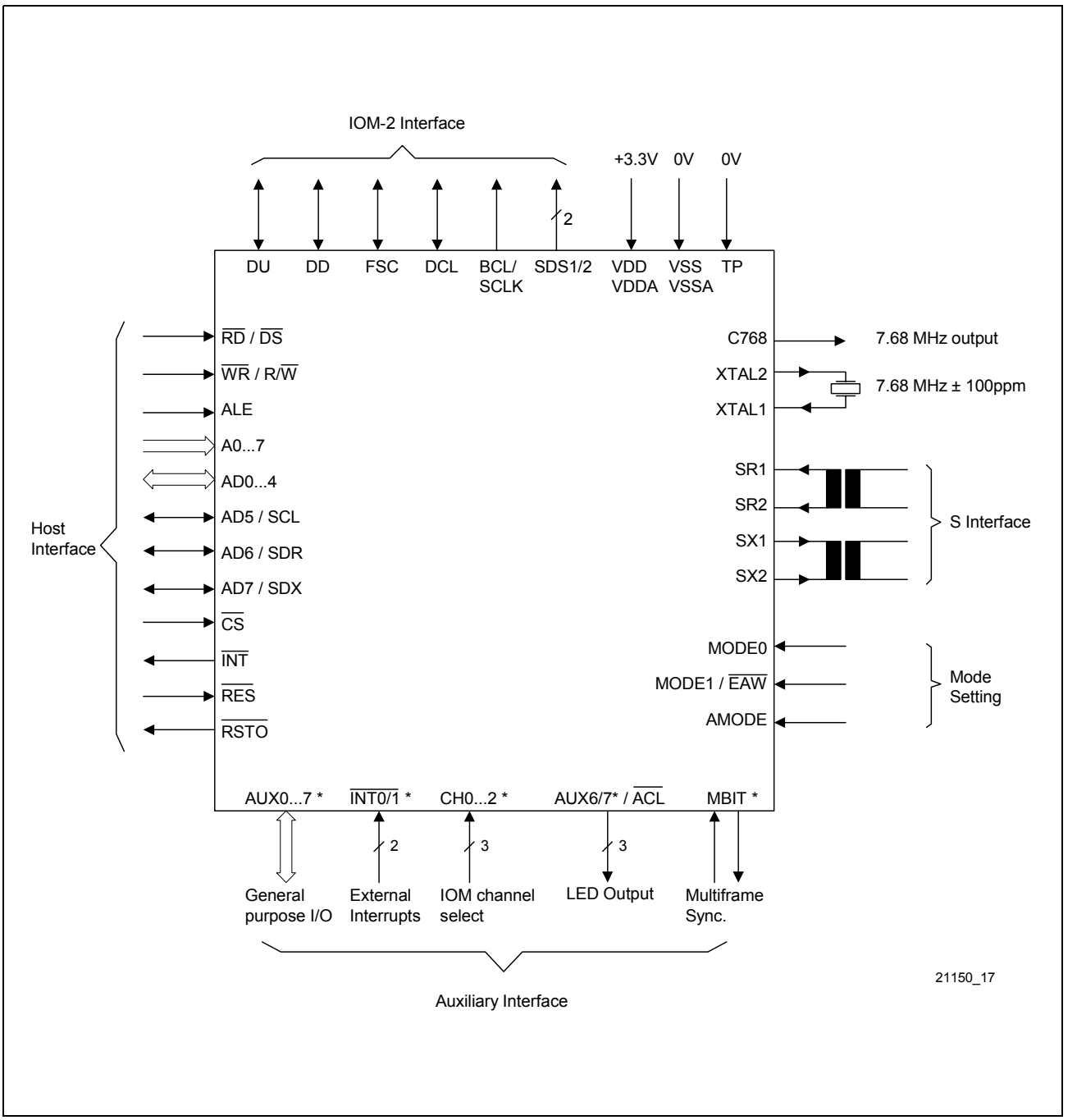



**Figure 1 Logic Symbol of the IPAC-X**

## 1.3 Typical Applications

The IPAC-X can be used in a variety of applications like

- ISDN PC adapter card for S interface (**Figure 2**)
- ISDN PC adapter card for U or S interface (**Figure 3**)
- ISDN voice/data terminal (**Figure 4**)
- ISDN stand-alone terminal with POTS interface (**Figure 5**)

An ISDN adapter card for a PC is built around the IPAC-X using a USB, PCI or ISA Plug and Play interface device depending on the required PC interface. The IPAC-X can be connected to any bus interface logic as it provides a standard 8-bit parallel µC interface and a serial control interface (SCI).

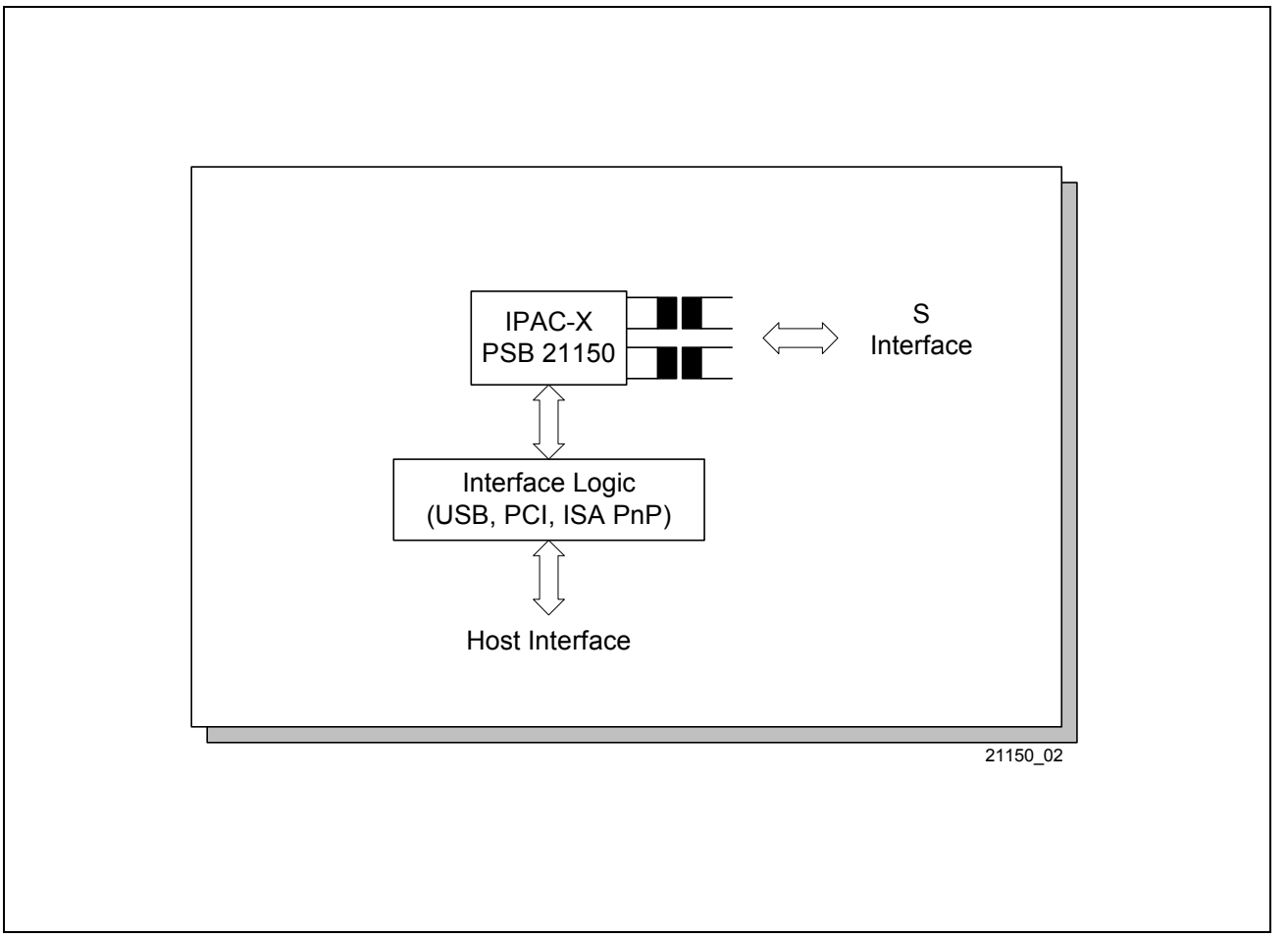



**Figure 2 ISDN PC Adapter Card for S Interface**

An ISDN adapter card which supports both U and S interface may be realized using the IPAC-X together with the PSB 21911 IEC-Q TE. The S interface may be configured for TE or LT-S mode supporting intelligent NT applications.

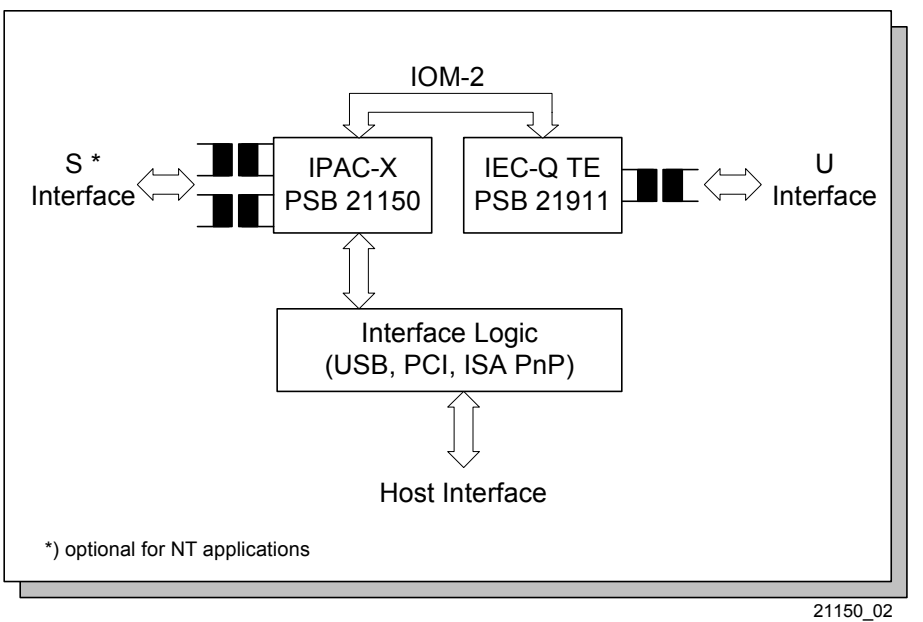



**Figure 3 ISDN PC Adapter Card for U or S Interface**

The figure below shows a voice data terminal developed on a PC card where the IPAC-X provides its functionality as data controller and S interface within a two chip solution. During ISDN calls the PSB 2163 ARCOFI-SP provides speakerphone functions and includes a DTMF generator. Additionally, a DTMF generator of keypad may be connected to the auxiliary interfce of the IPAC-X.

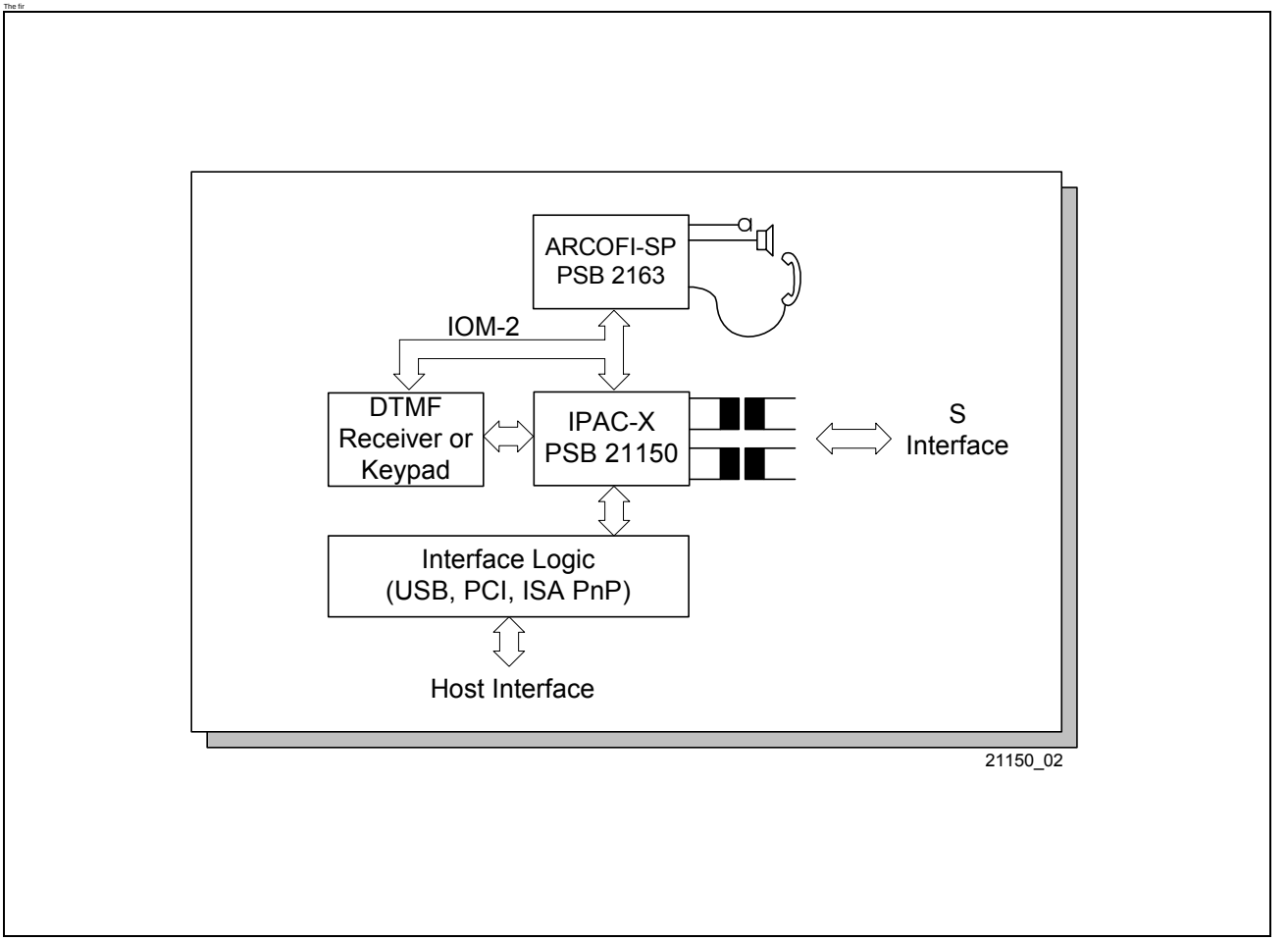



**Figure 4 ISDN Voice/Data Terminal**

The IPAC-X can be integrated in a microcontroller based stand-alone terminal that is connected to the communications interface of a PC. The SICOFI2-TE PSB 2132 enables connection of analog terminals (e.g. telephone or fax) to the dual channel POTS interface.

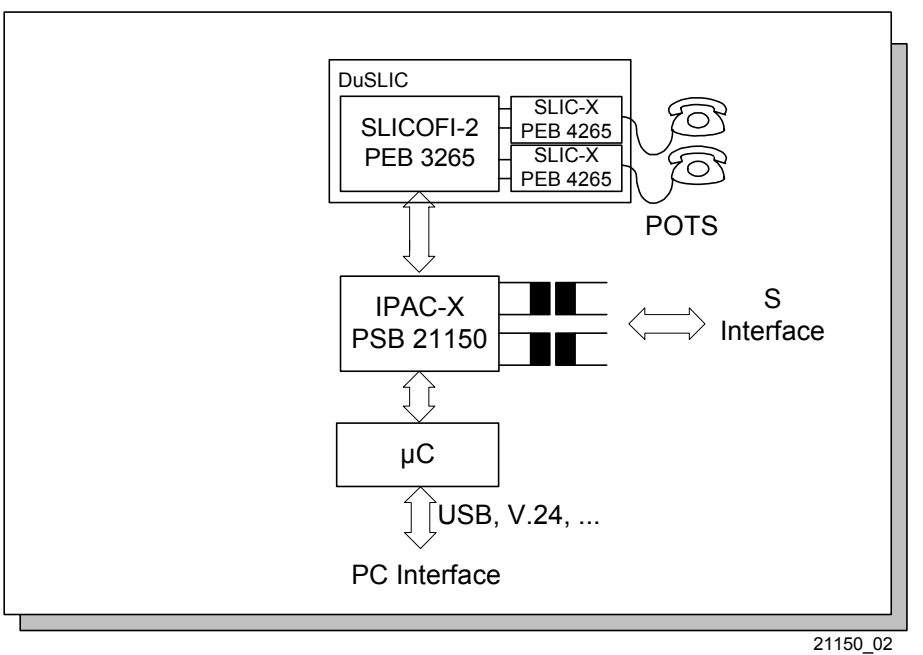



**Figure 5 ISDN Stand-Alone Terminal with POTS Interface**

# 2 Pin Configuration

P-MQFP-64-1
P-TQFP-64-1

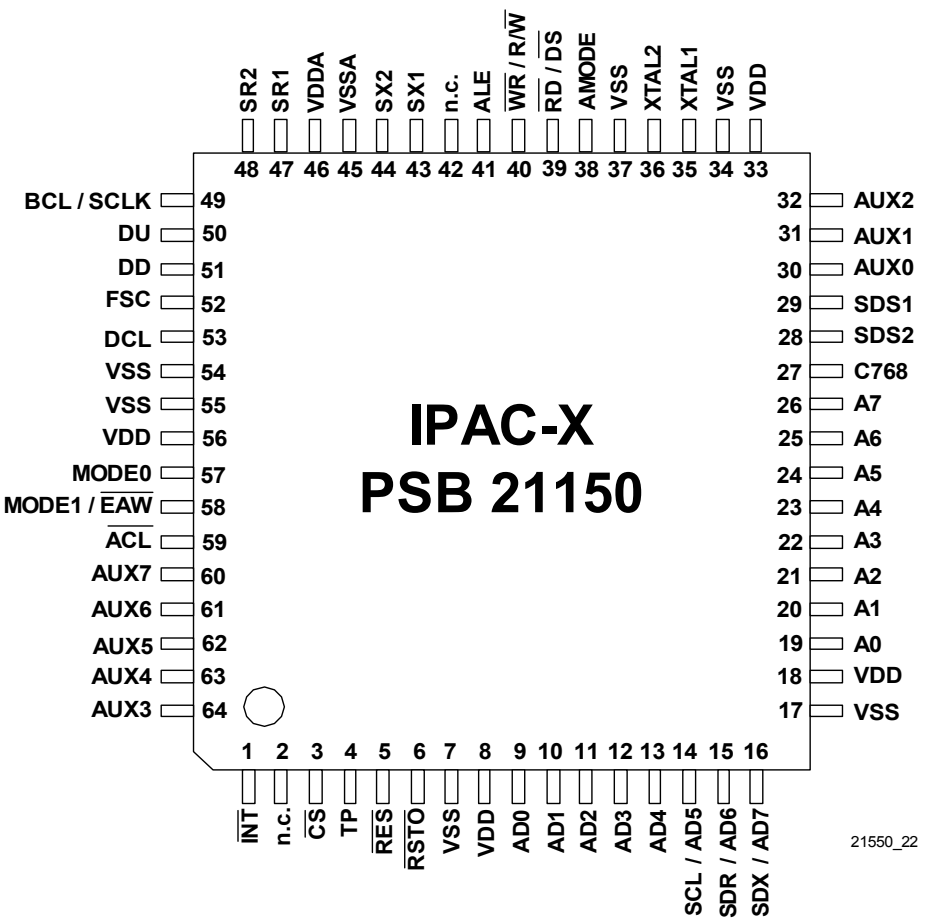



**Figure 6 Pin Configuration of the IPAC-X**

**Table 2 IPAC-X Pin Definitions and Functions**

| Pin No. MQFP-64 TQFP-64 | Symbol | Input (I) Output (O) Open Drain (OD) | Function |
|---|---|---|---|
| **Host Interface** | | | |
| 19<br>20<br>21<br>22<br>23<br>24<br>25<br>26 | A0<br>A1<br>A2<br>A3<br>A4<br>A5<br>A6<br>A7 | I<br>I<br>I<br>I<br>I<br>I<br>I<br>I | • **Non-Multiplexed Bus Mode:**<br>**Address Bus**<br>Address bus transfers addresses from the microcontroller to the IPAC-X. For indirect address mode only A0 is valid (A1-A7 to be connected to VDD).<br>• **Multiplexed Bus Mode:**<br>Not used in multiplexed bus mode. In this case A0-A7 should directly be connected to VDD. |
| 9<br>10<br>11<br>12<br>13 | AD0<br>AD1<br>AD2<br>AD3<br>AD4 | I/O<br>I/O<br>I/O<br>I/O<br>I/O | • **Multiplexed Bus Mode:**<br>**Address/data bus**<br>Transfers addresses from the microcontroller to the IPAC-X and data between the microcontroller and the IPAC-X.<br>• **Non-Multiplexed Bus Mode:**<br>**Data bus**<br>Transfers data between the microcontroller and the IPAC-X. |
| 14 | AD5<br><br><br><br><br><br><br>SCL | I/O<br><br><br><br><br><br><br>I | • **Multiplexed Bus Mode:**<br>**Address/data bus**<br>Address/data line AD5 if the parallel interface is selected.<br>• **Non-Multiplexed Bus Mode:**<br>**Data bus**<br>Data line D5 if the parallel interface is selected.<br><br>**SCI - Serial Clock**<br>Clock signal of the SCI interface if a serial interface is selected. |

**Table 2 IPAC-X Pin Definitions and Functions** (cont'd)

| Pin No. MQFP-64 TQFP-64 | Symbol | Input (I) Output (O) Open Drain (OD) | Function |
|---|---|---|---|
| 15 | AD6 | I/O | • **Multiplexed Bus Mode:**<br>**Address/data bus**<br>Address/data line AD6 if the parallel interface is selected.<br>• **Non-Multiplexed Bus Mode:**<br>**Data bus**<br>Data line D6 if the parallel interface is selected. |
| | SDR | I | **SCI - Serial Data Receive**<br>Receive data line of the SCI interface if a serial interface is selected. |
| 16 | AD7 | I/O | • **Multiplexed Bus Mode:**<br>**Address/data bus**<br>Address/data line AD7 if the parallel interface is selected.<br>• **Non-Multiplexed Bus Mode:**<br>**Data bus**<br>Data line D7 if the parallel interface is selected. |
| | SDX | OD | **SCI - Serial Data Transmit**<br>Transmit data line of the SCI interface if a serial interface is selected. |
| 39 | $\overline{RD}$ | I | **Read**<br>Indicates a read access to the registers (Siemens/ Intel bus mode). |
| | $\overline{DS}$ | I | **Data Strobe**<br>The rising edge marks the end of a valid read or write operation (Motorola bus mode). |
| 40 | $\overline{WR}$ | I | **Write**<br>Indicates a write access to the registers (Siemens/ Intel bus mode). |
| | R/$\overline{W}$ | I | **Read/Write**<br>A HIGH identifies a valid host access as a read operation and a LOW identifies a valid host access as a write operation (Motorola bus mode). |

**Table 2 IPAC-X Pin Definitions and Functions** (cont'd)

| Pin No. MQFP-64 TQFP-64 | Symbol | Input (I) Output (O) Open Drain (OD) | Function |
|---|---|---|---|
| 41 | ALE | I | **Address Latch Enable**<br>A HIGH on this line indicates an address on the external address/data bus (multiplexed bus type only).<br>ALE also selects the microcontroller interface bus type (multiplexed or non multiplexed). |
| 3 | $\overline{CS}$ | I | **Chip Select**<br>A low level indicates a microcontroller access to the IPAC-X. |
| 1 | $\overline{INT}$ | OD (O) | **Interrupt Request**<br>$\overline{INT}$ becomes active low (open drain) if the IPAC-X requests an interrupt.<br>The polarity can be reprogrammed to high active with push-pull chracteristic. |
| 5 | $\overline{RES}$ | I | **Reset**<br>A LOW on this input forces the IPAC-X into a reset state. |
| 38 | AMODE | I | **Address Mode**<br>Selects between direct (0) and indirect (1) register access mode. |
| **IOM-2 Interface** | | | |
| 52 | FSC | I/O | **Frame Sync**<br>8-kHz frame synchronization signal. |
| 53 | DCL | I/O | **Data Clock**<br>IOM-2 interface clock signal (double clock) (e.g 1.536 MHz in TE mode). |

**Table 2 IPAC-X Pin Definitions and Functions** (cont'd)

| Pin No. MQFP-64 TQFP-64 | Symbol | Input (I) Output (O) Open Drain (OD) | Function |
|---|---|---|---|
| 49 | BCL/ SCLK | O | **Bit Clock/S-Clock**<br>**TE-Mode:**<br>Bit clock output, identical to IOM-2 data rate (DCL/ 2).<br>**LT-T Mode:**<br>1.536 MHz output synchronous to S-interface.<br>**NT / LT-S Mode:**<br>Bit clock output derived from the DCL input clock divided by 2. |
| 51 | DD | I/O (OD) | **Data Downstream**<br>IOM-2 data signal in downstream direction. |
| 50 | DU | I/O (OD) | **Data Upstream**<br>IOM-2 data signal in upstream direction. |
| 29 | SDS1 | O | **Serial Data Strobe 1**<br>Programmable strobe signal for time slot and/or D-channel indication on IOM-2. |
| 28 | SDS2 | O | **Serial Data Strobe 2**<br>Programmable strobe signal for time slot and/or D-channel indication on IOM-2. |

**Auxiliary Interface**

| | | | |
|---|---|---|---|
| 30<br>31<br>32 | AUX0<br>AUX1<br>AUX2 | I/O (OD)<br>I/O (OD)<br>I/O (OD) | • **TE-Mode:**<br>**Auxiliary Port 0 - 2 (input/output)**<br>These pins are individually programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register.<br>• **LT-T/LT-S/NT Mode:**<br>**CH0-2 - IOM-2 Channel Select (input)**<br>These pins select one of eight channels on the IOM-2 interface. |
| 64 | AUX3 | I/O (OD) | **Auxiliary Port 3 (input/output)**<br>This pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register. |

**Table 2 IPAC-X Pin Definitions and Functions** (cont'd)

| Pin No. MQFP-64 TQFP-64 | Symbol | Input (I) Output (O) Open Drain (OD) | Function |
|---|---|---|---|
| 63 | AUX4 | I/O (OD) | • **Auxiliary Port 4 (input/output)**<br>This pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register.<br>• **MBIT (input/output)**<br>If ACFG2.A4SEL is set to '1', pin AUX4 is used as M-bit input (LT-S / NT / Int. NT mode) or as M-bit output (TE / LT-T mode) for multiframe synchronization. |
| 62 | AUX5 | I/O (OD) | • **Auxiliary Port 5 (input/output)**<br>This pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register.<br>• **FBOUT - FSC/BCL output**<br>If ACFG2.A5SEL is set to '1', pin AUX5 outputs either an FSC signal or a BCL signal selected via ACFG2.FBS. |
| 61 | AUX6 | I/O (OD) | **$\overline{\text{INT0}}$**<br>This pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register.<br>Additionally, as input it can generate a maskable interrupt to the host, which is either edge or level triggered. An internal pull up resistor is connected to this pin (open drain mode only), if push pull characteristic is selected no pull up is available.<br>As output an LED can directly be connected to this pin. |

**Table 2 IPAC-X Pin Definitions and Functions** (cont'd)

| Pin No. MQFP-64 TQFP-64 | Symbol | Input (I) Output (O) Open Drain (OD) | Function |
|---|---|---|---|
| 60 | AUX7 | I/O (OD) | **$\overline{\text{INT1}}$**<br>This pin is programmable as general input/output. The state of the pin can be read from (input) / written to (output) a register.<br>Additionally, as input it can generate a maskable interrupt to the host, which is either edge or level triggered. An internal pull up resistor is connected to this pin (open drain mode only), if push pull characteristic is selected no pull up is available.<br>As output an LED can directly be connected to this pin.<br>**SGO**<br>Instead of the above described function, AUX7 can also be programmed to output the S/G bit signal from the IOM-2 DD line. |

**Miscellaneous**

| | | | |
|---|---|---|---|
| 43<br>44 | SX1<br>SX2 | O<br>O | **S-Bus Transmitter Output (positive)**<br>**S-Bus Transmitter Output (negative)** |
| 47<br>48 | SR1<br>SR2 | I<br>I | **S-Bus Receiver Input**<br>**S-Bus Receiver Input** |
| 35<br><br><br><br><br>36 | XTAL1<br><br><br><br><br>XTAL2 | I<br><br><br><br><br>O | **Crystal 1**<br>Connection for a crystal or used as external clock input. 7.68 MHz clock or crystal required.<br>**Crystal 2**<br>Connection for a crystal. Not connected if an external clock is supplied to XTAL1 |
| 57 | MODE0 | I | **Mode 0 Select**<br>A LOW selects TE-mode and a HIGH selects LT-T / LT-S mode (see MODE1/$\overline{\text{EAW}}$). |

**Table 2 IPAC-X Pin Definitions and Functions** (cont'd)

| Pin No. MQFP-64 TQFP-64 | Symbol | Input (I) Output (O) Open Drain (OD) | Function |
|---|---|---|---|
| 58 | MODE1<br><br><br>$\overline{\text{EAW}}$ | I<br><br><br>I | The pin function depends on the setting of MODE0.<br>If MODE0=1: **Mode 1 Select**<br>A LOW selects LT-T mode and a HIGH selects LT-S mode.<br>If MODE0=0: **External Awake**<br>If a falling edge on this input is detected, the IPAC-X generates an interrupt and, if enabled, a reset pulse. |
| 59 | ACL | O | **Activation LED**<br>This pin can either function as a programmable output or it can automatically indicate the activated state of the S interface by a logic '0'.<br>An LED with pre-resistance may directly be connected to $\overline{\text{ACL}}$. |
| 27 | C768 | O | **Clock Output**<br>A 7.68 MHz clock is output to support other devices. This clock is not synchronous to the S interface. |
| 6 | $\overline{\text{RSTO}}$ | OD | **Reset Output**<br>Low active reset output, either from a watchdog timeout or programmed by the host. |
| 4 | TP | I | **Test Pin**<br>Must be connected to $V_{SS}$. |
| 2, 42 | n.c. | I | **not connected** |

**Power Supply**

| | | | |
|---|---|---|---|
| 8, 18, 33, 56 | $V_{DD}$ | – | **Digital Power Supply Voltage**<br>(3.3 V ± 5 %) |
| 46 | $V_{DDA}$ | – | **Analog Power Supply Voltage**<br>(3.3 V ± 5 %) |

**Table 2 IPAC-X Pin Definitions and Functions** (cont'd)

| Pin No. MQFP-64 TQFP-64 | Symbol | Input (I) Output (O) Open Drain (OD) | Function |
|---|---|---|---|
| 7, 17, 34, 37, 54, 55 | $V_{SS}$ | – | **Digital ground** (0 V) |
| 45 | $V_{SSA}$ | – | **Analog ground** (0 V) |

# 3 Description of Functional Blocks

## 3.1 General Functions and Device Architecture

**Figure 7** shows the architecture of the IPAC-X containing the following functions:

- S/T-interface transceiver
- Serial or parallel microcontroller interface
- Two B-channel HDLC-controller with 128 byte FIFOs per channel and per direction with programmable FIFO block size (threshold)
- One D-channel HDLC-controller with 64 byte FIFOs per direction with programmable FIFO block size (threshold)
- IOM-2 interface for terminal (TE mode), linecard (LT-T or LT-S) or NT applications
- D-channel access mechanism in all modes
- D-channel priority handler on IOM-2 for intelligent NT applications
- C/I- and Monitor channel handler
- Auxiliary interface with interrupt and general purpose I/O lines and LED drivers
- Clock and timing generation
- Digital PLL to synchronize the transceiver to the S/T interface
- Reset generation (watchdog timer)

The functional blocks are described in the following chapters.

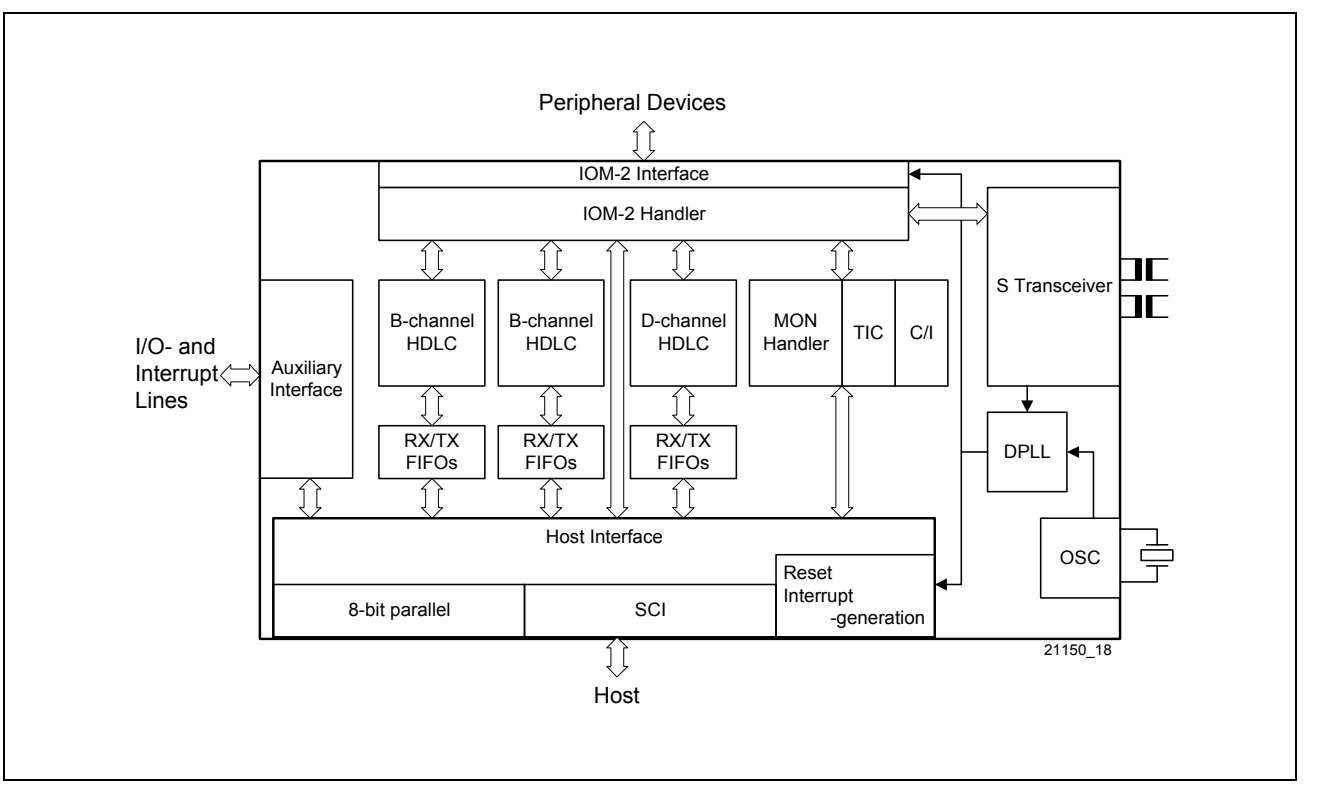



**Figure 7 Functional Block Diagram of the IPAC-X**

## 3.2 Microcontroller Interfaces

The IPAC-X supports a serial or a parallel microcontroller interface. For applications where no controller is connected to the IPAC-X microcontroller interface programming is done via the IOM-2 MONITOR channel from a master device. In such applications the IPAC-X operates in the IOM-2 slave mode (refer to the corresponding chapter of the IOM-2 MONITOR handler). This mode is suitable for control functions (e.g. programming registers of the S/T transceiver), but the band width is not sufficient for access to the HDLC controllers.

The interface selections are all done by pinstrapping (see **Table 3**). The selection pins are evaluated when the reset input $\overline{RES}$ is active. For the pin levels stated in the tables the following is defined:

'High', 'Low':dynamic pin; value must be 'High' or 'Low' only during reset
$V_{DD}$, $V_{SS}$: static pin; pin must statically be strapped to 'High' or 'Low' level
edge: dynamic pin; any transition ('High' to 'Low', 'Low' to 'High') has occured.

**Table 3 Host Interface Selection**

| PINS | | Serial /Parallel Interface | PINS | | Interface Type/Mode |
|---|---|---|---|---|---|
| $\overline{WR}$ (R/$\overline{W}$) | $\overline{RD}$ ($\overline{DS}$) | | CS | ALE | |
| 'High' | 'High' | Parallel | 'High' | $V_{DD}$ | Motorola |
| | | | | $V_{SS}$ | Siemens/Intel Non-Mux |
| | | | | edge | Siemens/Intel Mux |
| $V_{SS}$ | $V_{SS}$ | Serial | 'High' | $V_{SS}$ | Serial Control Interface(SCI) |
| | | No Host Interface | $V_{SS}$ | $V_{SS}$ | IOM-2 MONITOR Channel (Slave Mode) |

*Note: For a selected interface mode which doesn't need all input selection and address pins the unused pins must be tied to $V_{DD}$ or $V_{SS}$.*

The interfaces contain all circuitry necessary for the access to programmable registers, status registers and HDLC FIFOs. The mapping of all these registers can be found in **Chapter 4**.
The microcontroller interface also provides an interrupt request at pin $\overline{INT}$ which is low active by default but can be reprogrammed to high active, a reset input pin $\overline{RES}$ and a reset output pin $\overline{RSTO}$.
The interrupt request pin $\overline{INT}$ becomes active if the IPAC-X requests an interrupt and this can occur at any time.

### 3.2.1 Serial Control Interface (SCI)

The serial control interface (SCI) is compatible to the SPI interface of Motorola or Siemens C510 family of microcontrollers.
The SCI consists of 4 lines: SCL, SDX, SDR and $\overline{CS}$. Data is transferred via the lines SDR and SDX at the rate given by SCL. The falling edge of $\overline{CS}$ indicates the beginning of a serial access to the registers. The IPAC-X latches incoming data at the rising edge of SCL and shifts out at the falling edge of SCL. Each access must be terminated by a rising edge of $\overline{CS}$. Data is transferred in groups of 8 bits with the MSB first.
**Figure 8** shows the timing of a one byte read/write access via the serial control interface.

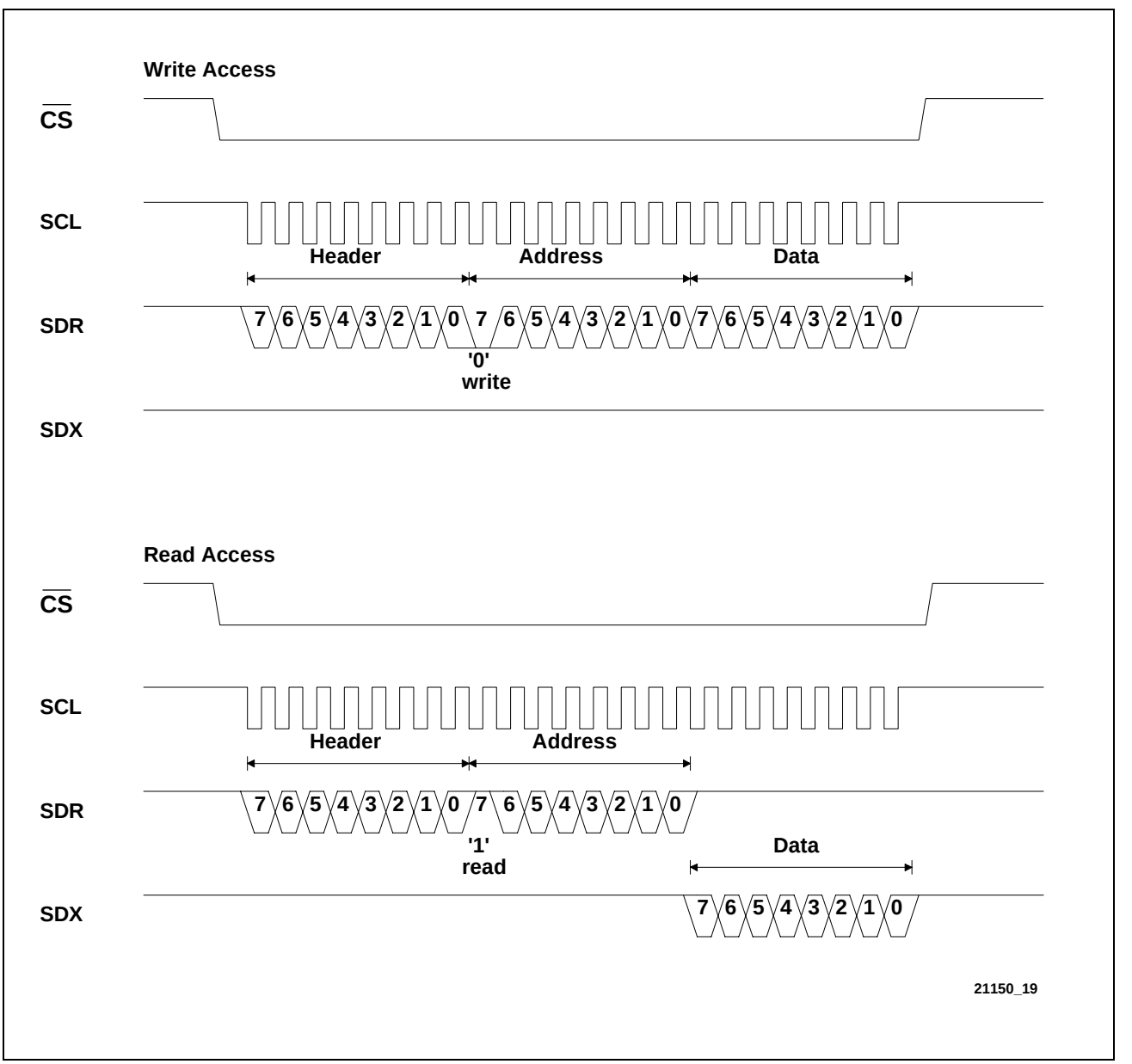



**Figure 8 Serial Control Interface Timing**

### 3.2.1.1 Programming Sequences

The basic structure of a read/write access to the IPAC-X registers via the serial control interface is shown in **Figure 9**.

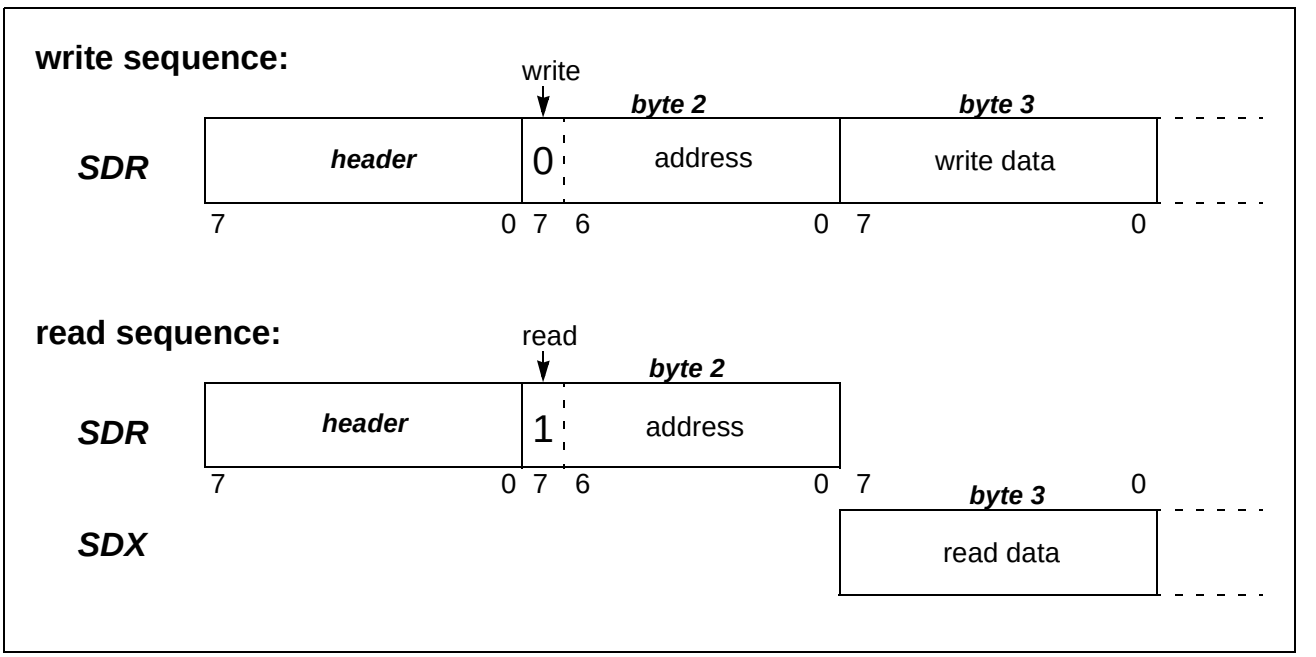



**Figure 9 Serial Control Interface Timing**

A new programming sequence starts with the transfer of a header byte. The header byte specifies different programming sequences allowing a flexible and optimized access to the individual functional blocks of the IPAC-X.
The possible sequences for access to the complete address range $00_H$-$7F_H$ are listed in **Table 4** and described after that.

**Table 4 Header Byte Code**

| Header Byte | Sequence | Sequence Type |
|---|---|---|
| $40_H/44_H$ | Adr-Data-Adr-Data | Alternating Read/Write (non-interleaved) |
| $48_H/4C_H$ | | Alternating Read/Write (interleaved) |
| $43_H/47_H$ | Adr-Data-Data-Data | Read-only/Write-only (constant address) |
| $41_H/45_H$ | | Read and following Write-only (non-interleaved) |
| $49_H/4D_H$ | | Read and following Write-only (interleaved) |

*Note: In order to access the address range $00_H$-$7F_H$ bit 2 of the header byte must be set to '0' (header bytes $40_H$, $48_H$, $43_H$, $41_H$, $49_H$), and for the addresses $80_H$-$FF_H$ bit 2 must be set to '1' (header bytes $44_H$, $4C_H$, $47_H$, $45_H$, $4D_H$).*

### Header $40_H$: Non-interleaved A-D-A-D Sequences

The non-interleaved A-D-A-D sequence gives direct read/write access to the complete address range and can have any length. In this mode SDX and SDR can be connected together allowing data transmission on one line.
Example for a read/write access with header $40_H$:

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| SDR | header | wradr | wrdata | rdadr | | rdadr | | wradr | wrdata | |
| SDX | | | | | rddata | | rdata | | | |

### Header $48_H$: Interleaved A-D-A-D Sequences

The interleaved A-D-A-D sequence gives direct read/write access to the complete address range and can have any length. This mode allows a time optimized access to the registers by interleaving the data on SDX and SDR (SDR and SDX must not be connected together).
Example for a read/write access with header $48_H$:

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| SDR | header | wradr | wrdata | rdadr | rdadr | wradr | wrdata | | | |
| SDX | | | | | rddata | rddata | | | | |

### Header $43_H$: Read-/Write- only A-D-D-D Sequence (Constant Address)

This mode can be used for a fast access to the HDLC FIFO data. Any address (rdadr, wradr) in the range $00_H$-$1F_H$ and $6A_H$/$7A_H$ gives access to the current FIFO location selected by an internal pointer which is automatically incremented with every data byte following the first address byte. The sequence can have any length and is terminated by the rising edge of $\overline{CS}$.

Example for a write access with header $43_H$:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| SDR | header | wradr | wrdata (wradr) | wrdata (wradr) | wrdata (wradr) | wrdata (wradr) | wrdata (wradr) | wrdata (wradr) | wrdata (wradr) | |
| SDX | | | | | | | | | | |

Example for a read access with header $43_H$:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| SDR | header | rdadr | | | | | | | | |
| SDX | | | rddata (rdadr) | rddata (rdadr) | rddata (rdadr) | rddata (rdadr) | rddata (rdadr) | rddata (rdadr) | rddata (rdadr) | |

### Header $41_H$: Non-interleaved A-D-D-D Sequence

This sequence allows in front of the A-D-D-D write access a non-interleaved A-D-A-D read access. This mode is useful for reading status information before writing to the HDLC XFIFO. The termination condition of the read access is the reception of the wradr. The sequence can have any length and is terminated by the rising edge of $\overline{CS}$.

Example for a read/write access with header $41_H$:

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| SDR | header | rdadr | | rdadr | | wradr | wrdata (wradr) | wrdata (wradr) | wrdata (wradr) | |
| SDX | | | rddata | | rddata | | | | | |

### Header $49_H$: Interleaved A-D-D-D Sequence

This sequence allows in front of the A-D-D-D write access an interleaved A-D-A-D read access. This mode is useful for reading status information before writing to the HDLC XFIFO. The termination condition of the read access is the reception of the wradr. The sequence can have any length and is terminated by the rising edge of the $\overline{CS}$ line.

Example for a read/write access with header $49_H$:

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| SDR | header | rdadr | rdadr | wradr | wrdata (wradr) | wrdata (wradr) | wrdata (wradr) | | | |
| SDX | | | rddata | rddata | | | | | | |

### 3.2.2 Parallel Microcontroller Interface

The 8-bit parallel microcontroller interface with address decoding on chip allows easy and fast microcontroller access.

The parallel interface of the IPAC-X provides three types of µP buses which are selected via pin ALE. The bus operation modes with corresponding pins are listed in **Table 5**.

**Table 5 Bus Operation Modes**

| | Bus Mode | Pin ALE | Control Pins |
|---|---|---|---|
| (1) | Motorola | $V_{DD}$ | $\overline{CS}$, R/$\overline{W}$, $\overline{DS}$ |
| (2) | Siemens/Intel non-multiplexed | $V_{SS}$ | $\overline{CS}$, $\overline{WR}$, $\overline{RD}$ |
| (3) | Siemens/Intel multiplexed | Edge | $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, ALE |

The occurrence of an edge on ALE, either positive or negative, at any time during the operation immediately selects the interface type (3). A return to one of the other interface types is possible only if a hardware reset is issued.

*Note: If the multiplexed address/data bus type (3) is selected, the unused address pins A0-A7 must be tied to $V_{DD}$.*

A read/write access to the IPAC-X registers can be done in **multiplexed or non-multiplexed** mode:

- In non-multiplexed mode the register address must be applied to the address bus (A0-A7) for the data access via the data bus (AD0-AD7).
- In multiplexed mode the address on the address/data bus (AD0-AD7) is latched in by ALE before a data read/write access via the same bus is performed.

The IPAC-X provides two different ways to address the register contents which is selected with the AMOD pin (’0’ = direct mode, ’1’ = indirect mode). **Figure 10** illustrates both register addressing modes.

**Direct address mode** (AMOD = ’0’): The register address to be read or written is directly set in the way described above.

**Indirect address mode** (AMOD = ’1’): Only the LSB of the address is used to select either the address register (A0 = ’0’) or the data register (A0 = ’1’). The microcontroller writes the register address to the ADDRESS register before it reads/writes data from/to the corresponding DATA register.
In indirect address mode the IPAC-X evaluates no address line except the least significant address bit. The remaining address lines must not be left open but have to be tied to logical ’1’.

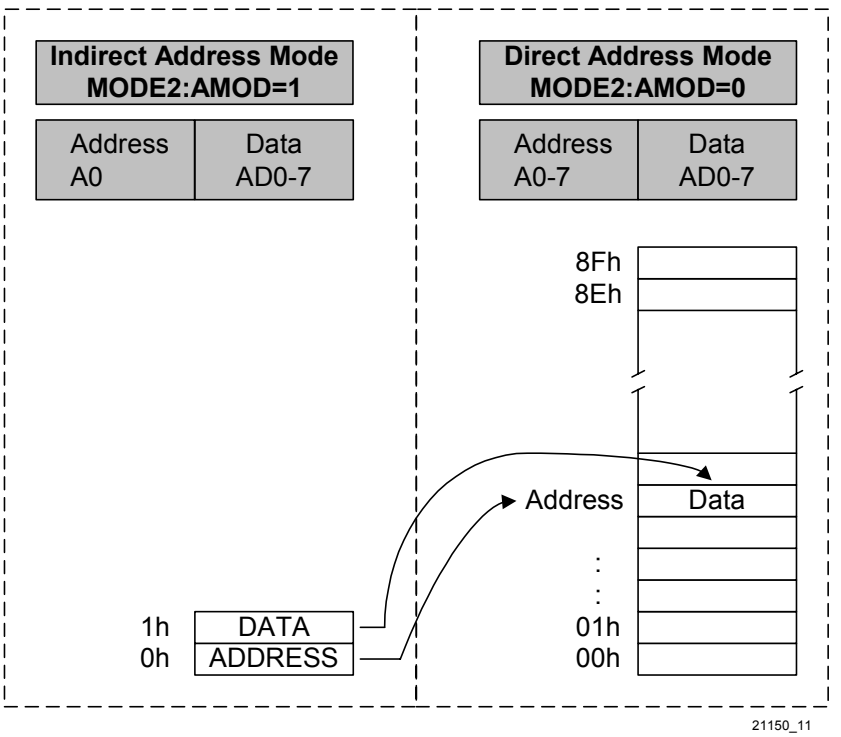



**Figure 10 Direct/Indirect Register Address Mode**

### 3.2.3 Interrupt Structure

Special events in the device are indicated by means of a single interrupt output, which requests the host to read status information from the device or transfer data from/to the device.

Since only one interrupt request pin ($\overline{INT}$) is provided, the cause of an interrupt must be determined by the host reading the interrupt status registers of the device.

The structure of the interrupt status registers is shown in **Figure 11**.

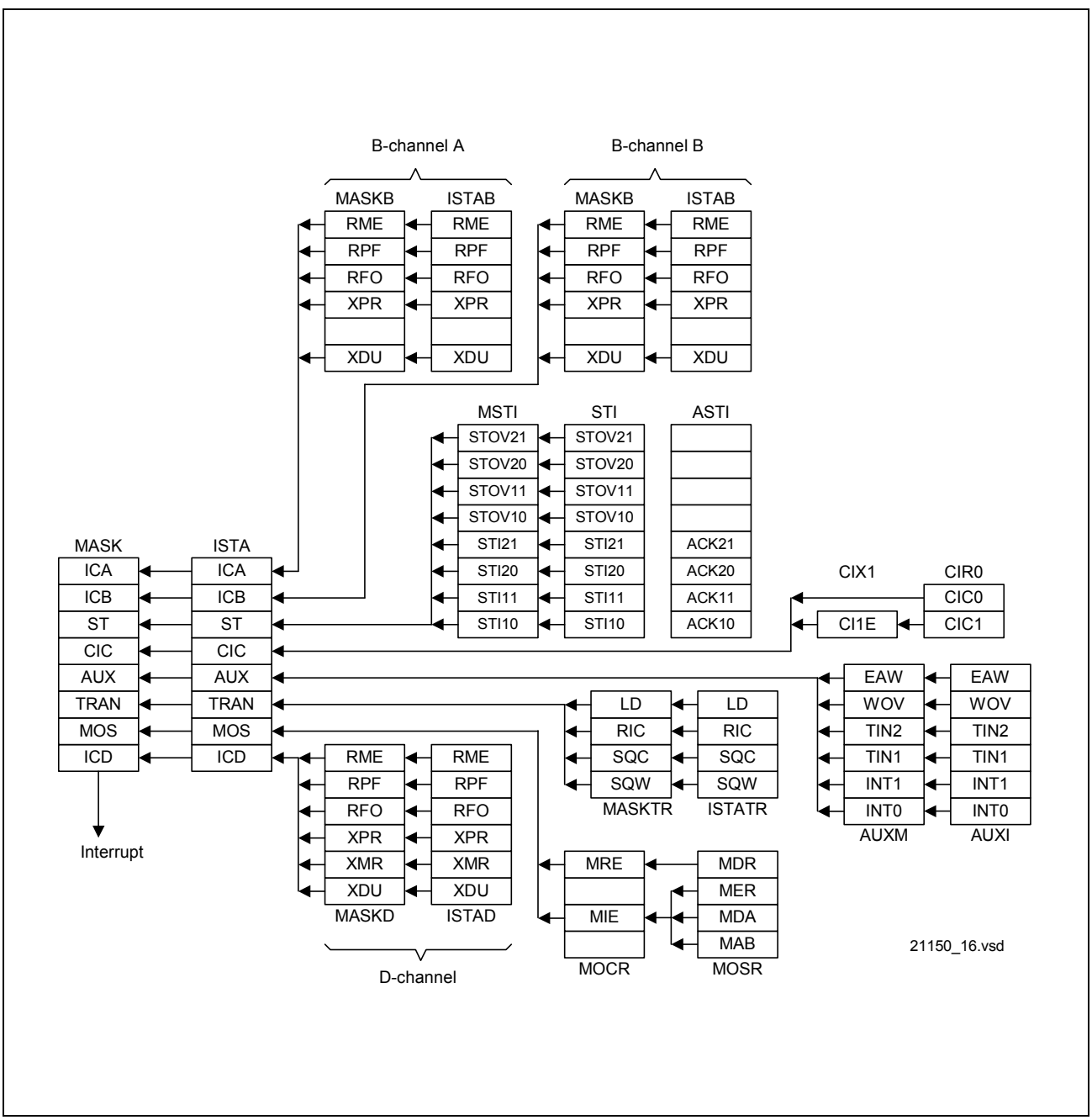



**Figure 11 Interrupt Status and Mask Registers**

All eight interrupt bits in the ISTA register point at interrupt sources in the D-channel HDLC Controller (ICD), B-channel HDLC controllers (ICA, ICB), Monitor- (MOS) and C/I- (CIC) handler, the transceiver (TRAN), the synchronous transfer (ST) and the auxiliary interrupts (AUXI).

All these interrupt sources are described in the corresponding chapters. After the device has requested an interrupt activating the interrupt pin ($\overline{INT}$), the host must read first the device interrupt status register (ISTA) in the associated interrupt service routine. The interrupt pin of the device remains active until all interrupt sources are cleared by reading the corresponding interrupt register. Therefore it is possible that the interrupt pin is still active when the interrupt service routine is finished.
Each interrupt indication of the interrupt status registers can selectively be masked by setting the respective bit in the MASK register.

For some interrupt controllers or hosts it might be necessary to generate a new edge on the interrupt line to recognize pending interrupts. This can be done by masking all interrupts at the end of the interrupt service routine (writing $FF_H$ into the MASK register) and write back the old mask to the MASK register.

### 3.2.4 Reset Generation

**Figure 12** shows the organization of the reset generation of the device.

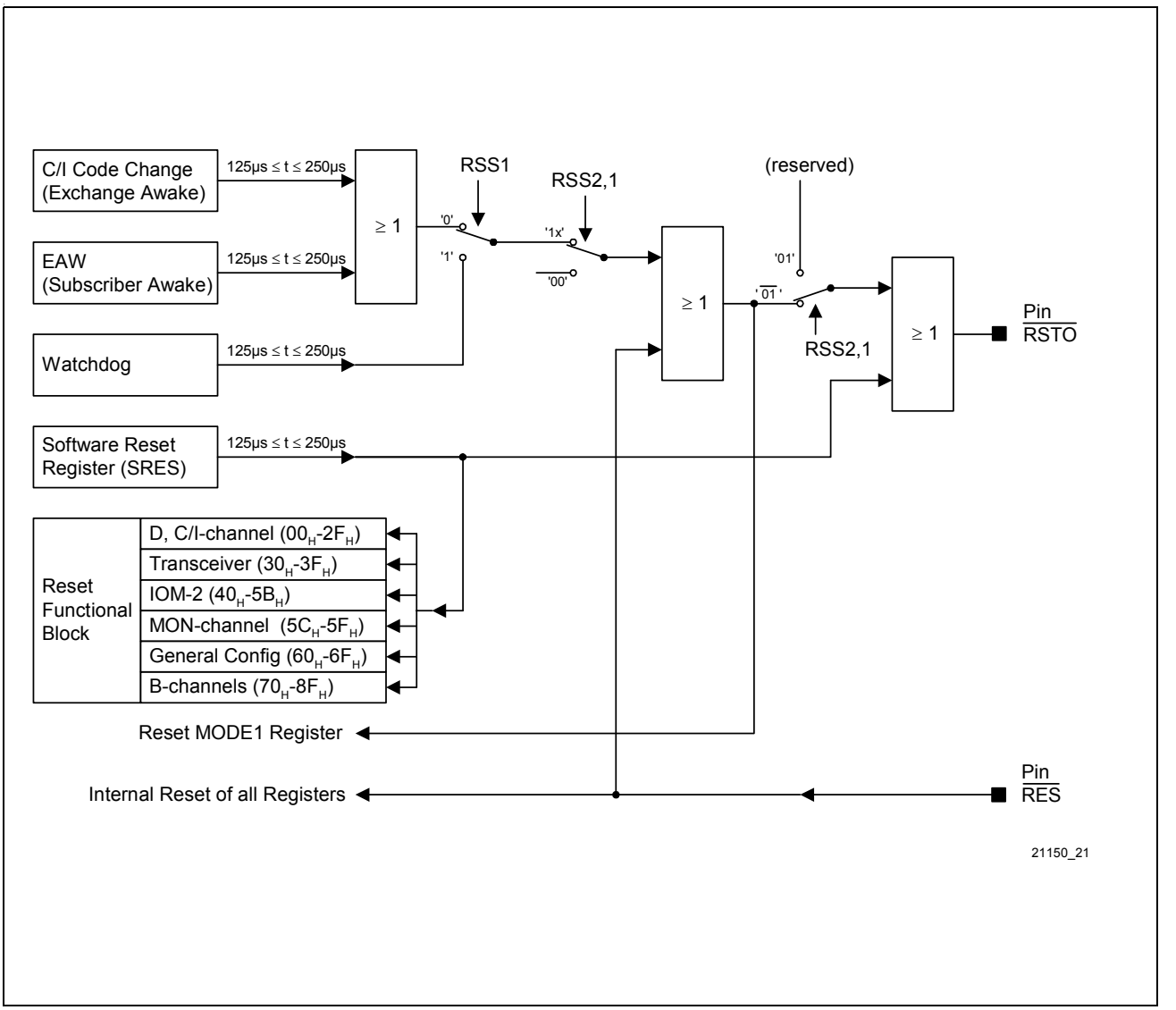



**Figure 12 Reset Generation**

#### Reset Source Selection

The internal reset sources C/I code change, $\overline{\text{EAW}}$ and Watchdog can be output at the low active reset pin $\overline{\text{RSTO}}$. The selection of these reset sources can be done with the RSS2,1 bits in the MODE1 register according **Table 6**.

The setting RSS2,1 = ’01’ is reserved for further use. In this case no reset is output at $\overline{\text{RSTO}}$. The internal reset sources sets the MODE1 register to its reset value.

**Table 6 Reset Source Selection**

| RSS2 Bit 1 | RSS1 Bit 0 | C/I Code Change | EAW | Watchdog Timer |
|---|---|---|---|---|
| 0 | 0 | -- | -- | -- |
| 0 | 1 | reserved | | |
| 1 | 0 | x | x | -- |
| 1 | 1 | -- | -- | x |

- **C/I Code Change (Exchange Awake)**
  A change in the downstream C/I channel (C/I0) generates an external reset pulse of 125 µs ≤ t ≤ 250 µs.
- **$\overline{\text{EAW}}$ (Subscriber Awake)**
  A low level on the $\overline{\text{EAW}}$ input starts the oscillator from the power down state and generates a reset pulse of 125 µs ≤ t ≤ 250 µs.
- Watchdog Timer

After the selection of the watchdog timer (RSS = ’11’) an internal timer is reset and started. During every time period of 128 ms the microcontroller has to program the WTC1- and WTC2 bits in the following sequence to reset and restart the watchdog timer:

| | WTC1 | WTC2 |
|---|---|---|
| 1. | 1 | 0 |
| 2. | 0 | 1 |

If not, the timer expires and a WOV-interrupt (ISTA Register) together with a reset pulse of 125 µs is generated.
Deactivation of the watchdog timer is only possible with a hardware reset.

### External Reset Input

At the $\overline{\text{RES}}$ input an external reset can be applied forcing the device in the reset state. This external reset signal is additionally fed to the $\overline{\text{RSTO}}$ output. The length of the reset signal is specified in **Chapter 5.9**.

After an external reset from the $\overline{\text{RES}}$ pin all registers of the device are set to its reset values (see register description in **Chapter 4**).

### Software Reset Register (SRES)

Every main functional block of the device can be reset separately by software setting the corresponding bit in the SRES register. A reset to external devices can also be controlled in this way. The reset state is activated by setting the corresponding bit to ’1’ and onchip

logic resets this bit again automatically after 4 BCL clock cycles. The address range of the registers which will be reset at each SRES bit is listed in **Figure 12**.

### 3.2.5 Timer Modes

The IPAC-X provides two timers which can be used for various purposes. Each of them provides two modes (**Table 7**), a count down timer interrupt, i.e. an interrupt is generated only once after expiration of the selected period, and a periodic timer interrupt, which means an interrupt is generated continuously after every expiration of that period.

**Table 7 IPAC-X Timers**

| Address | Register | Modes | Period |
|---|---|---|---|
| $24_H$ | TIMR1 | Periodic | 64 ... 2048 ms |
| | | Count Down | 64 ms ... 14.336 s |
| $65_H$ | TIMR2 | Periodic | 1 ... 63 ms |
| | | Count Down | 1 ... 63 ms |

When the programmed period has expired an interrupt is generated and indicated in the auxiliary interrupt status ISTA.AUX. The source of the interrupt can be read from AUXI (TIN1, TIN2) and each of the interrupt sources can be masked in AUXM.

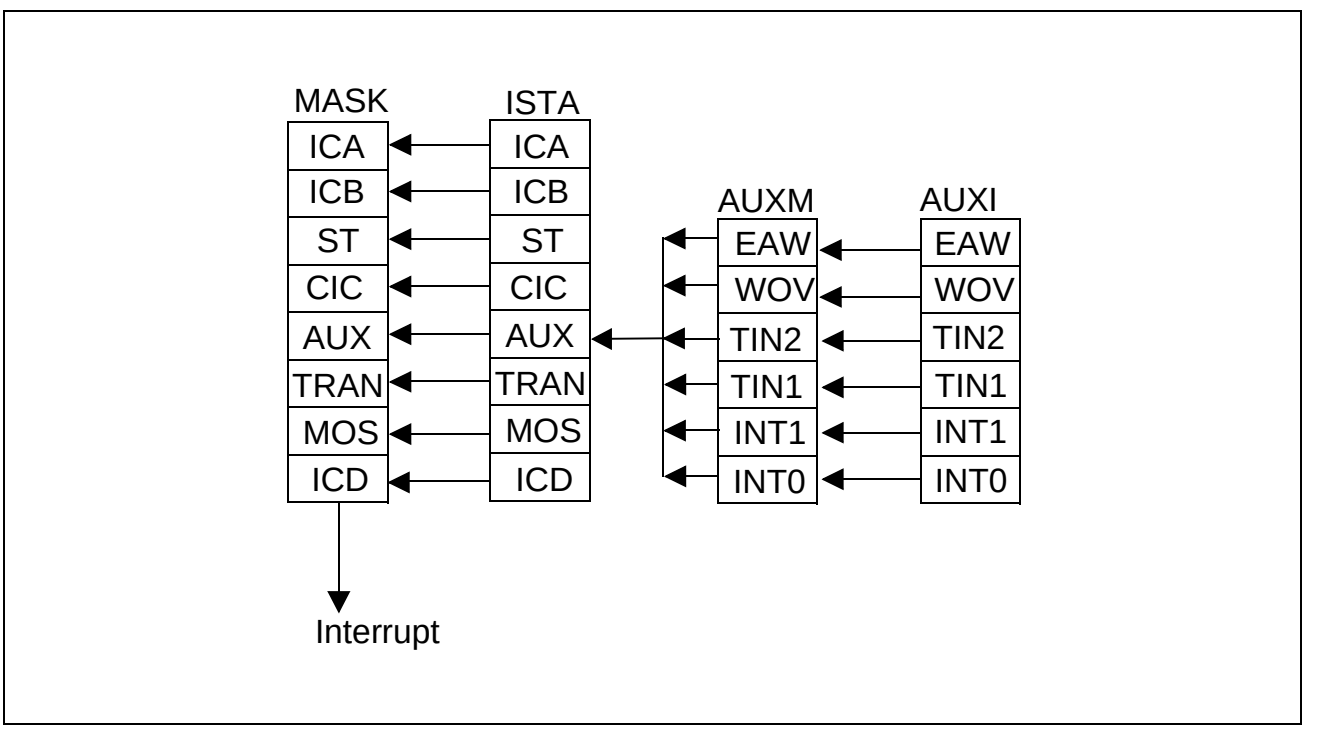



**Figure 13 Timer Interrupt Status Registers**

### Timer 1

The host controls the timer 1 by setting bit CMDRD.STI to start the timer and by writing register TIMR1 to stop the timer. After time period T1 an interrupt (AUXI.TIN1) is generated continuously if CNT=7 or a single interrupt is generated after timer period T if CNT<7 (**Figure 14**).

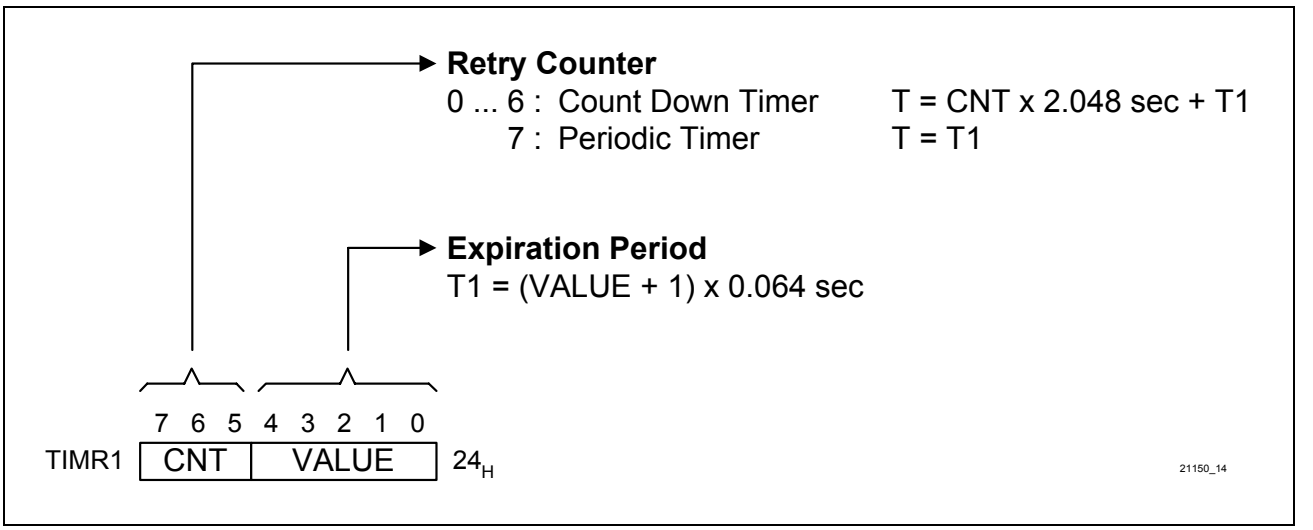



**Figure 14 Timer 1 Register**

### Timer 2

The host starts and stops timer 2 in TIMR2.CNT (**Figure 15**). If TIMR2.TMD=0 the timer is operating in count down mode, for TIMR2.TMD=1 a periodic interrupt AUXI.TIN2 is generated. The timer length (for count down timer) or the timer period (for periodic timer), respectively, can be configured to a value between 1 - 63 ms (TIMR2.CNT).

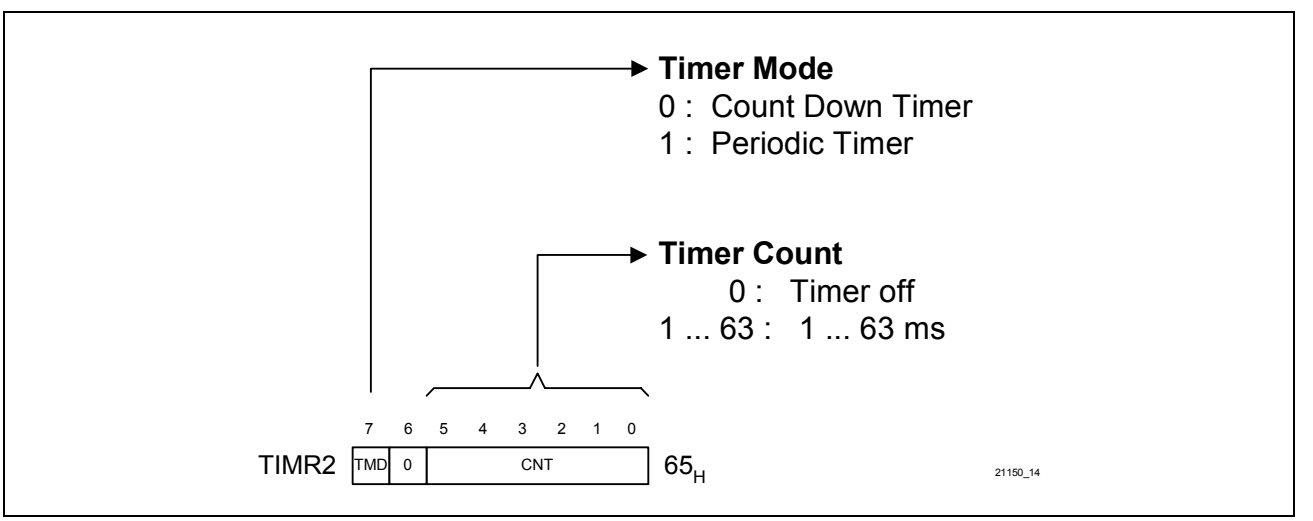



**Figure 15 Timer 2 Register**

### 3.2.6 Activation Indication via Pin ACL

The activated state of the S-interface is directly indicated via pin $\overline{\text{ACL}}$ (Activation LED). An LED with pre-resistance may directly be connected to this pin and a low level is driven on $\overline{\text{ACL}}$ as soon as the layer 1 state machine reaches the activated state (see **Figure 16**).

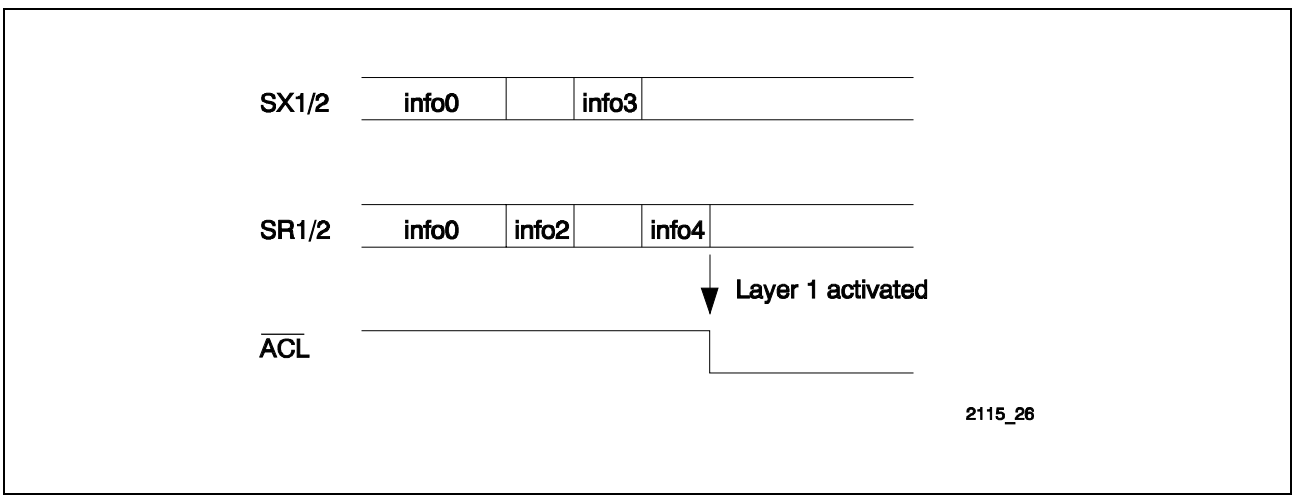



**Figure 16 ACL Indication of Activated Layer 1**

By default (ACFG2.ACL=0) the state of layer 1 is indicated at pin $\overline{\text{ACL}}$. If the automatic indication of the activated layer 1 is not required, the state on pin $\overline{\text{ACL}}$ can also be controlled by the host (see **Figure 17**).
If ACFG2.ACL=1 the LED on pin $\overline{\text{ACL}}$ can be switched on (ACFG2.LED=1) and off (ACFG2.LED=0) by the host.

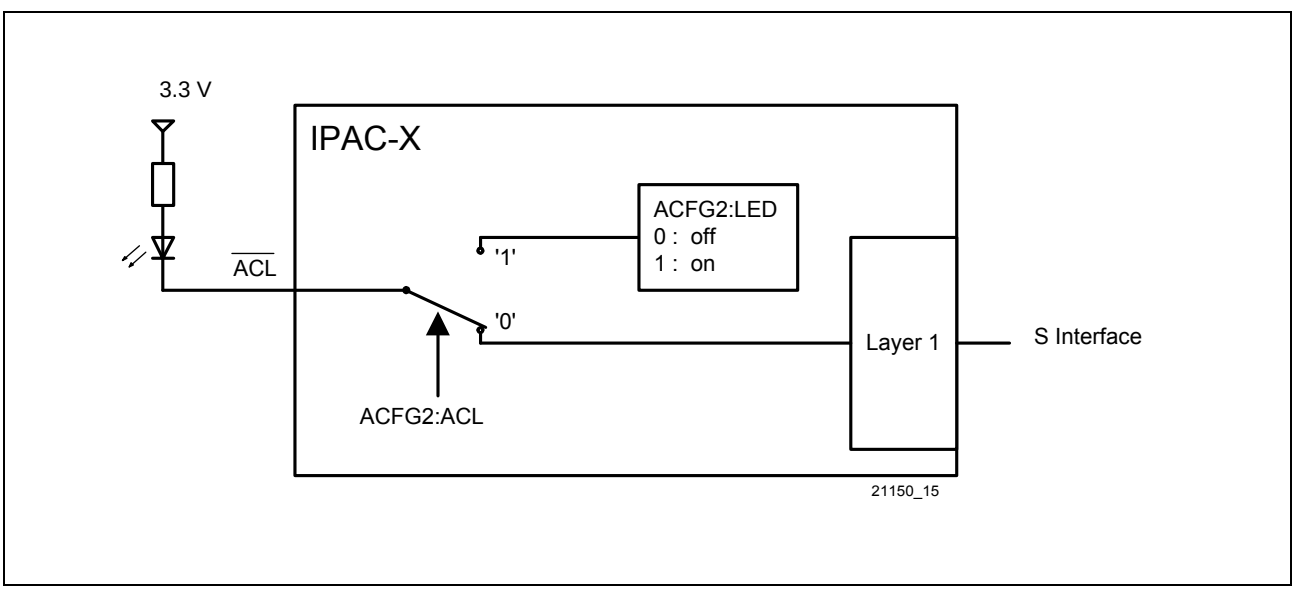



**Figure 17 ACL Configuration**

## 3.3 S/T-Interface

The layer-1 functions for the S/T interface of the IPAC-X are:

- Line transceiver functions for the S/T interface according to the electrical specifications of ITU-T I.430;
- Conversion of the frame structure between IOM-2 and S/T interface;
- Conversion from/to binary to/from pseudo-ternary code;
- Level detection
- Receive timing recovery for point-topoint, passive bus and extended passive bus configuration
- S/T timing generation using IOM-2 timing synchronous to system, or vice versa;
- D-channel access control and priority handling;
- D-channel echo bit generation by handling of the global echo bit;
- Activation/deactivation procedures, triggered by primitives received over the IOM-2 C/I channel or by INFO's received from the line;
- Execution of test loops.

The wiring configurations in user premises, in which the IPAC-X can be used, are illustrated in **Figure 18**.

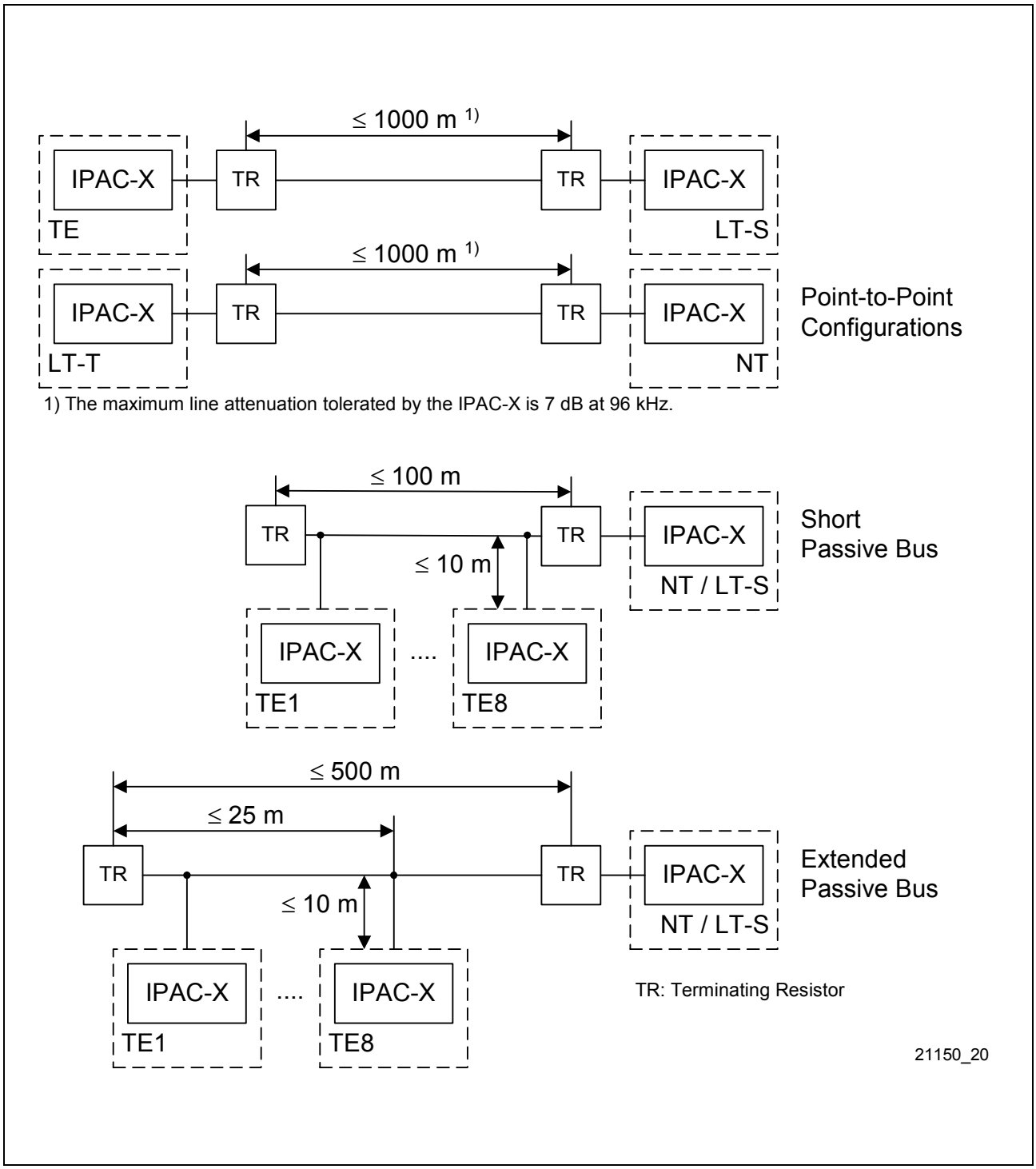



**Figure 18 Wiring Configurations in User Premises**

### 3.3.1 S/T-Interface Coding

Transmission over the S/T-interface is performed at a rate of 192 kbit/s. 144 kbit/s are used for user data (B1+B2+D), 48 kbit/s are used for framing and maintenance information.

#### Line Coding

The following figure illustrates the line code. A binary ONE is represented by no line signal. Binary ZEROs are coded with alternating positive and negative pulses with two exceptions:
For the required frame structure a code violation is indicated by two consecutive pulses of the same polarity. These two pulses can be adjacent or separated by binary ONEs.
In bus configurations a binary ZERO always overwrites a binary ONE.

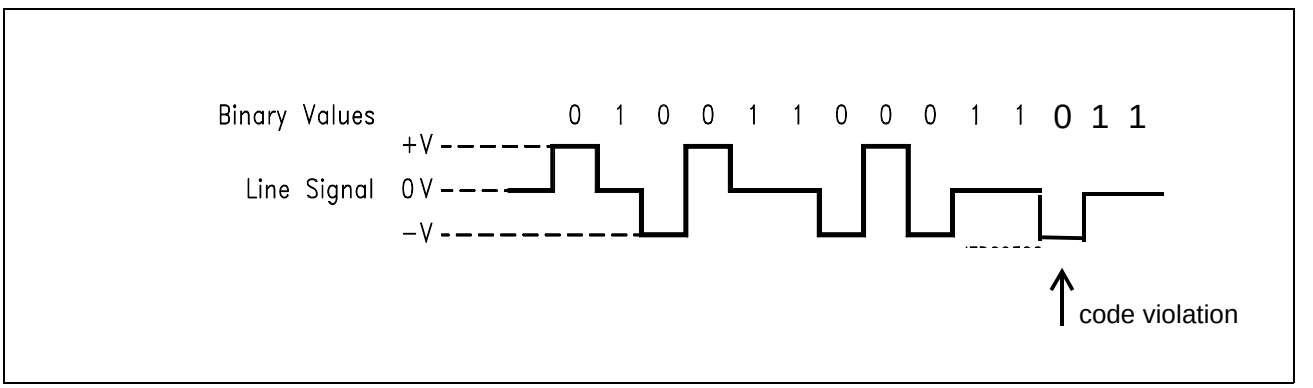



**Figure 19 S/T -Interface Line Code**

#### Frame Structure

Each S/T frame consists of 48 bits at a nominal bit rate of 192 kbit/s. For user data (B1+B2+D) the frame structure applies to a data rate of 144 kbit/s (see **Figure 20**).
In the direction TE → NT the frame is transmitted with a two bit offset. For details on the framing rules please refer to ITU I.430 section 6.3. The following figure illustrates the standard frame structure for both directions (NT → TE and TE → NT) with all framing and maintenance bits.

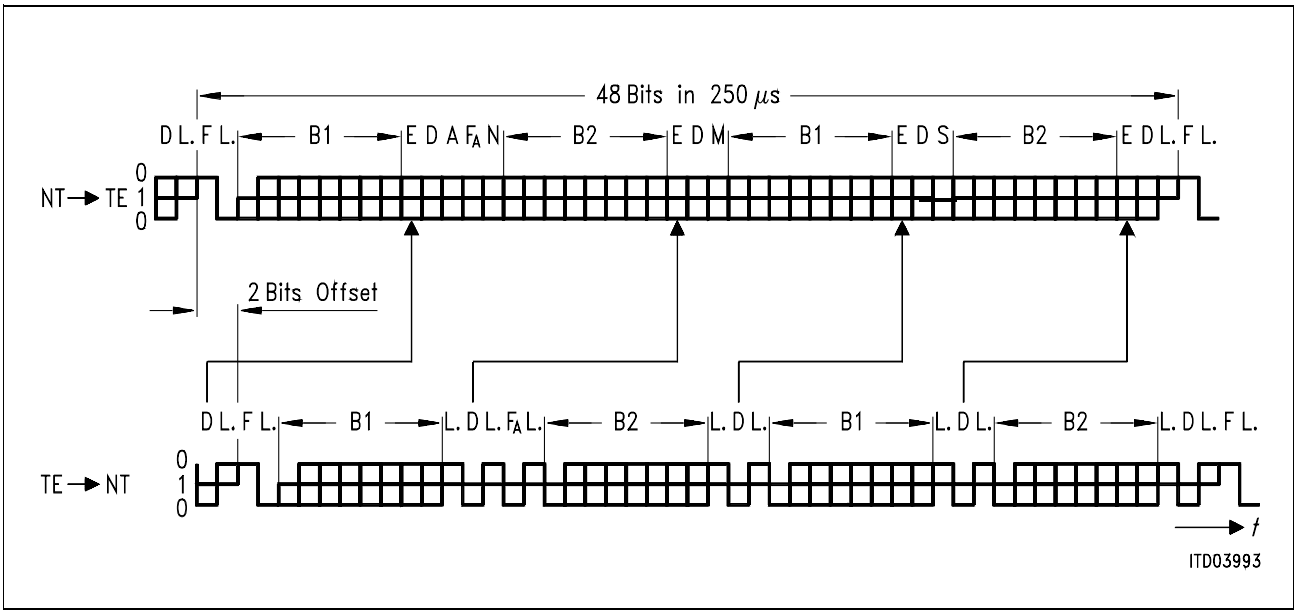



**Figure 20 Frame Structure at Reference Points S and T (ITU I.430)**

| | | |
|---|---|---|
| – F | Framing Bit | F = (0b) → identifies new frame (always positive pulse, always code violation) |
| – L. | D.C. Balancing Bit | L. = (0b) → number of binary ZEROs sent after the last L. bit was odd |
| – D | D-Channel Data Bit | Signaling data specified by user |
| – E | D-Channel Echo Bit | E = D → received E-bit is equal to transmitted D-bit |
| – $F_A$ | Auxiliary Framing Bit | See section 6.3 in ITU I.430 |
| – N | | N = $\overline{F_A}$ |
| – B1 | B1-Channel Data Bit | User data |
| – B2 | B2-Channel Data Bit | User data |
| – A | Activation Bit | A = (0b) → INFO 2 transmitted<br>A = (1b) → INFO 4 transmitted |
| – S | S-Channel Data Bit | $S_1$ channel data (see note below) |
| – M | Multiframing Bit | M = (1b) → Start of new multi-frame |

*Note: The ITU I.430 standard specifies S1 - S5 for optional use.*

### 3.3.2 S/T-Interface Multiframing

According to ITU recommendation I.430 a multi-frame provides extra layer 1 capacity in the TE-to-NT direction by using an extra channel between the TE and NT (Q-channel). The Q bits are defined to be the bits in the $F_A$ bit position.

In the NT-to-TE direction the S-channel bits are used for information transmission. One S channel (S1) out of five possible S-channels can be accessed by the IPAC-X.

In the NT-to-TE direction the S-channel bits are used for information transmission.

The S and Q channels are accessed via the µC interface or the IOM-2 MONITOR channel, respectively, by reading/writing the SQR or SQX bits in the S/Q channel registers (SQRRx, SQXRx).

**Table 8** shows the S and Q bit positions within the multi-frame.

**Table 8 S/Q-Bit Position Identification and Multi-Frame Structure**

| Frame Number | NT-to-TE $F_A$ Bit Position | NT-to-TE M Bit | NT-to-TE S Bit | TE-to-NT $F_A$ Bit Position |
|---|---|---|---|---|
| 1 | ONE | ONE | S11 | Q1 |
| 2 | ZERO | ZERO | S21 | ZERO |
| 3 | ZERO | ZERO | S31 | ZERO |
| 4 | ZERO | ZERO | S41 | ZERO |
| 5 | ZERO | ZERO | S51 | ZERO |
| 6 | ONE | ZERO | S12 | Q2 |
| 7 | ZERO | ZERO | S22 | ZERO |
| 8 | ZERO | ZERO | S32 | ZERO |
| 9 | ZERO | ZERO | S42 | ZERO |
| 10 | ZERO | ZERO | S52 | ZERO |
| 11 | ONE | ZERO | S13 | Q3 |
| 12 | ZERO | ZERO | S23 | ZERO |
| 13 | ZERO | ZERO | S33 | ZERO |
| 14 | ZERO | ZERO | S43 | ZERO |
| 15 | ZERO | ZERO | S53 | ZERO |
| 16 | ONE | ZERO | S14 | Q4 |
| 17 | ZERO | ZERO | S24 | ZERO |
| 18 | ZERO | ZERO | S34 | ZERO |
| 19 | ZERO | ZERO | S44 | ZERO |
| 20 | ZERO | ZERO | S54 | ZERO |
| 1 | ONE | ONE | S11 | Q1 |
| 2 | ZERO | ZERO | S21 | ZERO |

### TE Mode

After multi-frame synchronization has been established, the Q data will be inserted at the upstream (TE → NT) $F_A$ bit position in each 5th S/T frame (see **Table 8**).
When synchronization is not achieved or lost, each received $F_A$ bit is mirrored to the next transmitted $F_A$ bit.
Multi-frame synchronization is achieved after two complete multi-frames have been detected with reference to $F_A$/N bit and M bit positions. Multi-frame synchronization is lost if bit errors in $F_A$/N bit or M bit positions have been detected in two consecutive multi-frames. The synchronization state is indicated by the MSYN bit in the S/Q-channel receive register (SQRR1).
The multi-frame synchronization can be enabled or disabled by programming the MFEN bit in the S/Q-channel transmit register (SQXR1).

### NT Mode

The transceiver in NT mode starts multiframing if SQXR1.MFEN is set.

After multi-frame synchronization has been established in the TE, the Q data will be inserted at the upstream (TE → NT) $F_A$ bit position by the TE in each 5th S/T frame, the S data will be inserted at the downstream (NT → TE) S bit position in each S/T frame (see **Table 8**).

### Interrupt Handling for Multi-Framing

To trigger the microcontroller for a multi-frame access an interrupt can be generated once per multi-frame (SQW) or if the received S-channels (TE) or Q-channel (NT) have changed (SQC).
In both cases the microcontroller has access to the multiframe within the duration of one multiframe (5 ms).

### 3.3.3 Multiframe Synchronization (M-Bit)

The IPAC-X offers the capability to control the start of the multiframe from external signals, so applications which require synchronization between different S-interfaces are possible. Such an application is the connection of DECT base stations to PBX line cards.

For this purpose a multiplexed function of the AUX4 pin is used. If the ACFG2.A4SEL is set to “1” the pin is not used as general pupose I/O pin but as M-bit input (NT, LT-S) or as M-Bit output (TE, LT-T). The direction input/output of the pin MBIT is automatically selected with the operation mode.

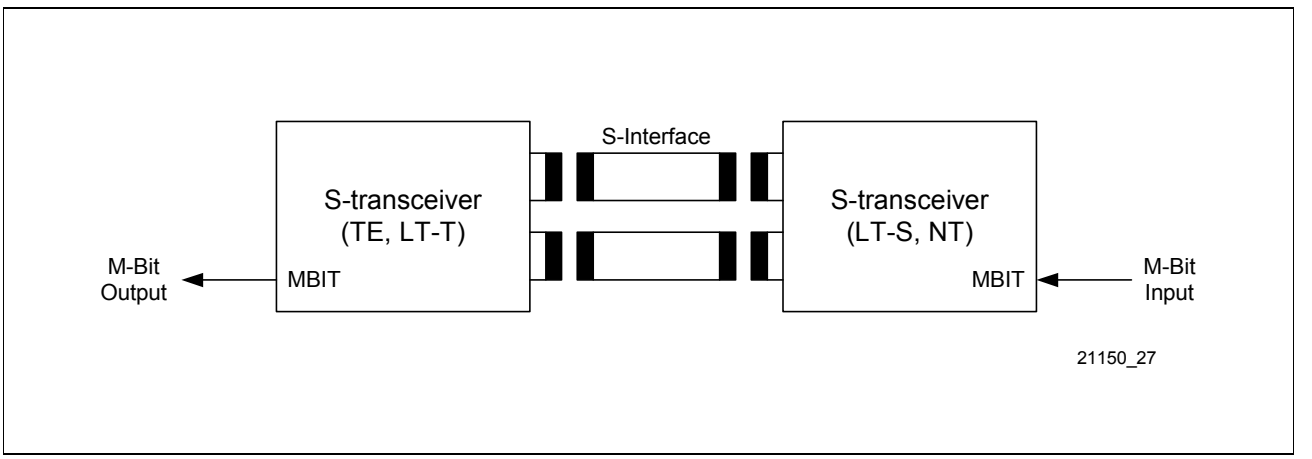



**Figure 21 Multiframe Synchronization using the M-Bit**

#### M-Bit Input (LT-S, NT-Mode)

The MBIT pin can be used to synchronize the multiframe structure between several S-transceivers. Multiframe generation must be enabled (SQXR1.MFEN=1).

The value of MBIT is sampled at the start of the F-bit of the S-frame.

If the input on MBIT is "1", the multiframe counter is reset to frame no. 20 and as a result, the bits $F_A$, M and S are transmitted as logic ZERO (line = “1”). If MBIT becomes "0" again, the multiframe counter counts 20 frames (starting with frame no. 1) and begins again autonomously.

If MBIT is kept "1", the multiframe counter is permanently reset and the bits $F_A$, M and S stay at logic ZERO (line = “1”). If MBIT becomes "0" for only one S-frame, the multiframe-counter reaches frame no. 1 at which a logic ONE (line = “0”) is transmitted in the $F_A$ and M-bit position and the S11 bit is transmitted.

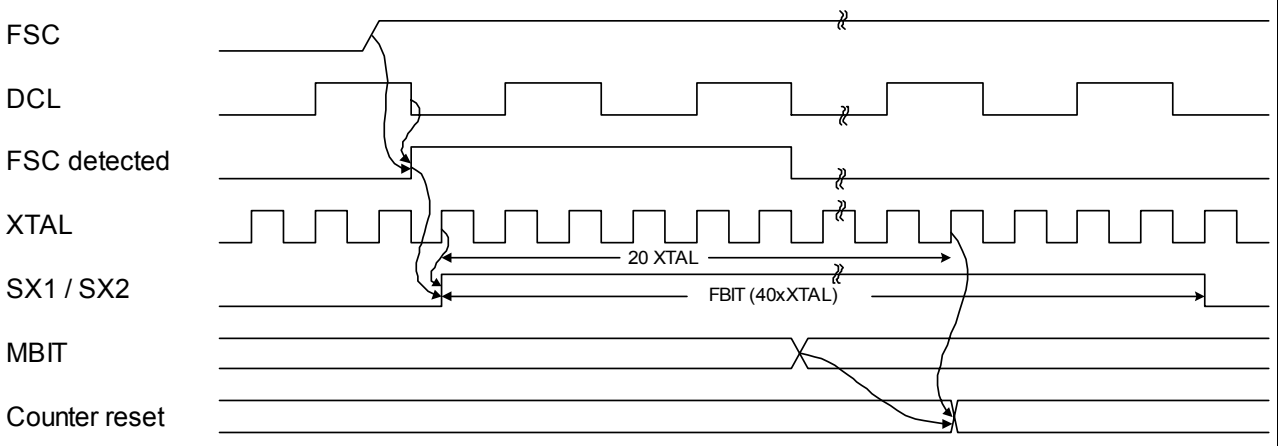
Thus, the M-bit can be used to transfer synchronization pulses of any length between different S-interfaces.

#### M-Bit Output (TE, LT-T Mode)

In TE and LT-T mode, the IPAC-X outputs the value of the M-bit on the MBIT pin.

The value of M should be sampled at the falling edge of FSC.

## Sample Time




The sample time of the MBIT input is related to the rising edge of FSC at the beginning of an S0 frame
-- min: 20 * 1 / xtal
-- max: 20 * 1 / xtal + 1 / xtal + 1 / dcl

**Figure 22 Sampling Time in LT-S / NT Mode (M-Bit input)**

## Frame Relationship

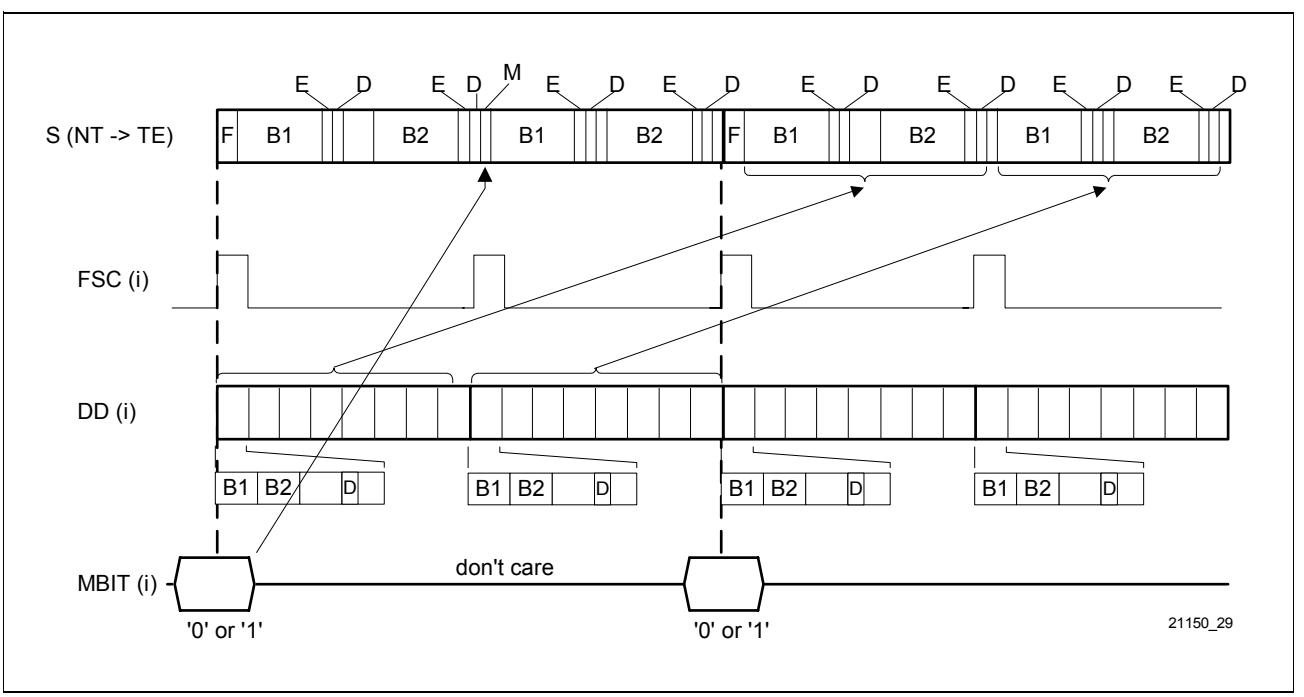



**Figure 23 Frame Relationship in LT-S / NT Mode (M-Bit input)**

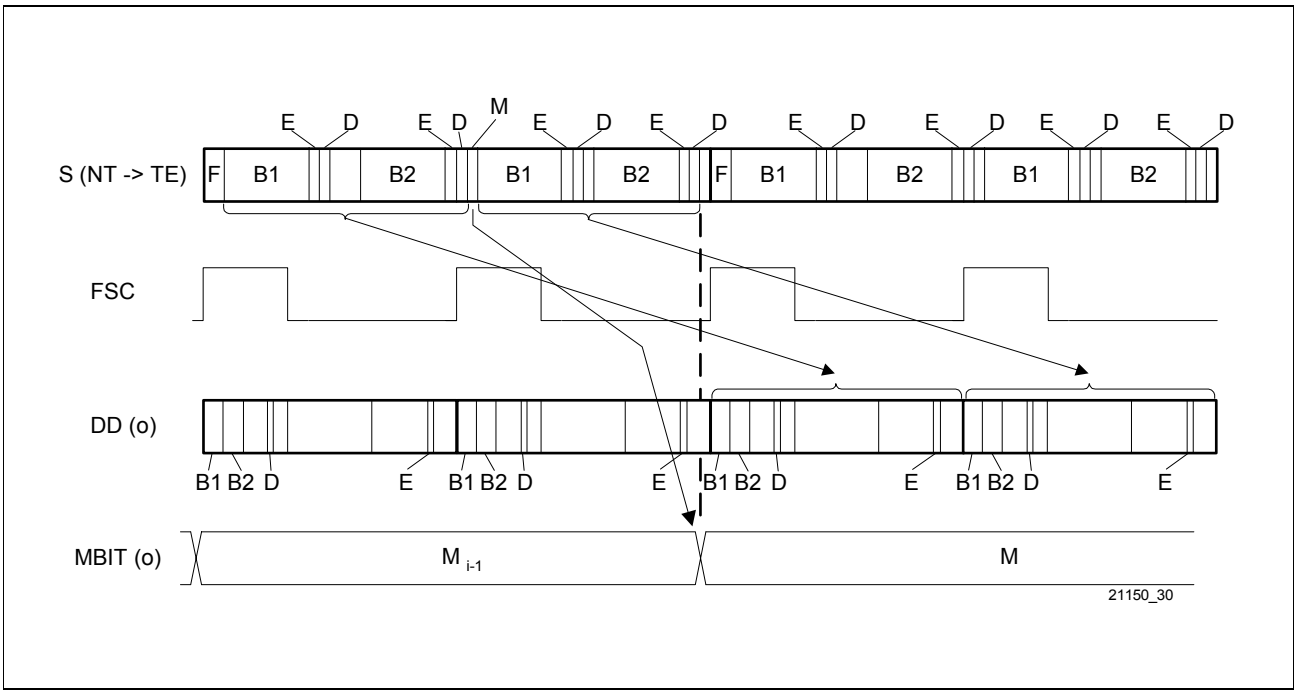



**Figure 24 Frame Relationship in TE / LT-T Mode (M-Bit output)**

### 3.3.4 Data Transfer and Delay between IOM-2 and S/T

**TE Mode**

In the state F7 (Activated) or if the internal layer-1 state machine is disabled and XINF of register TR_CMD is programmed to ’011’ the B1, B2, D and E bits are transferred transparently from the S/T to the IOM-2 interface. In all other states ’1’s are transmitted to the IOM-2 interface.

To transfer data transparently to the S/T interface any activation request C/I command (AR8, AR10 or ARL) is additionally necessary or if the internal layer-1 statemachine is disabled, bit TDDIS of register TR_CMD has additionally to be programmed to ’0’.

**Figure 25** shows the data delay between the IOM-2 and the S/T interface and vice versa.

For the D channel the delay from the IOM-2 to the S/T interface is only valid if S/G evaluation is disabled (MODED:DIM0=0). If S/G evaluation is enabled (MODED.DIM2-0=0x1) the delay depends on the selected priority and the relation between the echo bits on S and the D channel bits on the IOM-2, e.g. for priority 8 the timing relation between the 8th D-bit on S bus and the D-channel on IOM-2.

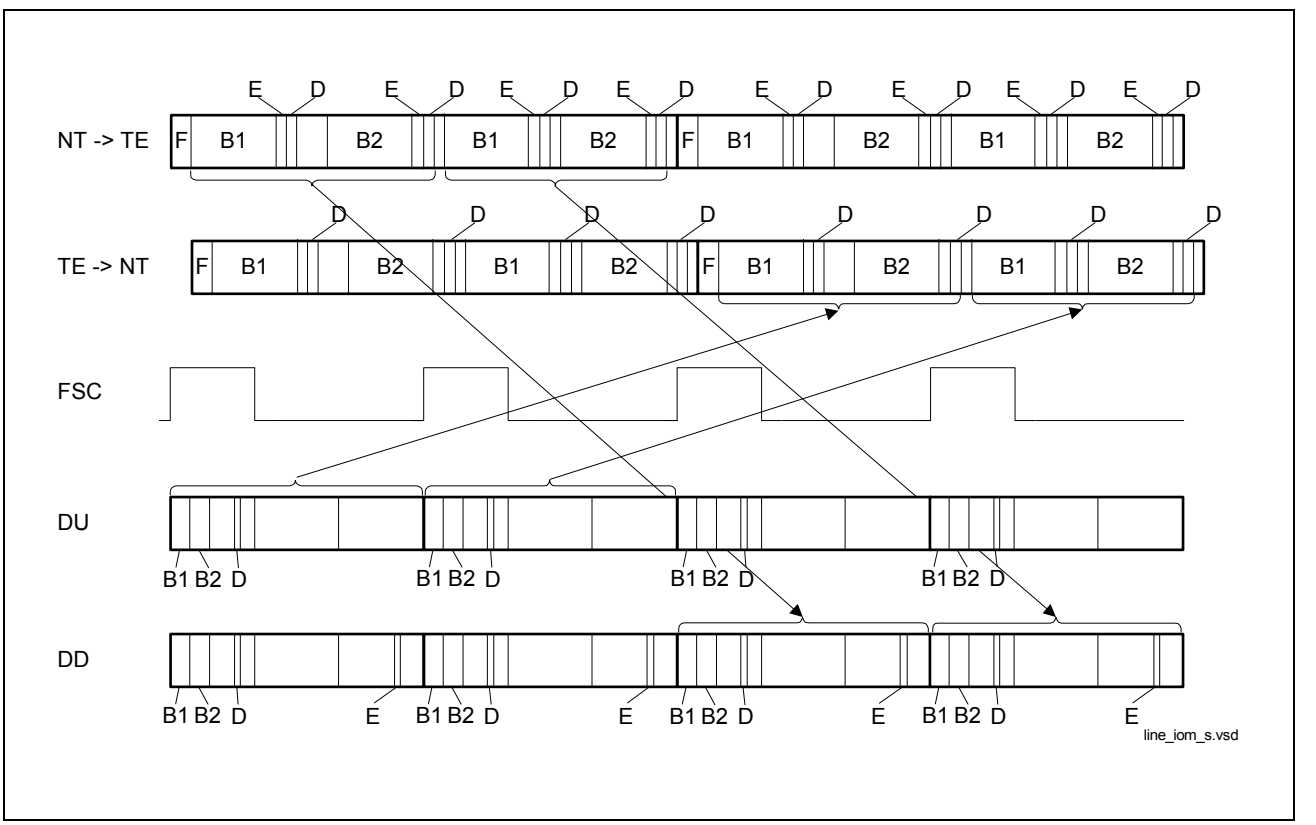



**Figure 25 Data Delay Between IOM-2 and S/T Interface Transparent Mode (TE mode only)**

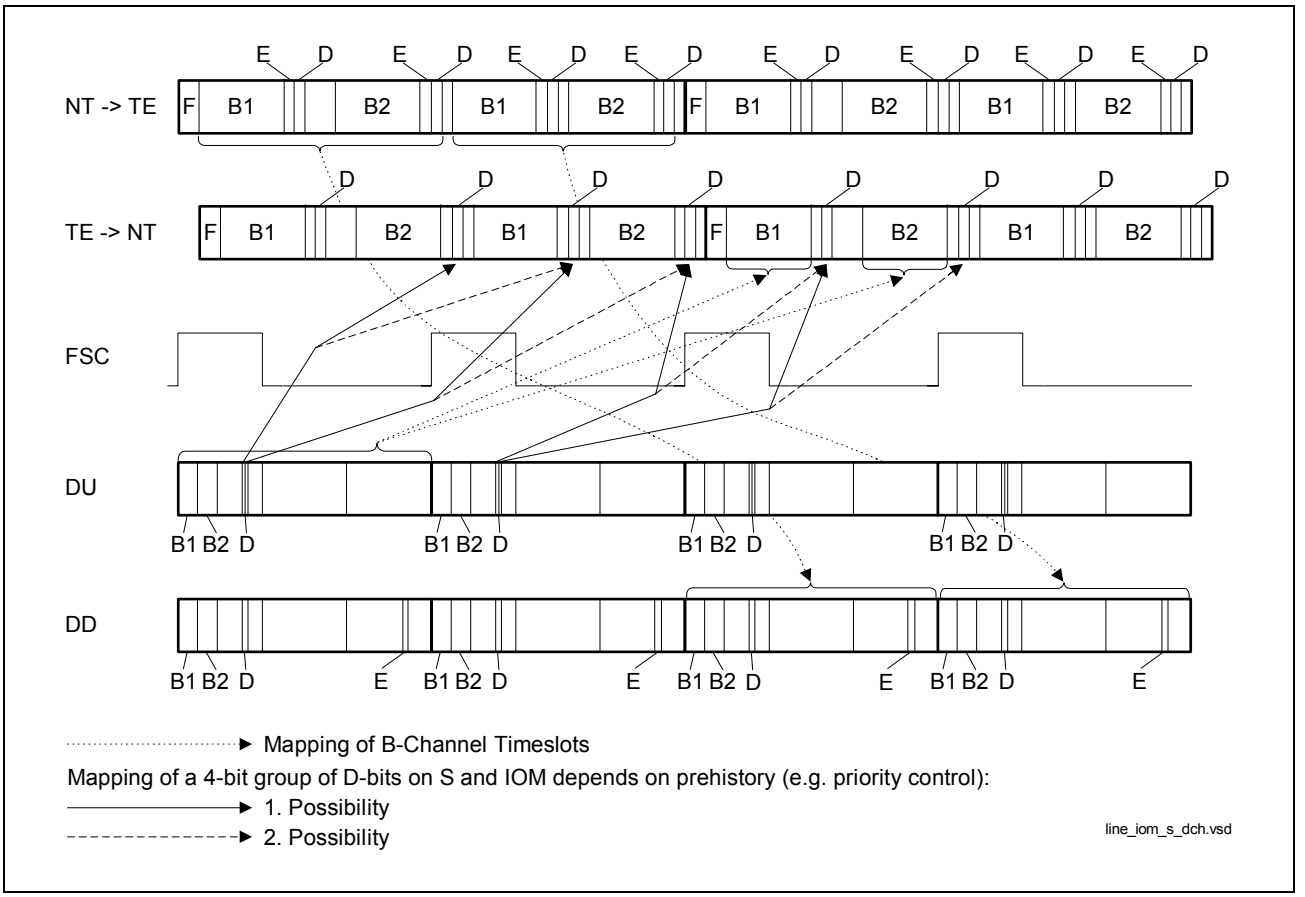



**Figure 26 Data Delay Between IOM-2 and S/T Interface With S/G Bit Evaluation (TE mode only)**

### LT-T Mode

In this mode the frame relation between S/T interface and IOM-2 is flexible.

### LT-S/NT Mode

In the state F7 (Activated) or if the internal layer-1 statemachine is disabled and XINF of register TR_CMD is programmed to ’011’ the B1, B2 and D bits are transferred transparently from the S/T to the IOM-2 interface. In all other states ’1’s are transmitted to the IOM-2 interface.

*Note: In intelligent NT the D-channel access can be blocked by the IOM-2 D-channel handler.*

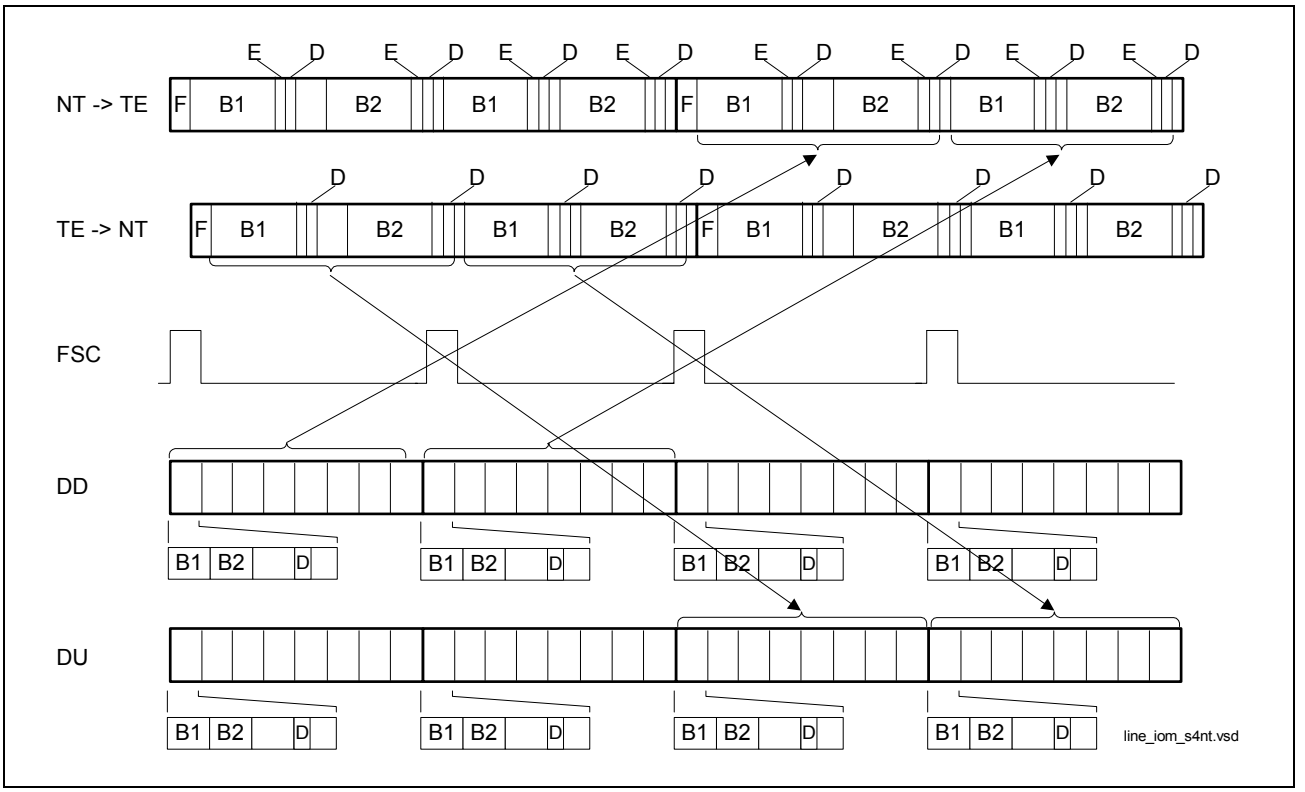



**Figure 27 Data Delay Between IOM-2 and S/T Interface With 8 IOM Channels (LT-S/NT mode only)**

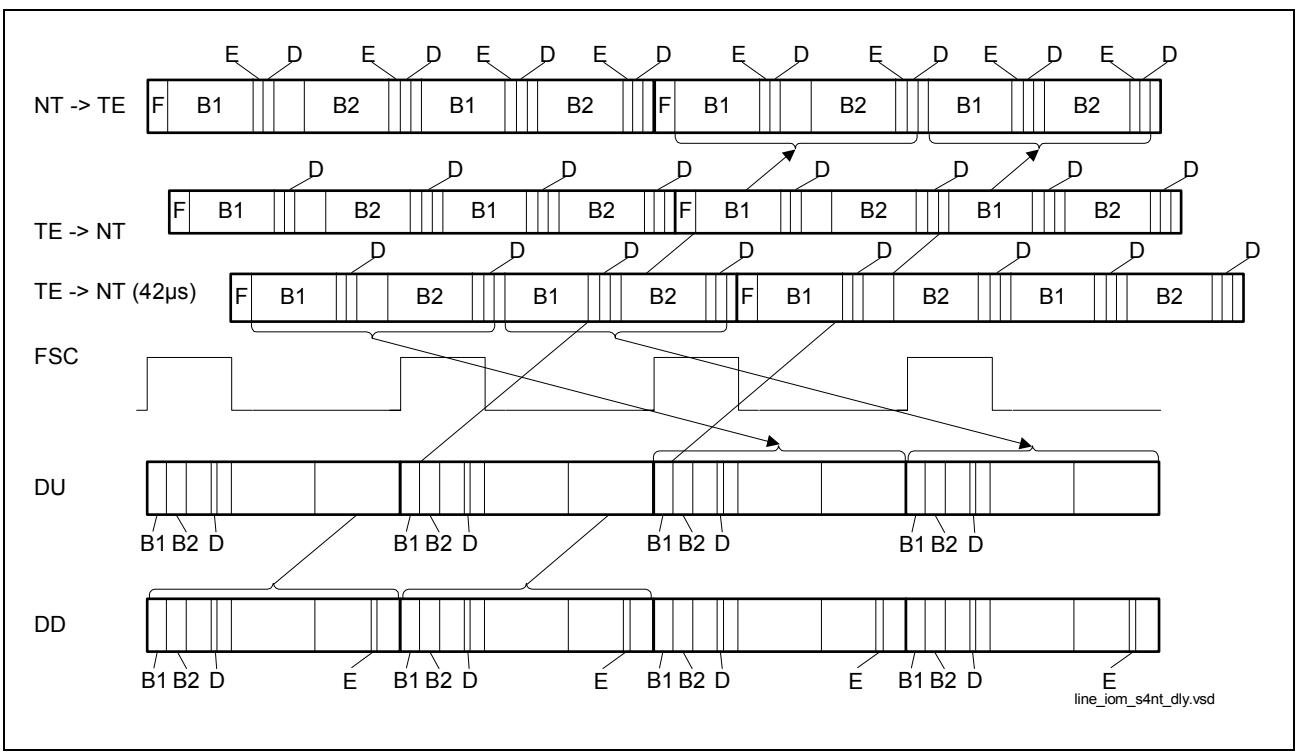



**Figure 28 Data Delay Between IOM-2 and S/T Interface With 3 IOM Channels and Maximum Receive Delay(LT-S/NT mode only)**

### 3.3.5 Transmitter Characteristics

The full-bauded pseudo-ternary pulse shaping is achieved with the integrated transmitter which is realized as a symmetrical current limited voltage source ($V_{SX1/SX2}$ = +/-1.0 V; $I_{max}$ = 26 mA). The equivalent circuit of the transmitter is shown in **Figure 29**.
The nominal pulse amplitude on the S-interface 750 mV (zero-peak) is adjusted with external resistors (see **Chapter 3.3.7.1**).

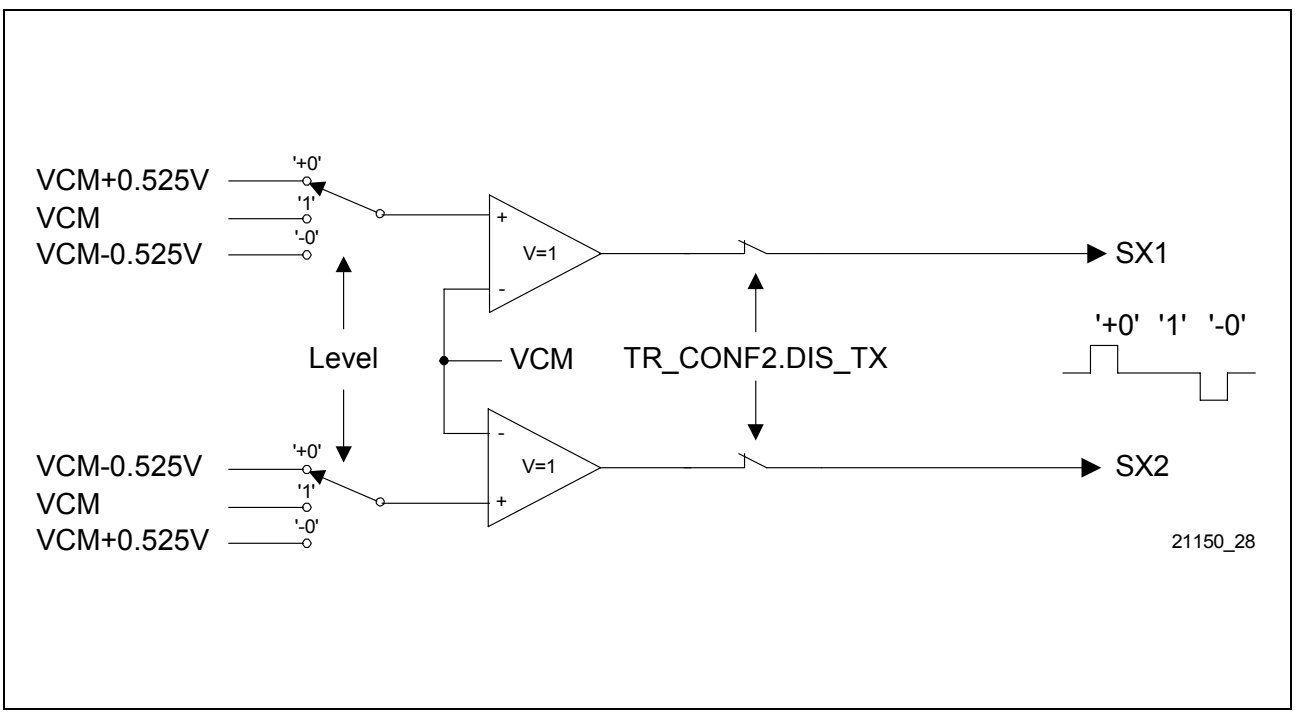



**Figure 29 Equivalent Internal Circuit of the Transmitter Stage**

### 3.3.6 Receiver Characteristics

The receiver consists of a differential input stage, a peak detector and a set of comparators. Additional noise immunity is achieved by digital oversampling after the comparators. A simplified equivalent circuit of the receiver is shown in **Figure 30**.

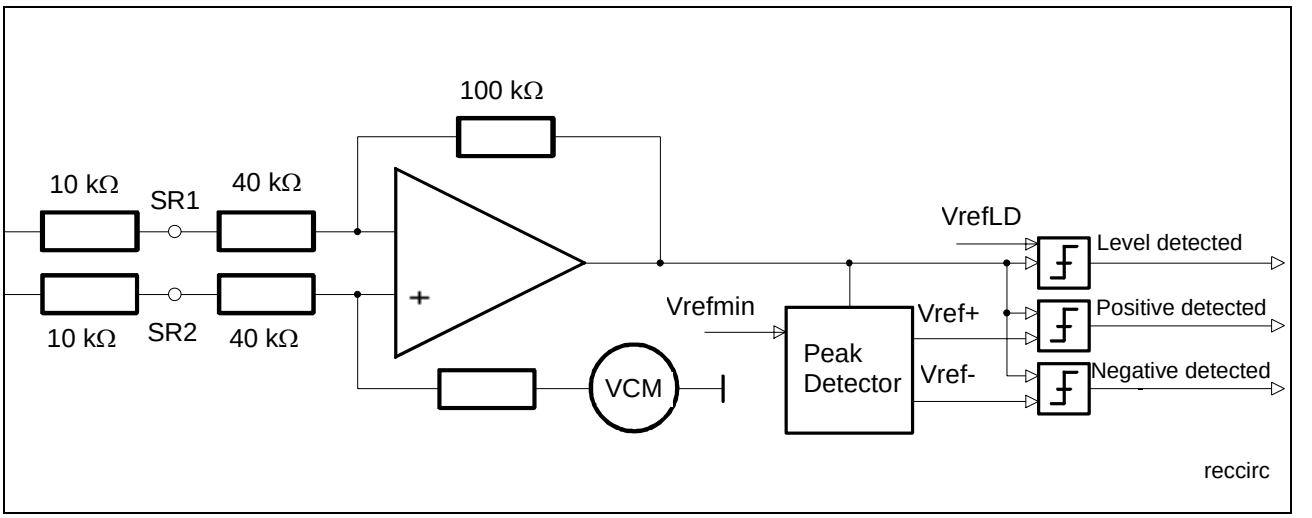



**Figure 30 Equivalent Internal Circuit of the Receiver Stage**

The input stage works together with external 10 kΩ resistors to match the input voltage to the internal thresholds. The data detection threshold Vref is continiously adapted between a maximal (Vrefmax) and a minimal (Vrefmin) reference level related to the line level. The peak detector requires maximum 2 µs to reach the peak value while storing the peak level for at least 250 µs (RC > 1 ms).
The additional level detector for power up/down control works with a fixed thresholds VrefLD. The level detector monitors the line input signals to detect whether an INFO is present. When closing an analog loop it is therefore possible to indicate an incoming signal during activated loop.

### 3.3.7 S/T Interface Circuitry

For both the receive and transmit direction a 1:1 transformer is used to connect the IPAC-X transceiver to the 4 wire S/T interface. Typical transformer characteristics can be found in the chapter on electrical characteristics. The connections of the line transformers is shown in **Figure 31**.

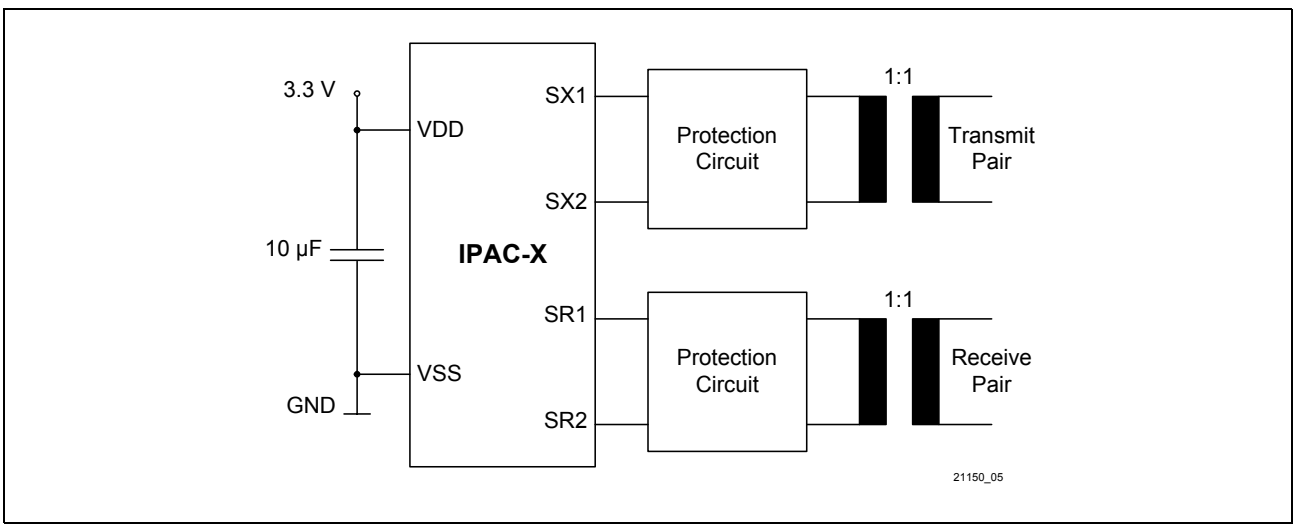



**Figure 31 Connection of Line Transformers and Power Supply to the IPAC-X**

For the transmit direction an external transformer is required to provide isolation and pulse shape according to the ITU-T recommendations.

#### 3.3.7.1 External Protection Circuitry

The ITU-T I.430 specification for both transmitter and receiver impedances in TEs results in a conflict with respect to external S-protection circuitry requirements:

– To avoid destruction or malfunction of the S-device it is desirable to drain off even small overvoltages reliably.
– To meet the 96 kHz impedance test specified for transmitters and receivers (for TEs only, ITU-T I.430 sections 8.5.1.2a and 8.6.1.1) the protection circuit must be dimensioned such that voltages below 1.2 V (ITU-T I.430 amplitude) x transformer ratio are not affected.

This requirement results from the fact that this test is also to be performed with no supply voltage being connected to the TE. Therefore the second reference point for overvoltages $V_{DD}$, is tied to GND. Then, if the amplitude of the 96 kHz test signal is greater than the combined forward voltages of the diodes, a current exceeding the specified one may pass the protection circuit.

The following recommendations aim at achieving the highest possible device protection against overvoltages while still fulfilling the 96 kHz impedance tests.

### Protection Circuit for Transmitter

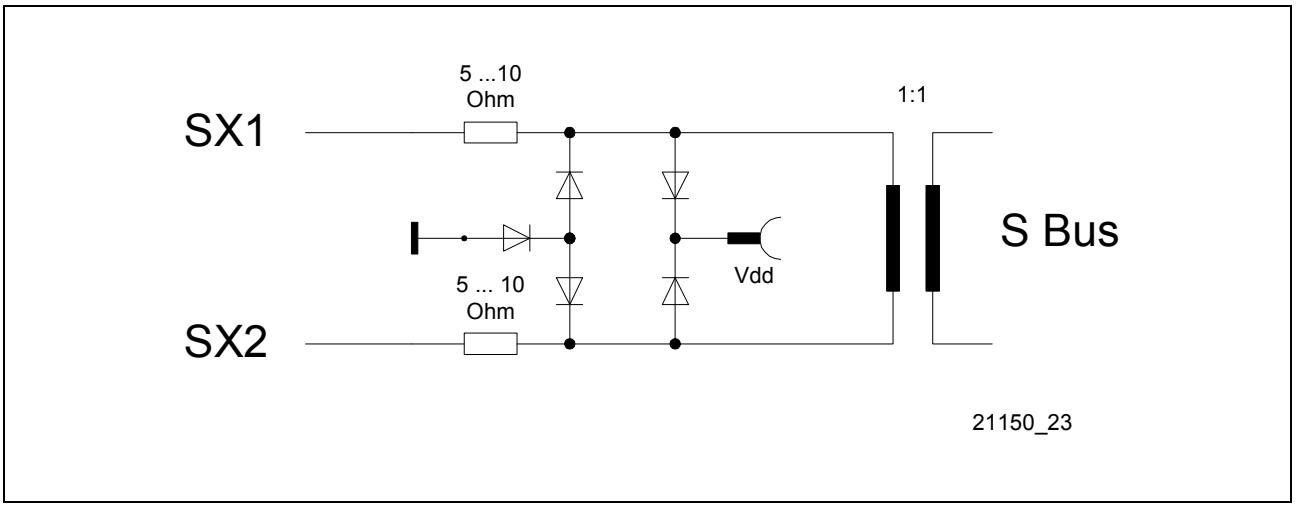



**Figure 32 External Circuitry for Transmitter**

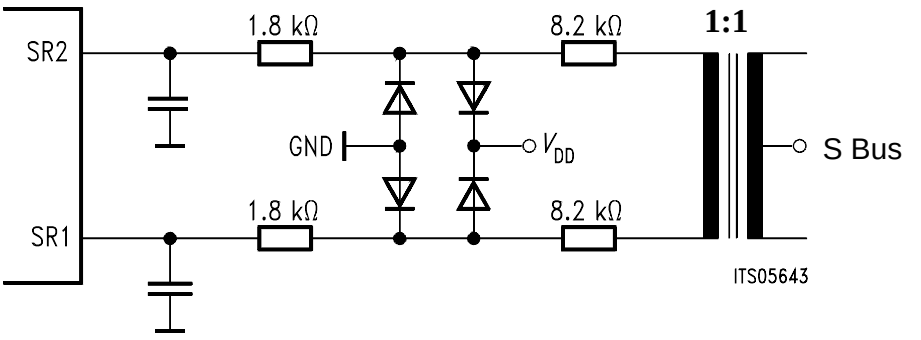
**Figure 32** illustrates the secondary protection circuit recommended for the transmitter.

The external resistors (5 ... 10 Ω) are required in order to adjust the output voltage to the pulse mask on the one hand and in order to meet the output impedance of minimum 20 Ω (transmission of a binary zero according to ITU-T I.430) on the other hand.
Two mutually reversed diode paths protect the device against positive or negative overvoltages on both lines.

An ideal protection circuit should limit the voltage at the SX pins from – 0.4 V to $V_{DD}$ + 0.4 V. With the circuit In **Figure 32** the pin voltage range is increased from – 0.7 V to $V_{DD}$ + 1.4 V. The resulting forward voltage of 1.4 V will prevent the protection circuit from becoming active if the 96 kHz test signal is applied while no supply voltage is present.

### Protection Circuit for Receiver

**Figure 33** illustrates the external circuitry used in combination with a symmetrical receiver. Protection of symmetrical receivers is rather simple.




Note: up to 10 pF capacitors are optional for noise reduction

**Figure 33 External Circuitry for Symmetrical Receivers**

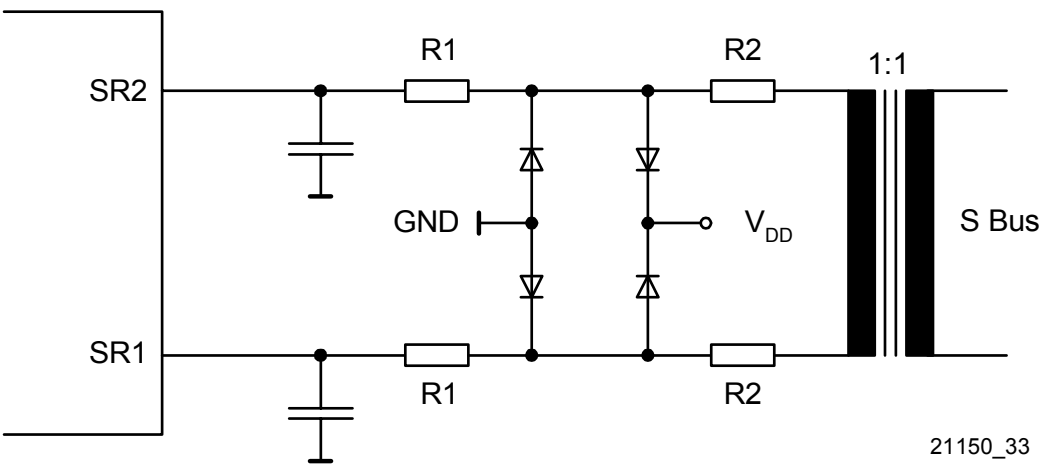
Between each receive line and the transformer a 10 kΩ resistor is used. This value is split into two resistors: one between transformer and protection diodes for current limiting during the 96 kHz test, and the second one between input pin and protection diodes to limit the maximum input current of the chip.

With symmetrical receivers no difficulties regarding LCL measurements are observed; compensation networks thus are obsolete.

In order to comply to the physical requirements of ITU-T recommendation I.430 and considering the national requirements concerning overvoltage protection and electromagnetic compatibility (EMC), the IPAC-X may need additional circuitry.

### 3.3.7.2 S-Transceiver Synchronization

Synchronization problems can occur on a S-Bus that is not terminated properly. Therefore, it is recommended to change the resistor values in the receive path. The sum of both resistors is increased from 10 kΩ (1.8 + 8.2) to e.g. 34 kΩ (6.8 + 27) for either receiver line. This change is possible but not necessary for a S-Bus that is terminated properly.




Note: Capacitors (up to 10 pF) are optional for noise reduction.

**Figure 34 External Circuitry for Symmetrical Receivers**

*Note: Lower or higher values than 34 kΩ may be used as well, however for values above 34 kΩ the additional delay must be compensated by setting TR_CONF2.PDS=1 (compensates 260 ns) so the allowed input phase delay is not violated.*

### 3.3.8 S/T Interface Delay Compensation (TE/LT-T Mode)

The S/T transmitter is shifted by two S/T bits minus 7 oscillator periods (plus analog delay plus delay of the external circuitry) with respect to the received frame. To compensate additional delay introduced into the receive and transmit path by the external circuit the delay of the transmit data can be reduced by another two oscillator periods (2 x 130 ns). Therefore PDS of the TR_CONF2 register must be programmed to ’1’. This delay compensation might be necessary in order to comply with the "total phase deviation input to output" requirement of ITU-T recommendation I.430 which specifies a phase deviation in the range of – 7% to + 15% of a bit period.

### 3.3.9 Level Detection Power Down

If MODE1.CFS is set to ’0’, the clocks are also provided in power down state, whereas if CFS is set to ’1’ only the analog level detector is active in power down state. All clocks, including the IOM-2 interface, are stopped (DD, DU are ’high’, DCL and BCL are ’low’).

An activation initiated from the exchange side will have the consequence that a clock signal is provided automatically if TR_CONF0.LDD is set to ’0’. If TR_CONF0.LDD is set to ’1’ the microcontroller has to take care of an interrupt caused by the level detect circuit (ISTATR.LD)

From the terminal side an activation must be started by setting and resetting the SPU-bit in the IOM_CR register and writing TIM to the CIX0 register or by resetting MODE1.CFS=0.

### 3.3.10 Transceiver Enable/Disable

The layer-1 part of the IPAC-X can be enabled/disabled by configuration (see **Figure 35**) with the two bits TR_CONF0.DIS_TR and TR_CONF2.DIS_TX .
By default all layer-1 functions with the exception of the transmitter buffer is enabled (DIS_TR = ’0’, DIS_TX = ’1’). With several terminals connected to the S/T interface, another terminal may keep the interface activated although the IPAC-X does not establish a connection. The receiver will monitor for incoming calls in this configuration. If the transceiver is disabled (DIS_TR = ’1’) all layer-1 functions are disabled including the level detection circuit of the receiver. In this case the power consumption of the Layer-1 is reduced to a minimum. The HDLC controller can still operate via IOM-2. The DCL and FSC pins become input.

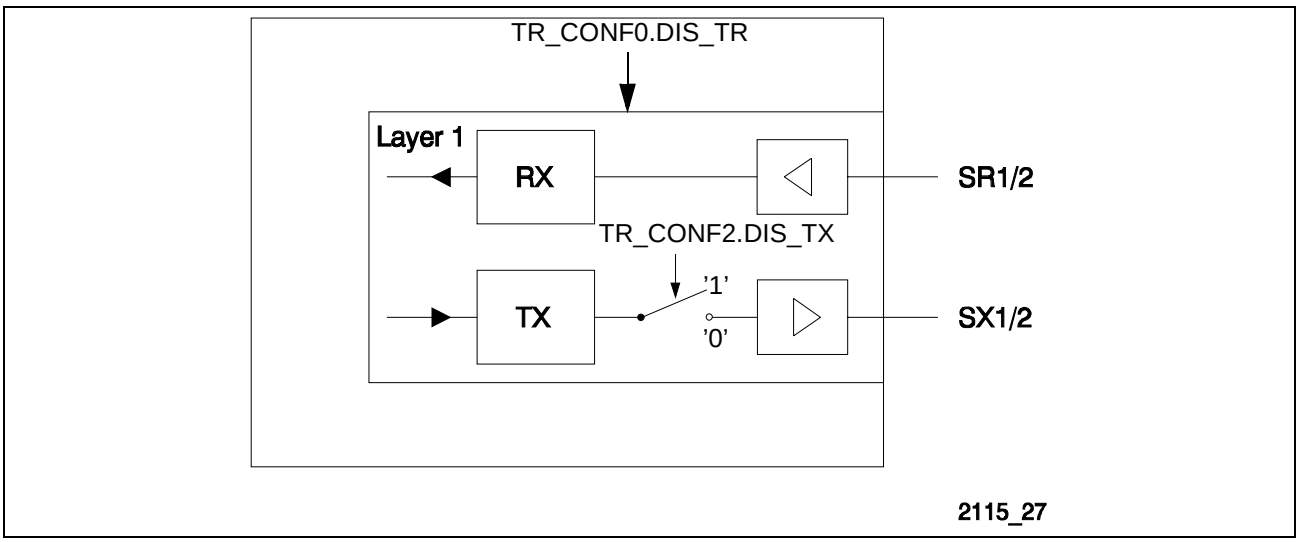



**Figure 35 Disabling of S/T Transmitter**

### 3.3.11 Test Functions

The IPAC-X provides test and diagnostic functions for the S/T interface:

*Note: For more details please refer to the application note “Test Function of new S-Transceiver family”*

– The **internal local loop** (internal Loop A) is activated by a C/I command ARL or by setting the bit LP_A (Loop Analog) in the TR_CMD register if the layer-1 statemachine

is disabled.
The transmit data of the transmitter is looped back internally to the receiver. The data of the IOM-2 input B- and D-channels are looped back to the output B- and D-channels.
The S/T interface level detector is enabled, i.e. if a level is detected this will be reported by the Resynchronization Indication (RSY) but the loop function is not affected.
Depending on the DIS_TX bit in the TR_CONF2 register the internal local loop can be transparent or non transparent to the S/T line.

– The **external local loop (external Loop A)** is activated in the same way as the internal local loop described above. Additionally the EXLP bit in the TR_CONF0 register has to be programmed and the loop has to be closed externally as described in **Figure 36**.
The S/T interface level detector is disabled.
This allows complete system diagnostics.
– In **remote line loop (RLP)** received data is looped back to the S/T interface. The D-channel information received from the line card is transparently forwarded to the output IOM-2 D-channel. The output B-channel information on IOM-2 is fixed to 'FF'$_H$ while this test loop is active. The remote loop is programmable in TR_CONF2.RLP.

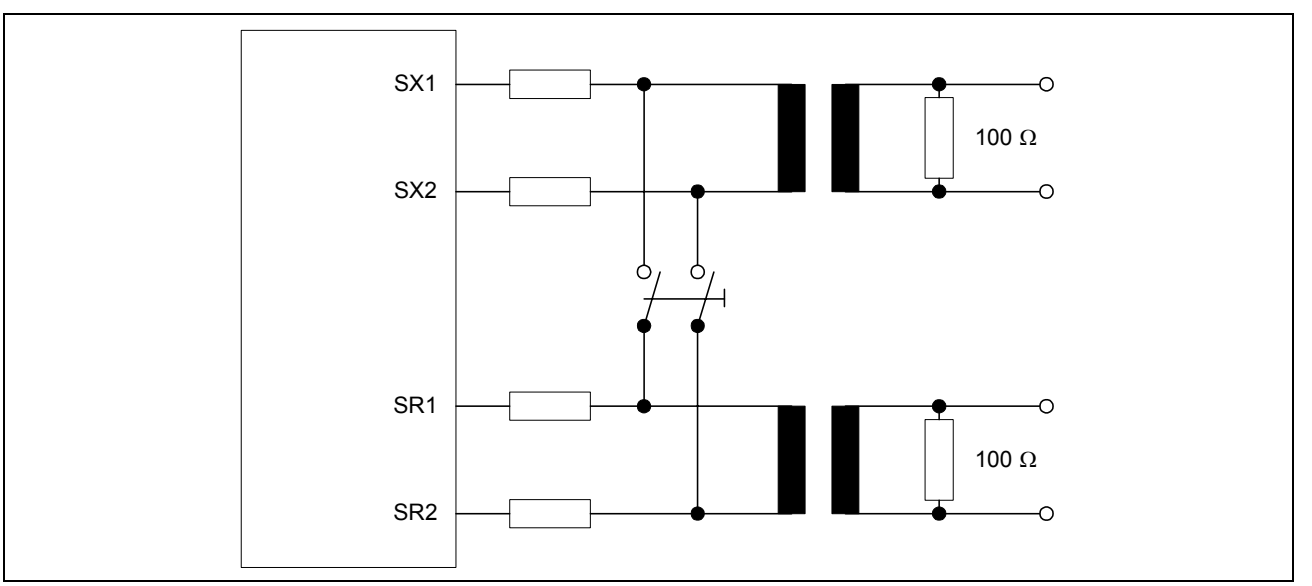



**Figure 36 External Loop at the S/T-Interface**

– Transmission of special test signals on the S/T interface according to the modified AMI code are initiated via a C/I command written in CIX0 register (see **Chapter 3.5.4**).

Two kinds of test signals may be transmitted by the IPAC-X:

– The single pulses are of alternating polarity. One pulse is transmitted in each frame resulting in a frequency of the fundamental mode of 2 kHz. The corresponding C/I command is SSP (Send Single Pulses).

– The continuous pulses are of alternating polarity. 48 pulses are transmitted in each frame resulting in a frequency of the fundamental mode of 96 kHz. The corresponding C/I command is SCP (Send Continuous Pulses).

## 3.4 Clock Generation

**Figure 37** shows the clock system of the IPAC-X. The oscillator is used to generate a 7.68 MHz clock signal ($f_{XTAL}$). In TE mode the DPLL generates the IOM-2 clocks FSC (8 kHz), DCL (1536 kHz) and BCL (768 kHz) synchronous to the received S/T frames. In LT modes these pins are input and in LT-T mode an 1536 kHz clock synchronous to S is output at SCLK which can be used for DCL input.

An internal clock divider provides an FSC (ACFG2.FBS=0) or BCL (ACFG2.FBS=1) output on pin AUX5/FBOUT derived from the DCL clock. The output can be enabled via ACFG2.A5SEL=1.

The FSC signal is used to generate the pulse lengths of the different reset sources C/I Code, $\overline{\text{EAW}}$ pin and Watchdog (see **Chapter 3.2.4**).

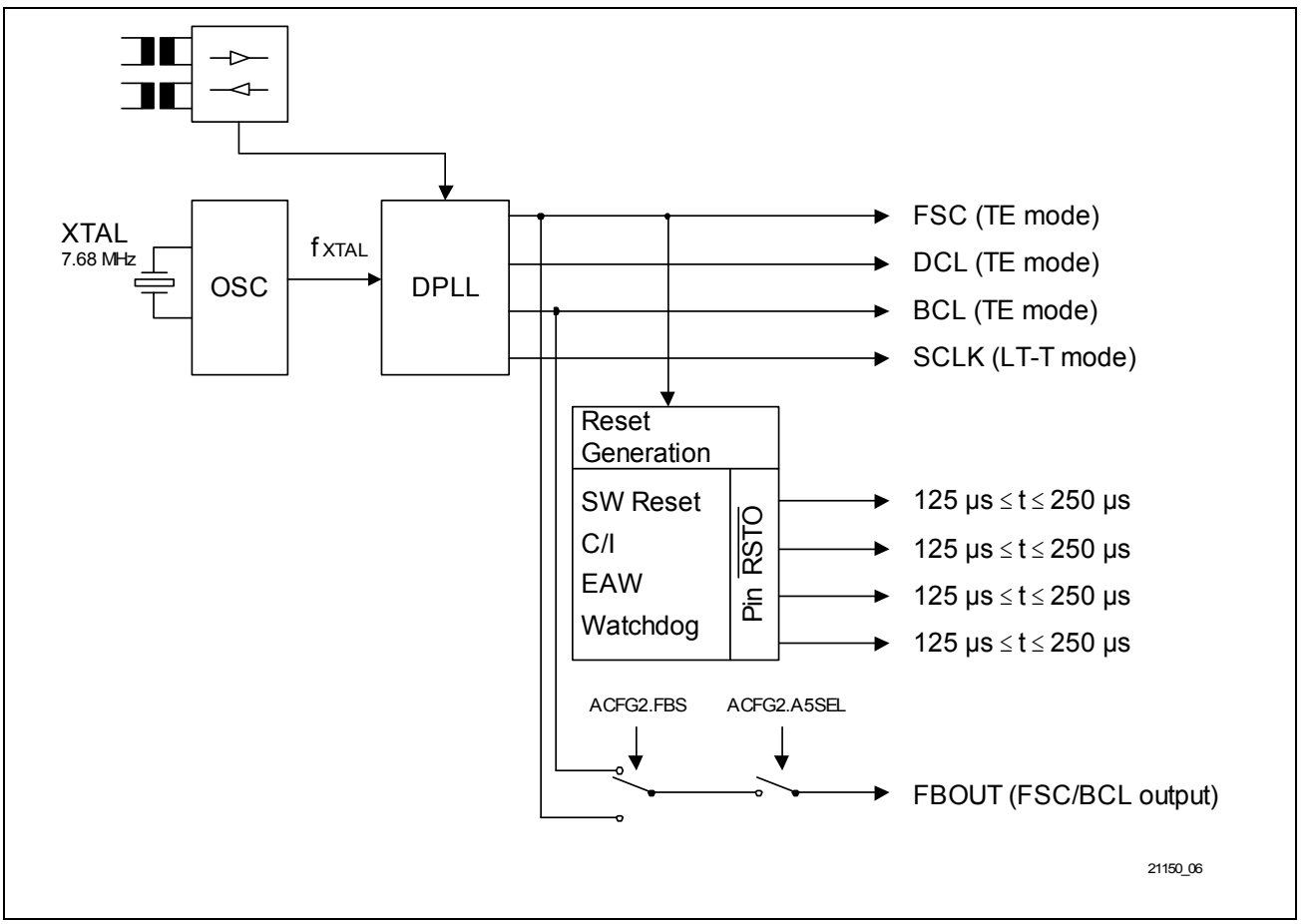



**Figure 37 Clock System of the IPAC-X**

**Table 9 Clock Modes**

| | TE | LT-T | LT-S | NT | Int. NT |
|---|---|---|---|---|---|
| Selected via | pin: MODE0=0 | pin:MODE1=0<br>MODE0=1 | pin:MODE1=1<br>MODE0=1 | bit:MODE2=0<br>MODE1=1<br>MODE0=0 | bit:MODE2=1<br>MODE1=1<br>MODE0=1 or<br>MODE0=0 *1) |
| FSC | o:8 kHz<br>(DIS_TR=0)<br>i:8 kHz<br>(DIS_TR=1) *2) | i:8 kHz | i:8 kHz | i:8 kHz | i:8 kHz |
| DCL | o:1536 kHz<br>(DIS_TR=0)<br>i:1536/768 kHz<br>(DIS_TR=1) *2) | i:1536 kHz<br>(from SCLK)<br>or 4096 kHz<br>(from ext. PLL) | i:512 kHz or<br>1536 kHz or<br>4096 kHz | i:512 kHz or<br>1536 kHz or<br>4096 kHz | i:1536 kHz |
| BCL/SCLK | o:768 kHz<br>(BCL) | o:1536 kHz<br>(SCLK) *5) | o:256 kHz or<br>768 kHz or<br>2048 kHz<br>(derived from<br>DCL/2) | o:256 kHz or<br>768 kHz or<br>2048 kHz<br>(derived from<br>DCL/2) | o:768 kHz<br>(derived from<br>DCL/2) |
| DU *6) | i | i | o | o | o |
| DD | o | o | i | i | i |
| AUX5/FBOUT<br>(A5SEL=1) *3) | o:FSC (FBS=0) or<br>BCL (FBS=1) | o:FSC (FBS=0) or<br>BCL (FBS=1) | o:FSC (FBS=0) or<br>BCL (FBS=1) | o:FSC (FBS=0) or<br>BCL (FBS=1) | o:FSC (FBS=0) or<br>BCL (FBS=1) |
| AUX0-2 | general purpose<br>I/O pins | CH0-2:<br>strap pins for IOM<br>channel select *4) | CH0-2:<br>strap pins for IOM<br>channel select *4) | CH0-2:<br>strap pins for IOM<br>channel select *4) | general purpose<br>I/O pins |

***Note: The IOM-2 interface is adaptive. This means in LT-S/NT and LT-T mode other frequencies for BCL and DCL are possible in the range of 512-4096 kHz (DCL) and 256-2048 kHz (BCL). For details please refer to the application note "Reconfigurable PBX".***

*Note: i = input; o = output;*
*For all input clocks typical values are given although other clock frequencies may be used, too.*
*1) The modes TE, LT-T and LT-S can directly be selected by strapping the pins MODE1 and MODE0. The mode can be reprogrammed in TR_MODE.MODE2-0 where NT and Intelligent NT can be selected additionally. In Int. NT mode MODE0 selects between NT state machine (0) and LT-S state machine (1).*
*2) In TE mode the S transceiver can be disabled (TR_CONF0.DIS_TR=1) so the IOM clocks become inputs and with IOM_CR.CLKM the DCL input can be selected to double clock (0) or single bit clock (1).*
*3) ACFG2.A5SEL=1 selects the FBOUT function (derived from IOM clocks) which provides an FSC/BCL output clock if clocks are present on IOM.*
*4) The number of IOM channels depends on the DCL clock, e.g. with DCL=1536 kHz 3 IOM channels and with DCL=4096 kHz 8 channels are available.*
*5) In LT-T mode the 1536 kHz output clock on SCLK is synchronous to the S interface and can be used as input for the DCL clock.<*
*6) The direction input/output refers to the direction of the B- and D-channel data stream across the S-transceiver. Due to the capabilites of the IOM-2 handler the direction of some other timeslots may be different if this is programmed by the host (e.g. for data exchange between different devices connected to IOM-2).*

### 3.4.1 Description of the Receive PLL (DPLL)

The receive PLL performs phase tracking between the F/L transition of the receive signal and the recovered clock. Phase adjustment is done by adding or subtracting 0.5 or 1 XTAL period to or from a 1.536-MHz clock cycle. The 1.536-MHz clock is than used to generate any other clock synchronized to the line.

During (re)synchronization an internal reset condition may effect the 1.536-MHz clock to have high or low times as short as 130 ns. After the S/T interface frame has achieved the synchronized state (after three consecutive valid pairs of code violations) the FSC output in TE mode is set to a specific phase relationship, thus causing once an irregular FSC timing.

The phase relationships of the clocks are shown in **Figure 38.**

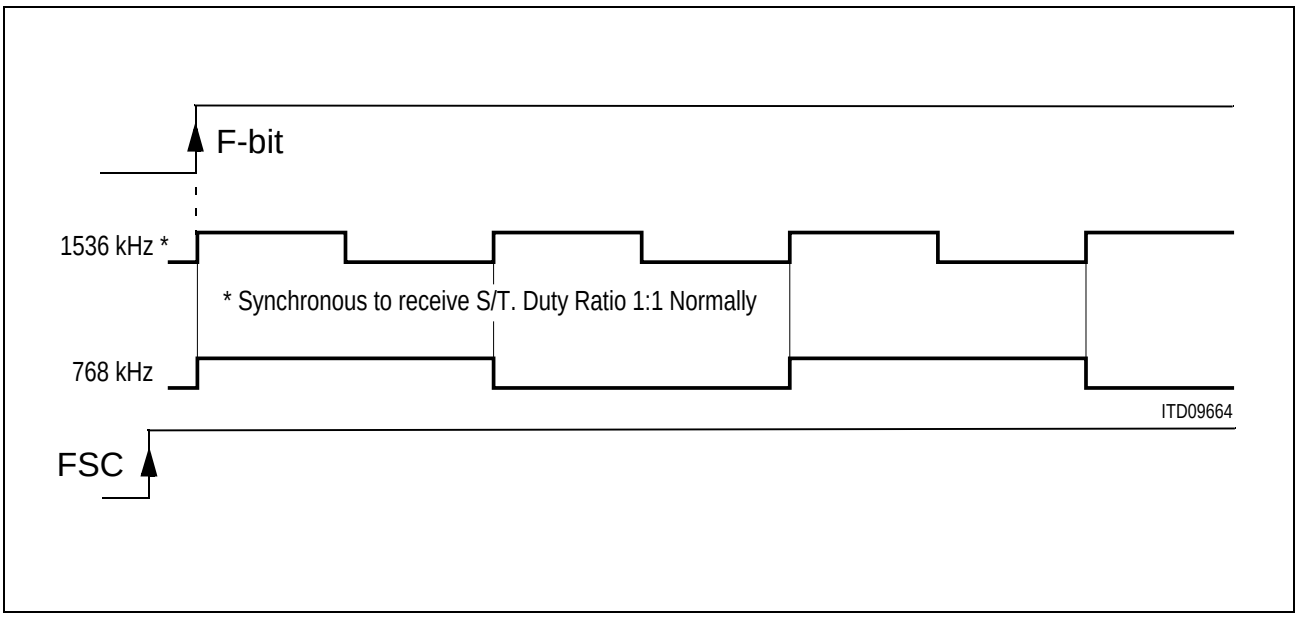



**Figure 38 Phase Relationships of IPAC-X Clock Signals**

### 3.4.2 Jitter

The timing extraction jitter of the IPAC-X conforms to ITU-T Recommendation I.430 (– 7% to + 7% of the S-interface bit period).

### 3.4.3 Oscillator Clock Output C768

The IPAC-X derives its system clocks from an external clock connected to XTAL1 (while XTAL2 is not connected) or from a 7.68 MHz crystal connected across XTAL1 and XTAL2.

At pin C768 a buffered 7.68 MHz output clock is provided to drive further devices, which is suitable in multiline applications for example (see **Figure 39**). This clock is not synchronized to the S-interface.

In power down mode the C768 output is disabled (low signal).

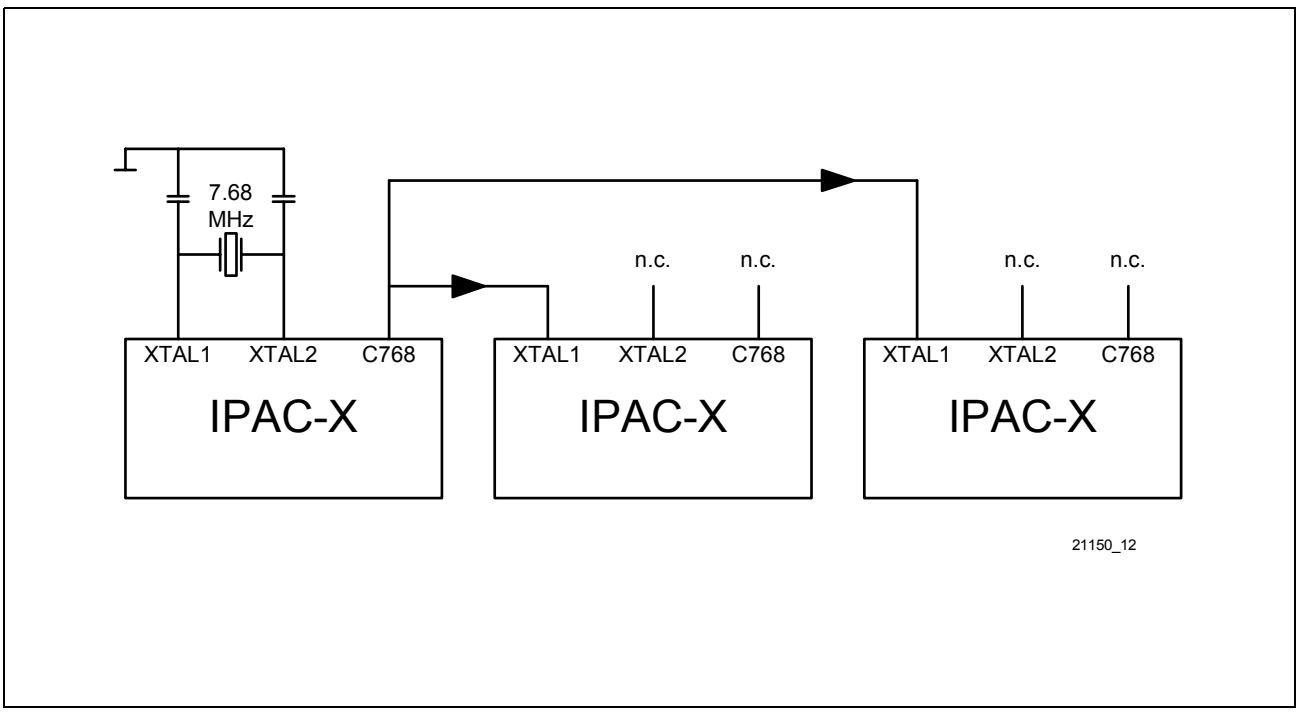



**Figure 39 Buffered Oscillator Clock Output**

## 3.5 Control of Layer-1

The layer-1 activation/ deactivation can be controlled by an internal state machine via the IOM-2 C/I0 channel or by software via the microcontroller interface directly. In the default state the internal layer-1 state machine of the IPAC-X is used. By setting the L1SW bit in the TR_CONF0 register the internal state machine can be disabled and the layer-1 commands, which are normally generated by the internal state machine are written directly in the TR_CMD register or indications read from the TR_STA register respectively. The IPAC-X layer-1 control flow is shown in **Figure 40**.

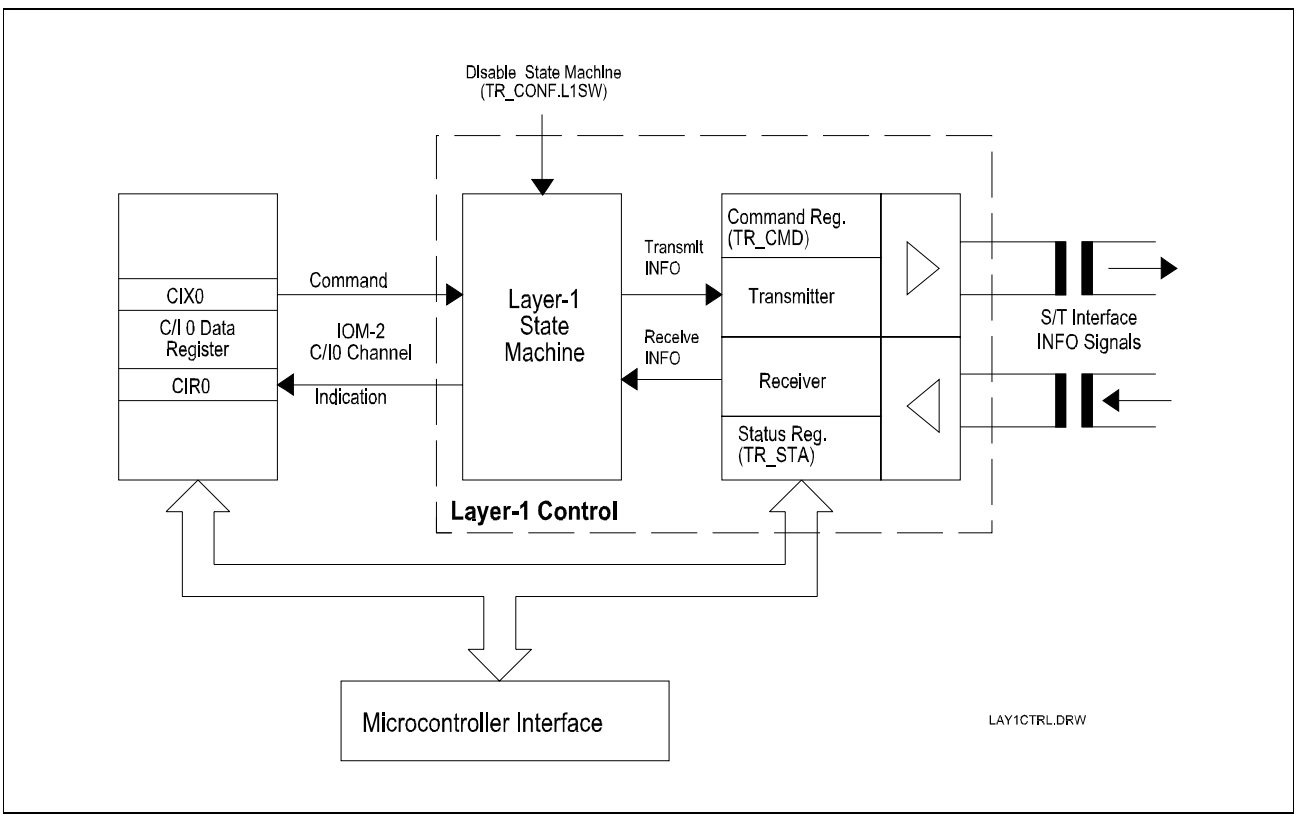



**Figure 40 Layer-1 Control**

In the following sections the layer-1 control by the IPAC-X state machine will be described. For the description of the IOM-2 C/I0 channel see also **Chapter 3.7.4**.

The layer-1 functions are controlled by commands issued via the CIX0 register. These commands, sent over the IOM-2 C/I channel 0 to layer 1, trigger certain procedures, such as activation/deactivation, switching of test loops and transmission of special pulse patterns. These procedures are governed by layer-1 state diagrams. Responses from layer 1 are obtained by reading the CIR0 register after a CIC interrupt (ISTA).

The state diagrams of the IPAC-X are shown in **Figure 42** and **Figure 43**. The activation/ deactivation implemented by the IPAC-X agrees with the requirements set forth in ITU recommendations. State identifiers F1-F8 are in accordance with ITU I.430.

State machines are the key to understanding the transceiver part of the IPAC-X. They include all information relevant to the user and enable him to understand and predict the behaviour of the IPAC-X. The state diagram notation is given in **Figure 41**. The informations contained in the state diagrams are:

– state name (based on ITU I.430)
– S/T signal transmitted (INFO)
– C/I code received
– C/I code transmitted
– transition criteria

The coding of the C/I commands and indications are described in detail in **Chapter 3.5.4**.

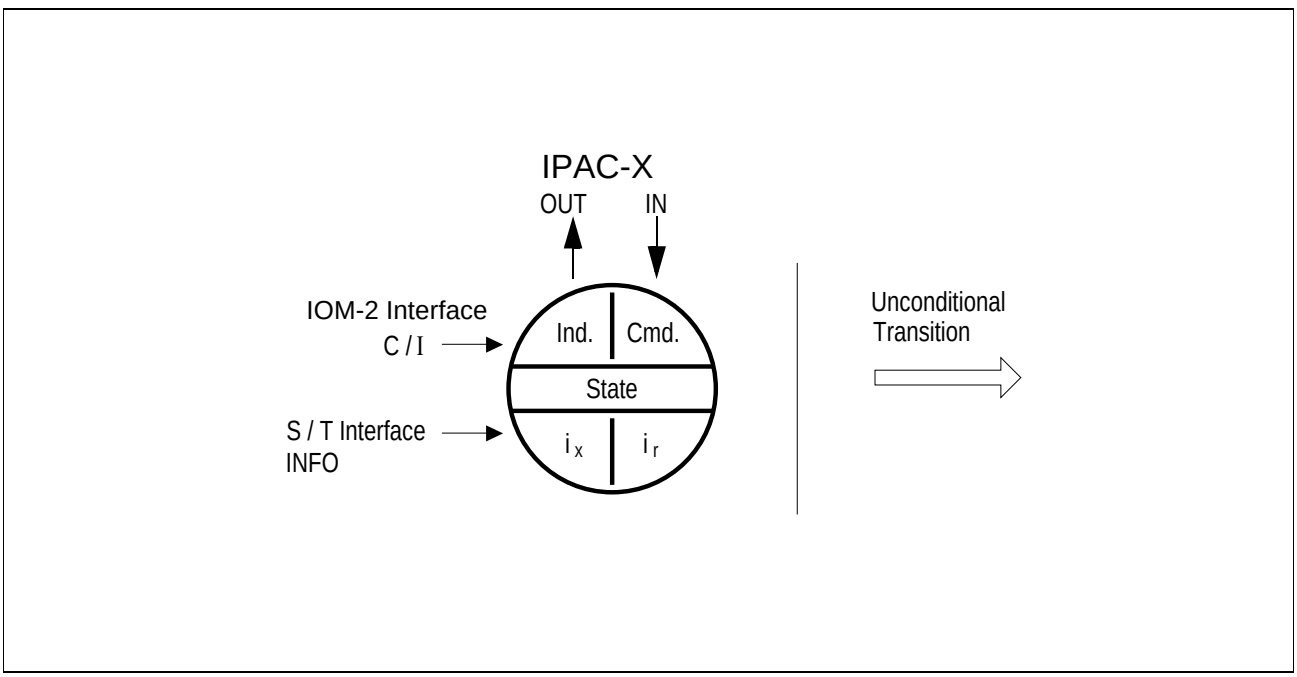



**Figure 41 State Diagram Notation**

The following example illustrates the use of a state diagram with an extract of the TE state diagram. The state explained is “F3 deactivated”.

The state may be entered:

– from the unconditional states (ARL, RES, TM)
– from state “F3 pending deactivation”, “F3 power up”, “F4 pending activation” or “F5 unsynchronized” after the C/I command “DI” has been received.

The following informations are transmitted:

– INFO 0 (no signal) is sent on the S/T-interface.

C/I message “DC” is issued on the IOM-2 interface.

The state may be left by either of the following methods:

– Leave for the state “F3 power up” in case C/I = “TIM” code is received.
– Leave for state “F4 pending activation” in case C/I = AR8 or AR10 is received.

– Leave for the state “F6 synchronized” after INFO 2 has been recognized on the S/T-interface.
– Leave for the state “F7 activated” after INFO 4 has been recognized on the S/T-interface.
– Leave for any unconditional state if any unconditional C/I command is received.

As can be seen from the transition criteria, combinations of multiple conditions are possible as well. A “∗” stands for a logical AND combination. And a “+” indicates a logical OR combination.

The sections following the state diagram contain detailed information on all states and signals used.

### 3.5.1 State Machine TE and LT-T Mode

#### 3.5.1.1 State Transition Diagram (TE, LT-T)

**Figure 42** shows the state transition diagram of the IPAC-X state machine. **Figure 43** shows this for the unconditional transitions (Reset, Loop, Test Mode i).

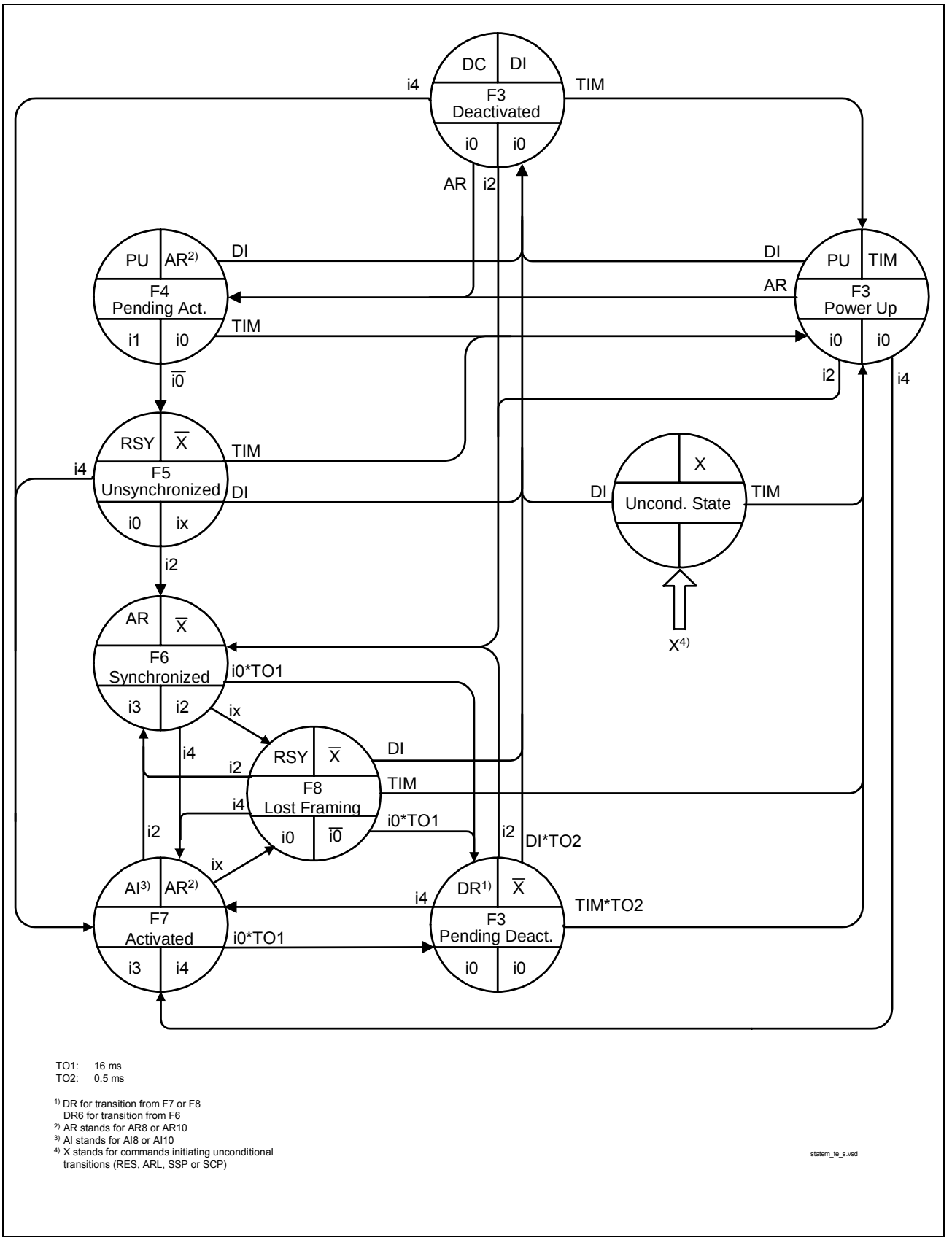



**Figure 42 State Transition Diagram (TE, LT-T)**

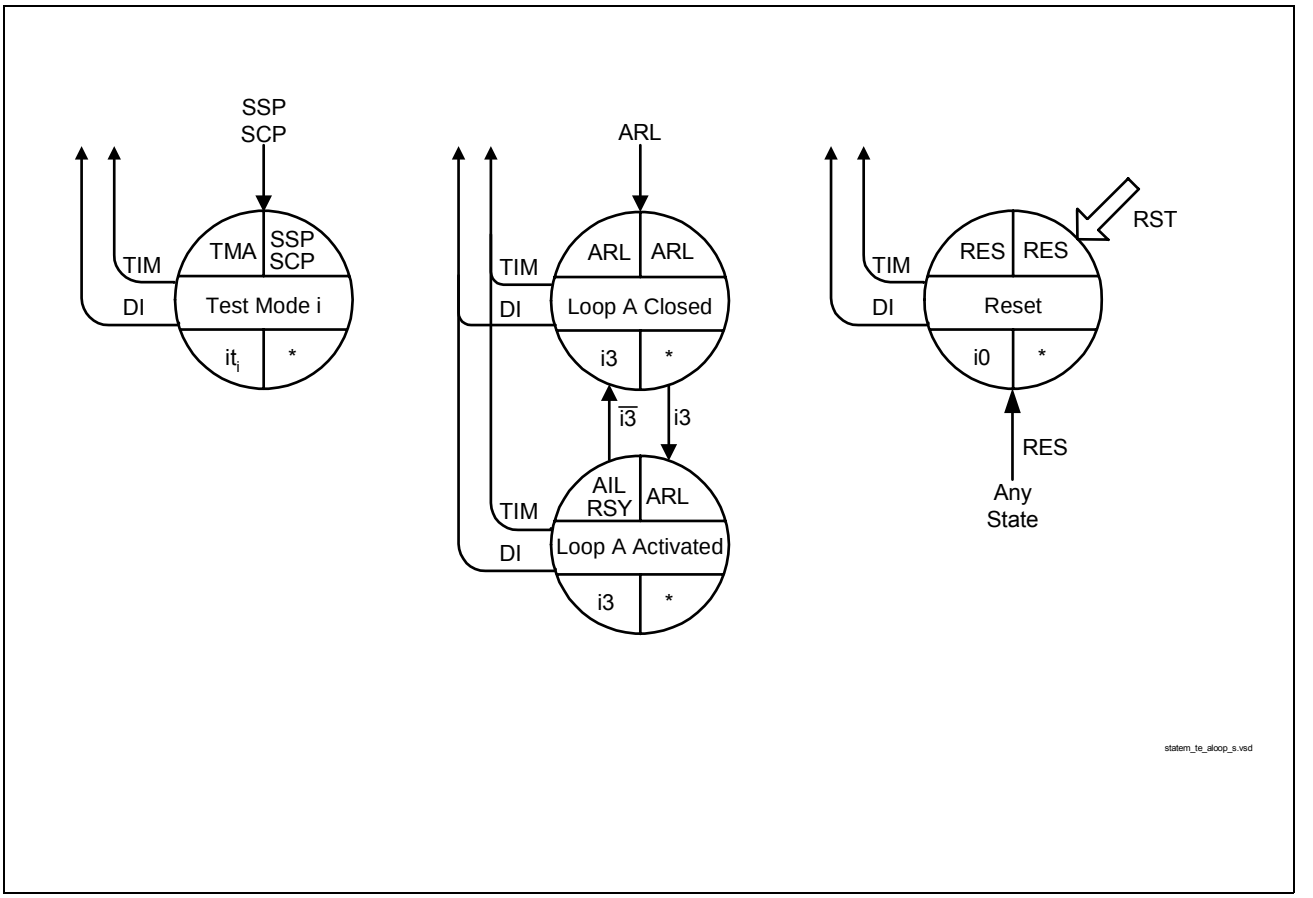



**Figure 43 State Transition Diagram of Unconditional Transitions (TE, LT-T)**

### 3.5.1.2 States (TE, LT-T)

F3 Pending Deactivation

State after deactivation from the S/T interface by info 0. Note that no activation from the terminal side is possible starting from this state. A 'DI' command has to be issued to enter the state 'Deactivated State'.

F3 Deactivated State

The S/T interface is deactivated and the clocks are deactivated 500 µs after entering this state and receiving info 0 if the CFS bit of the IPAC-X Configuration Register is set to "0". Activation is possible from the S/T interface and from the IOM-2 interface. The bit TR_CMD.PD is set and the analog part is powered down.

F3 Power Up

The S/T interface is deactivated (info 0 on the line) and the clocks are running.

F4 Pending Activation

The IPAC-X transmits info 1 towards the network, waiting for info 2.

F5 Unsynchronized

Any signal except info 2 or 4 detected on the S/T interface.

F6 Synchronized

The receiver has synchronized and detects info 2. Info 3 is transmitted to synchronize the NT.

F7 Activated

The receiver has synchronized and detects info 4. All user channels are now conveyed transparently to the IOM-2 interface.
To transfer user channels transparently to the S/T interface either the command AR8 or AR10 has to be issued and TR_STA.FSYN must be “1” (signal from remote side must be synchronous).

F8 Lost Framing

The receiver has lost synchronization in the states F6 or F7 respectively.

**Unconditional States**

Loop A Closed (internal or external)

The IPAC-X loops back the transmitter to the receiver and activates by transmission of info 3. The receiver has not yet synchronized.
For a non transparent internal loop the DIS_TX bit of register TR_CONF2 has to be set to ’1’.

Loop A Activated (internal or external)

The receiver has synchronized to info 3. Data may be sent. The indication “AIL” is output to indicate the activated state. If the loop is closed internally and the S/T line awake detector detects any signal on the S/T interface, this is indicated by “RSY”.

Test Mode - SSP

Single alternating pulses are transmitted to the S/T-interface resulting in a frequency of the fundamental mode of 2 kHz.

Test Mode - SCP

Continuous alternating pulses are transmitted to the S/T-interface resulting in a frequency of the fundamental mode of 96 kHz.

### 3.5.1.3 C/I Codes (TE, LT-T)

| Command | Abbr. | Code | Remark |
|---|---|---|---|
| Activation Request with priority class 8 | AR8 | 1000 | Activation requested by the IPAC-X, D-channel priority set to 8 (**see note**). |
| Activation Request with priority class 10 | AR10 | 1001 | Activation requested by the IPAC-X, D-channel priority set to 10 (**see note**). |
| Activation Request Loop | ARL | 1010 | Activation requested for the internal or external Loop A (**see note**).<br>For a non transparent internal loop bit DIS_TX of register TR_CONF2 has to be set to ’1’ additionally. |
| Deactivation Indication | DI | 1111 | Deactivation Indication. |
| Reset | RES | 0001 | Reset of the layer-1 state machine. |
| Timing | TIM | 0000 | Layer-2 device requires clocks to be activated. |
| Test mode SSP | SSP | 0010 | One AMI-coded pulse transmitted in each frame, resulting in a frequency of the fundamental mode of 2 kHz. |
| Test mode SCP | SCP | 0011 | AMI-coded pulses transmitted continuously, resulting in a frequency of the fundamental mode of 96 kHz. |

*Note: In the activated states (AI8, AI10 or AIL indication) the 2B+D channels are only transferred transparently to the S/T interface if one of the three “Activation Request” commands is permanently issued.*

| Indication | Abbr. | Code | Remark |
|---|---|---|---|
| Deactivation Request | DR | 0000 | Deactivation request via S/T-interface if left from F7/F8. |
| Reset | RES | 0001 | Reset acknowledge. |
| Test Mode Acknowledge | TMA | 0010 | Acknowledge for both SSP and SCP. |
| Slip Detected | SLD | 0011 | |
| Resynchronization during level detect | RSY | 0100 | Signal received, receiver not synchronous. |
| Deactivation Request from F6 | DR6 | 0101 | Deactivation Request from state F6. |
| Power up | PU | 0111 | IOM-2 interface clocking is provided. |
| Activation request | AR | 1000 | Info 2 received. |
| Activation request loop | ARL | 1010 | Internal or external loop A closed. |
| Illegal Code Violation | CVR | 1011 | Illegal code violation received. This function has to be enabled by setting the EN_ICV bit of register TR_CONF0. |
| Activation indication loop | AIL | 1110 | Internal or external loop A activated. |
| Activation indication with priority class 8 | AI8 | 1100 | Info 4 received,<br>D-channel priority is 8 or 9. |
| Activation indication with priority class 10 | AI10 | 1101 | Info 4 received,<br>D-channel priority is 10 or 11. |
| Deactivation confirmation | DC | 1111 | Clocks are disabled if CFS bit of register MODE1 is set to ’1’, quiescent state. |

### 3.5.1.4 Infos on S/T (TE, LT-T)

**Receive Infos on S/T (Downstream)**

| Name | Abbr. | Description |
|---|---|---|
| info 0 | i0 | No signal on S/T |
| info 2 | i2 | 4 kHz frame<br>A=’0’ |
| info 4 | i4 | 4 kHz frame<br>A=’1’ |
| info X | ix | Any signal except info 2 or info 4 |

**Transmit Infos on S/T (Upstream)**

| Name | Abbr. | Description |
|---|---|---|
| info 0 | i0 | No signal on S/T |
| info 1 | i1 | Continuous bit sequence of the form ’00111111’ |
| info 3 | i3 | 4 kHz frame |
| Test info 1 | $it_1$ | SSP - Send Single Pulses |
| Test info 2 | $it_2$ | SCP - Send Continuous Pulses |

## 3.5.2 State Machine LT-S Mode

### 3.5.2.1 State Transition Diagram (LT-S)

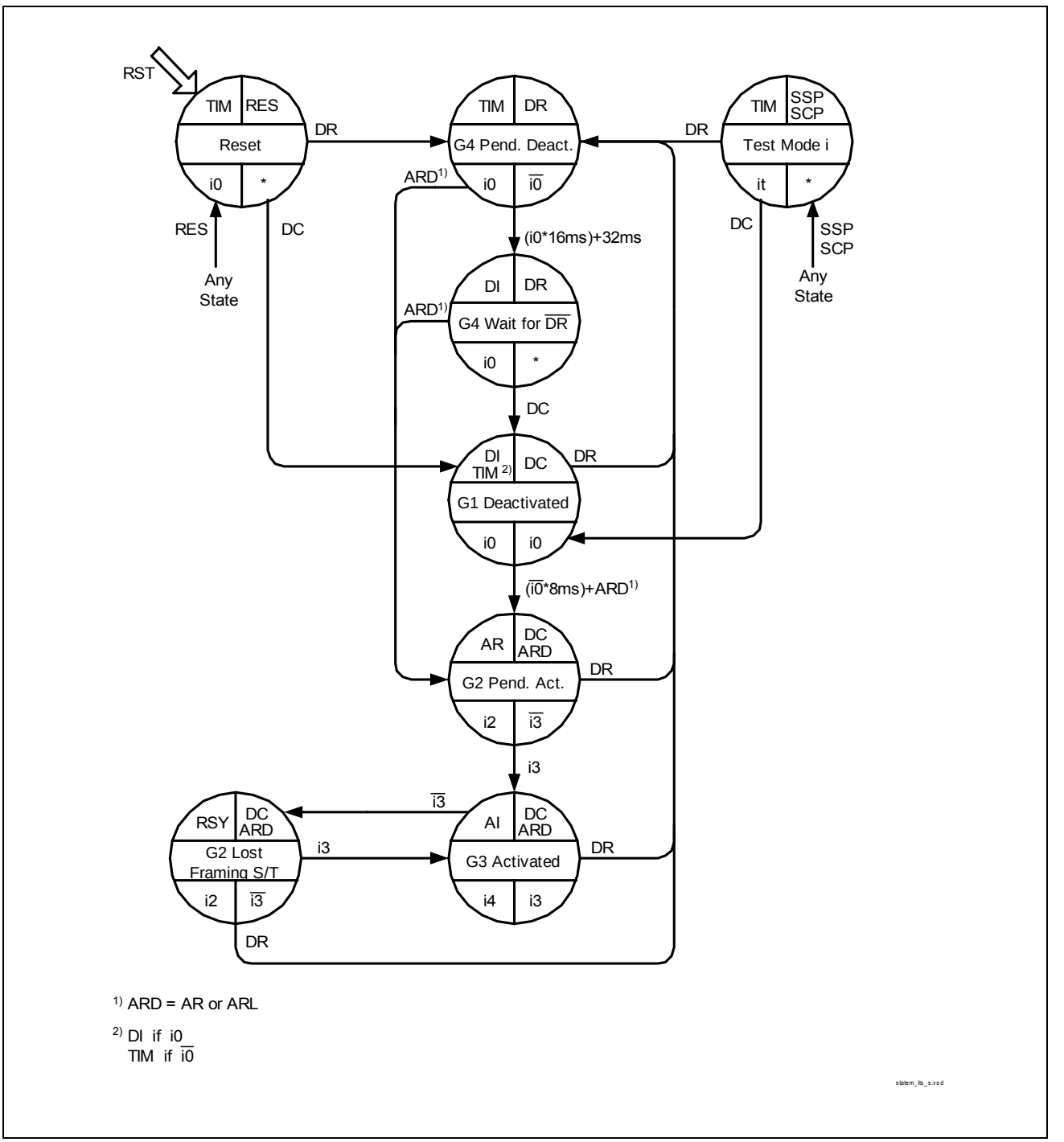



**Figure 44 State Transition Diagram (LT-S)**

*Note: State 'Test Mode' can be entered from any state except from state 'Test Mode' itself , i.e. C/I-code 'SSP/SCP' must not be followed by C/I-code 'SCP/SSP' directly.*

### 3.5.2.2 States (LT-S)

#### G1 Deactivated

The transceiver is not transmitting. There is no signal detected on the S/T-interface, and no activation command is received in the C/I channel. The clocks are deactivated if MODE1-CFS is set to 1. Activation is possible from the S/T interface and from the IOM-2 interface.

#### G2 Pending Activation

As a result of an $\overline{\text{INFO 0}}$ detected on the S/T line or an ARD command, the transceiver begins transmitting INFO 2 and waits for reception of INFO 3. The timer to supervise reception of INFO 3 is to be implemented in software. In case of an ARL command, loop 2 is closed.

#### G3 Activated

Normal state where INFO 4 is transmitted to the S/T-interface. The transceiver remains in this state as long as neither a deactivation nor a test mode is requested, nor the receiver looses synchronism.

When receiver synchronism is lost, INFO 2 is sent automatically. After reception of INFO 3, the transmitter keeps on sending INFO 4.

#### G2 Lost Framing

This state is reached when the transceiver has lost synchronism in the state G3 activated.

#### G4 Pending Deactivation

This state is triggered by a deactivation request DR. It is an unstable state: indication DI (state “G4 wait for DR.”) is issued by the transceiver when:

either INFO0 is received for a duration of 16 ms,

or an internal timer of 32 ms expires.

#### G4 Wait for $\overline{\text{DR}}$

Final state after a deactivation request. The transceiver remains in this state until DC is issued.

#### Unconditional States

#### Test Mode - SSP

Single alternating pulses are sent on the S/T-interface.

**Test Mode - SCP**

Continuous alternating pulses are sent on the S/T-interface.

### 3.5.2.3 C/I Codes (LT-S)

| Command | Abbr. | Code | Remark |
|---|---|---|---|
| Deactivation Request | DR | 0000 | DR - Deactivation Request. Initiates a complete deactivation from the exchange side by transmitting INFO 0. |
| Reset | RES | 0001 | Reset of state machine. Transmission of Info0. No reaction to incoming infos. RES is an unconditional command. |
| Send Single Pulses | SSP | 0010 | Send Single Pulses. |
| Send Continuous Pulses | SCP | 0011 | Send Continuous Pulses. |
| Activation Request | AR | 1000 | Activation Request. This command is used to start an exchange initiated activation. |
| Activation Request Loop | ARL | 1010 | Activation request loop. The transceiver is requested to operate an analog loop-back close to the S/T-interface. |
| Activation Indication Loop | AIL | 1110 | Activation Indication Loop. |
| Deactivation Confirmation | DC | 1111 | Deactivation Confirmation. Transfers the transceiver into a deactivated state in which it can be activated from a terminal (detection of $\overline{\text{INFO 0}}$ enabled). |

| Indication | Abbr. | Code | Remark |
|---|---|---|---|
| Timing | TIM | 0000 | Interim indication during activation procedure in G1. |
| Receiver not Synchronous | RSY | 0100 | Receiver is not synchronous |
| Activation Request | AR | 1000 | $\overline{\text{INFO 0}}$ received from terminal. Activation proceeds. |
| Illegal Code Ciolation | CVR | 1011 | Illegal code violation received. This function has to be enabled in TR_CONF0.EN_ICV. |

| Indication | Abbr. | Code | Remark |
|---|---|---|---|
| Activation Indication | AI | 1100 | Synchronous receiver, i.e. activation completed. |
| Deactivation Indication | DI | 1111 | Timer (32 ms) expired or INFO 0 received for a duration of 16 ms after deactivation request |

### 3.5.2.4 Infos on S/T (LT-S)

**Receive Infos on S/T (Downstream)**

I0 INFO 0 detected

$\overline{I0}$ Level detected (signal different to I0)

I3 INFO 3 detected

$\overline{I3}$ Any INFO other than INFO 3

**Transmit Infos on S/T (Upstream)**

I0 INFO 0

I2 INFO 2

I4 INFO 4

It Send Single Pulses (SSP).
Send Continuous Pulses (SCP).

## 3.5.3 State Machine NT Mode

### 3.5.3.1 State Transition Diagram (NT)

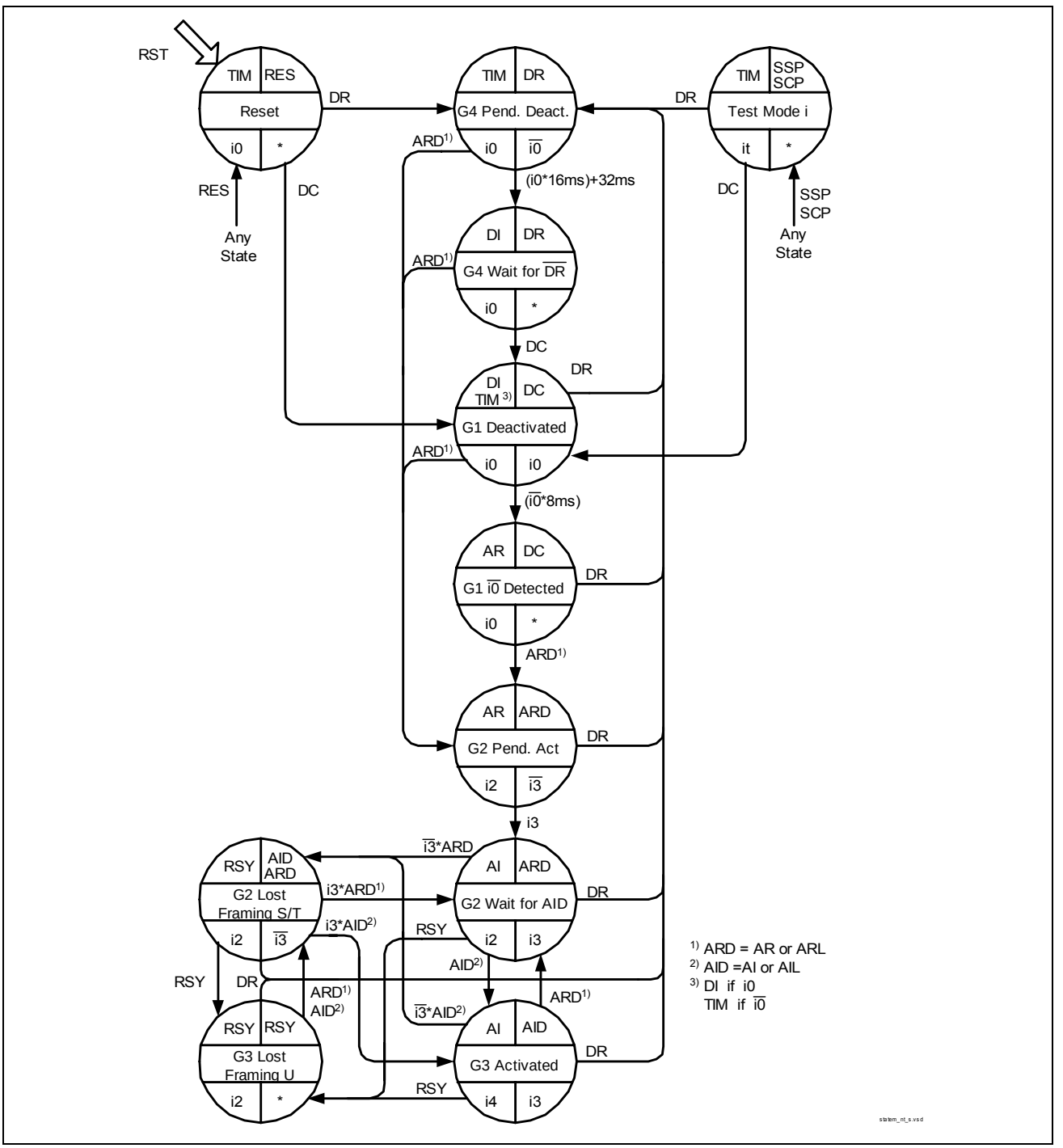



**Figure 45 State Transition Diagram (NT)**

*Note: State 'Test Mode' can be entered from any state except from state 'Test Mode' itself , i.e. C/I-code 'SSP/SCP' must not be followed by C/I-code 'SCP/SSP' directly.*

### 3.5.3.2 States (NT)

#### G1 Deactivated

The transceiver is not transmitting. There is no signal detected on the S/T-interface, and no activation command is received in the C/I channel. The clocks are deactivated if the bit MODE1.CFS to 1. Activation is possible from the S/T interface and from the IOM-2 interface.

#### G1 $\overline{\text{I0}}$ Detected

An $\overline{\text{INFO 0}}$ is detected on the S/T-interface, translated to an “Activation Request” indication in the C/I channel. The transceiver is waiting for an AR command, which normally indicates that the transmission line upstream (usually a two-wire U interface) is synchronized.

#### G2 Pending Activation

As a result of the ARD command, an INFO 2 is sent on the S/T-interface. INFO 3 is not yet received. In case of ARL command, loop 2 is closed.

#### G2 Wait for AID

INFO 3 was received, INFO 2 continues to be transmitted while the transceiver waits for a “switch-through” command AID from the device upstream.

#### G3 Activated

INFO 4 is sent on the S/T-interface as a result of the “switch through” command AID: the B and D-channels are transparent. On the command AIL, loop 2 is closed.

#### G2 Lost Framing S/T

This state is reached when the transceiver has lost synchronism in the state G3 activated.

#### G3 Lost Framing U

On receiving an RSY command which usually indicates that synchronization has been lost on the two-wire U interface, the transceiver transmits INFO 2.

#### G4 Pending Deactivation

This state is triggered by a deactivation request DR, and is an unstable state. Indication DI (state “G4 wait for DR”) is issued by the transceiver when:

either INFO0 is received for a duration of 16 ms

or an internal timer of 32 ms expires.

**G4 Wait for $\overline{\text{DR}}$**

Final state after a deactivation request. The transceiver remains in this state until DC is issued.

**Unconditional States**

**Test Mode SSP**

Send Single Pulses

**Test Mode SCP**

Send Continuous Pulses

### 3.5.3.3 C/I Codes (NT)

| Command | Abbr. | Code | Remark |
|---|---|---|---|
| Deactivation Request | DR | 0000 | DR - Deactivation Request. Initiates a complete deactivation from the exchange side by transmitting INFO 0. Unconditional command. |
| Reset | RES | 0001 | Reset of state machine. Transmission of Info0. No reaction to incoming infos. RES is an unconditional command. |
| Send Single Pulses | SSP | 0010 | Send Single Pulses. |
| Send Continuous Pulses | SCP | 0011 | Send Continuous Pulses. |
| Receiver not Synchronous | RSY | 0100 | Receiver is not synchronous |
| Activation Request | AR | 1000 | Activation Request. This command is used to start an exchange initiated activation. |
| Activation Request Loop | ARL | 1010 | Activation request loop. The transceiver is requested to operate an analog loop-back close to the S/T-interface. |
| Activation Indication | AI | 1100 | Synchronous receiver, i.e. activation completed. |

| Command | Abbr. | Code | Remark |
|---|---|---|---|
| Activation Indication Loop | AIL | 1110 | Activation Indication Loop |
| Deactivation Confirmation | DC | 1111 | Deactivation Confirmation. Transfers the transceiver into a deactivated state in which it can be activated from a terminal (detection of $\overline{\text{INFO 0}}$ enabled). |

| Indication | Abbr. | Code | Remark |
|---|---|---|---|
| Timing | TIM | 0000 | Interim indication during deactivation procedure. |
| Receiver not Synchronous | RSY | 0100 | Receiver is not synchronous. |
| Activation Request | AR | 1000 | $\overline{\text{INFO 0}}$ received from terminal. Activation proceeds. |
| Illegal Code Ciolation | CVR | 1011 | Illegal code violation received. This function has to be enabled in TR_CONF0.EN_ICV. |
| Activation Indication | AI | 1100 | Synchronous receiver, i.e. activation completed. |
| Deactivation Indication | DI | 1111 | Timer (32 ms) expired or INFO 0 received for a duration of 16 ms after deactivation request. |

### 3.5.4 Command/Indicate Channel Codes (C/I0) - Overview

The table below presents all defined C/I0 codes. A command needs to be applied continuously until the desired action has been initiated. Indications are strictly state orientated. Refer to the state diagrams in the previous sections for commands and indications applicable in various states.

| Code | | | | TE/LT-T | | LT-S | | NT | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | **Cmd** | **Ind** | **Cmd** | **Ind** | **Cmd** | **Ind** |
| 0 | 0 | 0 | 0 | TIM | DR | DR | TIM | DR | TIM |
| 0 | 0 | 0 | 1 | RES | RES | RES | – | RES | – |
| 0 | 0 | 1 | 0 | SSP | TMA | SSP | – | SSP | – |
| 0 | 0 | 1 | 1 | SCP | SLD | SCP | – | SCP | – |
| 0 | 1 | 0 | 0 | – | RSY | – | RSY | RSY | RSY |
| 0 | 1 | 0 | 1 | – | DR6 | – | – | – | – |
| 0 | 1 | 1 | 0 | – | – | – | – | – | – |
| 0 | 1 | 1 | 1 | – | PU | – | – | – | – |
| 1 | 0 | 0 | 0 | AR8 | AR | AR | AR | AR | AR |
| 1 | 0 | 0 | 1 | AR10 | – | – | – | – | – |
| 1 | 0 | 1 | 0 | ARL | ARL | ARL | – | ARL | – |
| 1 | 0 | 1 | 1 | – | CVR | – | CVR | – | CVR |
| 1 | 1 | 0 | 0 | – | AI8 | – | AI | AI | AI |
| 1 | 1 | 0 | 1 | – | AI10 | – | – | – | – |
| 1 | 1 | 1 | 0 | – | AIL | – | – | AIL | – |
| 1 | 1 | 1 | 1 | DI | DC | DC | DI | DC | DI |

## 3.6 Control Procedures

### 3.6.1 Example of Activation/Deactivation

An example of an activation/deactivation of the S/T interface initiated by the terminal with the time relationships mentioned in the previous chapters is shown in **figure 46**.

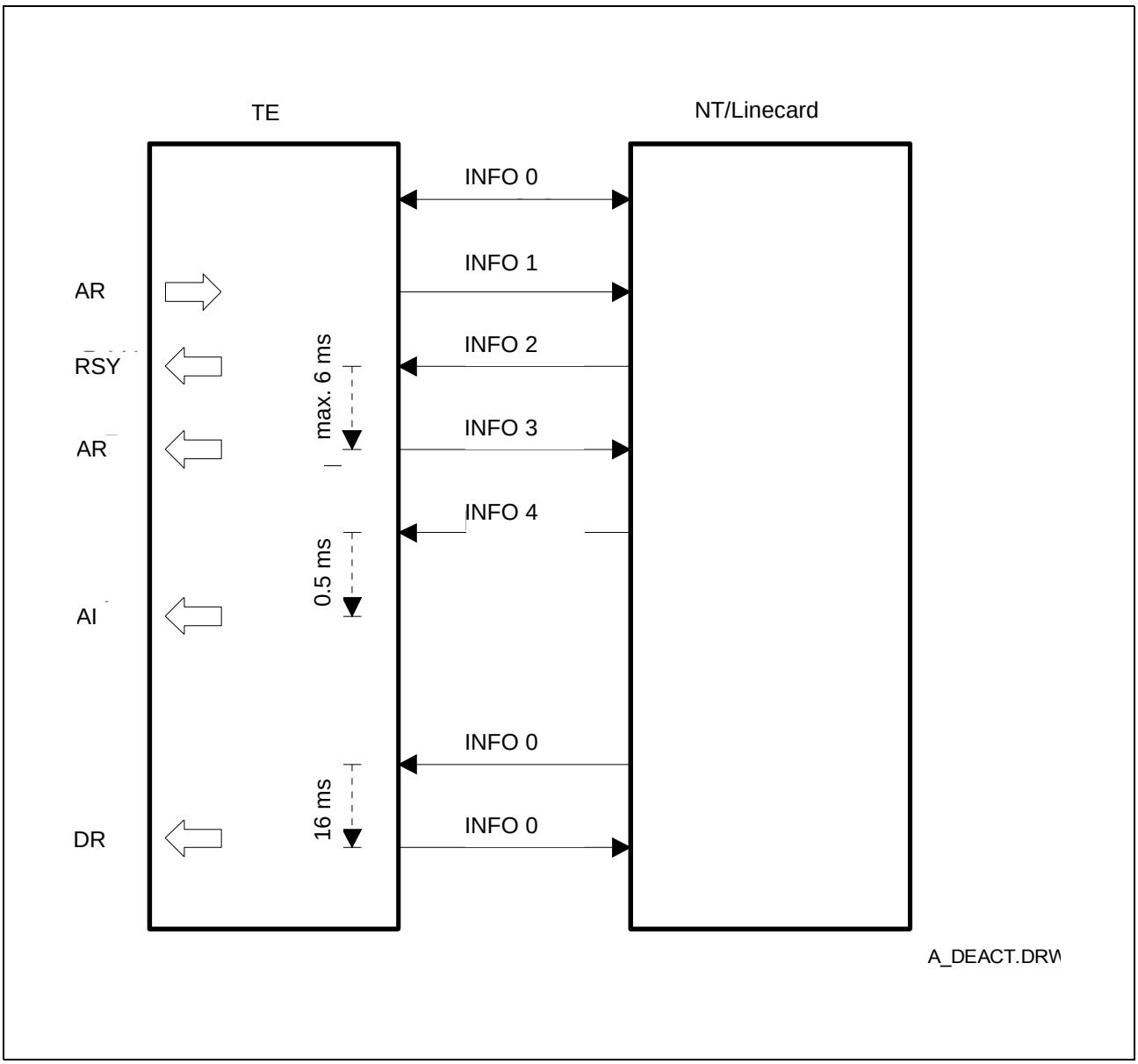



**Figure 46 Example of Activation/Deactivation Initiated by the Terminal**

### 3.6.2 Activation Initiated by the Terminal

INFO 1 has to be transmitted as long as INFO 0 is received.
INFO 0 has to be transmitted thereafter as long as no valid INFO (INFO 2 or INFO 4) is received.
After reception of INFO 2 or INFO 4 transmission of INFO 3 has to be started.
Data can be transmitted if INFO 4 has been received.

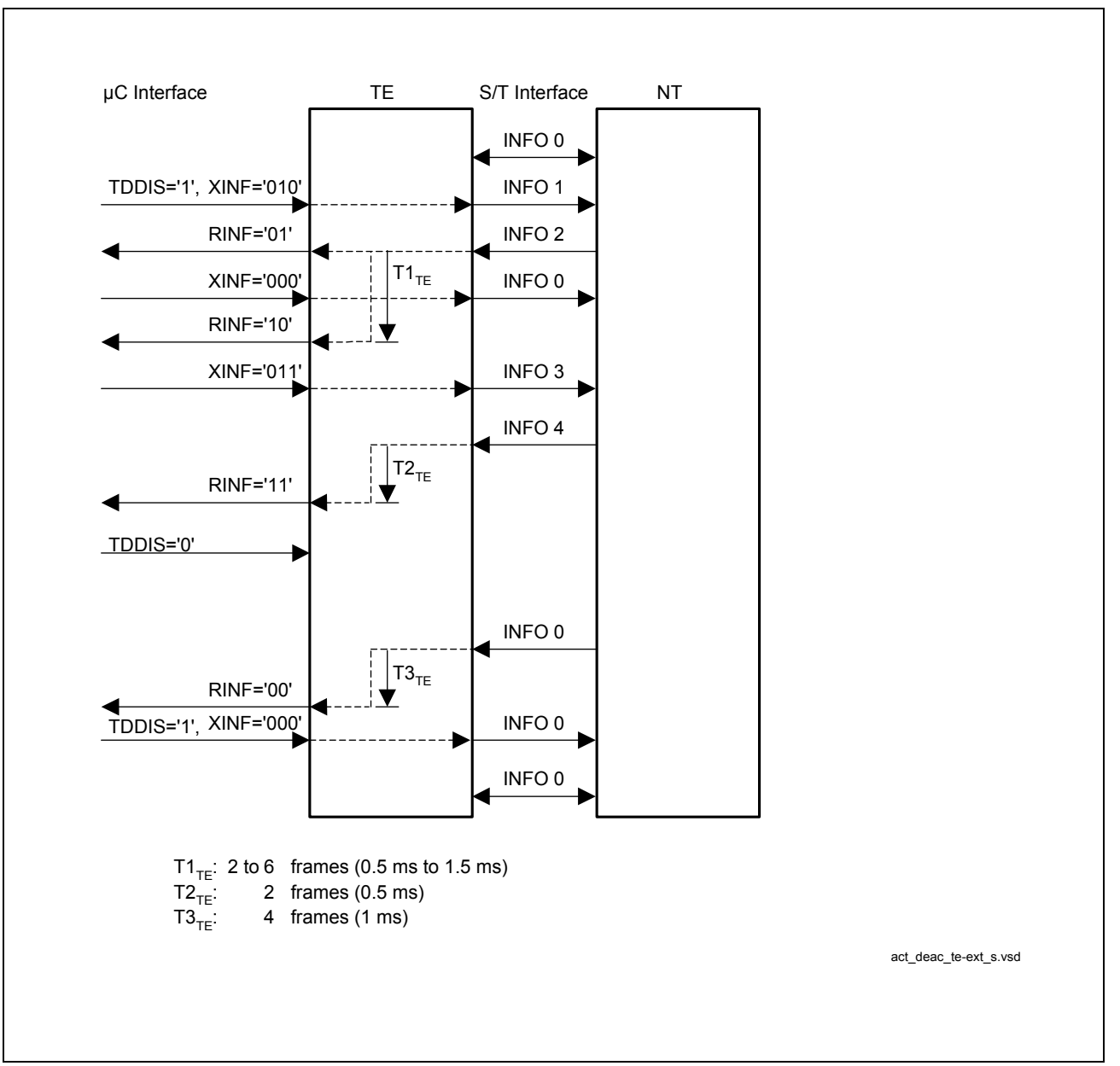



**Figure 47 Example of Activation/Deactivation initiated by the Terminal (TE). Activation/Deactivation Completely Under Software Control**

*Note: RINF and XINF are Receive- and Transmit-INFOs of register TR_STA.*

### 3.6.3 Activation initiated by the Network Termination NT

INFO 0 has to be transmitted as long as no valid INFO (INFO 2 or INFO 4) is received. After reception of INFO 2 or INFO 4 transmission of INFO 3 has to be started. Data can be transmitted if INFO 4 has been received.

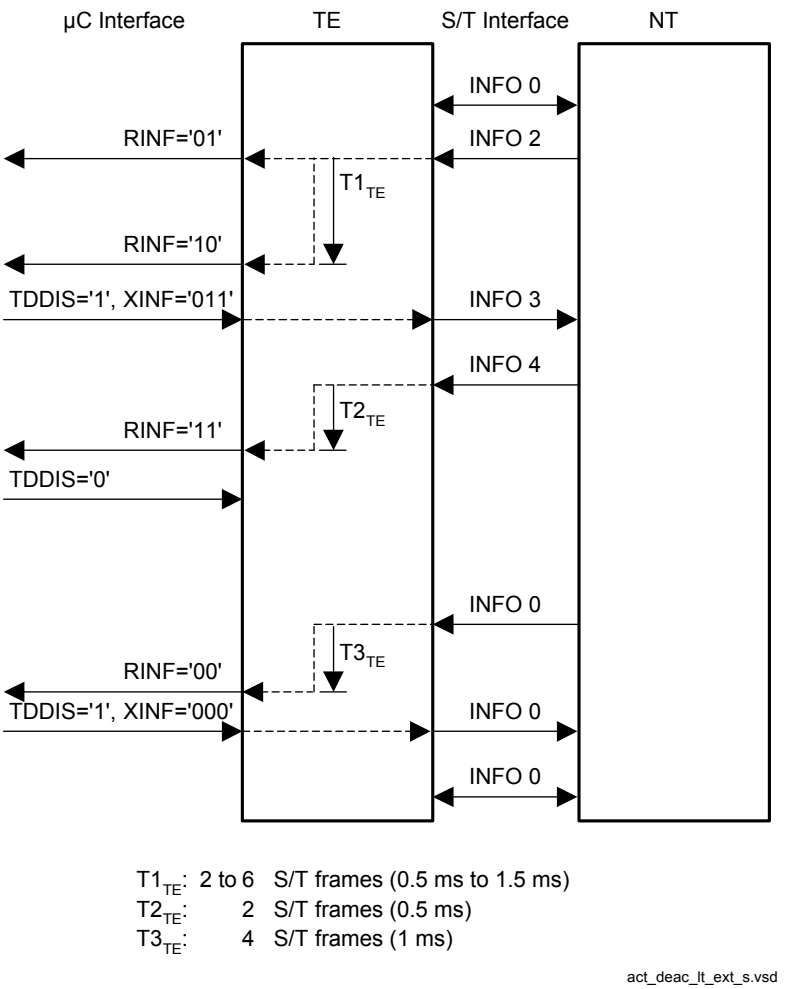



**Figure 48 Example of Activation/Deactivation Initiated by the Network Termination (NT). Activation/Deactivation Completely Under Software Control**

*Note: RINF and XINF are Receive- and Transmit-INFOs of register TR_STA.*

## 3.7 IOM-2 Interface

The IPAC-X supports the IOM-2 interface in linecard mode and in terminal mode with single clock and double clock. The IOM-2 interface consists of four lines: FSC, DCL, DD and DU. The rising edge of FSC indicates the start of an IOM-2 frame. The DCL and the BCL clock signals synchronize the data transfer on both data lines DU and DD. The DCL is twice the bit rate, the BCL rate is equal to the bit rate. The bits are shifted out with the rising edge of the first DCL clock cycle and sampled at the falling edge of the second clock cycle.

The IOM-2 interface can be enabled/disabled with the DIS_IOM bit in the IOM_CR register.

### TE Mode

A DCL signal and BCL signal (pin BCL/SCLK) output is provided and the FSC signal is generated by the receive DPLL which synchronizes it to the received S/T frame.

The BCL clock together with the two serial data strobe signals (SDS1, SDS2) can be used to connect time slot oriented standard devices to the IOM-2 interface. If the transceiver is disabled (TR_CON.DIS_TR) the DCL and FSC pins become input and the HDLC part can still work via IOM-2. In this case the clock mode bit (IOM_CR.CLKM) selects between a double clock and a single clock input for DCL.

The clock rate/frequency of the IOM-2 signals in TE mode are:
DD, DU: 768 kbit/s
FSC (o): 8 kHz
DCL (o): 1536 kHz (double clock rate)
BCL (o):768 kHz (single clock rate)
Option - Transceiver disabled (DIS_TR = ’1’):
FSC (i): 8 kHz
DCL (i): 1536 ... 4096 kHz, in steps of 512 kHz (double clock rate)

### LT-S, LT-T, NT, iNT Mode

The IOM-2 clock signals FSC and BCL are input.
In LT-T mode a 1536 kHz output clock synchronous to S is provided at pin SCLK which can directly be connected to the DCL input. Internal clock dividers provide for generation of an FSC or BCL output clock at pin FBOUT derived from DCL (see **Chapter 3.4**).

DD, DU: data rate = DCL/2 kbit/s (LT-T mode)
FSC (i): 8 kHz
DCL (i): 512 ... 4096 kHz, in steps of 512 kHz (double clock rate)
SCLK (o):1536 kHz (LT-T mode), BCL derived via DCL/2 (LT-S/NT mode)

*Note: In all modes the direction of the data lines DU and DD is not fix but depending on the timeslot which can be seen in the figures below.*

### IOM-2 Frame Structure (TE Mode)

The frame structure on the IOM-2 data ports (DU,DD) of a master device in IOM-2 terminal mode is shown in **Figure 49.**

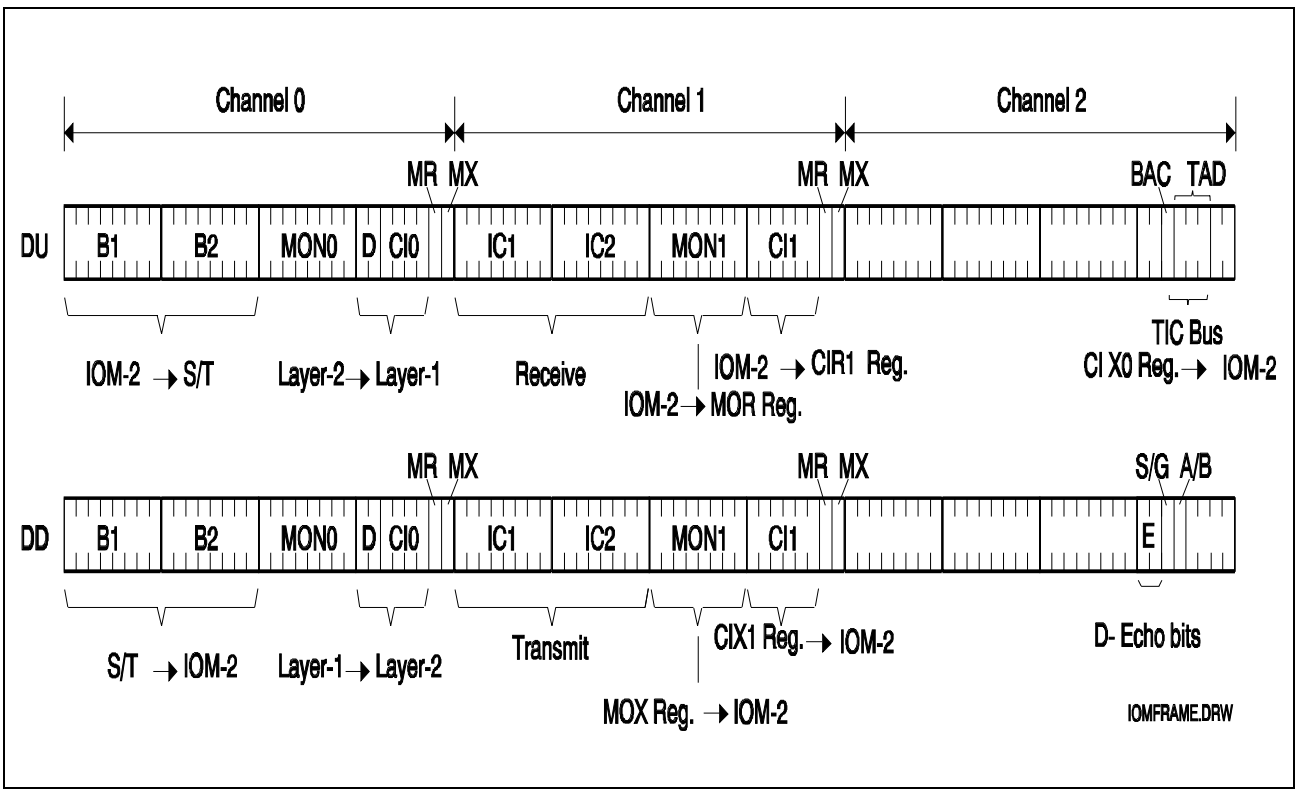



**Figure 49 IOM®-2 Frame Structure in Terminal Mode**

The frame is composed of three channels:

- Channel 0 contains 144-kbit/s of user and signaling data (2B + D), a MONITOR programming channel (MON0) and a command/indication channel (CI0) for control and programming of the layer-1 transceiver.
- Channel 1 contains two 64-kbit/s intercommunication channels (IC) plus a MONITOR and command/indicate channel (MON1, CI1) to program or transfer data to other IOM-2 devices.
- Channel 2 is used for the TIC-bus access. Only the command/indicate bits are specified in this channel.

### IOM-2 Frame Structure (LT-S, LT-T Modes)

This mode is used in LT-S and LT-T applications. The frame is a multiplex of up to eight IOM-2 channels (DCL = 4096 kHz, **Figure 50**), each of which has the structure described above.

The reset value for assignment to one of the eight channels (0 to 7) is done via pin strapping (CH0-2), however the host can reprogram the selected timeslot in DCH_TSDP.TSS.

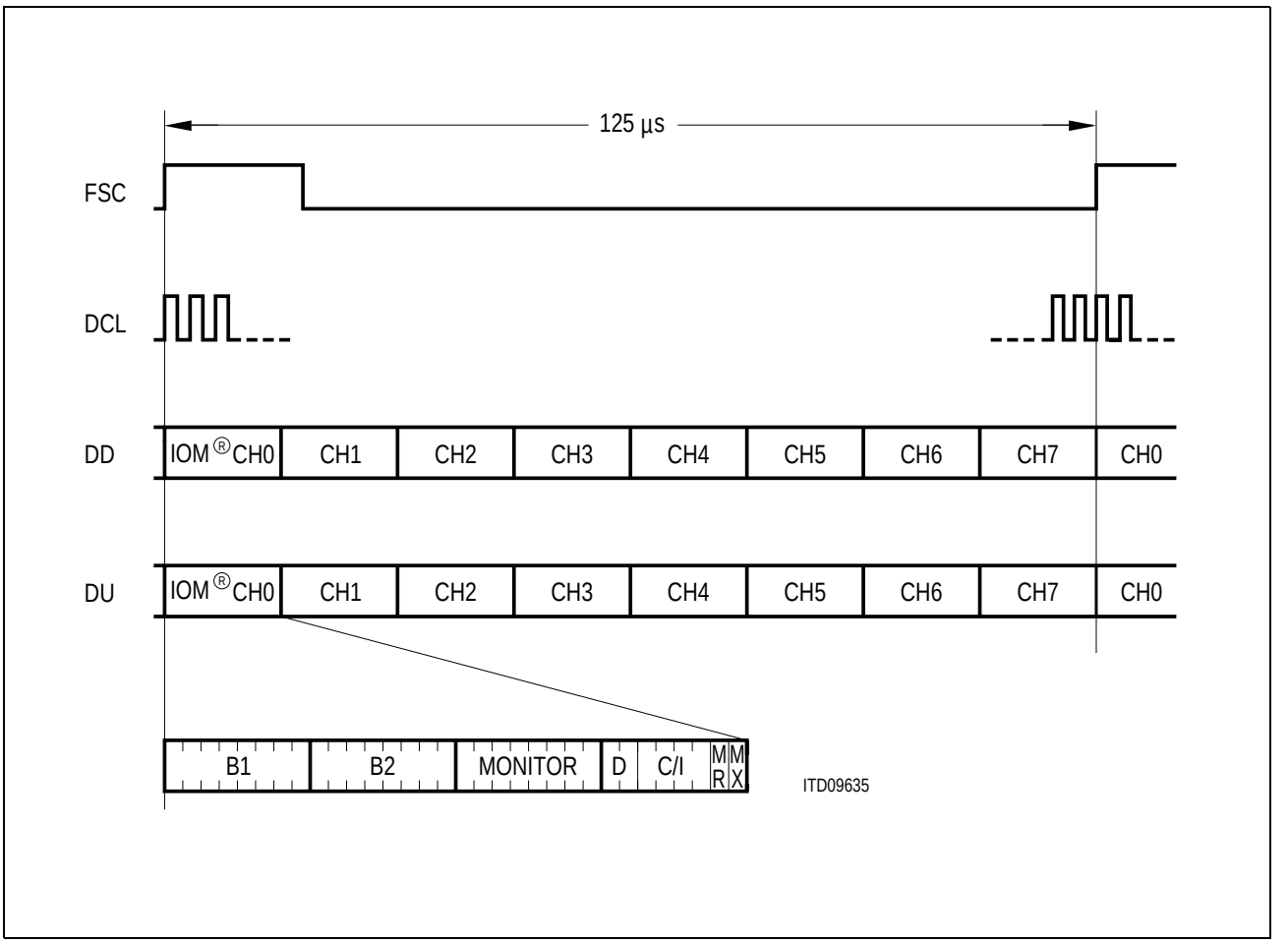



**Figure 50 Multiplexed Frame Structure of the IOM-2 Interface in Non-TE Timing Mode**

### IOM-2 Frame Structure (NT Mode)

In NT mode one IOM-2 channel is used (DCL=512 kHz). The channel structure is the same as described above.

### 3.7.1 IOM-2 Handler

The IOM-2 handler offers a great flexibility for handling the data transfer between the different functional units of the IPAC-X and voice/data devices connected to the IOM-2 interface. Additionally it provides a microcontroller access to all timeslots of the IOM-2 interface via the four controller data access registers (CDA). **Figure 51** shows the architecture of the IOM-2 handler. For illustrating the functional description it contains all configuration and control registers of the IOM-2 handler. A detailed register description can be found in **Chapter 4.4.**

The PCM data of the functional units

- Transceiver (TR) and the
- Controller data access (CDA)
- B-channel HDLC controllers

can be configured by programming the time slot and data port selection registers (TSDP). With the TSS bits (Time Slot Selection) the PCM data of the functional units can be assigned to each of the 32 PCM time slots of the IOM-2 frame. With the DPS bit (Data Port Selection) the output of each functional unit is assigned to DU or DD respectively. The input is assigned vice versa. With the data control registers (xxx_CR) the access to the data of the functional units can be controlled by setting the corresponding control bits (EN, SWAP).

The IOM-2 handler also provides access to the

- MONITOR channel (MON)
- C/I channels (C/I0,C/I1)
- TIC bus (TIC) and
- HDLC control

The access to these channels is controlled by the registers MON_CR, DCI_CR and BCHx_CR.
The IOM-2 interface with the two Serial Data Strobes (SDS1,2) is controlled by the control registers IOM_CR, SDS1_CR and SDS2_CR.

The reset configuration of the IPAC-X IOM-2 handler corresponds to the defined frame structure and data ports of a master device in IOM-2 terminal mode (see **Figure 49**).

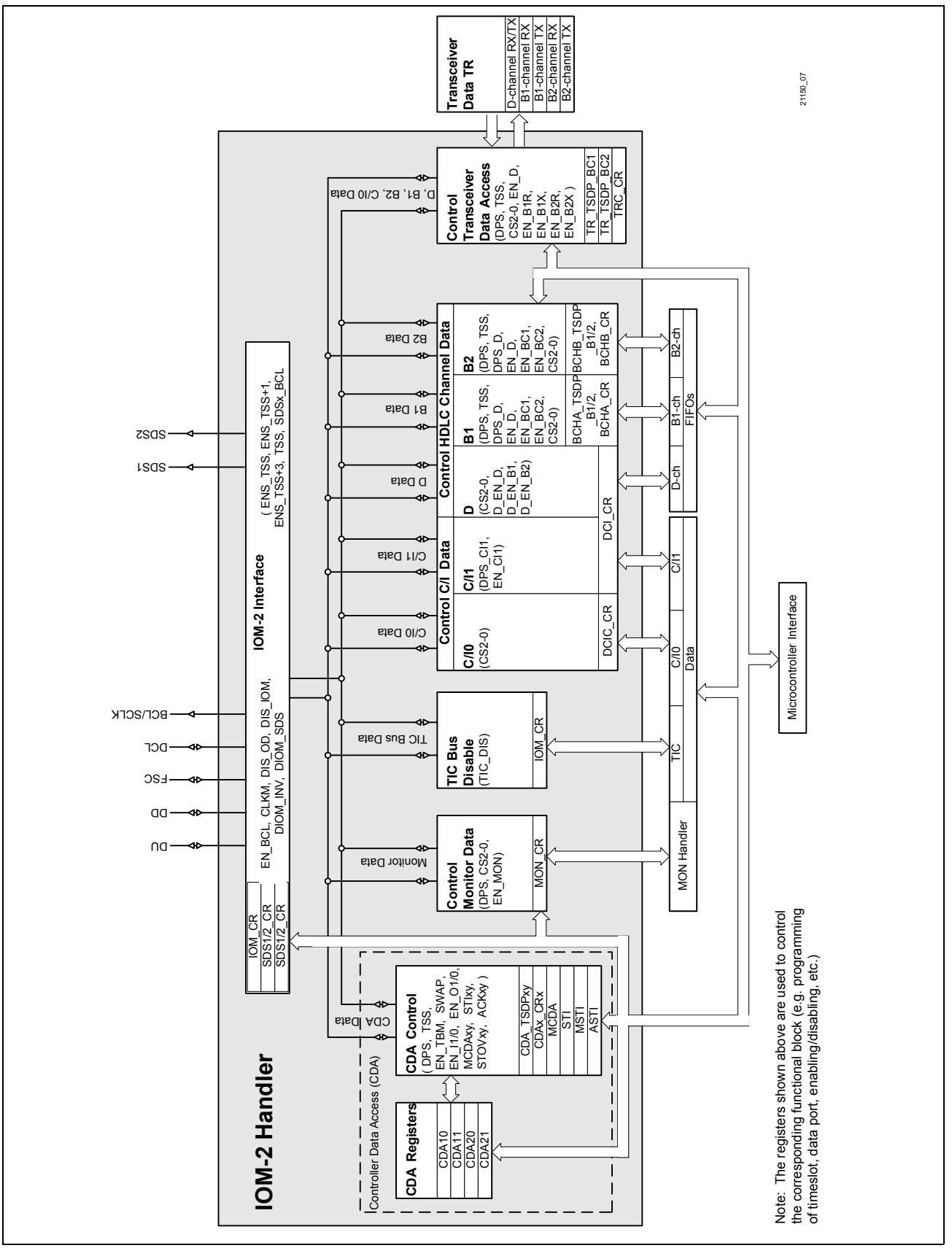



**Figure 51 Architecture of the IOM Handler (Example Configuration)**

### 3.7.1.1 Controller Data Access (CDA)

With its four controller data access registers (CDA10, CDA11, CDA20, CDA21) the IPAC-X IOM-2 handler provides a very flexible solution for the host access to up to 32 IOM-2 time slots.

The functional unit CDA (controller data access) allows with its control and configuration registers

- Looping of up to four independent PCM channels from DU to DD or vice versa over the four CDA registers
- Shifting of two independent PCM channels to another two independent PCM channels on both data ports (DU, DD). Between reading and writing the data can be manipulated (processed with an algorithm) by the microcontroller. If this is not the case a switching function is performed
- Monitoring of up to four time slots on the IOM-2 interface simultaneously
- Microcontroller read and write access to each PCM timeslot

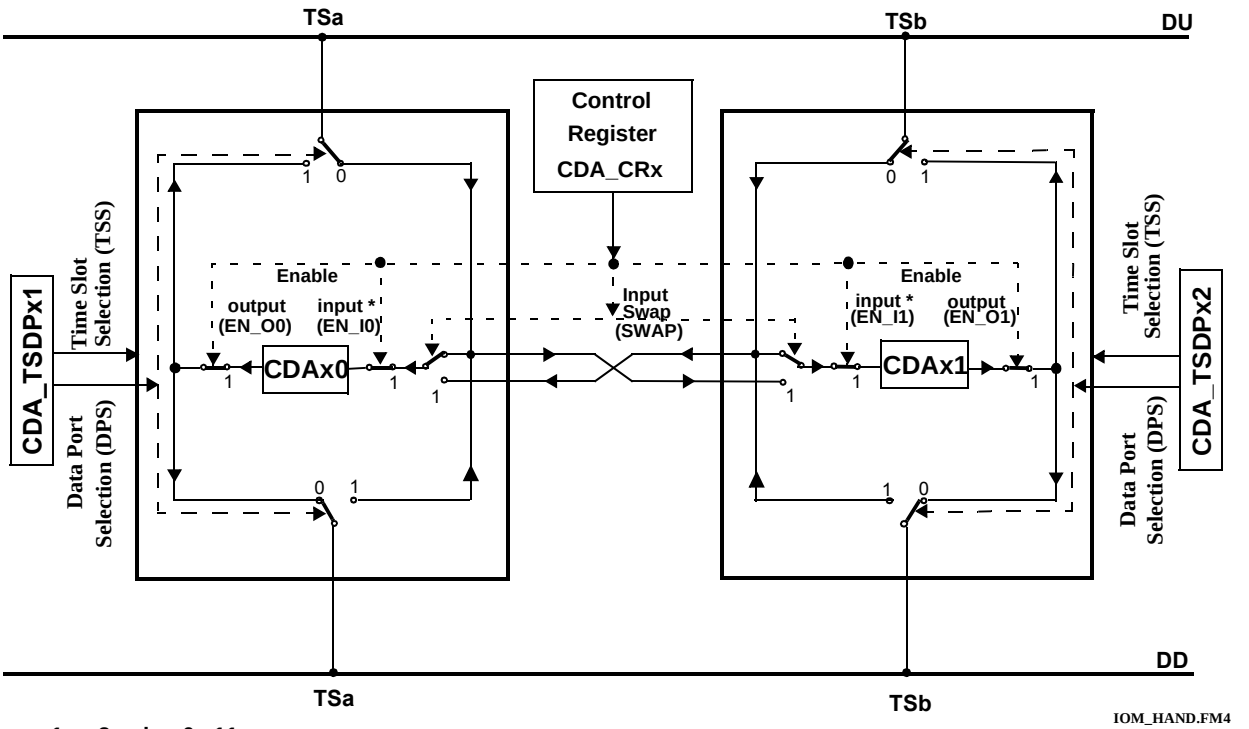
The access principle which is identical for the two channel register pairs CDA10/11 and CDA20/21 is illustrated in **Figure 52**. Each of the index variables x,y used in the following description can be 1 or 2 for x and 0 or 1 for y. The prefix ’CDA_’ from the register names has been omitted for simplification.

To each of the four CDAxy data registers a TSDPxy register is assigned by which the time slot and the data port can be determined. With the TSS (Time Slot Selection) bits a time slot from 0...31 can be selected. With the DPS (Data Port Selection) bit the output of the CDAxy register can be assigned to DU or DD respectively. The time slot and data port for the output of CDAxy is always defined by its own TSDPxy register. The input of CDAxy depends on the SWAP bit in the control registers CRx.

- If the SWAP bit = ’0’ (swap is disabled) the time slot and data port for the input and output of the CDAxy register is defined by its own TSDPxy register.
- If the SWAP bit = ’1’ (swap is enabled) the input port and timeslot of the CDAx0 is defined by the TSDP register of CDAx1 and the input port and timeslot of CDAx1 is defined by the TSDP register of CDAx0. The input definition for timeslot and data port CDAx0 are thus swapped to CDAx1 and for CDAx1 swapped to CDAx0. The output timeslots are not affected by SWAP.

The input and output of every CDAxy register can be enabled or disabled by setting the corresponding EN (-able) bit in the control register CDAx_CR. If the input of a register is disabled the output value in the register is retained.

Usually one input and one output of a functional unit (transceiver, HDLC controllers, CDA register) is programmed to a timeslot on IOM-2 (e.g. for B-channel transmission in upstream direction the HDLC controller writes data onto IOM and the transceiver reads data from IOM). For monitoring data in such cases a CDA register is programmed as described below under “Monitoring Data”. Besides that none of the IOM timeslots must be assigned more than one input and output of any functional unit.




x = 1 or 2; a,b = 0...11

*) In the normal mode (SWAP=0) the input of CDAx0 and CDAx1 is enabled via EN_I0 and EN_I1, respectively. If SWAP=1 EN_I0 controls the input of CDAx1 and EN_I1 controls the input of CDAx0. The output control (EN_O0 and EN_O1) is not affected by SWAP.

**Figure 52 Data Access via CDAx1 and CDAx2 Register Pairs**

### Looping and Shifting Data

Figure 53 gives examples for typical configurations with the above explained control and configuration possibilities with the bits TSS, DPS, EN and SWAP in the registers TSDPxy or CDAx_CR:

a) Looping IOM-2 time slot data from DU to DD or vice versa (SWAP = 0)

b) Shifting data from TSa to TSb and TSc to TSd in both transmission directions (SWAP = 1)

c) Switching data from TSa to TSb and looping from DU to DD or TSc to TSd and looping from DD to DU respectively

TSa is programmed in TSDP10, TSb in TSDP11, TSc in TSDP20 and TSd in TSDP21. It should also be noted that the input control of CDA registers is swapped if SWAP=1 while the output control is not affected (e.g. for CDA11 in example a: EN_I1=1 and EN_O1=1, whereas for CDA11 in example b: EN_I0=1 and EN_O1=1).

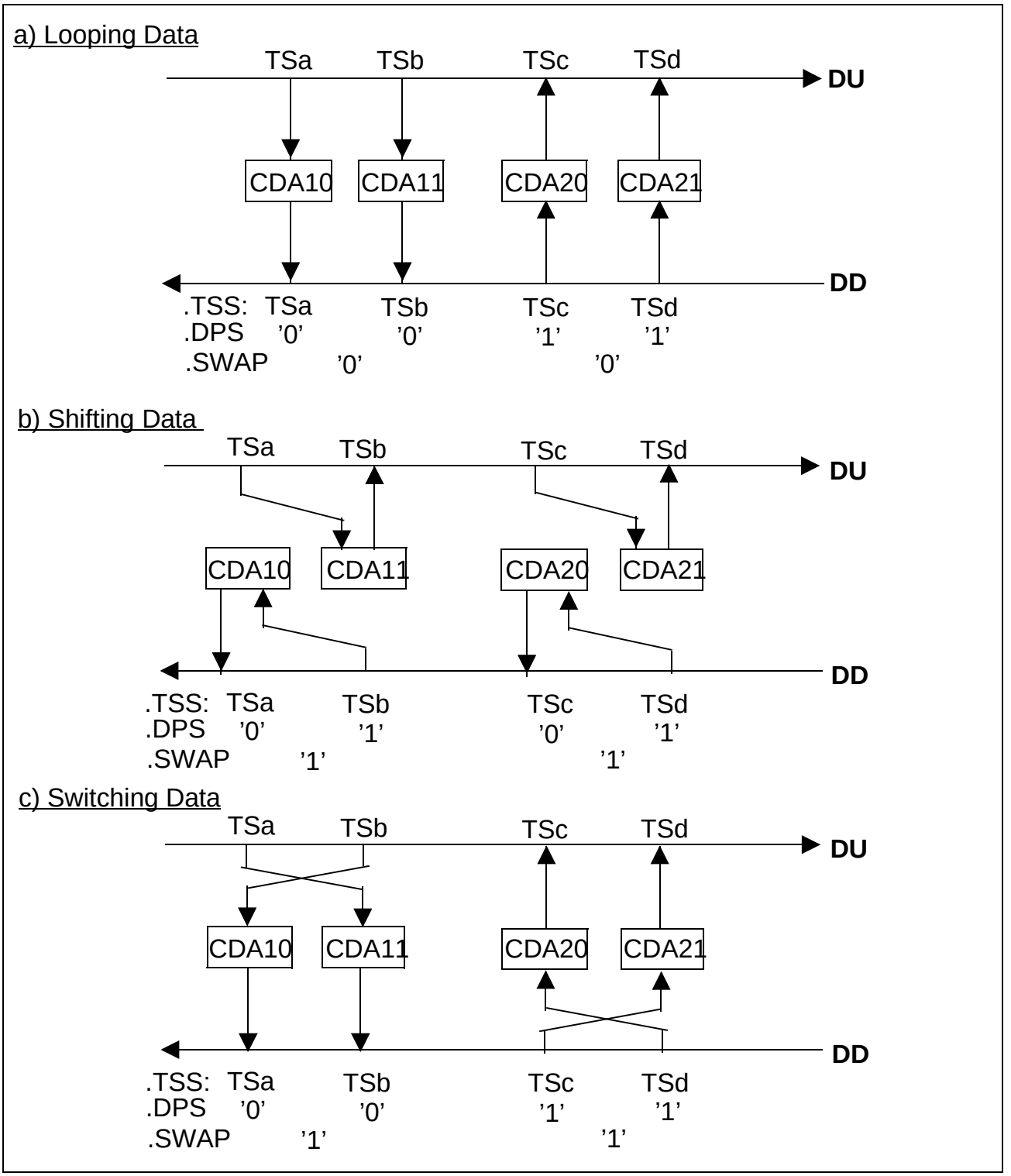



**Figure 53 Examples for Data Access via CDAxy Registers**

a) Looping Data
b) Shifting (Switching) Data
c) Switching and Looping Data

**Figure 54** shows the timing of looping TSa from DU to DD (a = 0...11) via CDAxy register. TSa is read in the CDAxy register from DU and is written one frame later on DD.

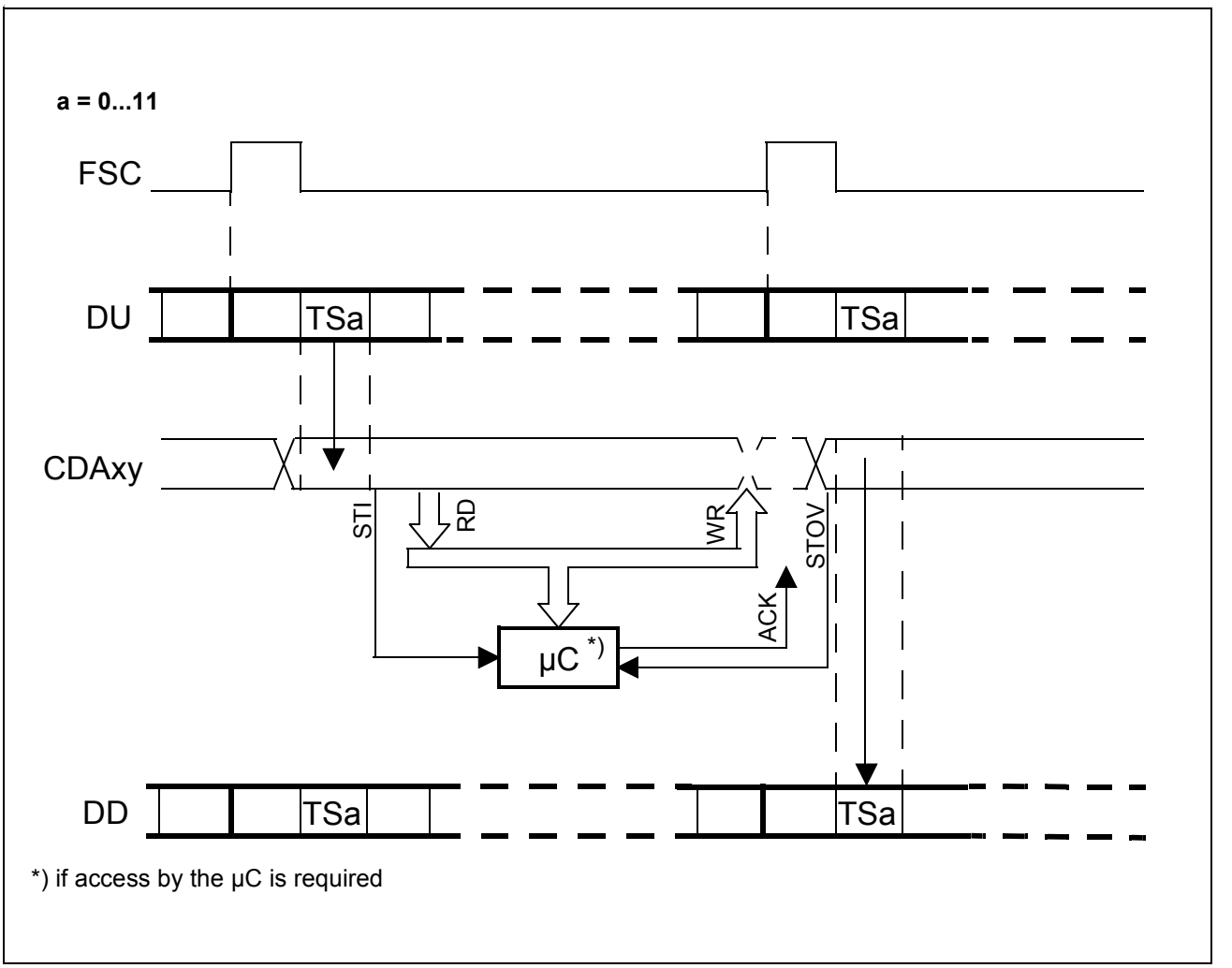



**Figure 54 Data Access when Looping TSa from DU to DD**

**Figure 55** shows the timing of shifting data from TSa to TSb on DU(DD). In **Figure 55a)** shifting is done in one frame because TSa and TSb didn't succeed direct one another (a,b = 0...9 and b ≥ a+2. In **Figure 55b)** shifting is done from one frame to the following frame. This is the case when the time slots succeed one other (b = a+1) or b is smaller than a (b < a).

At looping and shifting the data can be accessed by the controller between the synchronous transfer interrupt (STI) and the status overflow interrupt (STOV). STI and STOV are explained in the section 'Synchronous Transfer'. If there is no controller intervention the looping and shifting is done autonomous.

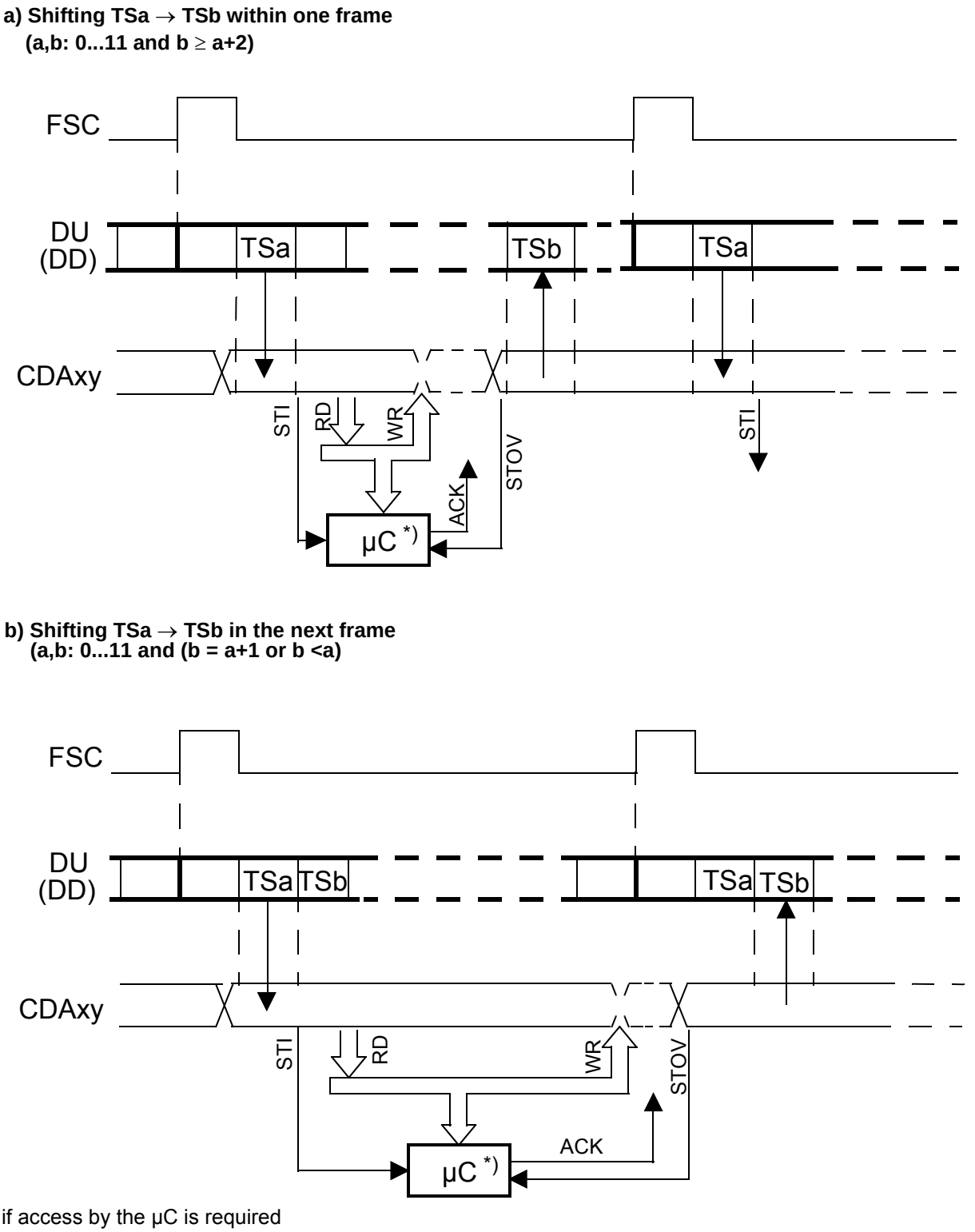



**Figure 55 Data Access When Shifting TSa to TSb on DU (DD)**

### Monitoring Data

**Figure 56** gives an example for monitoring of two IOM-2 time slots each on DU or DD simultaneously. For monitoring on DU and/or DD the channel registers with even numbers (CDA10, CDA20) are assigned to time slots with even numbers TS(2n) and the channel registers with odd numbers (CDA11, CDA21) are assigned to time slots with odd numbers TS(2n+1). The user has to take care of this restriction by programming the appropriate time slots..

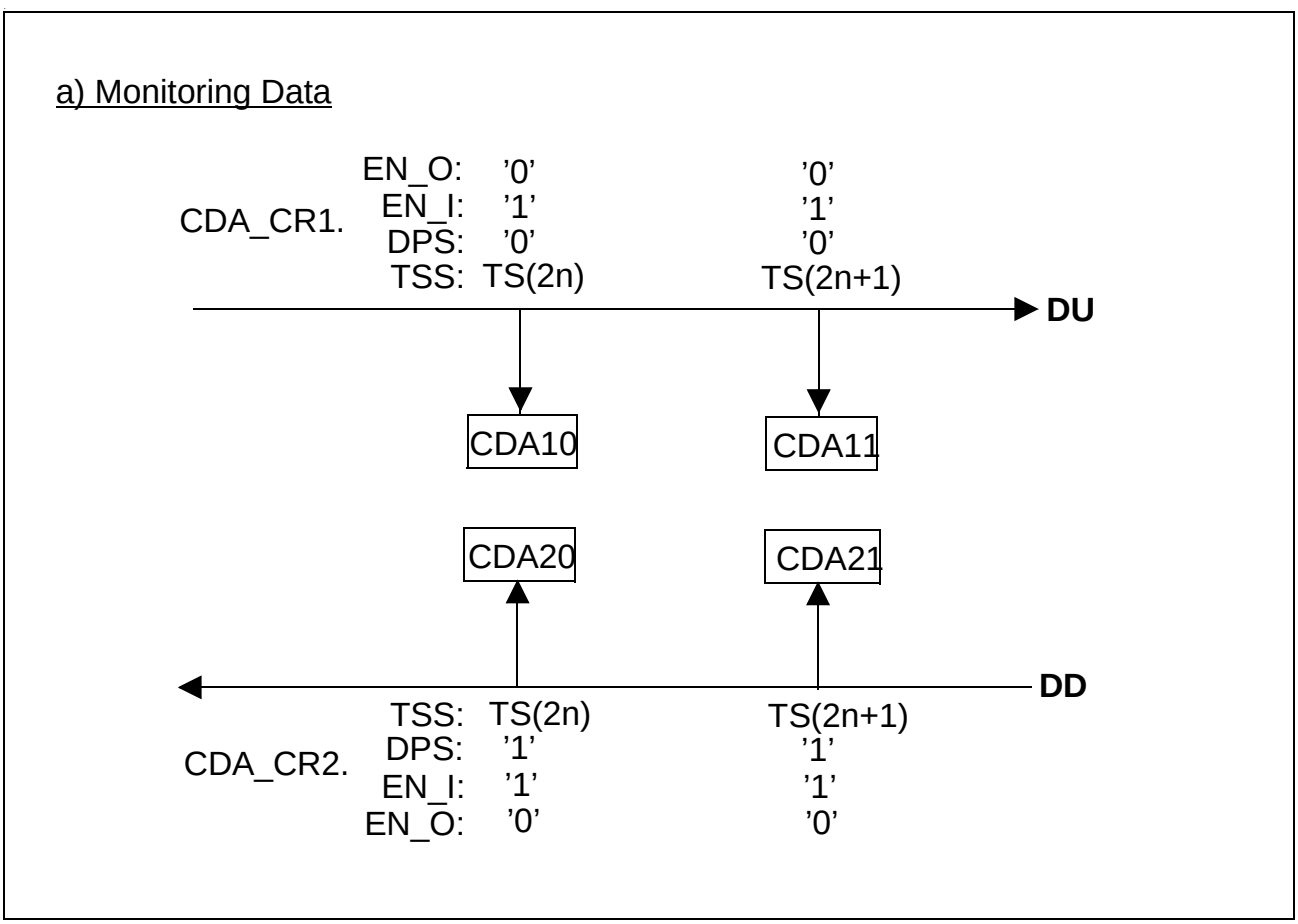



**Figure 56 Example for Monitoring Data**

### Monitoring TIC Bus

Monitoring the TIC bus (TS11) is handled as a special case. The TIC bus can be monitored with the registers CDAx0 by setting the EN_TBM (Enable TIC Bus Monitoring) bit in the control registers CRx. In this special case the TSDPx0 must be set to $08_h$ for monitoring from DU or $88_h$ for monitoring from DD respectively. By this it is possible to monitor the TIC bus (TS11) and the odd numbered D-channel (TS3) simultaneously on DU and DD.

### Synchronous Transfer

While looping, shifting and switching the data can be accessed by the controller between the synchronous transfer interrupt (STI) and the status overflow interrupt (STOV).

The microcontroller access to the CDAxy registers can be synchronized by means of four programmable synchronous transfer interrupts (STIxy)[1] and synchronous transfer overflow interrupts (STOVxy) [2] in the STI register.

Depending on the DPS bit in the corresponding CDA_TSDPxy register the STIxy is generated two (for DPS='0') or one (for DPS='1') BCL clock after the selected time slot (CDA_TSDPxy.TSS). One BCL clock is equivalent to two DCL clocks.

In the following description the index $xy_0$ and $xy_1$ are used to refer to two different interrupt pairs (STI/STOV) out of the four CDA interrupt pairs (STI10/STOV10, STI11/ STOV11, STI20/STOV20, STI21/STOV21).

An $STOVxy_0$ is related to its $STIxy_0$ and is only generated if $STIxy_0$ is enabled and not acknowledged. However, if $STIxy_0$ is masked, the $STOVxy_0$ is generated for any other $STIxy_1$ which is enabled and not acknowledged.

**Table 10** gives some examples for that. It is assumed that an STOV interrupt is only generated because an STI interrupt was not acknowledged before.

In example 1 only the $STIxy_0$ is enabled and thus $STIxy_0$ is only generated. If no STI is enabled, no interrupt will be generated even if STOV is enabled (example 2).

In example 3 $STIxy_0$ is enabled and generated and the corresponding $STOVxy_0$ is disabled. $STIxy_1$ is disabled but its $STOVxy_1$ is enabled, and therefore $STOVxy_1$ is generated due to $STIxy_0$. In example 4 additionally the corresponding $STOVxy_0$ is enabled, so $STOVxy_0$ and $STOVxy_1$ are both generated due to $STIxy_0$.

In example 5 additionally the $STIxy_1$ is enabled with the result that $STOVxy_0$ is only generated due to $STIxy_0$ and $STOVxy_1$ is only generated due to $STIxy_1$.

Compared to the previous example $STOVxy_0$ is disabled in example 6, so $STOVxy_0$ is not generated and $STOVxy_1$ is only generated for $STIxy_1$ but not for $STIxy_0$.

Compared to example 5 in example 7 a third $STOVxy_2$ is enabled and thus STOVxy2 is generated additionally for both $STIxy_0$ and $STIxy_1$.

1) In order to enable the STI interrupts the input of the corresponding CDA register has to be enabled. This is also valid if only a synchronous write access is wanted. The enabling of the output alone does not effect an STI interrupt.

2) In order to enable the STOV interrupts the output of the corresponding CDA register has to be enabled. This is also valid if only a synchronous read access is wanted. The enabling of the input alone does not effect an interrupt.

**Table 10 Examples for Synchronous Transfer Interrupts**

| Enabled Interrupts (Register MSTI) | | Generated Interrupts (Register STI) | | |
|---|---|---|---|---|
| **STI** | **STOV** | **STI** | **STOV** | |
| $xy_0$ | - | $xy_0$ | - | Example 1 |
| - | $xy_0$ | - | - | Example 2 |
| $xy_0$ | $xy_1$ | $xy_0$ | $xy_1$ | Example 3 |
| $xy_0$ | $xy_0$ ; $xy_1$ | $xy_0$ | $xy_0$ ; $xy_1$ | Example 4 |
| $xy_0$ ; $xy_1$ | $xy_0$ ; $xy_1$ | $xy_0$<br>$xy_1$ | $xy_0$<br>$xy_1$ | Example 5 |
| $xy_0$ ; $xy_1$ | $xy_1$ | $xy_0$<br>$xy_1$ | -<br>$xy_1$ | Example 6 |
| $xy_0$ ; $xy_1$ | $xy_0$ ; $xy_1$ ; $xy_2$ | $xy_0$<br>$xy_1$ | $xy_0$ ; $xy_2$<br>$xy_1$ ; $xy_2$ | Example 7 |

An STOV interrupt is not generated if all stimulating STI interrupts are acknowledged.

An STIxy must be acknowledged by setting the ACKxy bit in the ASTI register until two BCL clocks (for DPS='0') or one BCL clocks (for DPS='1') before the time slot which is selected for the appropriate STIxy.

The interrupt structure of the synchronous transfer is shown in **Figure 57**.

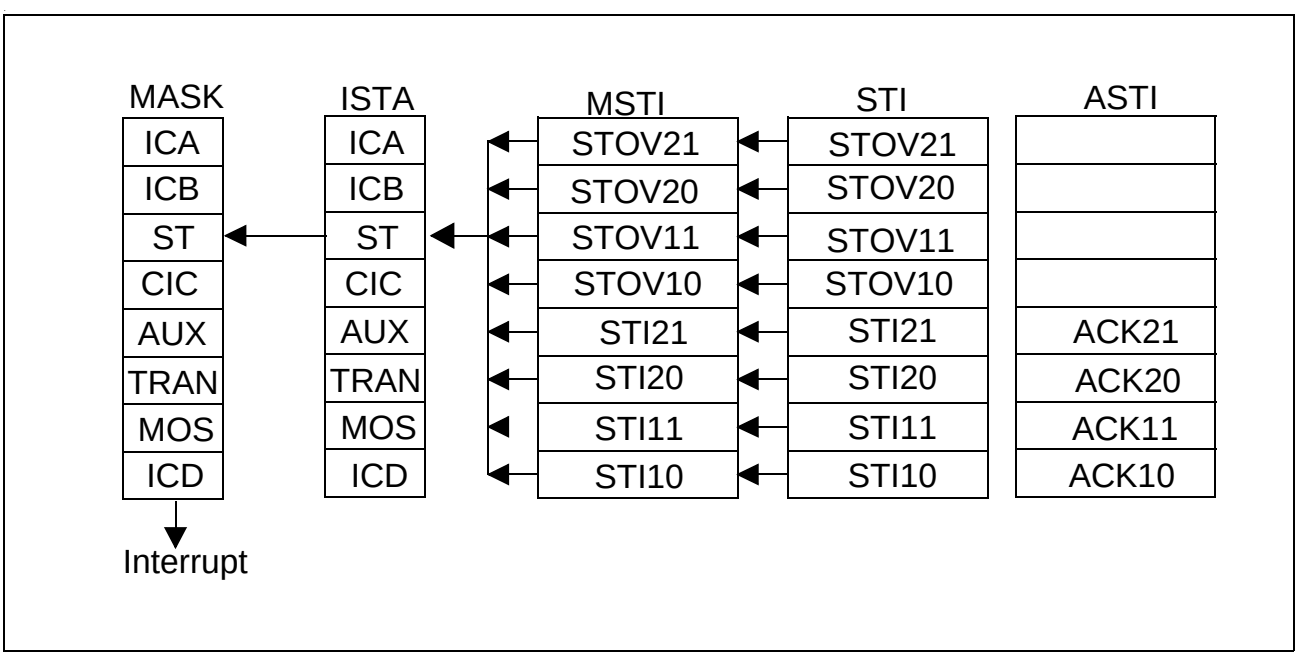



**Figure 57 Interrupt Structure of the Synchronous Data Transfer**

**Figure 58** shows some examples based on the timeslot structure. Figure a) shows at which point in time an STI and STOV interrrupt is generated for a specific timeslot. Figure b) is identical to example 3 above, figure c) corresponds to example 5 and figure d) shows example 4.

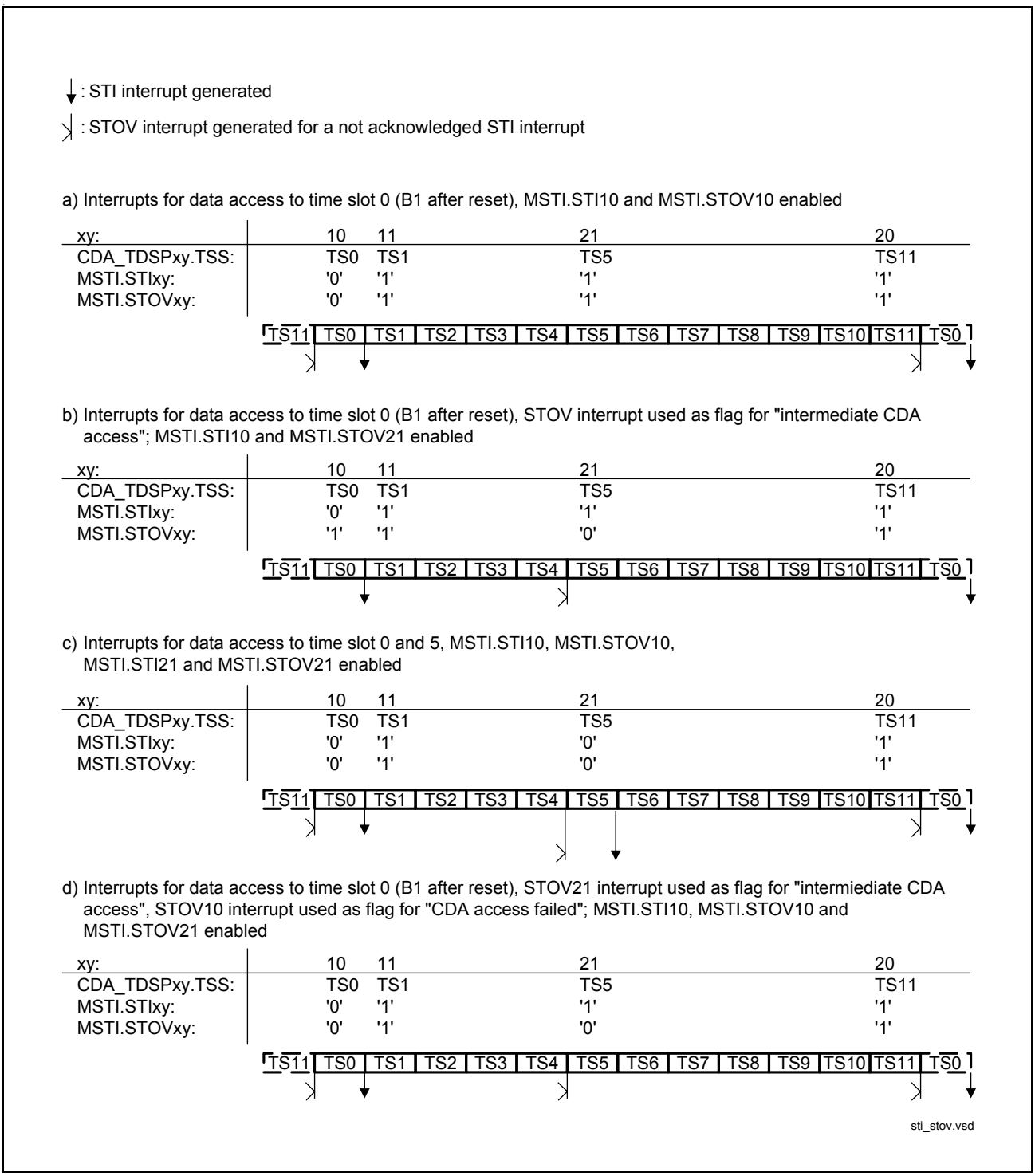



**Figure 58 Examples for the Synchronous Transfer Interrupt Control With One Enabled STIxy**

### Restrictions Concerning Monitoring and Shifting Data

Due to the hardware design, there are some restrictions for the CDA shifting data function and for the CDA monitoring data function. The selection of the CDA registers is restricted if other functional blocks of the IPAC-X (transceiver cores, HDLC controllers, CI handler, Monitor handler, TIC bus etc.) access the corresponding timeslot.

If no functional block is assigned to a certain timeslot, any CDA register can be used for monitoring or shifting it.

If a timeslot is already occupied by a functional block in a certain transmission direction, only CDA registers with odd numbers (CDA11/21) can be assigned to odd timeslots and CDA registers with even numbers (CDA10/20) can be assigned to even timeslots in the same transmission direction. For the other transmission direction every CDA register can be used. (Example: If TS 5 is already occupied in DD direction, only CDA11 and 21 can be used for monitoring it. For monitoring TS 5 in DU direction, also CDA10 or CDA20 could be used.)

If above guideline is not considered, data can be overwritten in corresponding timeslots. In this context no general rules can be derived in which way the data are overwritten.

The usage of the looping data and switching data functions are unrestricted.

### Restrictions Concerning Read/Write Access

If data shall be read out from a certain transmission direction and other data shall be written in the opposite transmission direction in the same timeslot, only special CDA register combinations can be used. The correct behavior can be achieved with the following CDA register combinations:

**Table 11 CDA Register Combinations with Correct Read/Write Access**

| CDA Register Combination | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| Data of the downstream timeslot is read by | CDA10 | CDA11 | CDA20 | CDA21 |
| Data is written to the upstream timeslot from | CDA20 | CDA21 | CDA10 | CDA11 |

With other register combinations unintended loops or erroneous monitorings can occur or wrong data is written to the IOM interface.

### Unexpected Write/Read Behavior of CDA Registers

If inputs and outputs are disabled, the programmed values of CDA10/11/20/21 registers cannot be read back. Instead of the expected value the content of the previous programming can be read out. The programmed value ($5A_H$ in the following example) will be fetched if the output is enabled.

**Example:**

w CDA1_CR = $00_H$ (inputs and outputs are disabled)
w CDA10 = $5A_H$ (example)
r CDA10 = $FF_H$ (old value of previous programming)
w CDA1_CR = $02_H$ (output of CDA10 is enabled)
r CDA10 = $5A_H$ (the programmed value can be read back)

### 3.7.1.2 IDSL Support

#### IOM-2 Interface

The IOM handler of the IPAC-X provides a flexible access of the B-channel HDLC controllers to the timeslots on IOM-2 which may be used for IDSL applications.

One of the two B-channel HDCL controllers is programmed to transparent mode and its FIFO is programmed to certain timeslot on IOM-2, while the second B-channel controller and the D-channel controller is unused (**Figure 59**)

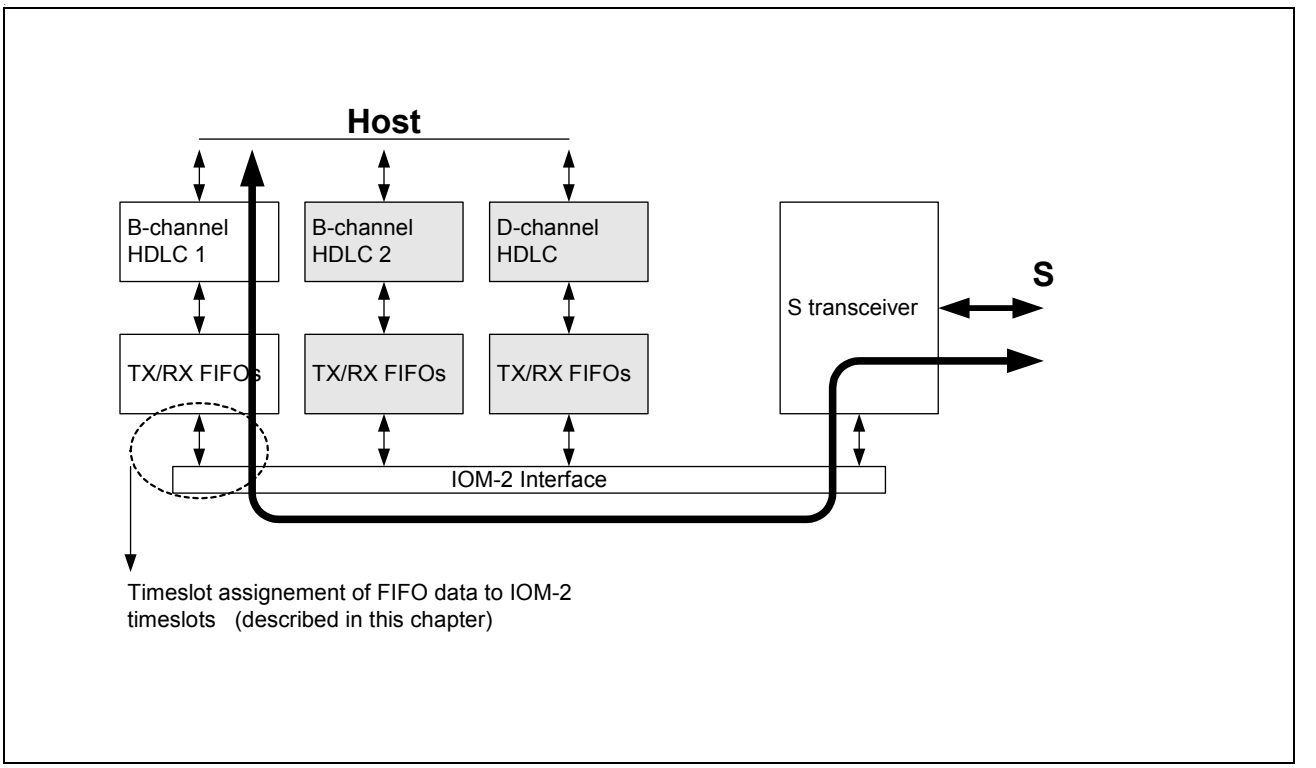



**Figure 59 Timeslot Assignment on IOM-2**

This B-channel HDLC controller is assigned to three timeslots on IOM-2, which are two 8-bit timeslots and one 2-bit timeslot. For each of the 3 timeslots the timeslot position (timeslot number) and data port (DU, DD) can individually be selected. Additionally, each of the 3 timeslots can individually be enabled/disabled so any combination of the 3

timeslots can be configured, i.e. during each FSC frame the HDLC/FIFO will access 2 bit, 8 bit, 10 bit, 16 bit or 18 bit.

Some examples for access to IOM timeslots are given in **Figure 60**:

- Example 1 shows 18-bit access to B1 + B2 + D
- Example 2 shows 10-bit access to B2 + D
- Example 3 shows 10-bit access to B1 + D in channel 1
- Example 4 shows 16-bit access to MON0 + MON1.

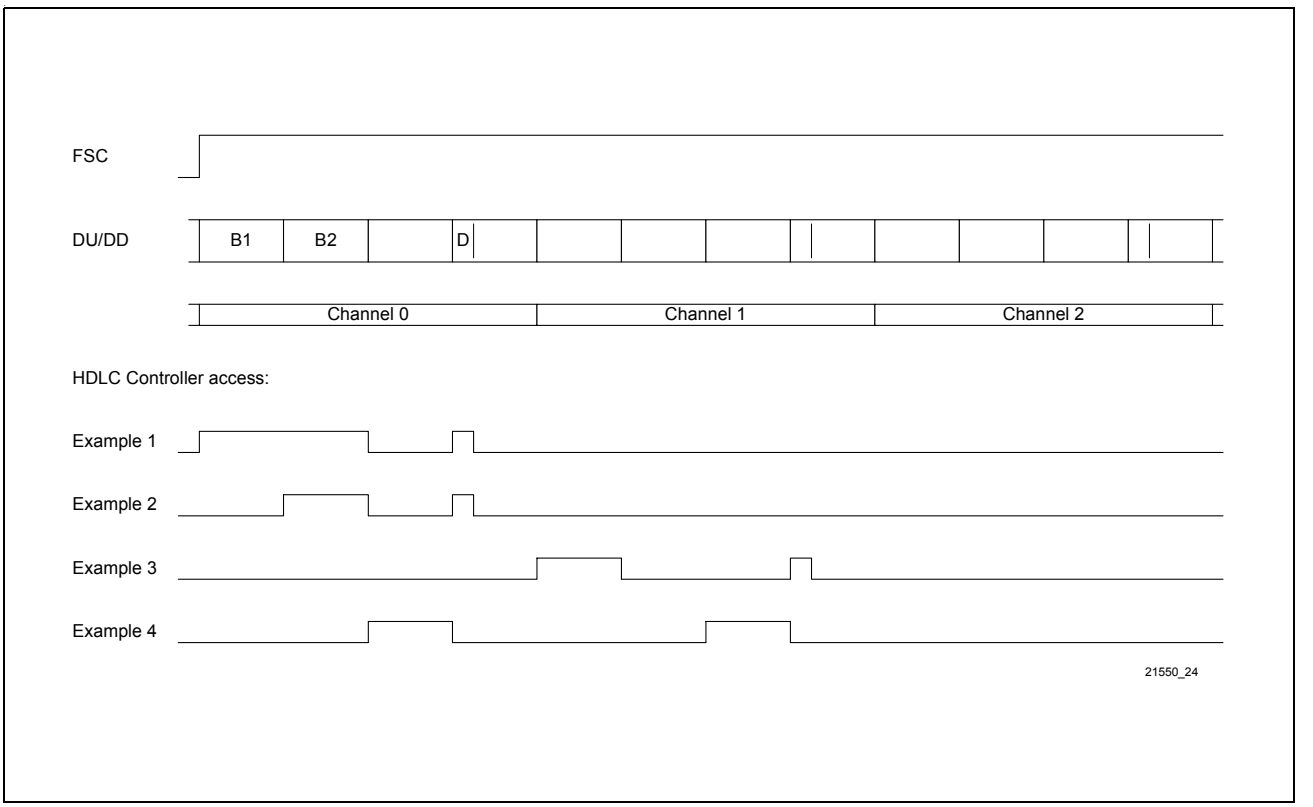



**Figure 60 Examples for HDLC Controller Access**

The following registers are used to configure one of the two B-channel HDLC controllers (channel A or B) for that (x = A or B):

- BCHx_TSDP_BC1 consists of bits for timeslot selection (TSS) and data port selection (DPS) to program the first 8-bit timeslot.
- BCHx_TSDP_BC2 consists of bits for timeslot selection (TSS) and data port selection (DPS) to program the second 8-bit timeslot.
- BCHx_CR consists of bits for channel selection (CS2-0) and data port selection (DPS_D) to program the 2-bit timeslot. Another 3 bits are used to selectively enable/ disable the first 8-bit timeslot (EN_BC1), the second 8-bit timeslot (EN_BC2) and the 2-bit timeslot (EN_D).

## S Interface

Data which is read from and written to the IOM-2 interface by the B-channel controller as described in the previous chapter is received from and transmitted to the S interface (**Figure 61**).

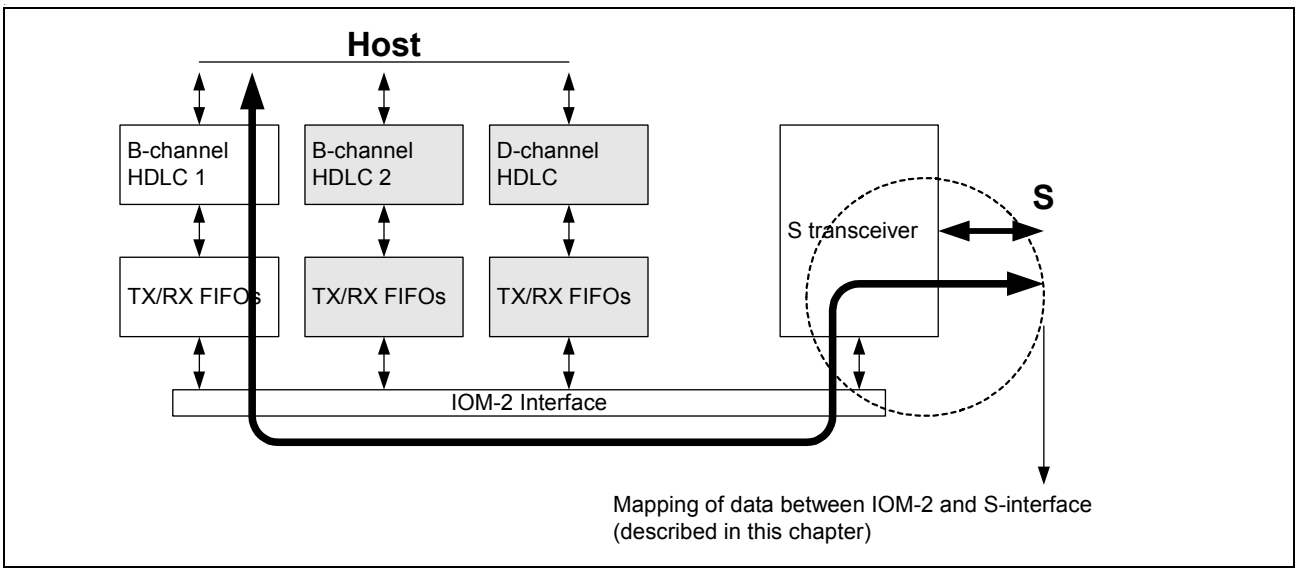



**Figure 61 Timeslot Assignment on S**

As the timeslot structure of the IOM-2 interface is different from the S interface, it is important to consider the delay and mapping of data between both interfaces.

**Figure 61** shows the example for bundling 2B+D channels for transmission of 144 kbit/s. Serial data from the FIFO is mapped to the corresponding B- and D-channel timeslots on IOM-2.

The ITU I.430 specifies the order and timeslot position of B- and D-channel data on the S-frame. Due to that the order of B- and D-channel data on S is different from IOM-2 which has the effect that mapping of data from IOM-2 to S will change the original order of the serial data stream. However, this has no effect as the remote receiver is using the same mechanism for mapping data between S and IOM-2. In IPAC-X B- and D-channel bits of one IOM-frame are mapped to the corresponding timeslots of the same S-frame.

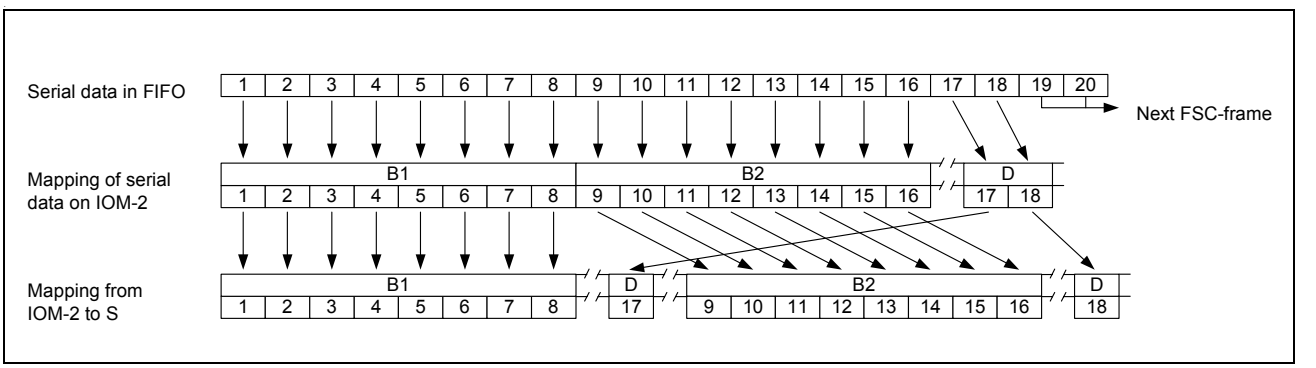



**Figure 62 Mapping of Bits from IOM-2 to S**

### 3.7.2 Serial Data Strobe Signal and Strobed Data Clock

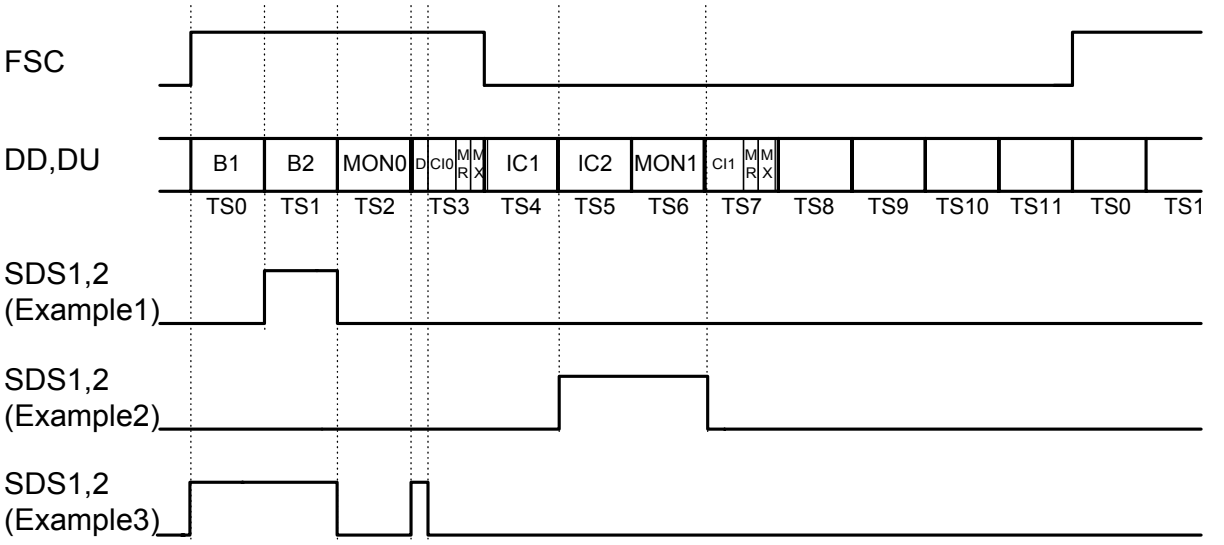
For timeslot oriented standard devices connected to the IOM-2 interface the IPAC-X provides two independent data strobe signals SDS1 and SDS2. Instead of a data strobe signal a strobed IOM-2 bit clock can be provided on pin SDS1 and SDS2.

#### 3.7.2.1 Serial Data Strobe Signal

The two strobe signals can be generated with every 8-kHz frame and are controlled by the registers SDS1/2_CR. By programming the TSS bits and three enable bits (ENS_TSS, ENS_TSS+1, ENS_TSS+3) a data strobe can be generated for the IOM-2 time slots TS, TS+1 and TS+3 and any combination of them.

The data strobes for TS and TS+1 are always 8 bits long (bit7 to bit0) whereas the data strobe for TS+3 is always 2 bits long (bit7, bit6).

**Figure 63** shows three examples for the generation of a strobe signal. In example 1 the SDS is active during channel B2 on IOM-2 whereas in the second example during IC2 and MON1. The third example shows a strobe signal for 2B+D channels which can be used e.g. for an IDSL (144kbit/s) transmission.




Example 1: TSS = '$0_H$'
ENS_TSS = '0'
ENS_TSS+1 = '1'
ENS_TSS+3 = '0'

Example 2: TSS = '$5_H$'
ENS_TSS = '1'
ENS_TSS+1 = '1'
ENS_TSS+3 = '0'

Example 3: TSS = '$0_H$'
ENS_TSS = '1'
ENS_TSS+1 = '1'
ENS_TSS+3 = '1'

strobe.vsd

For all examples SDS_CONF.SDS1/2_BCL must be set to “0”.

**Figure 63 Data Strobe Signal**

### 3.7.2.2 Strobed IOM-2 Bit Clock

The strobed IOM-2 bit clock is active during the programmed window. Outside the programmed window a ’0’ is driven. Two examples are shown in **Figure 64**.

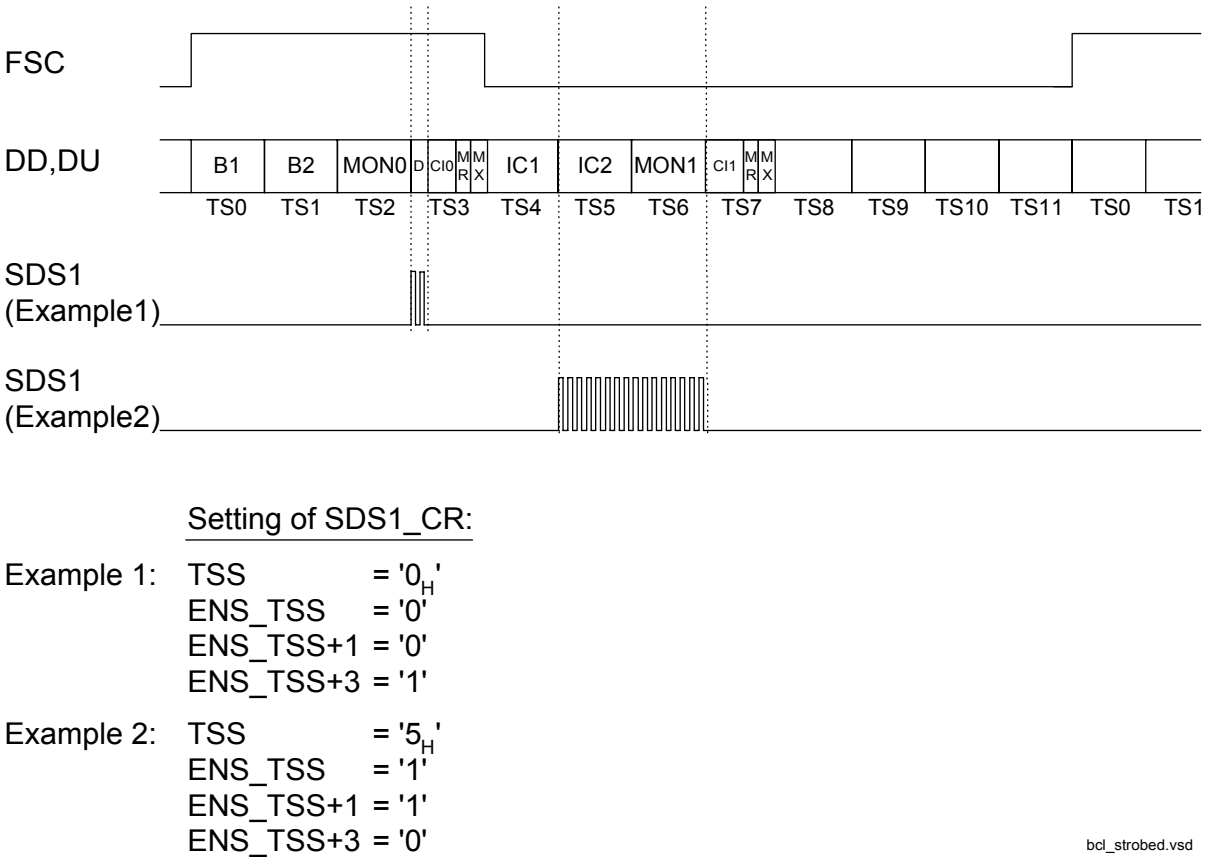



**Figure 64 Strobed IOM-2 Bit Clock. Register SDS_CONF Programmed to $01_H$**

The strobed bit clock can be enabled in SDS_CONF.SDS1/2_BCL.

### 3.7.3 IOM-2 Monitor Channel

The IOM-2 MONITOR channel (see **Figure 65**) is utilized for information exchange in the MONITOR channel between a master mode device and a slave mode device.

The MONTIOR channel data can be controlled by the bits in the MONITOR control register (MON_CR). For the transmission of the MONITOR data one of the IOM-2 channels (3 IOM-2 channels in TE mode, 8 channels in non TE mode) can be selected by setting the MONITOR channel selection bits (MCS) in the MONITOR control register (MON_CR).

The DPS bit in the same register selects between an output on DU or DD respectively and with EN_MON the MONITOR data can be enabled/disabled. The default value is MONITOR channel 0 (MON0) enabled and transmission on DD.

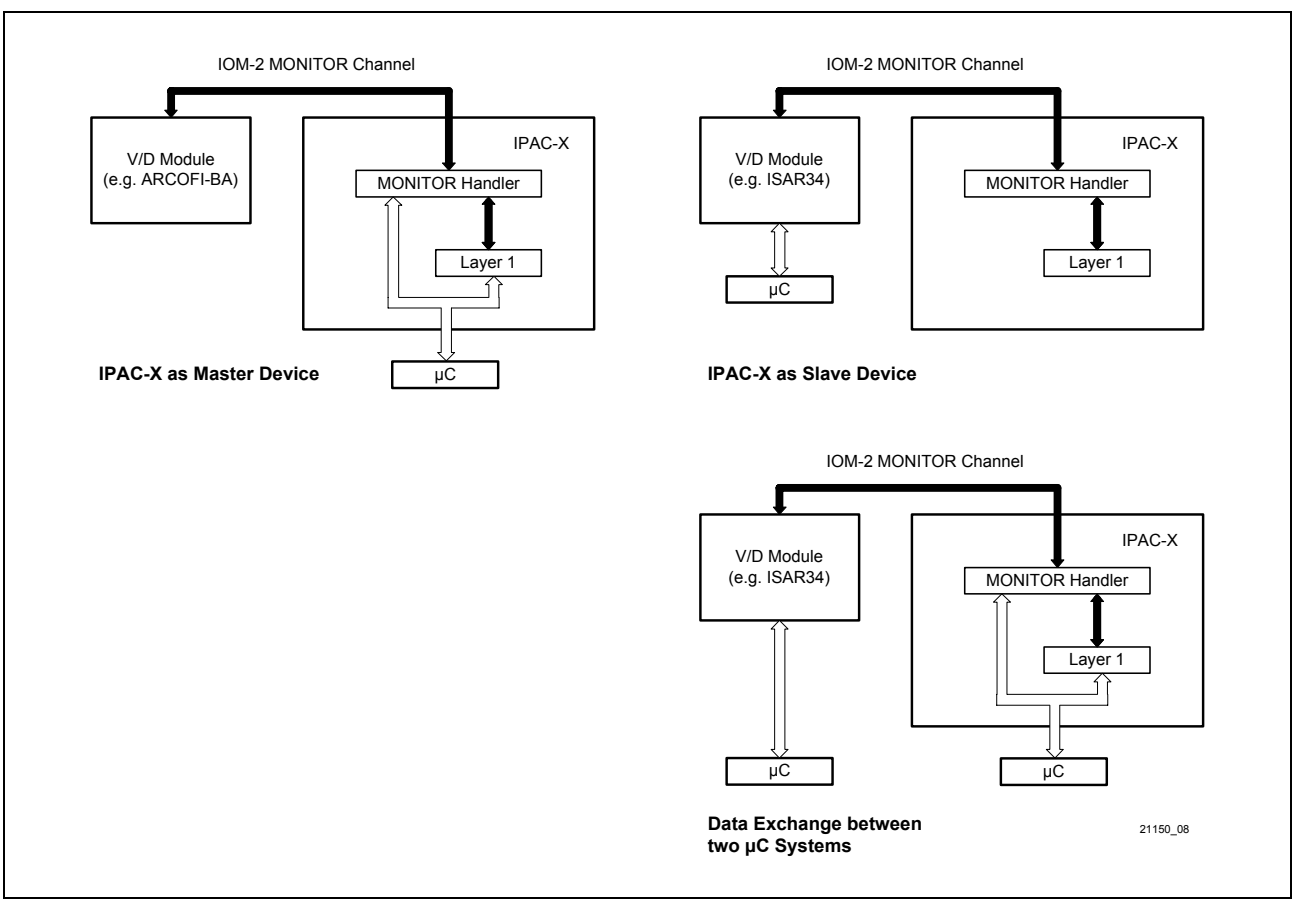



**Figure 65 Examples of MONITOR Channel Applications in IOM -2 TE Mode**

The MONITOR channel of the IPAC-X can be used in following applications which are illustrated in **Figure 65**:

- As a **master device** the IPAC-X can program and control other devices attached to the IOM-2 which do not need a parallel microcontroller interface, e.g. ARCOFI-BA PSB 2161. This facilitates redesigning existing terminal designs in which e.g. an interface of an expansion slot is realized with IOM-2 interface and monitor programming.
- As a **slave device** the transceiver part of the IPAC-X is programmed and controlled from a master device on IOM-2 (e.g. ISAR 34 PSB 7115). This is used in applications where no microcontroller is connected directly to the IPAC-X in order to simplify host interface connection. The HDLC controlling is processed by the master device therefore the HDLC data is transferred via IOM-2 interface directly to the master device.
- For **data exchange** between two microcontroller systems attached to two different devices on one IOM-2 backplane. Use of the MONITOR channel avoids the necessity of a dedicated serial communication path between the two systems. This simplifies the system design of terminal equipment.

### 3.7.3.1 Handshake Procedure

The MONITOR channel operates on an asynchronous basis. While data transfers on the bus take place synchronized to frame sync, the flow of data is controlled by a handshake procedure using the MONITOR Channel Receive (MR) and MONITOR Channel Transmit (MX) bits. Data is placed onto the MONITOR channel and the MX bit is activated. This data will be transmitted once per 8-kHz frame until the transfer is acknowledged via the MR bit.

The MONITOR channel protocol is described in the following section and **Figure 66** illustrates this. The relevant control and status bits for transmission and reception are listed in **Table 12** and **Table 13**.

**Table 12 Transmit Direction**

| Control/ Status Bit | Register | Bit | Function |
|---|---|---|---|
| Control | MOCR | MXC | MX Bit Control |
| | | MIE | Transmit Interrupt Enable |
| Status | MOSR | MDA | Data Acknowledged |
| | | MAB | Data Abort |
| | MSTA | MAC | Transmission Active |

**Table 13 Receive Direction**

| Control/ Status Bit | Register | Bit | Function |
|---|---|---|---|
| Control | MOCR | MRC | MR Bit Control |
| | | MRE | Receive Interrupt Enable |
| Status | MOSR | MDR | Data Received |
| | | MER | End of Reception |

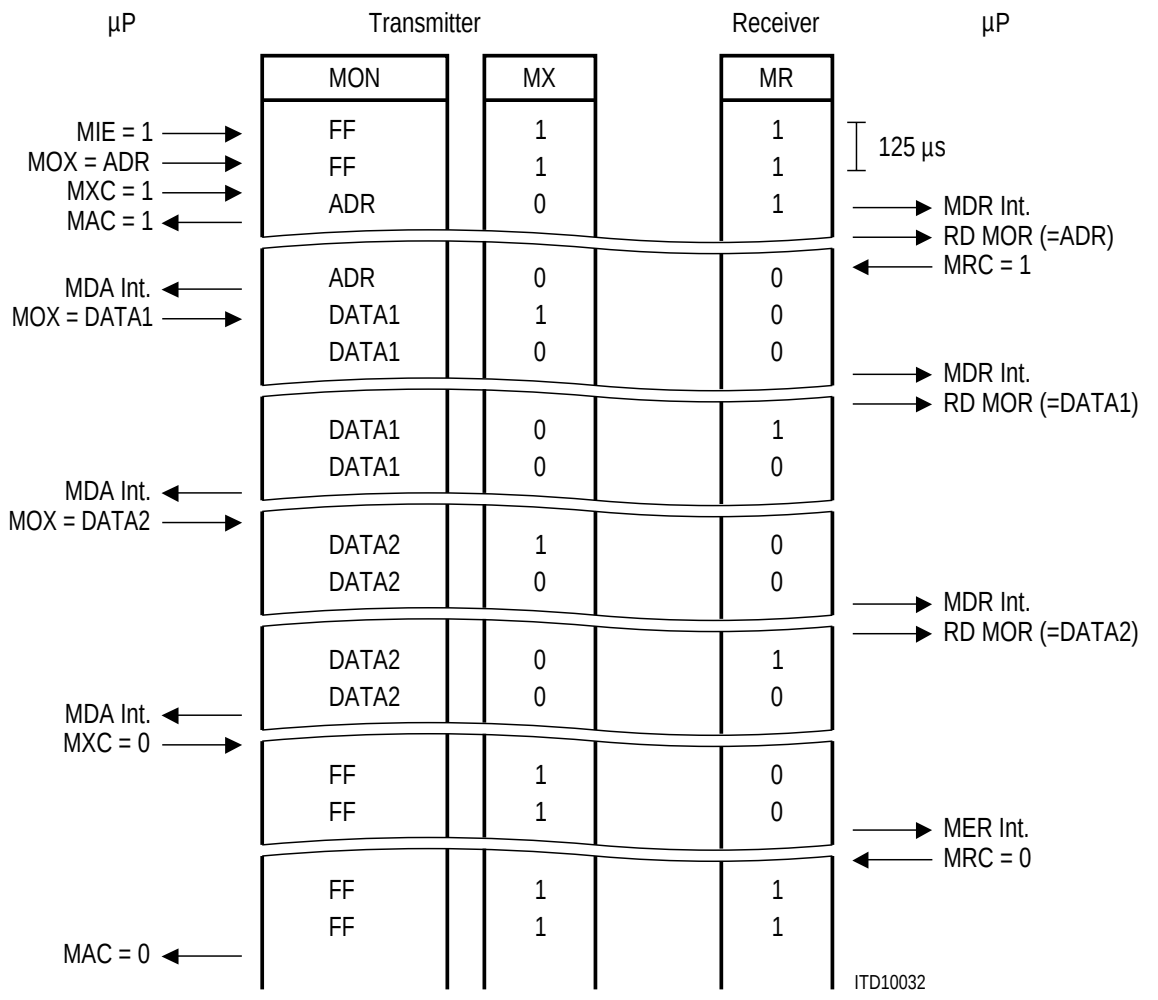



**Figure 66 MONITOR Channel Protocol (IOM-2)**

Before starting a transmission, the microprocessor should verify that the transmitter is inactive, i.e. that a possible previous transmission has been terminated. This is indicated by a ’0’ in the MONITOR Channel Active MAC status bit.

After having written the MONITOR Data Transmit (MOX) register, the microprocessor sets the MONITOR Transmit Control bit MXC to ’1’. This enables the MX bit to go active (0), indicating the presence of valid MONITOR data (contents of MOX) in the corresponding frame. As a result, the receiving device stores the MONITOR byte in its MONITOR Receive MOR register and generates an MDR interrupt status.

Alerted by the MDR interrupt, the microprocessor reads the MONITOR Receive (MOR) register. When it is ready to accept data (e.g. based on the value in MOR, which in a point-to-multipoint application might be the address of the destination device), it sets the MR control bit MRC to ’1’ to enable the receiver to store succeeding MONITOR channel bytes and acknowledge them according to the MONITOR channel protocol. In addition, it enables other MONITOR channel interrupts by setting MONITOR Interrupt Enable (MIE) to ’1’.

As a result, the first MONITOR byte is acknowledged by the receiving device setting the MR bit to ’0’. This causes a MONITOR Data Acknowledge MDA interrupt status at the transmitter.

A new MONITOR data byte can now be written by the microprocessor in MOX. The MX bit is still in the active (0) state. The transmitter indicates a new byte in the MONITOR channel by returning the MX bit active after sending it once in the inactive state. As a result, the receiver stores the MONITOR byte in MOR and generates a new MDR interrupt status. When the microprocessor has read the MOR register, the receiver acknowledges the data by returning the MR bit active after sending it once in the inactive state. This in turn causes the transmitter to generate an MDA interrupt status.

This "MDA interrupt – write data – MDR interrupt – read data – MDA interrupt" handshake is repeated as long as the transmitter has data to send. Note that the MONITOR channel protocol imposes no maximum reaction times to the microprocessor.

When the last byte has been acknowledged by the receiver (MDA interrupt status), the microprocessor sets the MONITOR Transmit Control bit MXC to ’0’. This enforces an inactive (’1’) state in the MX bit. Two frames of MX inactive signifies the end of a message. Thus, a MONITOR Channel End of Reception MER interrupt status is generated by the receiver when the MX bit is received in the inactive state in two consecutive frames. As a result, the microprocessor sets the MR control bit MRC to 0, which in turn enforces an inactive state in the MR bit. This marks the end of the transmission, making the MONITOR Channel Active MAC bit return to ’0’.

During a transmission process, it is possible for the receiver to ask a transmission to be aborted by sending an inactive MR bit value in two consecutive frames. This is effected by the microprocessor writing the MR control bit MRC to ’0’. An aborted transmission is indicated by a MONITOR Channel Data Abort MAB interrupt status at the transmitter.

The MONITOR transfer protocol rules are summarized in the following section:

- A pair of MX and MR in the inactive state for two or more consecutive frames indicates an **idle state** or an **end of transmission**.
- A **start of a transmission** is initiated by the transmitter by setting the MXC bit to ’1’ enabling the internal MX control. The receiver acknowledges the received first byte by setting the MR control bit to ’1’ enabling the internal MR control.
- The internal MX,MR control indicates or acknowledges a new byte in the MON slot by toggling MX,MR from the active to the inactive state for one frame.
- Two frames with the MX-bit in the inactive state indicate the **end of transmission**.
- Two frames with the MR-bit set to inactive indicate a receiver request for **abort**.
- The transmitter can **delay a transmission** sequence by sending the same byte continuously. In that case the MX-bit remains active in the IOM-2 frame following the first byte occurrence. Delaying a transmission sequence is only possible while the receiver MR-bit and the transmitter MX-bit are active.
- Since a **double last-look criterion** is implemented the receiver is able to receive the MON slot data at least twice (in two consecutive frames), the receiver waits for the acknowledge of the reception of two identical bytes in two successive frames.
- To control this handshake procedure a collision detection mechanism is implemented in the transmitter. This is done by making a **collision check** per bit on the transmitted MONITOR data and the MX bit.
- Monitor data will be transmitted repeatedly until its reception is acknowledged or the transmission time-out timer expires.
- Two frames with the MX bit in the inactive state indicates the **end of a message** (EOM).
- Transmission and reception of monitor messages can be performed simultaneously. This feature is used by the IPAC-X to send back the response before the transmission from the controller is completed (the IPAC-X does not wait for EOM from controller).

### 3.7.3.2 Error Treatment

In case the IPAC-X does not detect identical monitor messages in two successive frames, transmission is not aborted. Instead the IPAC-X will wait until two identical bytes are received in succession.

A transmission is aborted of the IPAC-X if:

- An error in the MR handshaking occurs
- A collision on the IOM-2 bus of the MONITOR data or MX bit occurs
- The transmission time-out timer expires

A reception is aborted by the device if:

- An error in the MX handshaking occurs or
- An abort request from the opposite device occurs

### MX/MR Treatment in Error Case

In the master mode the MX/MR bits are under control of the microcontroller through MXC or MRC, respectively. An abort is indicated by an MAB interrupt or MER interrupt, respectively.

In the slave mode the MX/MR bits are under control of the device. An abort is always indicated by setting the MX/MR bit inactive for two or more IOM-2 frames. The controller must react with EOM.

**Figure 67** shows an example for an abort requested by the receiver, **Figure 68** shows an example for an abort requested by the transmitter and **Figure 69** shows an example for a successful transmission.

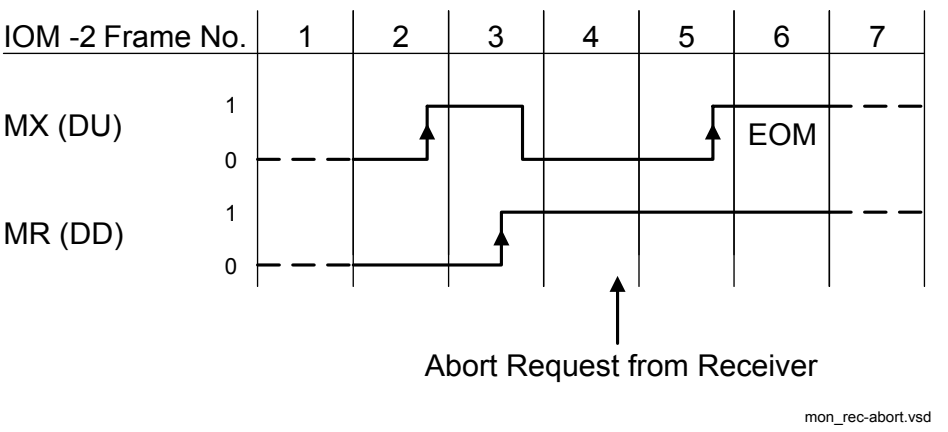



**Figure 67 Monitor Channel, Transmission Abort Requested by the Receiver**

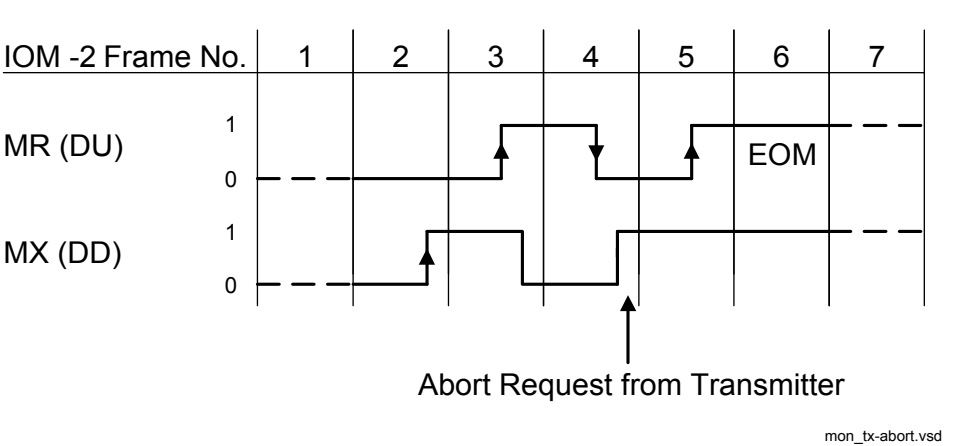



**Figure 68 Monitor Channel, Transmission Abort Requested by the Transmitter**

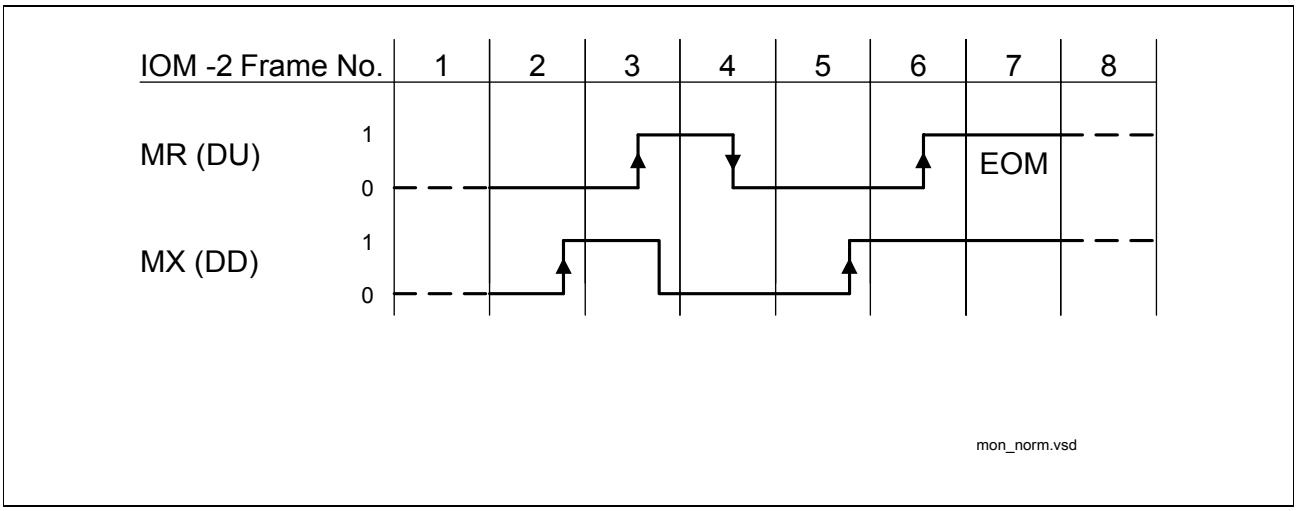



**Figure 69 Monitor Channel, Normal End of Transmission**

### 3.7.3.3 MONITOR Channel Programming as a Master Device

As a master device the IPAC-X can program and control other devices attached to the IOM-2 interface. The master mode is selected by default if one of the possible microcontroller interfaces are selected. The monitor data is written by the microprocessor in the MOX register and transmitted via IOM-2 DD (DU) line to the programmed/controlled device, e.g. ARCOFI-BA PSB 2161 or IEC-Q TE PSB 21911. The transfer of the commands in the MON channel is regulated by the handshake protocol mechanism with MX, MR which is described in the previous **Chapter 3.7.3.1**. If the transmitted command was a read command the slave device responds by sending the requested data.

The data structure of the transmitted monitor message depends on the device which is programmed. Therefore the first byte of the message is a specific address code which contains in the higher nibble a MONITOR channel address to identify different devices. The length of the messages depends on the accessed device and the type of MONITOR command.

### 3.7.3.4 MONITOR Channel Programming as a Slave Device

In applications without direct host controller connection the IPAC-X must operate in the MONITOR slave mode which can be selected by pinstrapping the microcontroller interface pins according **Table 3** respectively in **Chapter 3.2**. As a slave device the transceiver part of the IPAC-X is programmed and controlled by a master device at the IOM-2 interface. All programming data required by the IPAC-X is received in the MONITOR time slot on the IOM-2 and is transferred in the MOR register. The transfer of the commands in the MON channel is regulated by the handshake protocol mechanism with MX, MR which is described in the previous **Chapter 3.7.3.1**.
The first byte of the MONITOR message must contain in the higher nibble the MONITOR channel address code which is ’1010’ for the IPAC-X. The lower nibble distinguishes between a programming command or an identification command.

**Identification Command**

In order to be able to identify unambiguously different hardware designs of the IPAC-X by software, the following identification command is used:

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| DD 1st byte value | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| DD 2nd byte value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The IPAC-X responds to this DD identification sequence by sending a DU identification sequence:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| DU 1st byte value | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | |
| DU 2nd byte value | 0 | 1 | DESIGN | | | | | | <IDENT> |

DESIGN:six bit code, specific for each device in order to identify differences in operation, e.g.000001IPAC-XPEB 21150 V1.1.

This identification sequence is usually done once, when the terminal is connected for the first time. This function is used so that the software can distinguish between different possible hardware configurations. However this sequence is not compulsory.

### Programming Sequence

The programming sequence is characterized by a ’1’ being sent in the lower nibble of the received address code. The data structure after this first byte and the principle of a read/ write access to a register is similar to the structure of the serial control interface described in **Chapter 3.2.1.1**. For write access the header $43_H/47_H$ can be used and for read access the header $40_H/44_H$.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| DD 1st byte value | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| DD 2nd byte value | Header Byte | | | | | | | |
| DD 3rd byte value | R/W | Register Address | | | | | | |
| DD 4th byte value | Data 1 | | | | | | | |
| DD (nth + 3) byte value | Data n | | | | | | | |

All registers can be read back when setting the R/W bit in the byte for the command/ register address. The IPAC-X responds by sending its IOM-2 specific address byte ($A1_h$) followed by the requested data.

*Note: Application Hint:*

*It is not allowed to disable the MX- and MR-control in the programming device at the same time! First, the MX-control must be disabled, then the µC has to wait for an End of Reception before the MR-control may be disabled. Otherwise, the IPAC-X does not recognize an End of Reception.*

## 3.7.3.5 Monitor Time-Out Procedure

To prevent lock-up situations in a MONITOR transmission a time-out procedure can be enabled by setting the time-out bit (TOUT) in the MONITOR configuration register (MCONF). An internal timer is always started when the transmitter must wait for the reply of the addressed device. After 5 ms without reply the timer expires and the transmission will be aborted with a EOM (End of Message) command by setting the MX bit to ’1’ for two consecutive IOM-2 frames.

### 3.7.3.6 MONITOR Interrupt Logic

**Figure 70** shows the MONITOR interrupt structure of the IPAC-X. The MONITOR Data Receive interrupt status **MDR** has two enable bits, MONITOR Receive interrupt Enable (**MRE**) and MR bit Control (**MRC**). The MONITOR channel End of Reception **MER**, MONITOR channel Data Acknowledged **MDA** and MONITOR channel Data Abort **MAB** interrupt status bits have a common enable bit MONITOR Interrupt Enable **MIE**.

**MRE** prevents the occurrence of **MDR** status, including when the first byte of a packet is received. When **MRE** is active (1) but **MRC** is inactive, the **MDR** interrupt status is generated only for the first byte of a receive packet. When both **MRE** and **MRC** are active, **MDR** is always generated and all received MONITOR bytes - marked by a 1-to-0 transition in MX bit - are stored (additionally, an active **MRC** enables the control of the MR handshake bit according to the MONITOR channel protocol).

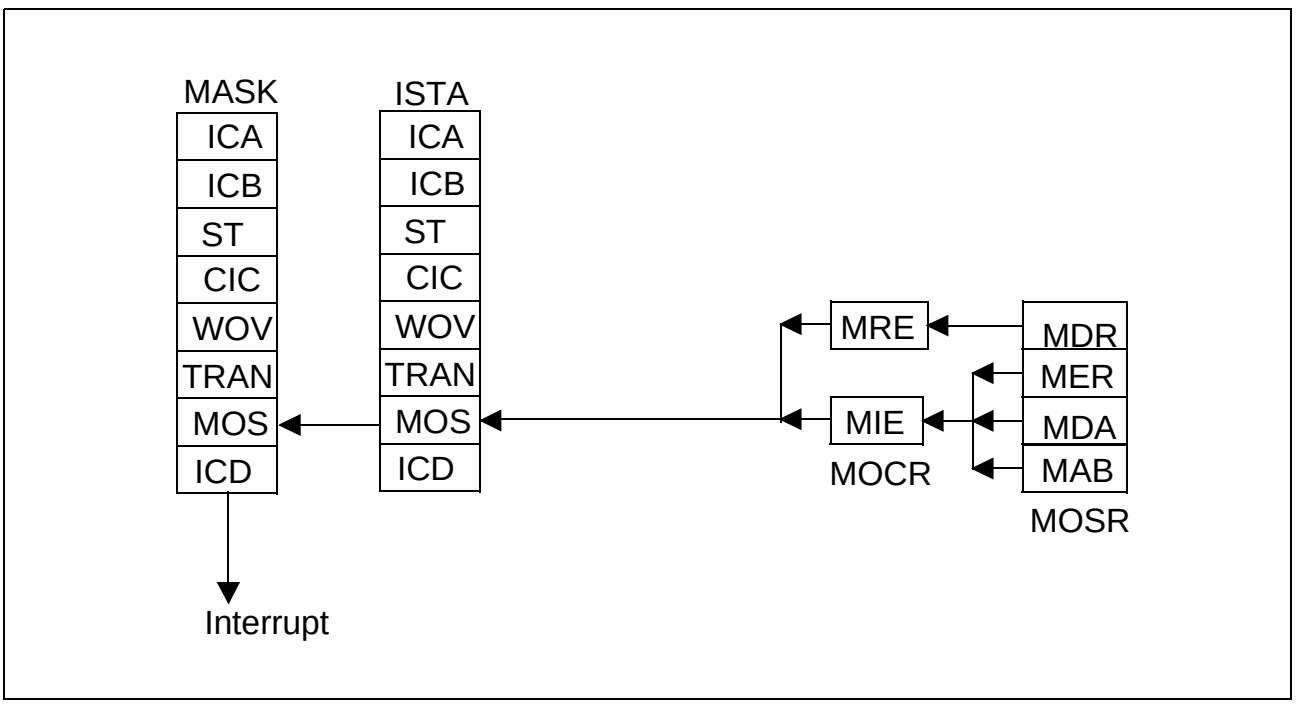



**Figure 70 MONITOR Interrupt Structure**

### 3.7.4 C/I Channel Handling

The Command/Indication channel carries real-time status information between the IPAC-X and another device connected to the IOM-2 interface.

1. One C/I channel (called C/I0) conveys the commands and indications between the layer-1 and the layer-2 parts of the IPAC-X. It can be accessed by an external layer-2 device e.g. to control the layer-1 activation/deactivation procedures. C/I0 channel access may be arbitrated via the TIC bus access protocol. In this case the arbitration is done in IOM-2 channel 2 (see **Figure 49**).

The C/I0 channel is accessed via register CIR0 (in receive direction, layer-1 to layer-2) and register CIX0 (in transmit direction, layer-2 to layer-1). The C/I0 code is four bits long. A listing and explanation of the layer-1 C/I codes can be found in **Chapter 3.5.4**.
In the receive direction, the code from layer-1 is continuously monitored, with an interrupt being generated anytime a change occurs (ISTA.CIC). A new code must be found in two consecutive IOM-2 frames to be considered valid and to trigger a C/I code change interrupt status (double last look criterion).

In the transmit direction, the code written in CIX0 is continuously transmitted in C/I0.

2. A second C/I channel (called C/I1) can be used to convey real time status information between the IPAC-X and various non-layer-1 peripheral devices, e.g. PSB 2161 ARCOFI-BA. The C/I1 channel consists of four or six bits in each direction. The width can be changed from 4bit to 6bit by setting bit CIX1.CICW.

In 4-bit mode 6-bits are written whereby the higher 2 bits must be set to “1” and 6-bits are read whereby only the 4 LSBs are used for comparison and interrupt generation (i.e. the higher two bits are ignored).

The C/I1 channel is accessed via registers CIR1 and CIX1. A change in the received C/I1 code is indicated by an interrupt status without double last look criterion.

#### CIC Interrupt Logic

**Figure 71** shows the CIC interrupt structure.

A CIC interrupt may originate:

– from a change in received C/I channel 0 code (CIC0)

or

– from a change in received C/I channel 1 code (CIC 1).

The two corresponding status bits CIC0 and CIC1 are read in CIR0 register. CIC1 can be individually disabled by clearing the enable bit CI1E in the CIX1 register. In this case the occurrence of a code change in CIR1 will not be displayed by CIC1 until the corresponding enable bit has been set to one.
Bits CIC0 and CIC1 are cleared by a read of CIR0.
An interrupt status is indicated every time a valid new code is loaded in CIR0 or CIR1. The CIR0 is buffered with a FIFO size of two. If a second code change occurs in the

received C/I channel 0 before the first one has been read, immediately after reading of CIR0 a new interrupt will be generated and the new code will be stored in CIR0. If several consecutive codes are detected, only the first and the last code is obtained at the first and second register read, respectively.

For CIR1 no FIFO is available. The actual code of the received C/I channel 1 is always stored in CIR1.

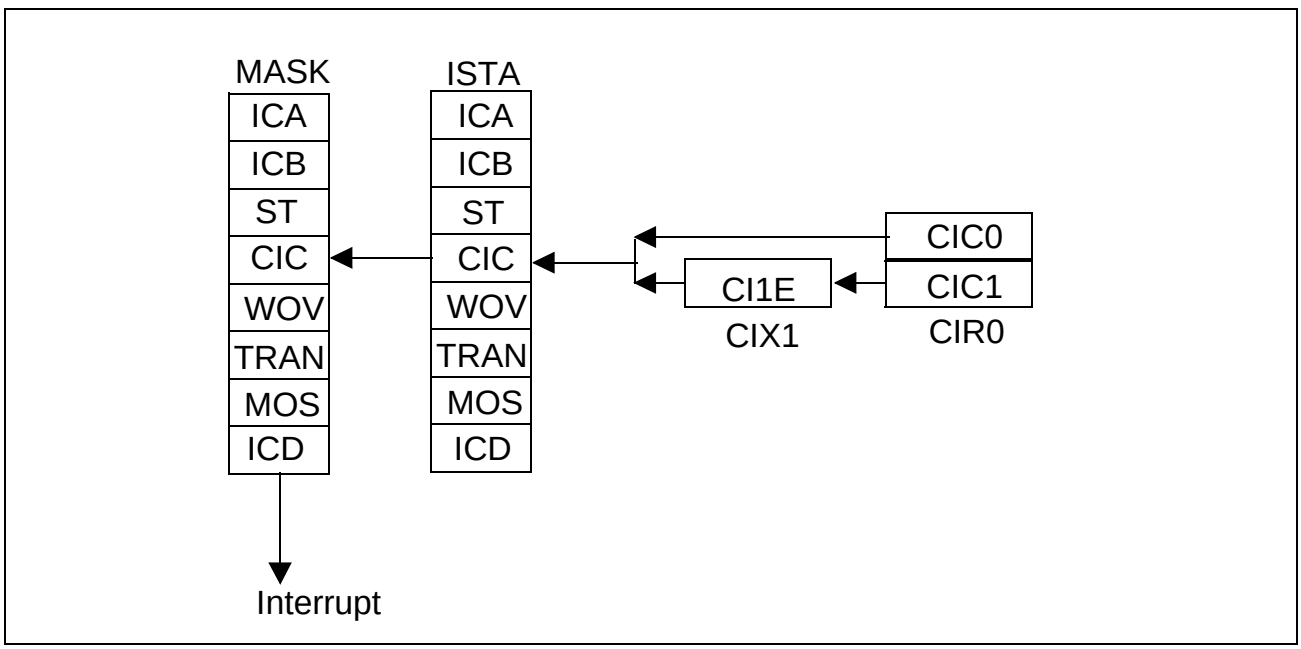



**Figure 71 CIC Interrupt Structure**

### 3.7.5 D-Channel Access Control

D-channel access control is defined to guarantee all connected TEs and HDLC controllers a fair chance to transmit data in the D-channel. Collisions are possible:

- on the IOM-2 interface if there is more than one HDLC controller connected

or

- on the S-interface when there is more than one terminal connected in a point to multipoint configuration (NT → TE1 … TE8).

Both arbitration mechanisms are implemented in the IPAC-X and will be described in the following two chapters.

#### 3.7.5.1 TIC Bus D-Channel Access Control

The TIC bus is imlemented to organize the access to the layer-1 functions provided in the IPAC-X (C/I-channel) and to the D-channel from up to 7 external communication controllers (see **Figure 72**).

***Note: The TIC Bus can be used in TE/iNT mode only. In other modes it has to be switched off in order not to disturb the layer-1 control and the HDLC controller. This is done by setting bit DIM 1 in register Mode D and bit 4 in register IOM_CR. For more details please refer to the application note "Reconfigurable PBX".***

To this effect the outputs of the D-channel controllers (e.g. ICC - ISDN Communication Controller PEB 2070) are wired-or (negative logic, i.e. a "0" wins) and connected to pin DU. The inputs of the ICCs are connected to pin DD. External pull-up resistors on DU/DD are required. The arbitration mechanism must be activated by setting MODED.DIM2-0=00x.

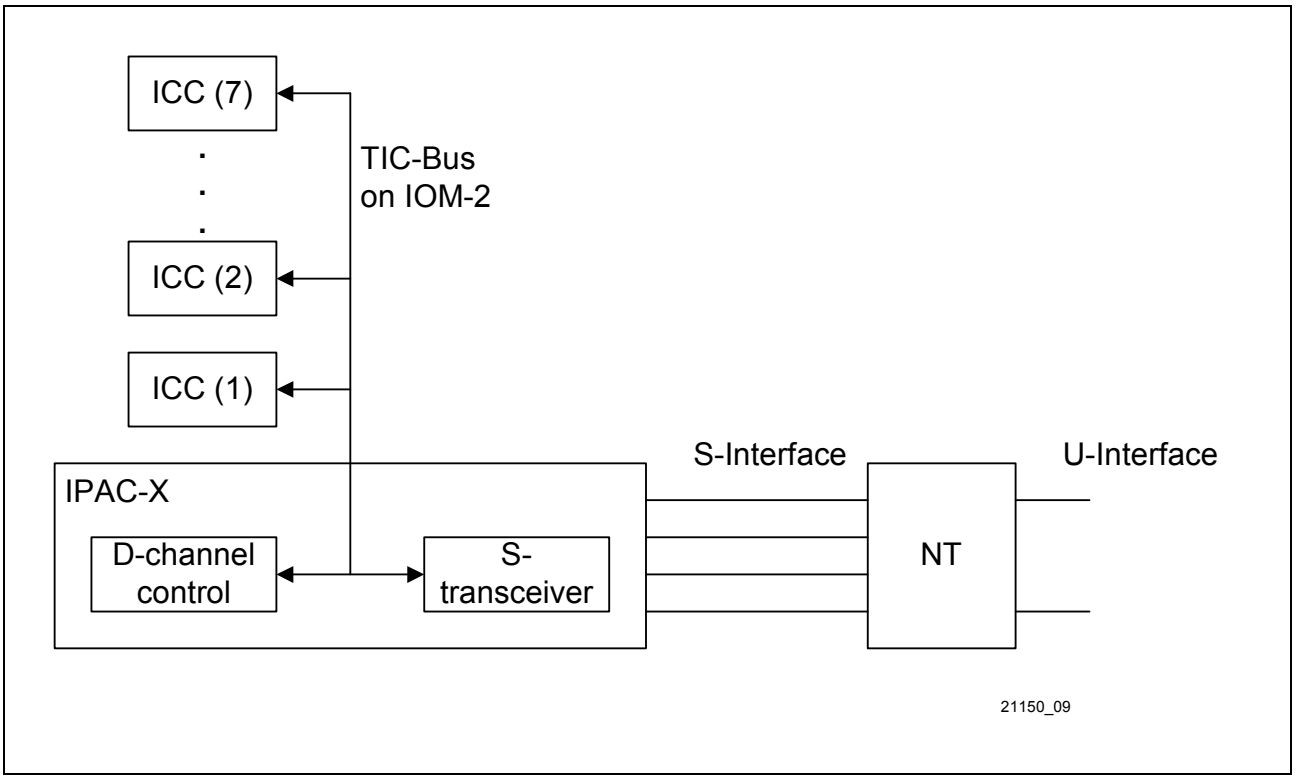



**Figure 72 Applications of TIC Bus in IOM-2 Bus Configuration**

The arbitration mechanism is implemented in the last octet in IOM-2 channel 2 of the IOM-2 interface (see **Figure 73**). An access request to the TIC bus may either be generated by software (µP access to the C/I channel) or by the IPAC-X itself (transmission of an HDLC frame in the D-channel). A software access request to the bus is effected by setting the BAC bit (CIX0 register) to ’1’.

In the case of an access request, the IPAC-X checks the Bus Accessed-bit BAC (bit 5 of last octet of CH2 on DU, see **Figure 73**) for the status "bus free“, which is indicated by a logical ’1’. If the bus is free, the IPAC-X transmits its individual TIC bus address TAD programmed in the CIX0 register (CIX0.TBA2-0). The IPAC-X sends its TIC bus address TAD and compares it bit by bit with the value on DU. If a sent bit set to ’1’ is read back as ’0’ because of the access of another D-channel source with a lower TAD, the IPAC-X withdraws immediately from the TIC bus, i.e. the remaining TAD bits are not transmitted. The TIC bus is occupied by the device which sends its address error-free. If more than one device attempt to seize the bus simultaneously, the one with the lowest address values wins. This one will set BAC=0 on TIC bus and starts D-channel transmission in the same frame.

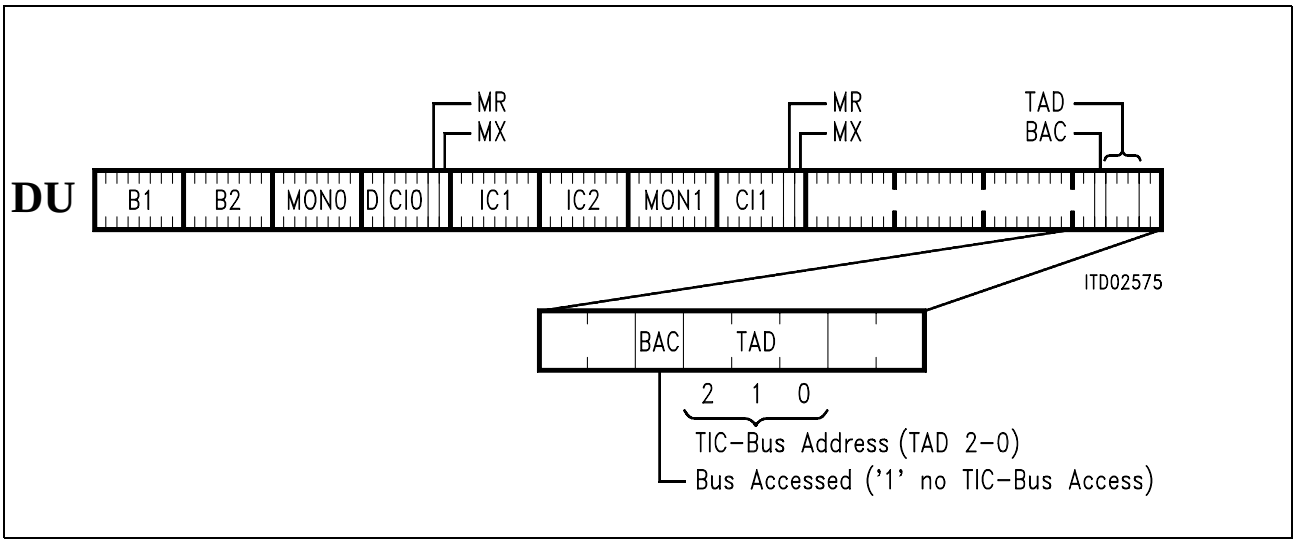



**Figure 73 Structure of Last Octet of Ch2 on DU**

When the TIC bus is seized by the IPAC-X, the bus is identified to other devices as occupied via the DU Ch2 Bus Accessed-bit state '0' until the access request is withdrawn. After a successful bus access, the IPAC-X is automatically set into a lower priority class, that is, a new bus access cannot be performed until the status "bus free" is indicated in two successive frames.

If none of the devices connected to the IOM-2 interface request access to the D and C/I channels, the TIC bus address 7 will be present. The device with this address will therefore have access, by default, to the D and C/I channels.

*Note: Bit BAC (CIX0 register) should be reset by the µP when access to the C/I channels is no more requested, to grant other devices access to the D and C/I channels.*

### 3.7.5.2 S-Bus Priority Mechanism for D-Channel

The S-bus access procedure specified in ITU I.430 was defined to organize D-channel access with multiple TEs connected to a single S-bus (see **Figure 75**).

To implement collision detection the D (channel) and E (echo) bits are used. The D-channel S-bus condition is indicated towards the IOM-2 interface with the S/G bit, i.e. the availability of the S/T interface D channel is indicated in bit 5 "Stop/Go" (S/G) of the DD last octet of Ch2 channel (**Figure 74**).

S/G = 1 : stop
S/G = 0 : go

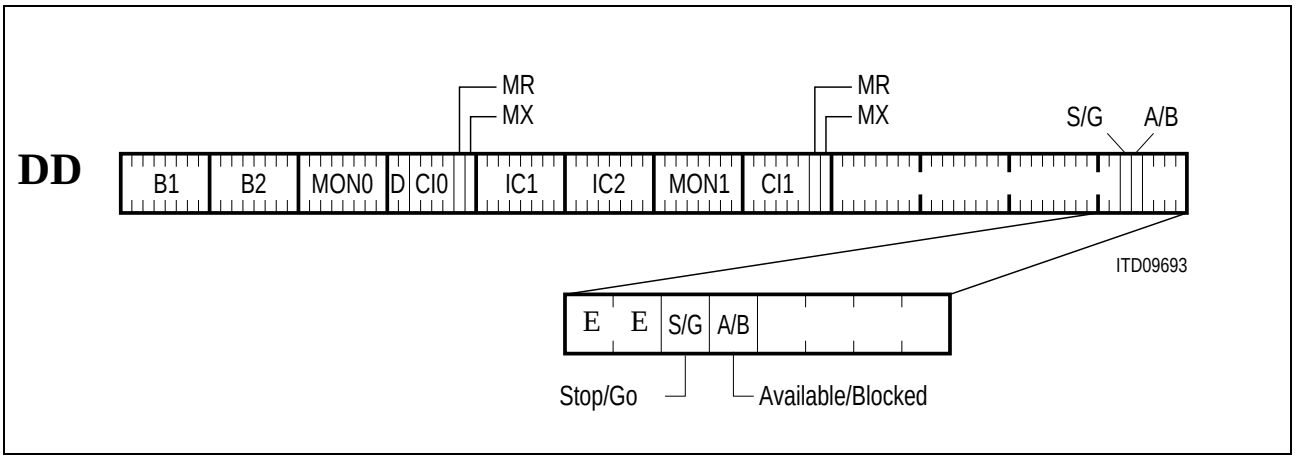



**Figure 74 Structure of Last Octet of Ch2 on DD**

The Stop/Go bit is available to other layer-2 devices connected to the IOM-2 interface to determine if they can access the S/T bus D channel.

The access to the D-channel is controlled by a priority mechanism which ensures that all competing TEs are given a fair access chance. This priority mechanism discriminates among the kind of information exchanged and information exchange history: Layer-2 frames are transmitted in such a way that signalling information is given priority (priority class 1) over all other types of information exchange (priority class 2). Furthermore, once a TE having successfully completed the transmission of a frame, it is assigned a lower level of priority of that class. The TE is given back its normal level within a priority class when all TEs have had an opportunity to transmit information at the normal level of that priority class.

The priority mechanism is based on a rather simple method: A TE not transmitting layer-2 frames sends binary 1s on the D-channel. As layer-2 frames are delimited by flags consisting of the binary pattern “01111110” and zero bit insertion is used to prevent flag imitation, the D-channel may be considered idle if more than seven consecutive 1s are detected on the D-channel. Hence by monitoring the D echo channel, the TE may determine if the D-channel is currently used by another TE or not.

A TE may start transmission of a layer-2 frame first when a certain number of consecutive 1s has been received on the echo channel. This number is fixed to 8 in priority class 1 and to 10 in priority class 2 for the normal level of priority; for the lower level of priority the number is increased by 1 in each priority class, i.e. 9 for class 1 and 11 for class 2.

A TE, when in the active condition, is monitoring the D echo channel, counting the number of consecutive binary 1s. If a 0 bit is detected, the TE restarts counting the number of consecutive binary 1s. If the required number of 1s according to the actual level of priority has been detected, the TE may start transmission of an HDLC frame. If a collision occurs, the TE immediately shall cease transmission, return to the D-channel monitoring state, and send 1s over the D-channel.

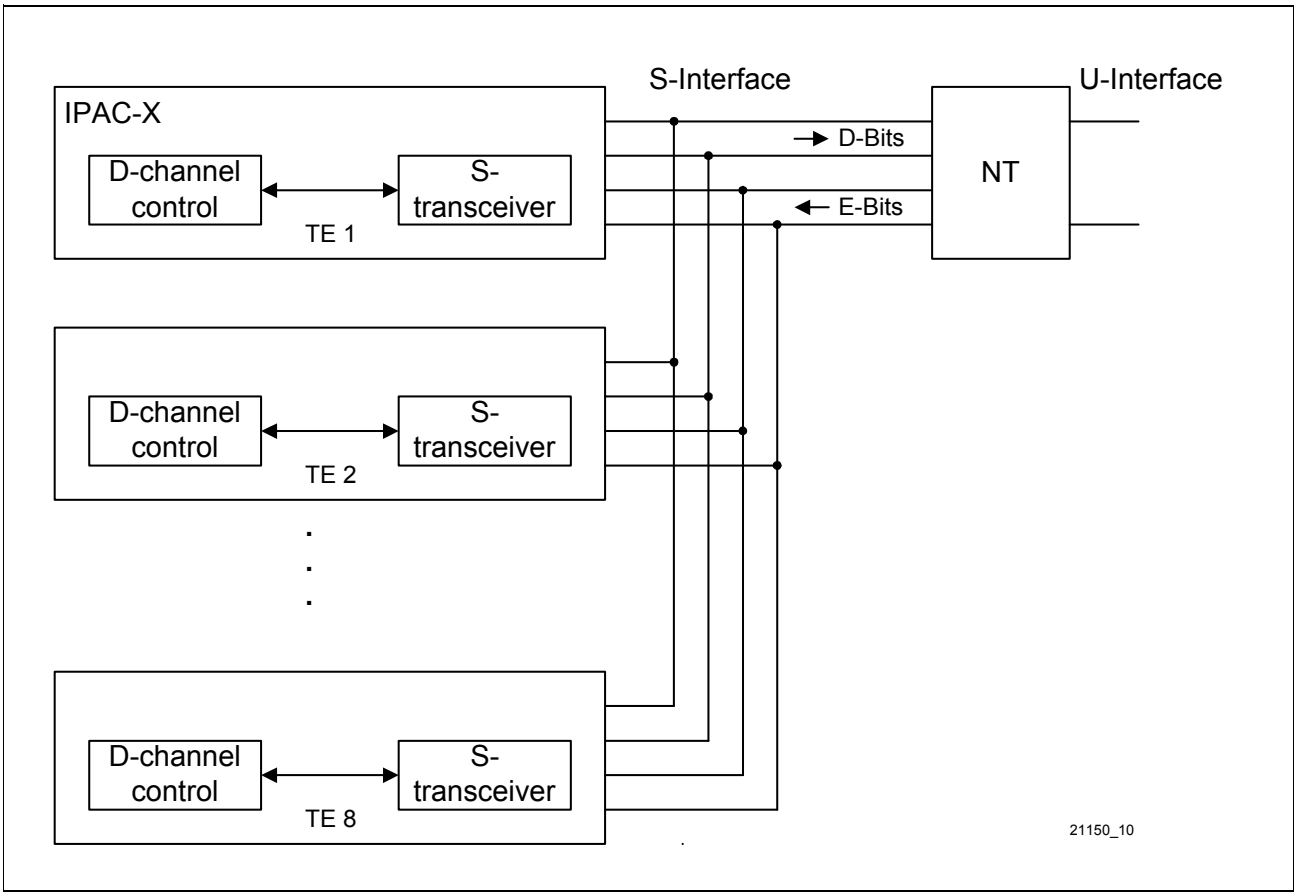



**Figure 75 D-Channel Access Control on the S-Interface**

### S-Bus D-channel Access Control in the IPAC-X

The above described priority mechanism is fully implemented in the IPAC-X. For this purpose the D-channel collission detection according to ITU I.430 must be enabled by setting MODED.DIM2-0 to ’0x1’. In this case the transceiver continuously compares the received E-echo bits with its own transmitted D data bits.
Depending on the priority class selected, 8 or 10 consecutive ONEs (high priority level, priority 8) need to be detected before the transceiver sends valid D-channel data on the upstream D-bits on S. In low priority level (priority 10) 10 or 11 consecutive ONEs are required.
The priority class (priority 8 or priority 10) is selected by transferring the appropriate activation command via the Command/Indication (C/I) channel of the IOM-2 interface to the transceiver. If the activation is initiated by a TE, the priority class is selected implicitly by the choice of the activation command. If the S-interface is activated from the NT, an activation command selecting the desired priority class should be programmed at the TE on reception of the activation indication (AI8 or AI10). In the activated state the priority class may be changed whenever required by simply programming the desired activation request command (AR8 or AR10).

### 3.7.5.3 S-Bus D-Channel Control in LT-T

If the TE frame structure on the IOM-2 interface is selected, the same D-channel access procedures as described in **Chapter 3.7.5.2** are used in LT-T mode.

For other frame structures used in LT-T mode, D-channel access on S is handled similarly, with the difference that the S/G bit is not available on IOM-2 but only on the S/G bit output pin (SGO).

### 3.7.5.4 D-Channel Control in the Intelligent NT (TIC- and S-Bus)

In intelligent NT applications (selected via register TR_MODE.MODE2-0) the IPAC-X has to share the upstream D-channel with one or more D-channel controllers on the IOM-2 interface and with all connected TEs on the S interface.

The transceiver incorporates an elaborate statemachine for D-channel priority handling on IOM-2. For the access to the D-channel a similar arbitration mechanism as on the S interface (writing D-bits, reading back E-bits) is performed for all D-channel sources on IOM-2. Due to this an equal and fair access is guaranteed for all D-channel sources on both the S interface and the IOM-2 interface.

This arbitration mechanism is only available in IOM-2 TE mode (12 PCM timeslots) per frame with enabled TIC bus. The access to the upstream D-channel is handled via the S/G bit for the HDLC controllers and via E-bit for all connected terminals on S (E-bits are inverted to block the terminals on S). Furthermore, if more than one HDLC source is requesting D-channel access on IOM-2 the TIC bus mechanism is used.

The arbiter permanently counts the “1s” in the upstream D-channel on IOM-2. If the necessary number of “1s” is counted and an HDLC controller on IOM-2 requests upstream D-channel access (BAC bit is set to 0), the arbiter allows this D-channel controller immediate access and blocks other TEs on S (E-bits are inverted). Similar as on the S-interface the priority for D-channel access on IOM-2 can be configured to 8 or 10 (TR_CMD.DPRIO).

The upstream device can stop all D-channel sources by setting the A/B-bit to 0. The S/G bit is not evaluated in this mode.

The configuration settings of the IPAC-X in intelligent NT applications are summarized in **Table 14**.

**Table 14 IPAC-X Configuration Settings in Intelligent NT Applications**

| Functional Block | Configuration Description | Configuration Setting |
|---|---|---|
| Layer 1 | Select Intelligent NT mode | Transceiver Mode Register:<br>TR_MODE.MODE0 = 0 (NT state machine)<br>or<br>TR_MODE.MODE0 = 1 (LT-S state machine)<br><br>TR_MODE.MODE1 = 1<br>TR_MODE.MODE2 = 1 |
| Layer 2 | Enable S/G bit evaluation | D-channel Mode Register:<br>MODED.DIM2-0 = 001 |

*Note: For mode selection in the TR_MODE register the MODE1/2 bits are used to select intelligent NT mode, MODE0 selects NT or LT-S state machine.*

With the configuration settings shown above the IPAC-X in intelligent NT applications provides for equal access to the D-channel for terminals connected to the S-interface and for D-channel sources on IOM-2.
For a detailed understanding the following sections provide a complete description on the procedures used by the D-channel priority handler on IOM-2, although it may not be necessary to study that in order to use this mode.

### 1. NT D-Channel Controller Transmits Upstream

In the initial state (’Ready’ state) neither the local D-channel sources nor any of the terminals connected to the S-bus transmit in the D-channel.

The IPAC-X S-transceiver thus receives BAC = “1” (IOM-2 DU line) and transmits S/G = “1” (IOM-2 DD line). The access will then be established according to the following procedure:

- Local D-channel source verifies that BAC bit is set to ONE (currently no bus access).
- Local D-channel source issues TIC bus address and verifies that no controller with higher priority requests transmission (TIC bus access must always be performed even if no other D-channel sources are connected to IOM-2).
- Local D-channel source issues BAC = “0” to block other sources on IOM-2 and to announce D-channel access.
- IPAC-X S-transceiver pulls S/G bit to ZERO (’Idle’ state) as soon as n D-bits = ’1’ are counted on IOM-2 (see note) to allow for further D-channel access.
- IPAC-X S-transceiver transmits inverted echo channel (E bits) on the S-bus to block all connected S-bus terminals (E = $\overline{D}$).
- Local D-channel source commences with D data transmission on IOM-2 as long as it receives S/G = “0”.
- After D-channel data transmission is completed the controller sets the BAC bit to ONE.
- IPAC-X S-transceiver transmits non-inverted echo (E = D).
- IPAC-X S-transceiver pulls S/G bit to ONE (’Ready’ state) to block the D-channel controller on IOM-2.

*Note: Right after transmission the S/G bit is pulled to ’1’ until n successive D-bits = ’1’ occur on the IOM-2 interface. As soon as n D-bits = ’1’ are seen, the S/G bit is set to ’0’ and the IPAC-X D-channel controller may start transmission again (if TIC bus is occupied). This allows an equal access for D-channel sources on IOM-2 and on the S interface.*
*The number n depends on configuration settings (selected priority 8 or 10) and the condition of the previous transmission, i.e. if an abort was seen (n = 8 or 10, respectively) or if the last transmission was successful (n = 9 or 11, respectively).*

**Figure 76** illustrates the signal flow in an intelligent NT.

### 2. Terminal Transmits D-Channel Data Upstream

The initial state is identical to that described in the last paragraph. When one of the connected S-bus terminals needs to transmit in the D-channel, access is established according to the following procedure:

- IPAC-X S-transceiver (in intelligent NT) recognizes that the D-channel on the S-bus is active.
- IPAC-X S-transceiver transfers S-bus D-channel data transparently through to the upstream IOM-2 bus (IOM-2 channel 0).

For both cases described above the exchange indicates via the A/B bit (controlled by layer 1) that D-channel transmission on this line is permitted (A/B = “1”). Data transmission could temporarily be prohibited by the exchange when only a single D-channel controller handles more lines (A/B = “0”, ELIC-concept).
In case the exchange prohibits D data transmission on this line the A/B bit is set to “0” (block). For $U_{PN}$ applications with S extension this forces the intelligent NT IPAC-X S-transceiver to transmit an inverted echo channel on the S-bus, thus disabling all terminal requests, and switches S/G to $\overline{A/B}$, which blocks the D-channel controller in the intelligent NT.

*Note: Although the IPAC-X S-transceiver operates in LT-S mode and is pinstrapped to IOM-2 channel 0 or 1 it will write into IOM-2 channel 2 at the S/G bit position.*

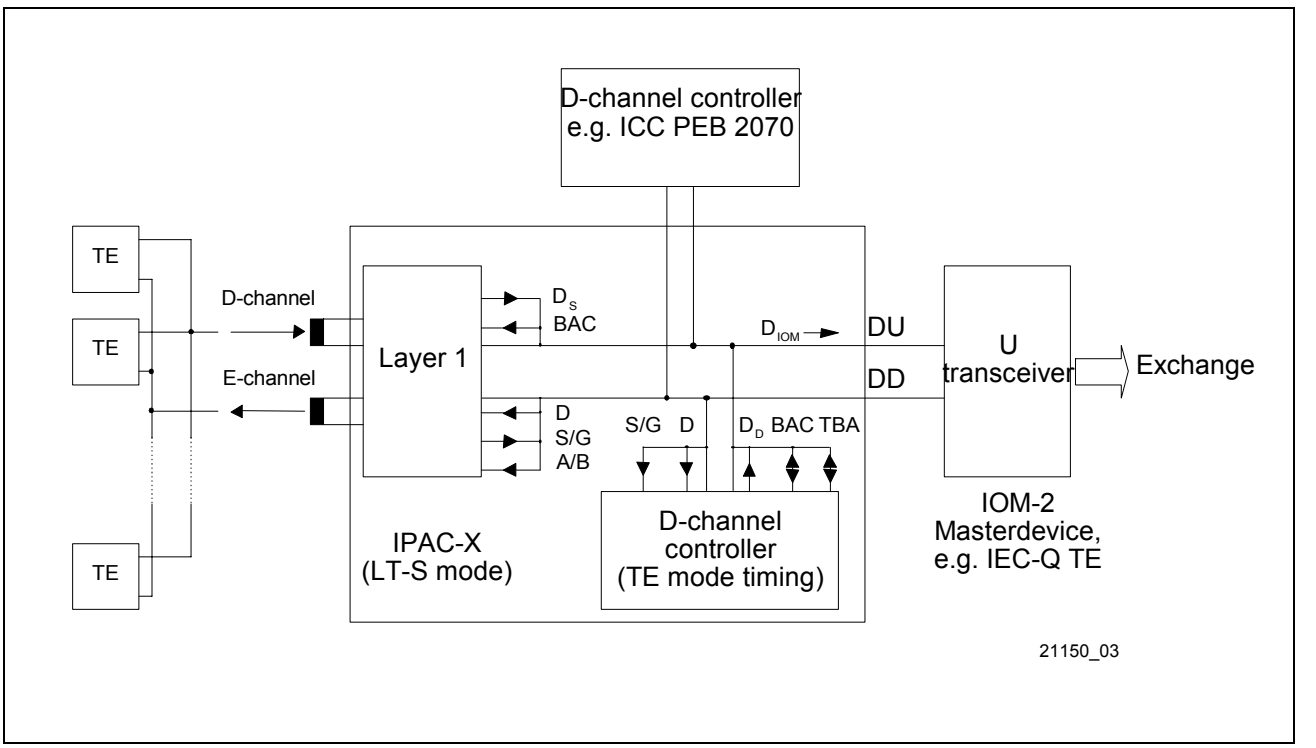



**Figure 76 Data Flow for Collision Resolution Procedure in Intelligent NT**

### 3.7.6 Activation/Deactivation of IOM-2 Interface

The IOM-2 interface can be switched off in the inactive state, reducing power consumption to a minimum. In this deactivated state is FSC = ’1’, DCL and BCL = ’0’ and the data lines are ’1’.

The IOM-2 interface can be kept active while the S interface is deactivated by setting the CFS bit to "0" (MODE1 register). This is the case after a hardware reset. If the IOM-2 interface should be switched off while the S interface is deactivated, the CFS bit should be set to ’1’. In this case the internal oscillator is disabled when no signal (info 0) is present on the S bus and the C/I command is ’1111’ = DIU. If the TE wants to activate the line, it has first to activate the IOM-2 interface either by using the "Software Power Up" function (IOM_CR.SPU bit) or by setting the CFS bit to "0" again.

The deactivation procedure is shown in **Figure 77**. After detecting the code DIU (Deactivate Indication Upstream) the layer 1 of the IPAC-X responds by transmitting DID (Deactivate Indication Downstream) during subsequent frames and stops the timing signals synchronously with the end of the last C/I (C/I0) channel bit of the fourth frame.

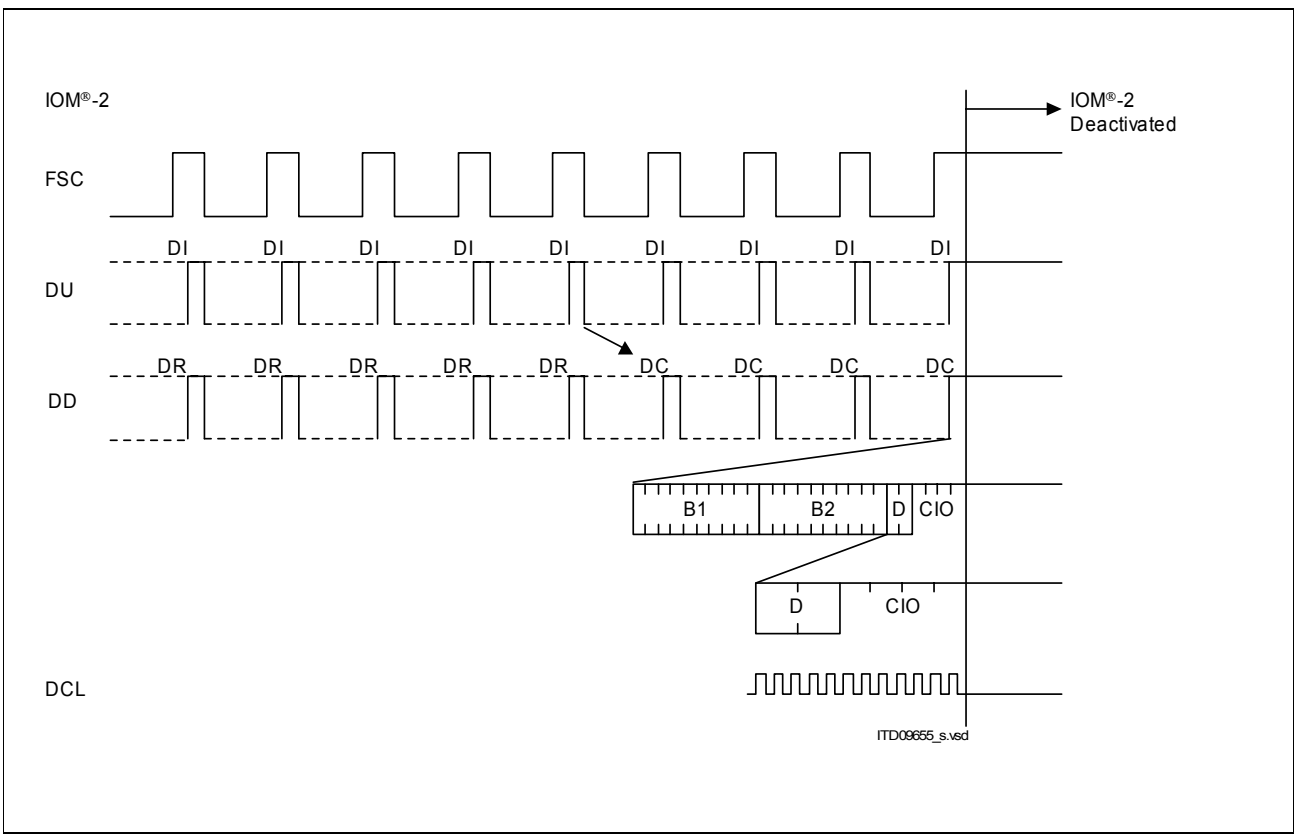


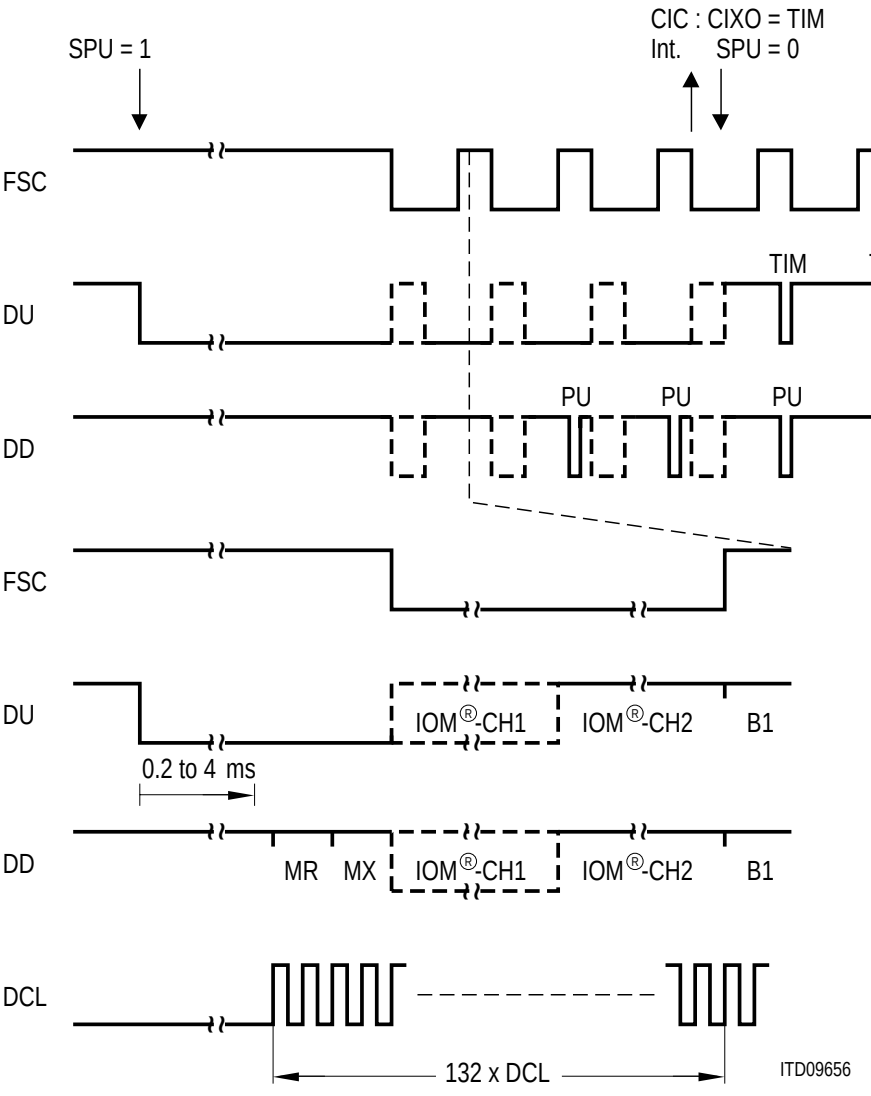

**Figure 77 Deactivation of the IOM-2 Interface**

The clock pulses will be enabled again when the DU line is pulled low (bit SPU in the IOM_CR register), i.e. the C/I command TIM = "0000" is received by layer 1, or when a non-zero level on the S-line interface is detected (if TR_CONF0.LDD=0). The clocks are turned on after approximately 0.2 to 4 ms depending on the oscillator.

DCL is activated such that its first rising edge occurs with the beginning of the bit following the C/I (C/I0) channel.

After the clocks have been enabled this is indicated by the PU code in the C/I channel and, consequently, by a CIC interrupt. The DU line may be released by resetting the Software Power Up bit IOM_CR ='0' and the C/I code written to CIX0 before (e.g. TIM or AR8) is output on DU.

The IPAC-X supplies IOM-2 timing signals as long as there is no DIU command in the C/I (C/I0) channel. If timing signals are no longer required and activation is not yet requested, this is indicated by programming DIU in the CIX0 register.




Note: The value "132 x DCL" is only valid for IOM configurations with 3 IOM channels.

**Figure 78 Activation of the IOM-2 interface**

### Asynchronous Awake (LT-S, NT, Int. NT mode)

The transceiver is in power down mode (deactivated state) and MODE1.CFS=1 (TR_CONF0.LDD is don’t care in this case). Due to any signal on the line the level detect circuit will asynchronously pull the DU line on IOM-2 to “0” which is deactivated again after 2 ms if the oscillator is fully operational. If the oscillator is just starting up in operational mode, the 2 ms duration is extended correspondingly.

## 3.8 Auxiliary Interface

### 3.8.1 Mode Dependent Functions

The AUX interface provides various functions, which depend on the operation mode (TE, LT-T, LT-S, NT or Intelligent NT mode) selected by pins MODE0 and MODE1/$\overline{\text{EAW}}$ (see **Table 15**). After reset the pins are switched as inputs until further configuration is done by the host.

**Table 15 AUX Pin Functions**

| Pin | TE, Int. NT mode | LT-T, LT-S, NT mode |
|---|---|---|
| AUX0 | AUX0 (i/o) | CH0 (i) |
| AUX1 | AUX1 (i/o) | CH1 (i) |
| AUX2 | AUX2 (i/o) | CH2 (i) |
| AUX3 | AUX3 (i/o) | AUX3 (i/o) |
| AUX4 | AUX4 (i/o) / MBIT | AUX4 (i/o) / MBIT |
| AUX5 | AUX5 (i/o) / FBOUT (o) | AUX5 (i/o) / FBOUT (o) |
| AUX6 | INT0 (i/o) | INT0 (i/o) |
| AUX7 | INT1 (i/o) / SGO (o) | INT1 (i/o) / SGO (o) |

**AUX0-5 (TE, Int. NT mode), AUX3-5 (LT-T, LT-S, NT mode)**

These pins can be used as programmable I/O lines.

As inputs (AOE.OEx=1) the state at the pin is latched in when the host performes read operation to register ARX.

As outputs (AOE.OEx=0) the value in register ATX is driven on the pins with a minimum delay after the write operation to this register is performed. They can be configured as open drain (ACFG1.ODx=0) or push/pull outputs (ACFG1.ODx=1). The status (’1’ or ’0’) at output pins can be read back from register ARX, which may be different from the ATX value, e.g. if another device drives a different level.

**FBOUT**

AUX5 is multiplexed with the selectable FSC/BCL output FBOUT, i.e. the host can select either standard I/O characteristic (ACFG2.A5SEL=0, default) or FBOUT functionality (ACFG2.A5SEL=1). FBOUT provides either an FSC (ACFG2.FBS=0, default) or BCL signal (ACFG2.FBS=1) which are derived from the DCL clock (also see **Chapter 3.4**).

**$\overline{\text{INT0}}$, $\overline{\text{INT1}}$**

In all modes two pins can be used as programmable I/O with optional interrupt input capability (default after reset, i.e. both interrupts masked).

The $\overline{\text{INT0/1}}$ pins are general input or output pins like AUX0-5 (see description above). In addition to that, as inputs they can generate an interrupt to the host (AUXI.INT0/1) which is maskable in AUXM.INT0/1. The interrupt input is either edge or level triggered (ACFG2.EL0/1).
As outputs both pins can directly be connected to an LED with preresistor.

For both pins AUX6/7 internal pull-up resistors are provided if the pin is configured as input or as output with open drain chracteristic. The internal pull-ups are disabled if output mode with push/pull characteristic is selected.

**SGO**

AUX7 provides the additional capability to output the S/G bit from the IOM-2 interface by setting ACFG2.A7SEL=1.

**MBIT**

If ACFG2.A4SEL is set to “1” the pin AUX4 is used for Multiframe Synchronizstion (see **Chapter 3.3.3**) and all configuration as general purpose I/O pin is don’t care. In TE and LT-T modes it is used as M-Bit output and in LT-S, NT and Int. NT mode it is used as M-Bit input.

**CH0, CH1, CH2**

In linecard mode one FSC frame is a multiplex of up to eight IOM-2 channels, each of them consisting of B1-, B2-, MONITOR-, D- and C/I-channel and MR- and MX-bits.
So in LT-T and LT-S mode one of eight channels on the IOM-2 interface is selected by CH0-2. These pins must be strapped to VDD or VSS according to **Table 16**.

**Table 16 IOM-2 Channel Selection**

| CH2 | CH1 | CH0 | Channel on IOM-2 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

For DCL = 1.536 MHz one of the IOM-2 channels 0 - 2 can be selected, for DCL = 4.096 MHz any of the eight IOM-2 channels can be selected.

The channel select pins have direct effect on the timeslot selection of the following registers:

- TR_TSDP_BC1
- TR_TSDP_BC2
- TR_CR, TRC_CR
- DCI_CR, DCIC_CR
- MON_CR

## 3.9 HDLC Controllers

The IPAC-X contains three HDLC controllers which can arbitrarily be used for the layer-2 functions of the D- channel protocol (LAPD) and B-channel protocols. By setting the Enable HDLC channel bits (EN_D, EN_B1H, EN_B2H) in the DCI_CR/BCH_CR registers each of the HDLC controllers can access the D or B-channels or any combination of them e.g. 18-bit IDSL data (2B+D).

They perform the framing functions used in HDLC based communication: flag generation/recognition, bit stuffing, CRC check and address recognition.

The D-channel FIFO has a size of 64 byte per direction. Each of the two B-channel FIFOs has a size of 128 bytes per direction. They are implemented as cyclic buffers. The transceiver reads and writes data sequentially with constant data rate whereas the data transfer between FIFO and microcontroller uses a block oriented protocol with variable block sizes.

The configuration, control and status bits related to the HDLC controllers are all assigned to the following address ranges:

**Table 17 HDLC Controller Address Range**

| | **FIFO Address** | **Config/Ctrl/Status Registers** |
|---|---|---|
| D-channel | $00_H$-$1F_H$ | $20_H$-$29_H$ |
| B-channel A | $7A_H$ | $70_H$-$79_H$ |
| B-channel B | $8A_H$ | $80_H$-$89_H$ |

*Note: For B-channel data access a single address location is used to read from and write to the FIFO. For D-channel access the address range $00_H$-$1F_H$ is used (similar as in ISAC-S PEB 2086), however a single address from this range is sufficient to access the FIFO as the internal FIFO pointer is incremented automatically independent from the external address.*

The mechanisms for access to the FIFOs are identical for D- and B-channels, therefore the following description applies to both of them and for simplification specific references like registers are indicated by an “x” (stands for “D” and “B”) to indicate it is relevant for D- and B-channel (e.g. ISTAx means ISTAD/ISTAB).

### 3.9.1 Message Transfer Modes

The HDLC controllers can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus the receive data flow and the address recognition features can be programmed in a flexible way to satisfy different system requirements.

**The structure of a D-channel two-byte address (LAPD) is shown below:**

| High Address Byte | | | Low Address Byte | |
|---|---|---|---|---|
| SAPI1, 2, SAPG | C/R | 0 | TEI 1, 2, TEIG | EA |

For address recognition on the D-channel the IPAC-X contains four programmable registers for individual SAPI and TEI values (SAP1, 2 and TEI1, 2), plus two fixed values for the “group” SAPI (SAPG = ’FE’ or ’FC’) and TEI (TEIG = ’FF’).
The received C/R bit is excluded from the address comparison. EA is the address field extension bit which must be set to ’1’ according to HDLC LAPD.

**The structure of a B-channel two-byte address is as follows:**

| High Address Byte | | | Low Address Byte |
|---|---|---|---|
| RAH1, 2, Group Address | C/R | 0 | RAL1, 2, Group Address |

For address recognition on the B-channel the IPAC-X contains four programmable registers for individual Receive Address High and Low values (RAH1, 2 and RAL1, 2), plus two fixed values for the High Address Byte (Group Address = ’FE’ or ’FC’) and one fixed value for the Low Address Byte (Group Address = ’FF’).
The received C/R bit is excluded from the address comparison. EA is the address field extension bit which must be set to ’1’ according to HDLC LAPD.

**Operating Modes**

There are 5 different operating modes which can be selected via the mode selection bits MDS2-0 in the MODEx registers:

**Non-Auto Mode** (MDS2-0 = ’01x’)

Characteristics: Full address recognition with one-byte (MDS = ’010’) or two-byte (MDS = ’011’) address comparison

All frames with valid addresses are accepted and the bytes following the address are transferred to the µP via RFIFOx. Additional information is available in RSTAx.

**Transparent Mode 0** (MDS2-0 = ’110’).

Characteristics: No address recognition

Every received frame is stored in RFIFOx (first byte after opening flag to CRC field). Additional information can be read from RSTAx.

**Transparent Mode 1** (MDS2-0 = ’111’).

Characteristics: SAPI recognition (D-channel)
High byte address recognition (B-channel)

A comparison is performed on the first byte after the opening flag with SAP1, SAP2 and “group” SAPI ($FE_H$/$FC_H$) for D-channel, and with RAH1, RAH2 and group address ($FE_H$/$FC_H$) for B-channel. In the case of a match, all the following bytes are stored in RFIFOx. Additional information can be read from RSTAx.

**Transparent Mode 2** (MDS2-0 = ’101’).

Characteristics: TEI recognition (D-channel)
Low byte address recognistion (B-channel)

A comparison is performed only on the second byte after the opening flag, with TEI1, TEI2 and group TEI ($FF_H$) for D-channel, and with RAL1 and RAL2 for B-channel. In case of a match the rest of the frame is stored in the RFIFOx. Additional information is available in RSTAx.

**Extended Transparent Mode** (MDS2-0 = ’100’).

Characteristics: Fully transparent

In extended transparent mode fully transparent data transmission/reception without HDLC framing is performed i.e. without FLAG generation/recognition, CRC generation/check, bitstuffing mechanism. This allows user specific protocol variations.
Also refer to **Chapter 3.9.5**.

## 3.9.2 Data Reception

### 3.9.2.1 Structure and Control of the Receive FIFO

The cyclic receive FIFO buffers with a length of 64-byte for D-channel and 128 byte for each of the two B-channels have variable FIFO block sizes (thresholds) of

- 4, 8, 16 or 32 bytes for D-channel and
- 8, 16, 32 or 64 bytes for B-channels

which can be selected by setting the corresponding RFBS bits in the EXMx registers. The variable block size allows an optimized HDLC processing concerning frame length, I/O throughput and interrupt load.
The transfer protocol between HDLC FIFO and microcontroller is block oriented with the microcontroller as master. The control of the data transfer between the CPU and the IPAC-X is handled via interrupts (IPAC-X → Host) and commands (Host → IPAC-X).

There are three different interrupt indications in the ISTAx registers concerned with the reception of data:

– **RPF** (**R**eceive **P**ool **F**ull) interrupt, indicating that a data block of the selected length (EXMx.RFBS) can be read from RFIFOx. The message which is currently received exceeds the block size so further blocks will be received to complete the message.
– **RME** (**R**eceive **M**essage **E**nd) interrupt, indicating that the reception of one message is completed, i.e. either
  • a short message is received
  (message length ≤ the defined block size (EXMx.RFBS)) or
  • the last part of a long message is received
  (message length > the defined block size (EXMx.RFBS))
  and is stored in the RFIFOx.
– **RFO** (**R**eceive **F**rame **O**verflow) interrupt, indicating that a complete frame could not be stored in RFIFOx and is therefore lost as the RFIFOx is occupied. This occurs if the host fails to respond quickly enough to RPF/RME interrupts since previous data was not read by the host.

There are two control commands that are used with the reception of data:

– **RMC** (**R**eceive **M**essage **C**omplete) command, telling the IPAC-X that a data block has been read from the RFIFOx and the corresponding FIFO space can be released for new receive data.
– **RRES** (**R**eceiver **R**eset) command, resetting the HDLC receiver and clearing the receive FIFO of any data (e.g. used before start of reception). It has to be used after a change of the message transfer mode. Pending interrupt indications of the receiver are not cleared by RRES, but have to be cleared by reading these interrupts.

*Note: The significant interrupts and commands are underlined as only these are commonly used during a normal reception sequence.*

The following description of the receive FIFO operation is illustrated in **Figure 79** for a RFIFOx block size (threshold) of 16 and 32 bytes.

The RFIFOx requests service from the microcontroller by setting a bit in the ISTAx register, which causes an interrupt (RPF, RME, RFO). The microcontroller then reads status information (RBCHx,RBCLx), data from the RFIFOx and then may change the receive FIFO block size (EXMx.RFBS). A block transfer is completed by the microcontroller via a receive message complete (CMDRx.RMC) command. This causes the space of the transferred bytes being released for new data and in case the frame was complete (RME) the reset of the receive byte counter RBC (RBCHx,RBCLx)[1)].

The total length of the frame is contained in the RBCHx and RBCLx registers which contain a 12 bit number (RBC11...0), so frames up to 4095 byte length can be counted.

1) If RMC is omitted, then no new interrupt can be generated.

If a frame is longer than 4095 bytes, the RBCH.OV (overflow) bit will be set. The least significant bits of RBCLx contain the number of valid bytes in the last data block indicated by RMEx (length of last data block ≤ selected block size). **Table 18** shows which RBC bits contain the number of bytes in the last data block or number of complete data blocks respectively. If the number of bytes in the last data block is ’0’ the length of the last received block is equal to the block size.

**Table 18 Receive Byte Count With RBC11...0 in the RBCHx/RBCLx Registers**

| EXMD1.RFBS bits (D-channel) | EXMB.RFBS bits (B-channel) | Selected block size | Number of | |
|---|---|---|---|---|
| | | | complete data blocks in | bytes in the last data block in |
| -- | ’00’ | 64 byte | RBC11...6 | RBC5...0 |
| ’00’ | ’01’ | 32 byte | RBC11...5 | RBC4...0 |
| ’01’ | ’10’ | 16 byte | RBC11...4 | RBC3...0 |
| ’10’ | ’11’ | 8 byte | RBC11...3 | RBC2...0 |
| ’11’ | -- | 4 byte | RBC11...2 | RBC1...0 |

The transfer block size (EXMx.RFBS) is 32 bytes for D-channel and 64 bytes for B-channel by default. If it is necessary to react to an incoming frame within the first few bytes the microcontroller can set the RFIFOx block size to a smaller value. Each time a CMDRx.RMC or CMDRx.RRES command is issued, the RFIFOx access controller sets its block size to the value specified in EXMR.RFBS, so the microcontroller has to write the new value for RFBS before the RMC command. When setting an initial value for RFBS before the first HDLC activities, a RRES command must be issued afterwards.

The RFIFOx can hold any number of frames fitting in the 64 bytes (D-channel)/128 bytes (B-channel). At the end of a frame, the RSTAx byte is always appended.

All generated interrupts are inserted together with all additional information into a wait line to be individually passed to the host. For example if several data blocks have been received to be read by the host and the host acknowledges the current block, a new RPF or RME interrupt from the wait line is immediately generated to indicate new data.

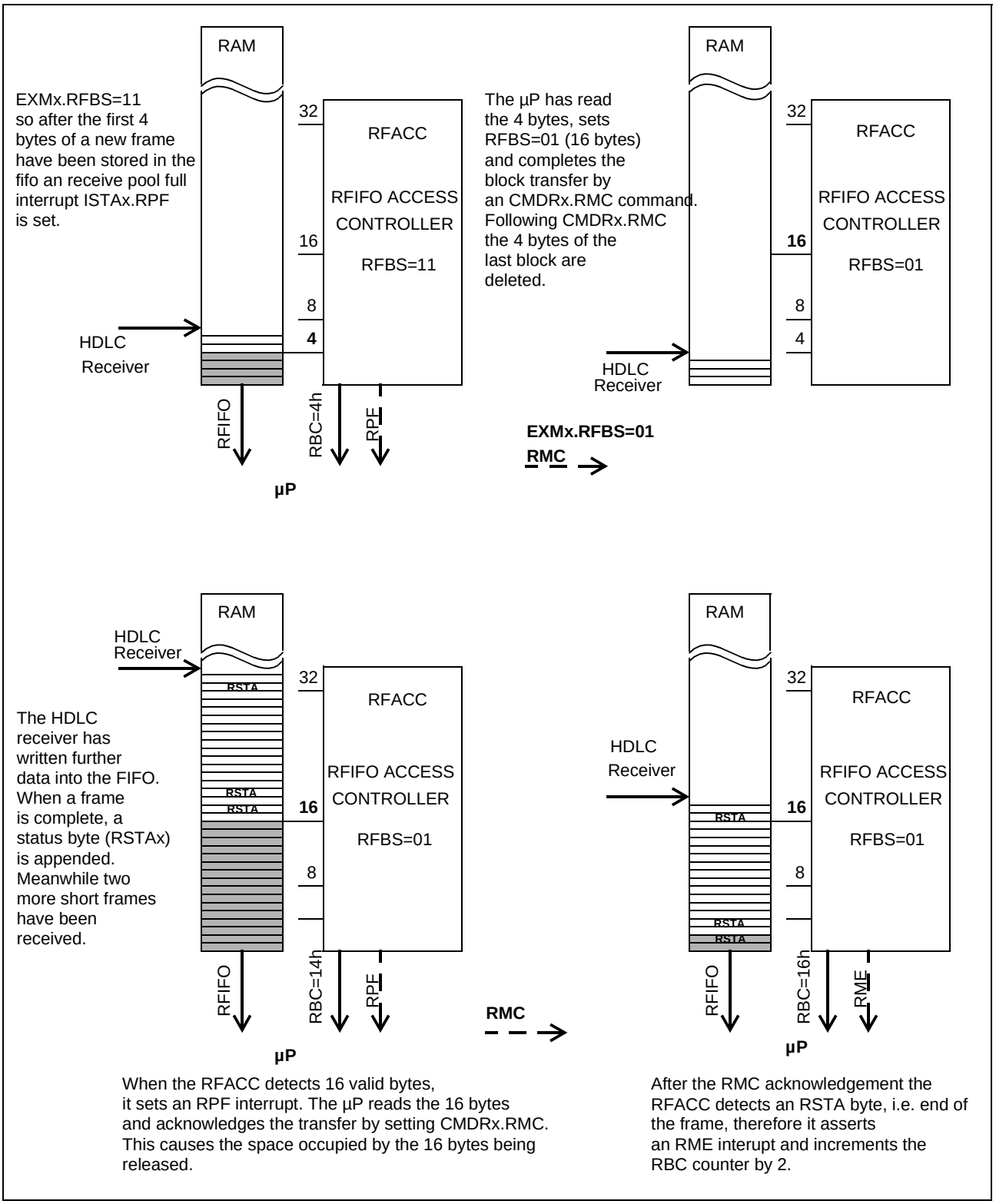



**Figure 79 RFIFO Operation**

### Possible Error Conditions during Reception of Frames

If parts of a frame get lost because the receive FIFO is full, the Receive Data Overflow (RDO) byte in the RSTAx byte will be set. If a complete frame is lost, i.e. if the FIFO is full when a new frame is received, the receiver will assert a Receive Frame Overflow (RFO) interrupt.

The microcontroller sees a cyclic buffer, i.e. if it tries to read more data than available, it reads the same data again and again. On the other hand, if it doesn't read or doesn't want to read all data, they are deleted anyway after the RMC command.

If the microcontroller reads data without a prior RME or RPF interrupt, the content of the RFIFOx would not be corrupted, but new data is only transferred to the host as long as new valid data is available in the RFIFOx, otherwise the last data is read again and again.

The general procedures for a data reception sequence are outlined in the flow diagram in **Figure 80**.

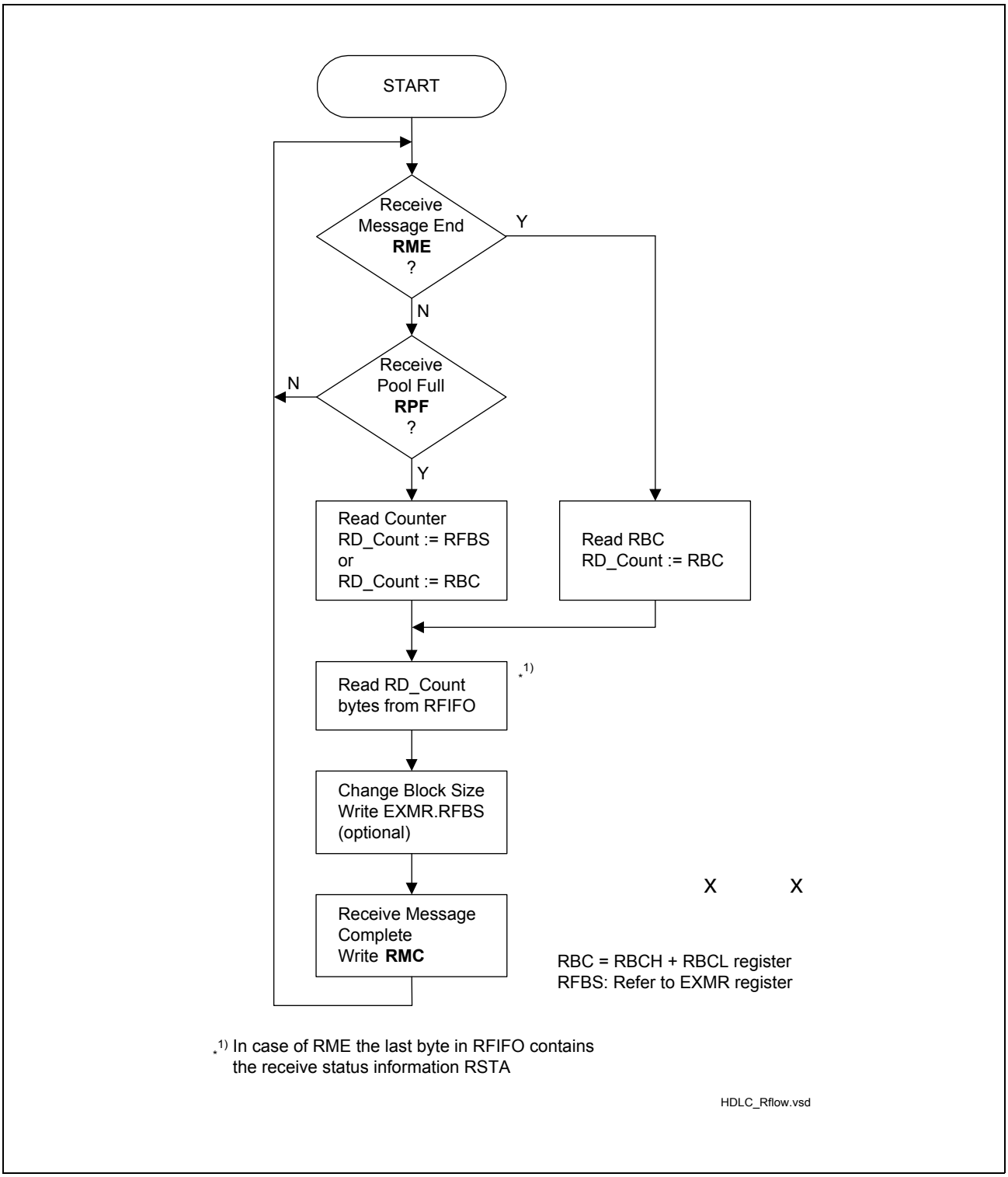



**Figure 80 Data Reception Procedures**

**Figure 81** gives an example of an interrupt controlled reception sequence, supposed that a long frame (68 byte) followed by two short frames (12 byte each) are received. The FIFO threshold (block size) is set to 32 byte in this example:

- After 32 byte of frame 1 have been received an RPF interrupt is generated to indicate that a data block can be read from the RFIFOx.
- The host reads the first data block from RFIFOx and acknowledges the reception by RMC. Meanwhile the second data block is received and stored in RFIFOx.
- The second 32 byte block is indicated by RPF which is read and acknowledged by the host as described before.
- The reception of the remaining 4 bytes plus RSTAx are indicated by RME (i.e. the receive status is always appended to the end of the frame).
- The host gets the number of bytes (COUNT = 5) from RBCLx/RBCHx and reads out the RFIFOx and optionally the status register RSTA. The frame is acknowledged by RMC.
- The second frame is received and indicated by RME interrupt.
- The host gets the number of bytes (COUNT = 13) from RBCLx/RBCHx and reads out the RFIFOx and optionally the status register. The RFIFOx is acknowledged by RMC.
- The third frame is transferred in the same way.

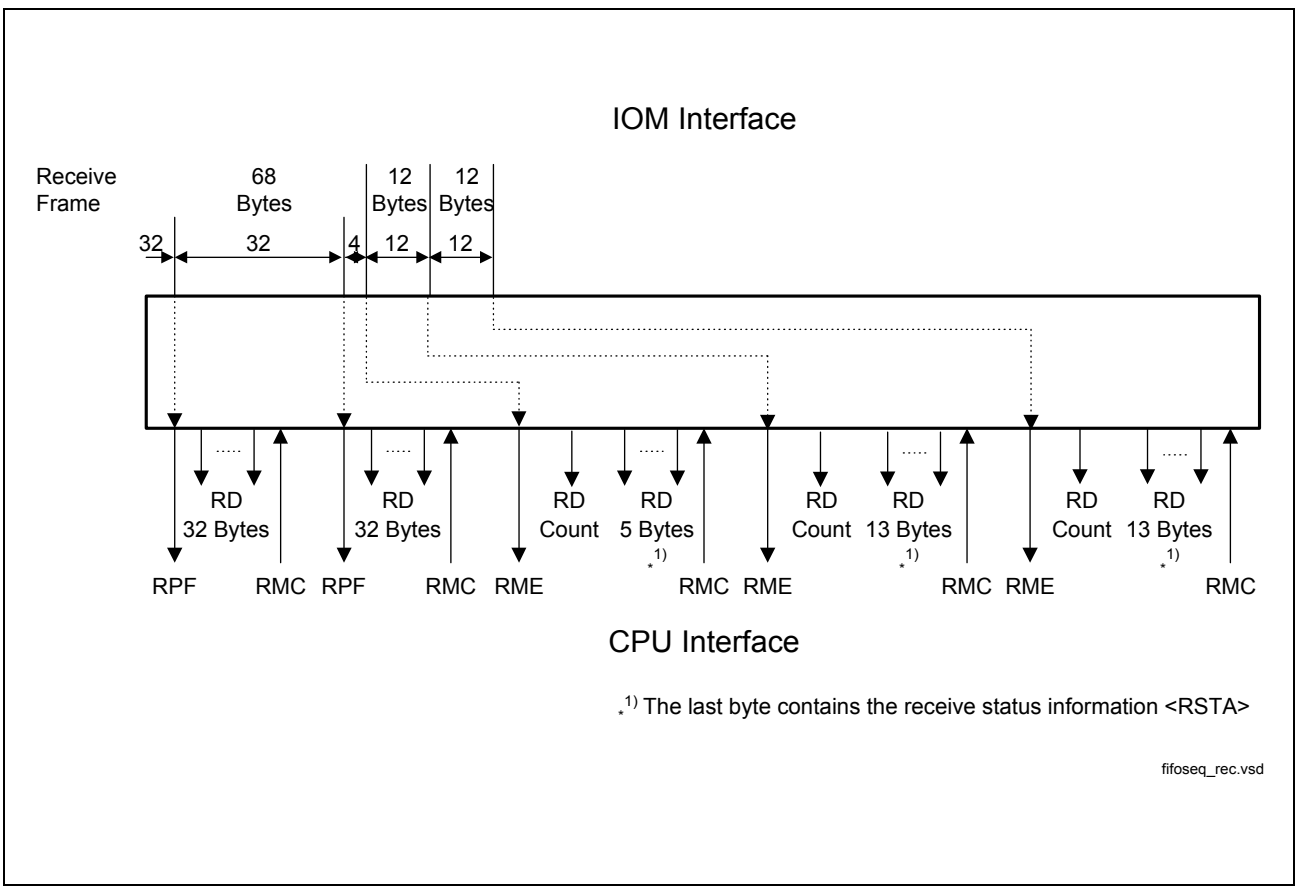



**Figure 81 Reception Sequence Example**

### 3.9.2.2 Receive Frame Structure

The management of the received HDLC frames as affected by the different operating modes (see **Chapter 3.9.1**) is shown in **Figure 82**.

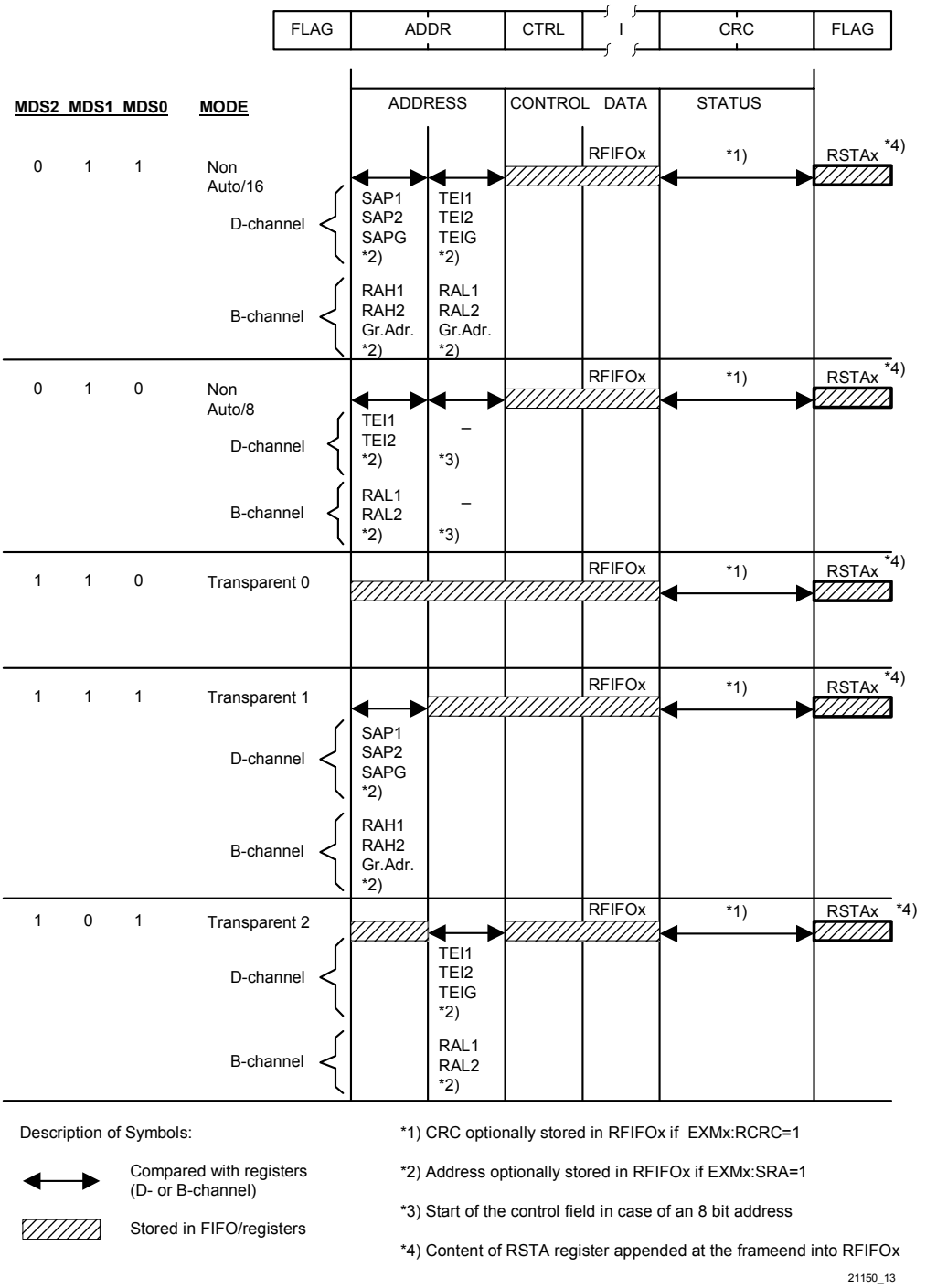



**Figure 82 Receive Data Flow**

The IPAC-X indicates to the host that a new data block can be read from the RFIFOx by means of an RPF interrupt (see previous chapter). User data is stored in the RFIFOx and information about the received frame is available in the RBCLx and RBCHx registers and the RSTAx bytes which are listed in **Table 19**.

**Table 19 Receive Information at RME Interrupt**

| Information | Register | Bit | Mode |
|---|---|---|---|
| Type of frame (Command/ Response) | RSTAx | C/R | Non-auto mode, 2-byte address field Transparent mode 1 |
| Recognition of SAPI | RSTAD RSTAB | SA1, 0 HA1, 0 | Non-auto mode, 2-byte address field Transparent mode 1 |
| Recognition of TEI | RSTAD RSTAB | TA LA | All except transparent mode 0 |
| Result of CRC check (correct/incorrect) | RSTAx | CRC | All |
| Valid Frame | RSTAx | VFR | All |
| Abort condition detected (yes/no) | RSTAx | RAB | All |
| Data overflow during reception of a frame (yes/no) | RSTAx | RDO | All |
| Number of bytes received in RFIFO | RBCL | RBC4-0 | All |
| Message length | RBCLx RBCHx | RBC11-0 | All |
| RFIFO Overflow | RBCHx | OV | All |

The RSTAx register is always appended in the RFIFOx as last byte to the end of a frame.

*Note: The number of bytes received in RFIFOx depends on the selected receive FIFO threshold (EXMx.RFBS).*

### 3.9.3 Data Transmission

#### 3.9.3.1 Structure and Control of the Transmit FIFO

The cyclic transmit FIFO buffers with a length of 64-byte for D-channel and 128 byte for each of the two B-channels have variable FIFO block sizes (thresholds) of

- 16 or 32 bytes for D-channel and
- 32 or 64 bytes for B-channels

which can be selected by setting the corresponding XFBS bits in the EXMx registers. There are three different interrupt indications in the ISTAx registers concerned with the transmission of data:

**XPR** (**T**ransmit **P**ool **R**eady) interrupt, indicating that a data block of up to 16 or 32 byte (D-channel), 32 or 64 byte (B-channel) can be written to the XFIFOx (block size selected via EXMx.XFBS).

An XPR interrupt is generated either

- after an XRES (Transmitter Reset) command (which is issued for example for frame abort) or
- when a data block from the XFIFOx is transmitted and the corresponding FIFO space is released to accept further data from the host.

– **XDU** (**T**ransmit **D**ata **U**nderrun) interrupt, indicating that the transmission of the current frame has been aborted (seven consecutive ’1’s are transmitted) as the XFIFOx holds no further transmit data. This occurs if the host fails to respond to an XPR interrupt quickly enough.

– Only valid for D-channel:
**XMR** (**T**ransmit **M**essage **R**epeat) interrupt, indicating that the transmission of the complete last frame has to be repeated as a collision on the S bus has been detected and the XFIFOx does not hold the first data bytes of the frame (collision after the 16th/ 32nd byte or after the 32nd/64th byte of the frame, respectively).
The occurence of an XDU or XMR interrupt clears the XFIFOx and an XMR interrupt is issued together with an XDU or XMR interrupt, respectively. Data cannot be written to the XFIFOx as long as an XDU/XMR interrupt is pending.
Three different control commands are used for transmission of data:

– **XTF** (**T**ransmit **T**ransparent **F**rame) command, telling the IPAC-X that up to 16 or 32 byte (D-channel) or 32 or 64 byte (B-channel) have been written to the XFIFOx and should be transmitted. A start flag is generated automatically.

– **XME** (**T**ransmit **M**essage **E**nd) command, telling the IPAC-X that the last data block written to the XFIFOx completes the corresponding frame and should be transmitted. This implies that according to the selected mode a frame end (CRC + closing flag) is generated and appended to the frame.

– **XRES** (**T**ransmitter **R**eset) command, resetting the HDLC transmitter and clearing the transmit FIFO of any data. After an XRES command the transmitter always sends an abort sequence, i.e. this command can be used to abort a transmission. Pending

interrupt indications of the transmitter are not cleared by XRES, but have to be cleared by reading these interutps.
Optionally two additional status conditions can be read by the host:

– **XDOV** (**T**ransmit **D**ata **O**verflow), indicating that the data block size has been exceeded, i.e. more than 16 or 32 byte (D-channel) or 32 or 64 byte (B-channel) were entered and data was overwritten.
– **XFW** (**T**ransmit **F**IFO **W**rite Enable), indicating that data can be written to the XFIFOx. This status flag may be polled instead of or in addition to XPR.

*Note: The significant interrupts and commands are underlined as only these are usually used during a normal transmission sequence.*

The XFIFO requests service from the microcontroller by setting a bit in the ISTAx register, which causes an interrupt (XPR, XDU, XMR). The microcontroller can then read the status register STARx (XFW, XDOV), write data in the FIFO and it can change the transmit FIFO block size (EXMx.XFBS) if required.
The instant of the initiation of a transmit pool ready (XPR) interrupt after different transmit control commands is listed in **Table 20**.

**Table 20 XPR Interrupt (Availability of XFIFOx) After XTF, XME Commands**

| CMDRx Register | Transmit pool ready (XPR) interrupt initiated ... |
|---|---|
| XTF | as soon as the selected buffer size in the FIFOx is available. |
| XTF & XME | after the successful transmission of the closing flag.<br>The transmitter always sends an abort sequence. |
| XME | as soon as the selected buffer size in the FIFO is available, two consecutive frames share flags. |

When setting XME the transmitter appends the CRC and the endflag at the end of the frame. When XTF & XME has been set, the XFIFOx is locked until successful transmission of the current frame, so a consecutive XPR interrupt also indicates successful transmission of the frame whereas after XME or XTF the XPR interrupt is asserted as soon as there is space for one data block in the XFIFOx.

The transfer block size is 32 bytes (for D-channel) or 64 bytes (for B-channel) by default, but sometimes, if the microcontroller has a high computational load, it is useful to increase the maximum reaction time for an XPR interrupt. The maximum reaction time is:

$t_{max}$ = (XFIFOx size - XFBS) / data transmission rate

With a selected block size of 16 bytes (D-channel only) an XPR interrupt indicates when a transmit FIFO space of at least 16 bytes is available to accept further data, i.e. there

are still a maximum of 48 bytes (64 bytes - 16 bytes) to be transmitted. With a 32 bytes block size (D- or B-channel) the XPR is initiated when a transmit FIFO space of at least 32 bytes is available to accept further data, i.e. there are still a maximum of 32 bytes (D-channel: 64 bytes - 32 bytes) or 96 bytes (B-channel: 128 bytes - 32 bytes) to be transmitted. The maximum reaction time for the smaller block size is 50 % higher with the trade-off of a doubled interrupt load. With a selected block size an XPR always indicates the available space in the XFIFOx, so any number of bytes smaller than the selected XFBS may be stored in the FIFO during one “write block“ access cycle.

Similar to RFBS for the receive FIFO, a new setting of XFBS takes effect after the next XTF,XME or XRES command. XRES resets the XFIFOx.

The XFIFOx can hold any number of frames fitting in the 64 bytes (D-channel) or 128 bytes (B-channel), respectively.

### Possible Error Conditions During Transmission of Frames

If the transmitter sees an empty FIFO, i.e. if the microcontroller doesn’t react fast enough to an XPR interrupt, an XDU (transmit data underrun) interrupt will be generated. If the HDLC channel becomes unavailable during transmission the transmitter tries to repeat the current frame as specified in the LAPD protocol. This is impossible after the first data block has been sent (16 or 32 bytes for D-channel; 32 or 64 byte for B-channel), in this case an XMR transmit message repeat interrupt is set and the microcontroller has to send the whole frame again.

Both XMR and XDU interrupts cause a reset of the XFIFOx. The XFIFOx is locked while an XMR or XDU interrupt is pending, i.e. all write actions of the microcontroller will be ignored as long as the microcontroller hasn’t read the ISTAx register with the set XDU, XMR interrupts.

If the microcontroller writes more data than allowed (block size), then the data in the XFIFOx will be corrupted and the STARx.XDOV bit is set. If this happens, the microcontroller has to abort the transmission by CMDRx.XRES and start new.

The general procedures for a data transmission sequence are outlined in the flow diagram in **Figure 83**.

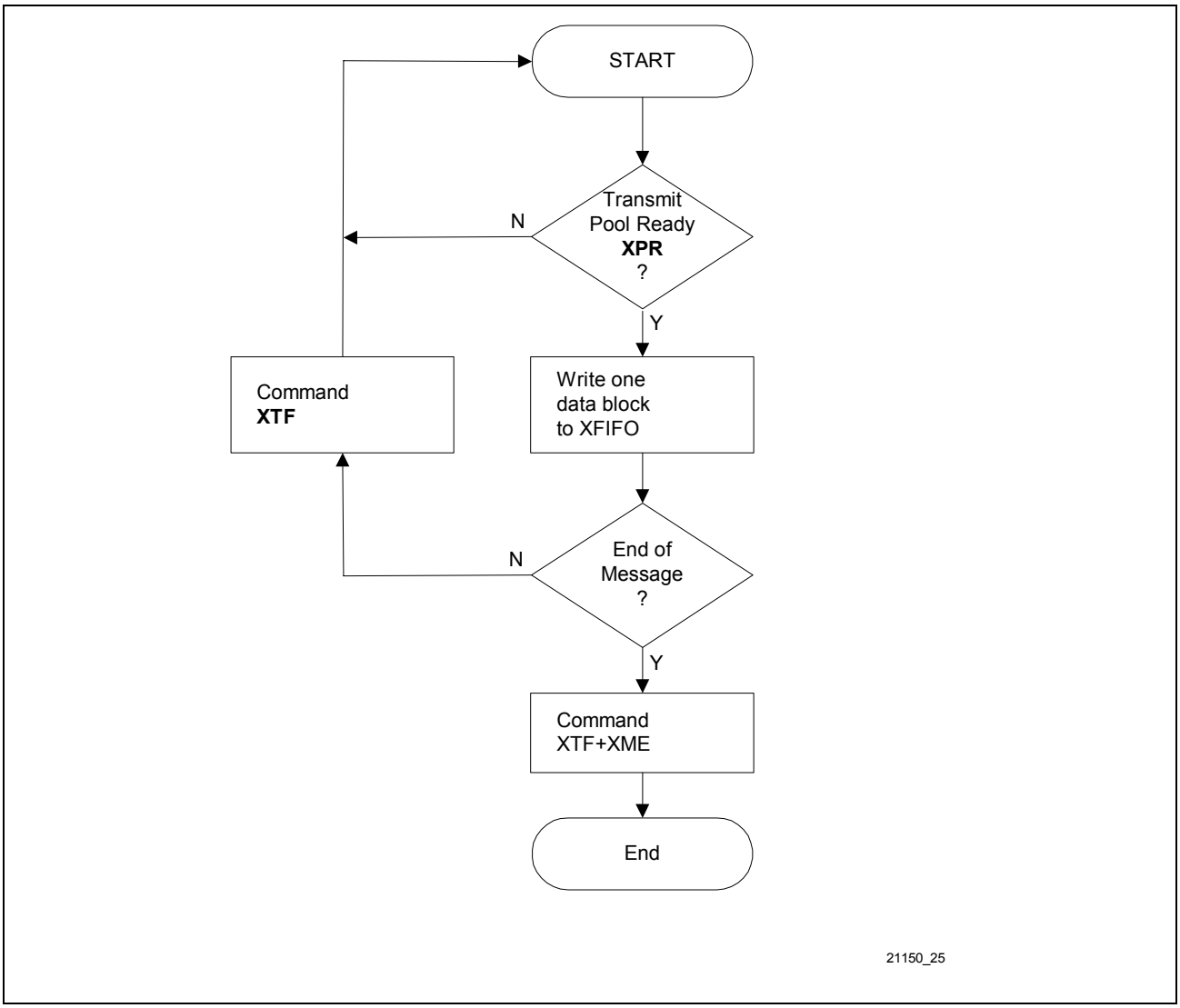



**Figure 83 Data Transmission Procedure**

The following description gives an example for the transmission of a 76 byte frame with a selected block size of 32 byte:

- The host writes 32 bytes to the XFIFOx, issues an XTF command and waits for an XPR interrupt in order to continue with entering data.
- The IPAC-X immediately issues an XPR interrupt (as remaining XFIFOx space is not used) and starts transmission.
- Due to the XPR interrupt the host writes the next 32 bytes to the XFIFOx, followed by the XTF command, and waits for XPR.
- As soon as the last byte of the first block is transmitted, the IPAC-X releases an XPR (XFIFOx space of first data block is free again) and continues transmitting the second block.
- The host writes the remaining 12 bytes of the frame to the XFIFOx and issues the XTF command together with XME to indicate that this is the end of frame.
- After the last byte of the frame has been transmitted the IPAC-X releases an XPR interrupt and the host may proceed with transmission of a new frame.

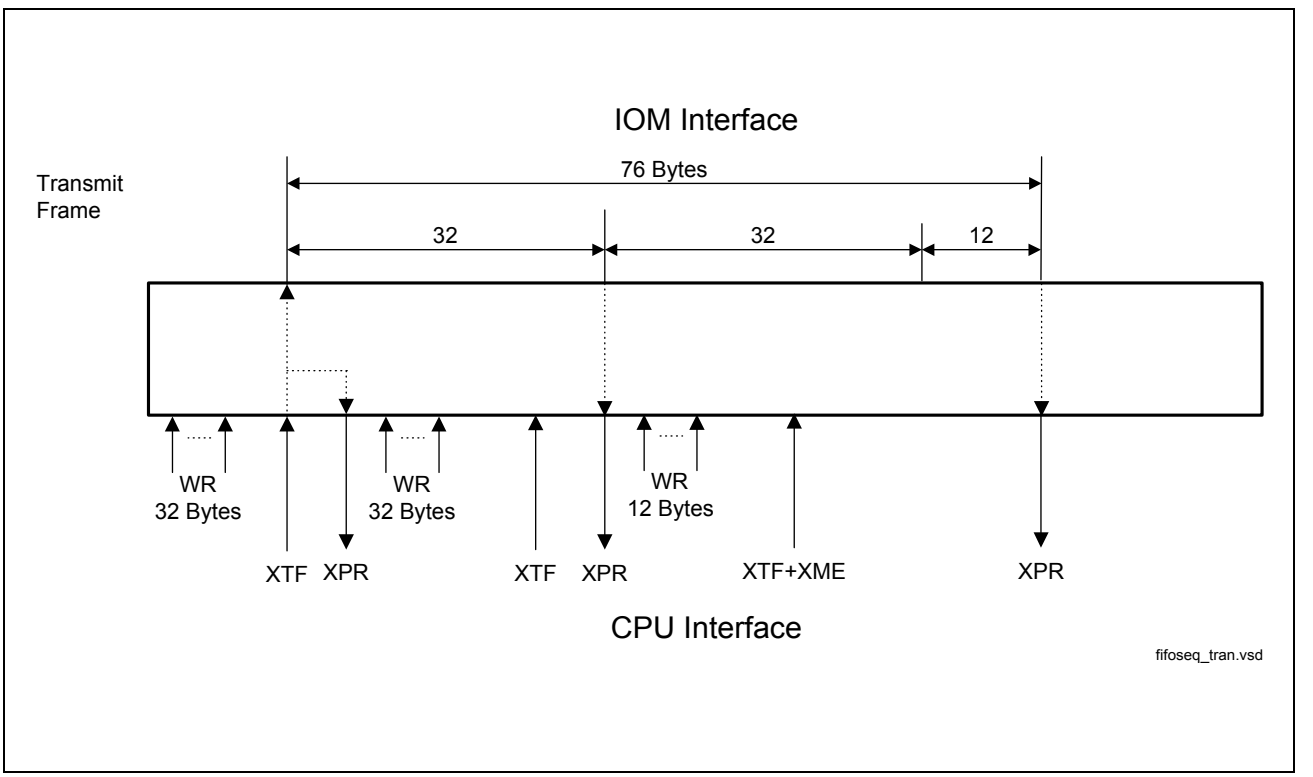



**Figure 84 Transmission Sequence Example**

### 3.9.3.2 Transmit Frame Structure

The transmission of transparent frames (XTF command) is shown in **Figure 85**.

For transparent frames, the whole frame including address and control field must be written to the XFIFOx. The host configures whether the CRC is generated and appended to the frame (default) or not (selected in EXMx.XCRC).

Further, the host selects the interframe time fill signal which is transmitted between HDCL frames (EXMx.ITF). One option is to send continuous flags ('01111110'), however if D-channel access handling (collision resolution on the S bus) is required, the signal must be set to idle (continuous '1's are transmitted). Reprogramming of ITF takes effect only after the transmission of the current frame has been completed or after an XRES command.

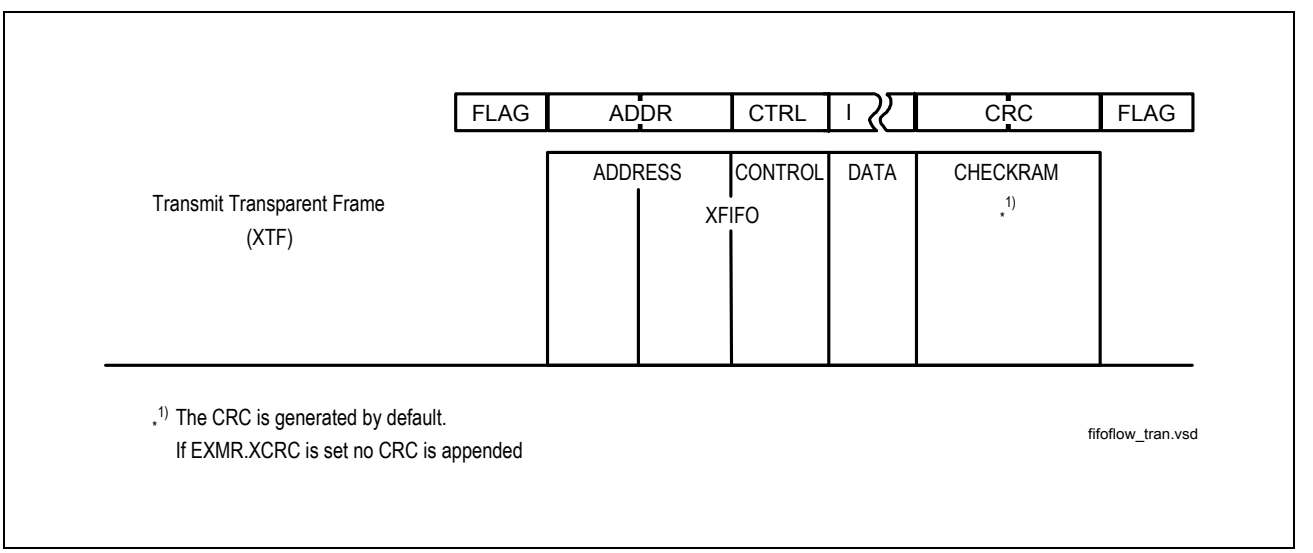



**Figure 85 Transmit Data Flow**

### 3.9.4 Access to IOM-2 channels

By setting the enable HDLC data bits (EN_D, EN_B1H, EN_B2H) in the DCI_CR register (D-channel) and in the BCH_CR register (B-channel) the HDLC controller can access the D, B1 and B2 channels or any combination of them (e.g. 18 bit IDSL data 2B+D). In all modes (except extended transparent mode) transmission always works frame aligned, i.e. it starts with the first selected channel, whereas reception searches for a flag anywhere in the serial data stream.

### 3.9.5 Extended Transparent Mode

This non-HDLC mode is selected by setting MODE2...0 to '100'. In extended transparent mode fully transparent data transmission/reception without HDLC framing is performed i.e. without FLAG generation/recognition, CRC generation/check, bitstuffing mechanism. This allows user specific protocol variations.

### Transmitter

The transmitter sends the data out of the FIFO without manipulation. Transmission is always IOM-2 frame aligned and byte aligned, i.e. transmission starts in the first selected channel (B1, B2, D, according to the setting of register DCI_CR or BCH_CR in the IOM-2 Handler) of the next IOM-2 frame.

The FIFO indications and commands are the same as in other modes.

If the microcontroller sets XTF & XME the transmitter responds with an XPR interrupt after sending the last byte, then it returns to its idle state (sending continuous ‘1’).

If the collision detection is enabled in D-channel (MODE.DIM = ’0x1’) the stop go bit (S/G) can be used as clear to send indication as in any other mode. If the S/G bit is set to ’1’ (stop) during transmission the transmitter responds always with an XMR (transmit message repeat) interrupt.

If the microcontroller fails to respond to a XPR interrupt in time and the transmitter runs out of data then it will assert an XDU (transmit data underrun) interrupt.

### Receiver

The reception is IOM-2 frame aligned and byte aligned, like transmission, i.e. reception starts in the first selected channel (B1, B2, D, according to the setting of registers DCI_CR and BCH_CR in the IOM-2 Handler) of the next IOM-2 frame. The FIFO indications and commands are the same as in others modes.

All incoming data bytes are stored in the RFIFOx and is additionally made available in RSTAx. If the FIFO is full an RFO interrupt is asserted (EXMx.SRA = ’0’).

*Note: In the extended transparent mode the EXMx register has to be set to ’xxx00000’*

### 3.9.6 HDLC Controller Interrupts

The cause of an interrupt related to the HDLC controllers is indicated in the ISTA register by the ICD bit for D-channel, ICA for B-channel A and ICB for B-channel B. These bits point to the different interrupt sources of the HDLC controllers in the ISTAD and ISTAB registers. The individual interrupt sources of the HDLC controllers during reception and transmission of data are explained in **Chapter 3.9.2.1** or **Chapter 3.9.3.1**, respectively.

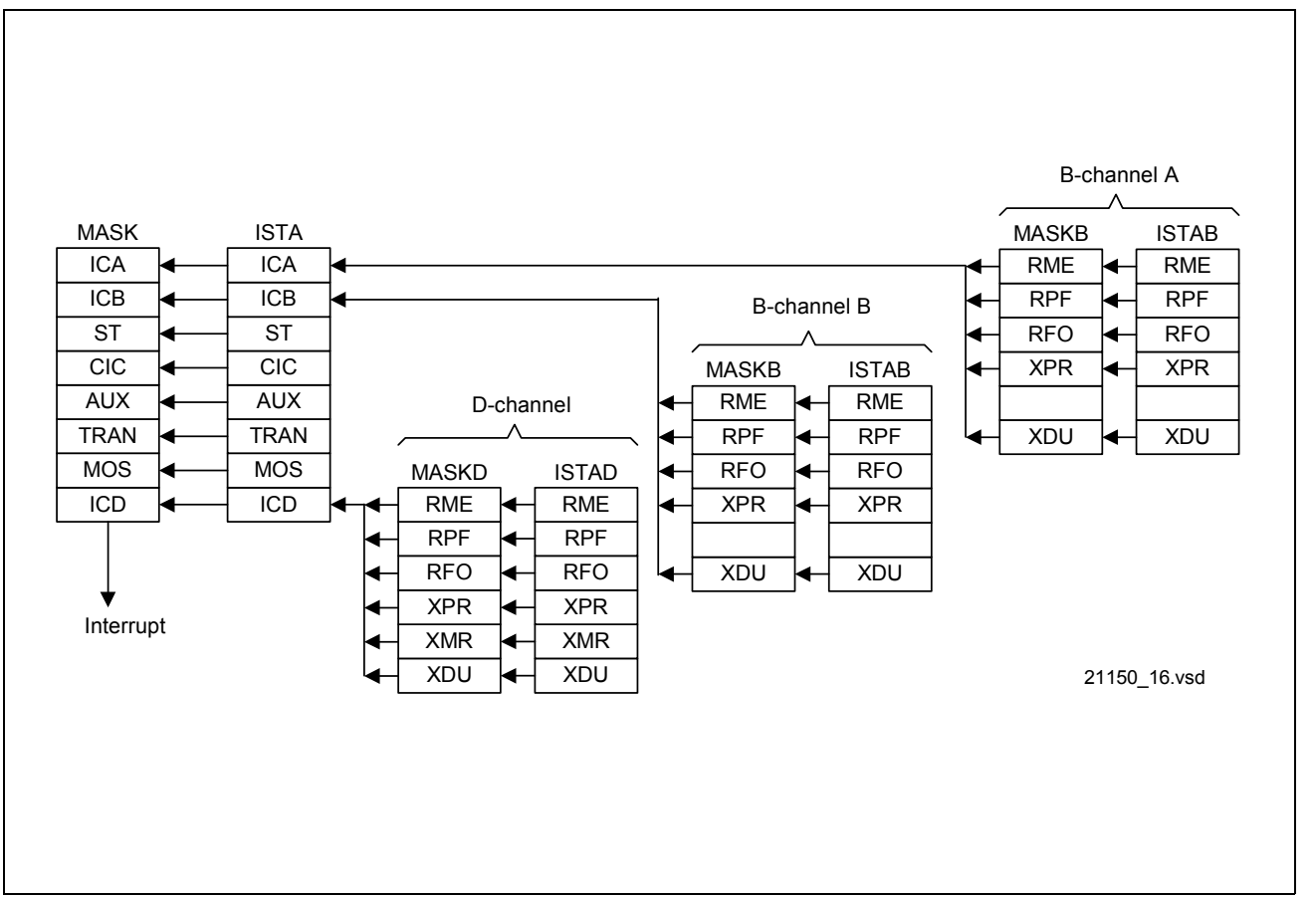



**Figure 86 Interrupt Status Registers of the HDLC Controllers**

Each interrupt source in the ISTAD and ISTAB registers can selectively be masked by setting the corresponding bit in MASKD/MASKB to “1”.

## 3.10 Test Functions

The IPAC-X provides test and diagnostic functions for the S-interface, the D-channel and each of the two B-channels:

- Digital loop via TLP (Test Loop, TMD and TMB registers) command bit (**Figure 87**): The TX path of layer 2 is internally connected with the RX path of layer 2. The output from layer 1 (S/T) on DD is ignored. This is used for testing IPAC-X functionality excluding layer 1 (loopback between XFIFOx and RFIFOx).

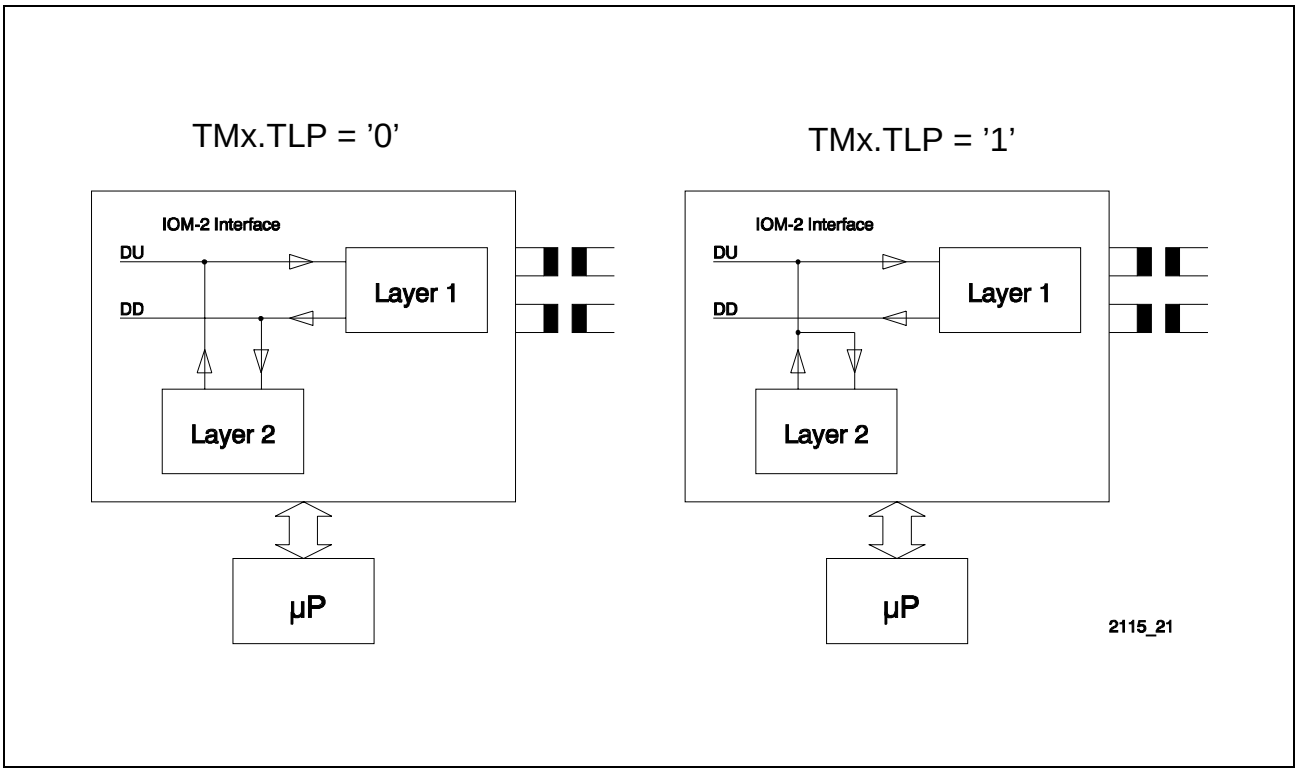



**Figure 87 Layer 2 Test Loops**

- Test of layer-2 functions while disabling all layer-1 functions and pins associated with them (including clocking) via bit TR_CONF0.DIS_TR. The HDLC controllers can still operate via IOM-2. DCL and FSC pins become input.

- Loop at the analog end of the S interface;

  TE / LT-T mode

  Test loop 3 is activated with the C/I channel command Activate Request Loop (ARL). An S interface is not required since INFO3 is looped back internally to the receiver. When the receiver has synchronized itself to this signal, the message "Test Indication" (or "Awake Test Indication") is delivered in the C/I channel. No signal is transmitted over the S interface.
  In the test loop mode the S interface awake detector is enabled, i.e. if a level is detected (e.g. Info 2/Info 4) this will be reported by the Resynchronization Indication (RSY). The loop function is not effected by this condition and the internally generated 192-kHz line clock does not depend on the signal received at the S interface.

  NT / LT-S mode

  Test loop 2 is likewise activated over the IOM-2 interface with Activate Request Loop (ARL). No S line is required. INFO4 is looped back internally to the receiver and also sent to the S interface. When the receiver is synchronized, the message "AIU" is sent in the C/I channel. In the test loop mode the S interface awake detector is disabled, and echo bits are set to logical "0".

- Transmission of special test signals on the S/T interface according to the modified AMI code are initiated via a C/I command written in CIX0 register.

  Two kinds of test signals may be sent by the IPAC-X:

  – single pulses and
  – continuous pulses.

  The single pulses are of alternating polarity, one S interface bit period wide, 0.25 ms apart, with a repetition frequency of 2 kHz. Single pulses can be sent in all applications. The corresponding C/I command in TE, LT-S and LT-T applications is TM1.

  Continuous pulses are likewise of alternating polarity, one S-interface bit period wide, but they are sent continuously. The repetition frequency is 96 kHz. Continuous pulses may be transmitted in all applications. This test mode is entered in LT-S, LT-T and TE applications with the C/I command TM2.

# 4 Detailed Register Description

The register mapping of the IPAC-X is shown in **Figure 88**.

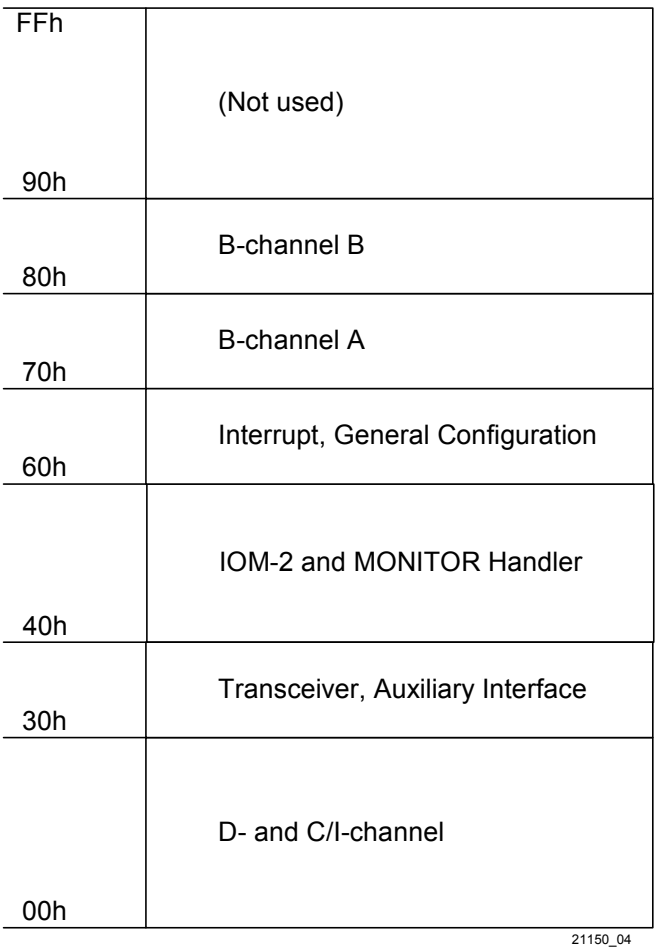



**Figure 88 Register Mapping of the IPAC-X**

The register address range from $00_H$-$2F_H$ is assigned to the D-channel HDLC controller and the C/I-channel handler.

The register set ranging from $30_H$-$3F_H$ pertains to the transceiver and auxiliary interface registers.

The address range from $40_H$-$5B_H$ is assigned to the IOM handler with the registers for timeslot and data port selection (TSDP) and the control registers (CR) for the transceiver data (TR), Monitor data (MON), HDLC/CI data (HCI) and controller access data (CDA), serial data strobe signal (SDS), IOM interface (IOM) and synchronous transfer interrupt (STI).

The address range from $5C_H$-$5F_H$ pertains to the MONITOR handler.

General interrupt and configuration registers are contained in the address range $60_H$-$65_H$.

The address range $70_H$-$8F_H$ is assigned to the two B-channel FIFOs and HDLC controllers having an identical set of registers.

The register summaries of the IPAC-X are shown in the following tables containing the abbreviation of the register name and the register bits, the register address, the reset values and the register type (Read/Write). A detailed register description follows these register summaries.

The register summaries and the description are sorted in ascending order of the register address.

**D-channel HDLC, C/I-channel Handler**

| Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDR | R/W | RES |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RFIFOD | D-Channel Receive FIFO | | | | | | | | $00_H$-$1F_H$ | R | |
| XFIFOD | D-Channel Transmit FIFO | | | | | | | | $00_H$-$1F_H$ | W | |
| ISTAD | RME | RPF | RFO | XPR | XMR | XDU | 0 | 0 | $20_H$ | R | $10_H$ |
| MASKD | RME | RPF | RFO | XPR | XMR | XDU | 1 | 1 | $20_H$ | W | $FF_H$ |
| STARD | XDOV | XFW | 0 | 0 | RACI | 0 | XACI | 0 | $21_H$ | R | $40_H$ |
| CMDRD | RMC | RRES | 0 | STI | XTF | 0 | XME | XRES | $21_H$ | W | $00_H$ |
| MODED | MDS2 | MDS1 | MDS0 | 0 | RAC | DIM2 | DIM1 | DIM0 | $22_H$ | R/W | $C0_H$ |
| EXMD1 | XFBS | RFBS | | SRA | XCRC | RCRC | 0 | ITF | $23_H$ | R/W | $00_H$ |
| TIMR1 | CNT | | | VALUE | | | | | $24_H$ | R/W | $00_H$ |
| SAP1 | SAPI1 | | | | | | 0 | MHA | $25_H$ | W | $FC_H$ |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SAP2 | SAPI2 | | | | | | 0 | MLA | $26_H$ | W | $FC_H$ |
| RBCLD | RBC7 | | | | | | | RBC0 | $26_H$ | R | $00_H$ |
| RBCHD | 0 | 0 | 0 | OV | RBC11 | | | RBC8 | $27_H$ | R | $00_H$ |
| TEI1 | TEI1 | | | | | | | EA1 | $27_H$ | W | $FF_H$ |
| TEI2 | TEI2 | | | | | | | EA2 | $28_H$ | W | $FF_H$ |
| RSTAD | VFR | RDO | CRC | RAB | SA1 | SA0 | C/R | TA | $28_H$ | R | $0F_H$ |
| TMD | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TLP | $29_H$ | R/W | $00_H$ |
| | reserved | | | | | | | | $2A\text{-}2D_H$ | | |
| CIR0 | CODR0 | | | | CIC0 | CIC1 | S/G | BAS | $2E_H$ | R | $F3_H$ |
| CIX0 | CODX0 | | | | TBA2 | TBA1 | TBA0 | BAC | $2E_H$ | W | $FE_H$ |
| CIR1 | CODR1 | | | | | | CICW | CI1E | $2F_H$ | R | $FE_H$ |
| CIX1 | CODX1 | | | | | | CICW | CI1E | $2F_H$ | W | $FE_H$ |

### Transceiver, Auxiliary Interface

| NAME | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDR | R/W | RES |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TR_CONF0 | DIS_TR | BUS | EN_ICV | 0 | L1SW | 0 | EXLP | LDD | $30_H$ | R/W | $01_H$ |
| TR_CONF1 | 0 | RPLL_ADJ | EN_SFSC | 0 | 0 | x | x | x | $31_H$ | R/W | |
| TR_CONF2 | DIS_TX | PDS | 0 | RLP | 0 | 0 | SGP | SGD | $32_H$ | R/W | $80_H$ |
| TR_STA | RINF | | SLIP | ICV | 0 | FSYN | 0 | LD | $33_H$ | R | $00_H$ |
| TR_CMD | XINF | | | DPRIO | TDDIS | PD | LP_A | 0 | $34_H$ | R/W | $08_H$ |
| SQRR1 | MSYN | MFEN | 0 | 0 | SQR11 | SQR12 | SQR13 | SQR14 | $35_H$ | R | $40_H$ |
| SQXR1 | 0 | MFEN | 0 | 0 | SQX11 | SQX12 | SQX13 | SQX14 | $35_H$ | W | $4F_H$ |

### Transceiver, Auxiliary Interface

| NAME | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDR | R/W | RES |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SQRR2 | SQR21 | SQR22 | SQR23 | SQR24 | SQR31 | SQR32 | SQR33 | SQR34 | $36_H$ | R | $00_H$ |
| SQXR2 | SQX21 | SQX22 | SQX23 | SQX24 | SQX31 | SQX32 | SQX33 | SQX34 | $36_H$ | W | $00_H$ |
| SQRR3 | SQR41 | SQR42 | SQR43 | SQR44 | SQR51 | SQR52 | SQR53 | SQR54 | $37_H$ | R | $00_H$ |
| SQXR3 | SQX41 | SQX42 | SQX43 | SQX44 | SQX51 | SQX52 | SQX53 | SQX54 | $37_H$ | W | $00_H$ |
| ISTATR | 0 | x | x | x | LD | RIC | SQC | SQW | $38_H$ | R | $00_H$ |
| MASKTR | 1 | 1 | 1 | 1 | LD | RIC | SQC | SQW | $39_H$ | R/W | $FF_H$ |
| TR_ MODE | 0 | 0 | 0 | 0 | DCH_ INH | MODE 2 | MODE 1 | MODE 0 | $3A_H$ | R/W | $00_H$ |
| | reserved | | | | | | | | $3B_H$ | | |
| ACFG1 | OD7 | OD6 | OD5 | OD4 | OD3 | OD2 | OD1 | OD0 | $3C_H$ | R/W | $00_H$ |
| ACFG2 | A7SEL | A5SEL | FBS | A4SEL | ACL | LED | EL1 | EL0 | $3D_H$ | R/W | $00_H$ |
| AOE | OE7 | OE6 | OE5 | OE4 | OE3 | OE2 | OE1 | OE0 | $3E_H$ | R/W | $FF_H$ |
| ARX | AR7 | AR6 | AR5 | AR4 | AR3 | AR2 | AR1 | AR0 | $3F_H$ | R | |
| ATX | AT7 | AT6 | AT5 | AT4 | AT3 | AT2 | AT1 | AT0 | $3F_H$ | W | $00_H$ |

### IOM Handler (Timeslot , Data Port Selection, CDA Data and CDA Control Register)

| Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDR | R/W | RES |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CDA10 | Controller Data Access Register (CH10) | | | | | | | | 40H | R/W | FFH |
| CDA11 | Controller Data Access Register (CH11) | | | | | | | | 41H | R/W | FFH |
| CDA20 | Controller Data Access Register (CH20) | | | | | | | | 42H | R/W | FFH |
| CDA21 | Controller Data Access Register (CH21) | | | | | | | | 43H | R/W | FFH |
| CDA_ TSDP10 | DPS | 0 | 0 | TSS | | | | | 44H | R/W | 00H |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CDA_TSDP11 | DPS | 0 | 0 | TSS | | | | | 45H | R/W | 01H |
| CDA_TSDP20 | DPS | 0 | 0 | TSS | | | | | 46H | R/W | 80H |
| CDA_TSDP21 | DPS | 0 | 0 | TSS | | | | | 47H | R/W | 81H |
| BCHA_TSDP_BC1 | DPS | 0 | 0 | TSS | | | | | 48H | R/W | 80H |
| BCHA_TSDP_BC2 | DPS | 0 | 0 | TSS | | | | | 49H | R/W | 81H |
| BCHB_TSDP_BC1 | DPS | 0 | 0 | TSS | | | | | 4AH | R/W | 81H |
| BCHB_TSDP_BC2 | DPS | 0 | 0 | TSS | | | | | 4BH | R/W | 85H |
| TR_TSDP_BC1 | DPS | 0 | 0 | TSS | | | | | 4CH | R/W | |
| TR_TSDP_BC2 | DPS | 0 | 0 | TSS | | | | | 4DH | R/W | |
| CDA1_CR | 0 | 0 | EN_TBM | EN_I1 | EN_I0 | EN_O1 | EN_O0 | SWAP | 4EH | R/W | 00H |
| CDA2_CR | 0 | 0 | EN_TBM | EN_I1 | EN_I0 | EN_O1 | EN_O0 | SWAP | 4FH | R/W | 00H |

**IOM Handler (Control Registers, Synchronous Transfer Interrupt Control), MONITOR Handler**

| Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDR | R/W | RES |
|---|---|---|---|---|---|---|---|---|---|---|---|

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TR_CR (CI_CS=0) | EN_D | EN_B2R | EN_B1R | EN_B2X | EN_B1X | CS2-0 | | | $50_H$ | R/W | |
| TRC_CR (CI_CS=1) | 0 | 0 | 0 | 0 | 0 | CS2-0 | | | $50_H$ | R/W | |
| BCHA_CR | DPS_D | 0 | EN_D | EN_BC2 | EN_BC1 | CS2-0 | | | $51_H$ | R/W | $80_H$ |
| BCHB_CR | DPS_D | 0 | EN_D | EN_BC2 | EN_BC1 | CS2-0 | | | $52_H$ | R/W | $81_H$ |
| DCI_CR (CI_CS=0) | DPS_CI1 | EN_CI1 | D_EN_D | D_EN_B2 | D_EN_B1 | CS2-0 | | | $53_H$ | R/W | |
| DCIC_CR (CI_CS=1) | 0 | 0 | 0 | 0 | 0 | CS2-0 | | | $53_H$ | R/W | 00H |
| MON_CR | DPS | EN_MON | 0 | 0 | 0 | CS2-0 | | | $54_H$ | R/W | |
| SDS1_CR | ENS_TSS | ENS_TSS+1 | ENS_TSS+3 | TSS | | | | | $55_H$ | R/W | $00_H$ |
| SDS2_CR | ENS_TSS | ENS_TSS+1 | ENS_TSS+3 | TSS | | | | | $56_H$ | R/W | $00_H$ |
| IOM_CR | SPU | DIS_AW | CI_CS | TIC_DIS | EN_BCL | CLKM | DIS_OD | DIS_IOM | $57_H$ | R/W | $08_H$ |
| STI | STOV21 | STOV20 | STOV11 | STOV10 | STI21 | STI20 | STI11 | STI10 | $58_H$ | R | $00_H$ |
| ASTI | 0 | 0 | 0 | 0 | ACK21 | ACK20 | ACK11 | ACK10 | $58_H$ | W | $00_H$ |
| MSTI | STOV21 | STOV20 | STOV11 | STOV10 | STI21 | STI20 | STI11 | STI10 | $59_H$ | R/W | $FF_H$ |
| SDS_CONF | 0 | 0 | 0 | 0 | DIOM_INV | DIOM_SDS | SDS2_BCL | SDS1_BCL | $5A_H$ | R/W | $00_H$ |
| MCDA | MCDA21 | | MCDA20 | | MCDA11 | | MCDA10 | | $5B_H$ | R | $FF_H$ |
| MOR | MONITOR Receive Data | | | | | | | | $5C_H$ | R | $FF_H$ |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MOX | MONITOR Transmit Data | | | | | | | | $5C_H$ | W | $FF_H$ |
| MOSR | MDR | MER | MDA | MAB | 0 | 0 | 0 | 0 | $5D_H$ | R | $00_H$ |
| MOCR | MRE | MRC | MIE | MXC | 0 | 0 | 0 | 0 | $5E_H$ | R/W | $00_H$ |
| MSTA | 0 | 0 | 0 | 0 | 0 | MAC | 0 | TOUT | $5F_H$ | R | $00_H$ |
| MCONF | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TOUT | $5F_H$ | W | $00_H$ |

### Interrupt, General Configuration Registers

| NAME | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDR | R/W | RES |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISTA | ICA | ICB | ST | CIC | AUX | TRAN | MOS | ICD | $60_H$ | R | $00_H$ |
| MASK | ICA | ICB | ST | CIC | AUX | TRAN | MOS | ICD | $60_H$ | W | $FF_H$ |
| AUXI | 0 | 0 | EAW | WOV | TIN2 | TIN1 | INT1 | INT0 | $61_H$ | R | $00_H$ |
| AUXM | 1 | 1 | EAW | WOV | TIN2 | TIN1 | INT1 | INT0 | $61_H$ | W | $FF_H$ |
| MODE1 | 0 | 0 | 0 | WTC1 | WTC2 | CFS | RSS2 | RSS1 | $62_H$ | R/W | $00_H$ |
| MODE2 | 0 | 0 | 0 | 0 | INT_ POL | 0 | 0 | PPSDX | $63_H$ | R/W | $00_H$ |
| ID | 0 | 0 | DESIGN | | | | | | $64_H$ | R | $01_H$ |
| SRES | RES_ CI | RES_ BCHA | RES_ BCHB | RES_ MON | RES_ DCH | RES_ IOM | RES_ TR | RES_ RSTO | $64_H$ | W | $00_H$ |
| TIMR2 | TMD | 0 | CNT | | | | | | $65_H$ | R/W | $00_H$ |
| | reserved | | | | | | | | $66_H$- $6F_H$ | | |

### B-channel HDLC Control Registers (channel A / B)

| Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDR | R/W | RES |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISTAB | RME | RPF | RFO | XPR | 0 | XDU | 0 | 0 | $70_H$/$80_H$ | R | $10_H$ |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MASKB | RME | RPF | RFO | XPR | 1 | XDU | 1 | 1 | $70_H/80_H$ | W | $FF_H$ |
| STARB | XDOV | XFW | 0 | 0 | RACI | 0 | XACI | 0 | $71_H/81_H$ | R | $40_H$ |
| CMDRB | RMC | RRES | 0 | 0 | XTF | 0 | XME | XRES | $71_H/81_H$ | W | $00_H$ |
| MODEB | MDS2 | MDS1 | MDS0 | 0 | RAC | 0 | 0 | 0 | $72_H/82_H$ | R/W | $C0_H$ |
| EXMB | XFBS | RFBS | | SRA | XCRC | RCRC | 0 | ITF | $73_H/83_H$ | R/W | $00_H$ |
| | reserved | | | | | | | | $74_H/84_H$ | | |
| RAH1 | RAH1 | | | | | | 0 | MHA | $75_H/85_H$ | W | $00_H$ |
| RAH2 | RAH2 | | | | | | 0 | MLA | $76_H/86_H$ | W | $00_H$ |
| RBCLB | RBC7 | | | | | | | RBC0 | $76_H/86_H$ | R | $00_H$ |
| RBCHB | 0 | 0 | 0 | OV | RBC11 | | | RBC8 | $77_H/87_H$ | R | $00_H$ |
| RAL1 | RAL1 | | | | | | | | $77_H/87_H$ | W | $00_H$ |
| RAL2 | RAL2 | | | | | | | | $78_H/88_H$ | W | $00_H$ |
| RSTAB | VFR | RDO | CRC | RAB | HA1 | HA0 | C/R | LA | $78_H/88_H$ | R | $0E_H$ |
| TMB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TLP | $79_H/89_H$ | R/W | $00_H$ |
| RFIFOB | B-Channel Receive FIFO | | | | | | | | $7A_H/8A_H$ | R | |
| XFIFOB | B-Channel Transmit FIFO | | | | | | | | $7A_H/8A_H$ | W | |
| | reserved | | | | | | | | $7B_H$-$7F_H$ $8B_H$-$8F_H$ | | |

## 4.1 D-channel HDLC Control and C/I Registers

### 4.1.1 RFIFOD - Receive FIFO D-Channel

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| RFIFOD | Receive data | | | | | | | | RD (00-1F) |

A read access to any address within the range 00h-1Fh gives access to the “current” FIFO location selected by an internal pointer which is automatically incremented after each read access. This allows for the use of efficient “move string” type commands by the microcontroller.

The RFIFOD contains up to 32 bytes of received data.

After an ISTAD.RPF interrupt, a complete data block is available. The block size can be 4, 8, 16 or 32 bytes depending on the EXMD2.RFBS setting.

After an ISTAD.RME interrupt, the number of received bytes can be obtained by reading the RBCLD register.

### 4.1.2 XFIFOD - Transmit FIFO D-Channel

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| XFIFOD | Transmit data | | | | | | | | WR (00-1F) |

A write access to any address within the range 00-1F$_H$ gives access to the “current” FIFO location selected by an internal pointer which is automatically incremented after each write access. This allows the use of efficient “move string” type commands by the microcontroller.

Depending on EXMD2.XFBS up to 16 or 32 bytes of transmit data can be written to the XFIFOD following an ISTAD.XPR interrupt.

### 4.1.3 ISTAD - Interrupt Status Register D-Channel

Value after reset: 10$_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| ISTAD | RME | RPF | RFO | XPR | XMR | XDU | 0 | 0 | RD (20) |

### RME ... Receive Message End

One complete frame of length less than or equal to the defined block size (EXMD1.RFBS) or the last part of a frame of length greater than the defined block size has been received. The contents are available in the RFIFOD. The message length and additional information may be obtained from RBCHD and RBCLD and the RSTAD register.

### RPF ... Receive Pool Full

A data block of a frame longer than the defined block size (EXMD1.RFBS) has been received and is available in the RFIFOD. The frame is not yet complete.

### RFO ... Receive Frame Overflow

The received data of a frame could not be stored, because the RFIFOD is occupied. The whole message is lost.

This interrupt can be used for statistical purposes and indicates that the microcontroller does not respond quickly enough to an RPF or RME interrupt (ISTAD).

### XPR ... Transmit Pool Ready

A data block of up to the defined block size 16 or 32 (EXMD1.XFBS) can be written to the XFIFOD.

An XPR interrupt will be generated in the following cases:

- after an XTF or XME command as soon as the 16 or 32 bytes in the XFIFO are available and the frame is not yet complete
- after an XTF together with an XME command is issued, when the whole frame has been transmitted
- after a reset of the transmitter (XRES)
- after a device reset

### XMR ... Transmit Message Repeat

The transmission of the last frame has to be repeated because a collision on the S bus has been detected after the $16^{th}$/$32^{nd}$ data byte of a transmit frame.

If an XMR interrupt occurs the transmit FIFO is locked until the XMR interrupt is read by the host (interrupt cannot be read if masked in MASKD).

### XDU ... Transmit Data Underrun

The current transmission of a frame is aborted by transmitting seven ’1’s because the XFIFOD holds no further data. This interrupt occurs whenever the microcontroller has failed to respond to an XPR interrupt (ISTAD register) quickly enough, after having initiated a transmission and the message to be transmitted is not yet complete.

If an XDU interrupt occurs the transmit FIFO is locked until the XDU interrupt is read by the host (interrupt cannot be read if masked in MASKD).

### 4.1.4 MASKD - Mask Register D-Channel

Value after reset: $FF_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| MASKD | RME | RPF | RFO | XPR | XMR | XDU | 1 | 1 | WR (20) |

Each interrupt source in the ISTAD register can selectively be masked by setting the corresponding bit in MASKD to ’1’. Masked interrupt status bits are not indicated when ISTAD is read. Instead, they remain internally stored and pending until the mask bit is reset to ’0’.

### 4.1.5 STARD - Status Register D-Channel

Value after reset: $40_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| STARD | XDOV | XFW | 0 | 0 | RACI | 0 | XACI | 0 | RD (21) |

**XDOV ... Transmit Data Overflow**

More than 16 or 32 bytes (according to selected block size) have been written to the XFIFOD, i.e. data has been overwritten.

**XFW ... Transmit FIFO Write Enable**

Data can be written to the XFIFOD. This bit may be polled instead of (or in addition to) using the XPR interrupt.

**RACI ... Receiver Active Indication**

The D-channel HDLC receiver is active when RACI = ’1’. This bit may be polled. The RACI bit is set active after a begin flag has been received and is reset after receiving an abort sequence.

### XACI ... Transmitter Active Indication

The D-channel HDLC-transmitter is active when XACI = ’1’. This bit may be polled. The XACI-bit is active when an XTF-command is issued and the frame has not been completely transmitted

## 4.1.6 CMDRD - Command Register D-Channel

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| CMDRD | RMC | RRES | 0 | STI | XTF | 0 | XME | XRES | WR (21) |

### RMC ... Receive Message Complete

Reaction to RPF (Receive Pool Full) or RME (Receive Message End) interrupt. By setting this bit, the microcontroller confirms that it has fetched the data, and indicates that the corresponding space in the RFIFOD may be released.

### RRES ... Receiver Reset

HDLC receiver is reset, the RFIFOD is cleared of any data.

### STI ... Start Timer 1

The IPAC-X timer 1 is started when STI is set to one. The timer is stopped by writing to the TIMR1 register.

*Note: Timer 2 is controlled by the TIMR2 register only.*

### XTF ... Transmit Transparent Frame

After having written up to 16 or 32 bytes (EXMD1.XFBS) to the XFIFOD, the microcontroller initiates the transmission of a transparent frame by setting this bit to ’1’. The opening flag is automatically added to the message by the IPAC-X (except in the extended transparent mode where no flags are used).

### XME ... Transmit Message End

By setting this bit to ’1’ the microcontroller indicates that the data block written last to the XFIFOD completes the corresponding frame. The IPAC-X terminates the transmission by appending the CRC (if EXMD1.XCRC=0) and the closing flag sequence to the data (except in the extended transparent mode where no such framing is used).

**XRES ... Transmitter Reset**

The D-channel HDLC transmitter is reset and the XFIFOD is cleared of any data. This command can be used by the microcontroller to abort a frame currently in transmission.

*Note: After an XPR interrupt further data has to be written to the XFIFOD and the appropriate Transmit Command (XTF) has to be written to the CMDRD register again to continue transmission, when the current frame is not yet complete (see also XPR in ISTAD).*
*During frame transmission, the 0-bit insertion according to the HDLC bit-stuffing mechanism is done automatically.*

## 4.1.7 MODED - Mode Register

Value after reset: $C0_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| MODED | MDS2 | MDS1 | MDS0 | 0 | RAC | DIM2 | DIM1 | DIM0 | RD/WR (22) |

**MDS2-0 ... Mode Select**

Determines the message transfer mode of the HDLC controller, as follows:

| MDS2-0 | Mode | Number of Address Bytes | Address Comparison | | Remark |
|---|---|---|---|---|---|
| | | | 1.Byte | 2.Byte | |
| 0 0 0 | Reserved | | | | |
| 0 0 1 | Reserved | | | | |
| 0 1 0 | Non-Auto mode | 1 | TEI1,TEI2 | – | One-byte address compare. |
| 0 1 1 | Non-Auto mode | 2 | SAP1,SAP2,SAPG | TEI1,TEI2,TEIG | Two-byte address compare. |
| 1 0 0 | Extended transparent mode | | | | |

| MDS2-0 | Mode | Number of Address Bytes | Address Comparison | | Remark |
|---|---|---|---|---|---|
| | | | 1.Byte | 2.Byte | |
| 1 1 0 | Transparent mode 0 | – | – | – | No address compare. All frames accepted. |
| 1 1 1 | Transparent mode 1 | > 1 | SAP1,SAP2,SAPG | – | High-byte address compare. |
| 1 0 1 | Transparent mode 2 | > 1 | – | TEI1,TEI2,TEIG | Low-byte address compare. |

*Note: SAP1, SAP2: two programmable address values for the first received address byte (in the case of an address field longer than 1 byte);*
*SAPG = fixed value FC / $FE_H$.*
*TEI1, TEI2: two programmable address values for the second (or the only, in the case of a one-byte address) received address byte;*
*TEIG = fixed value $FF_H$*
*Two different methods of the high byte and/or low byte address comparison can be selected by setting SAP1.MHA and/or SAP2.MLA.*

### RAC ... Receiver Active

The D-channel HDLC receiver is activated when this bit is set to ’1’. If set to ’0’ the HDLC data is not evaluated in the receiver.

### DIM2-0 ... Digital Interface Modes

These bits define the characteristics of the IOM Data Ports (DU, DD). The DIM0 bit enables/disables the collission detection. The DIM1 bit enables/disables the TIC bus access. The effect of the individual DIM bits is summarized in the table below**.**

| DIM2 | DIM1 | DIM0 | Characteristics |
|---|---|---|---|
| 0 | | 0 | Transparent D-channel, the collission detection is disabled |
| 0 | | 1 | Stop/go bit evaluated for D-channel access handling |
| 0 | 0 | | Last octet of IOM channel 2 used for TIC bus access |
| 0 | 1 | | TIC bus access is disabled |
| 1 | x | x | Reserved |

### 4.1.8 EXMD1- Extended Mode Register D-channel 1

Value after reset: $00_H$

| | 7 | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|
| EXMD1 | XFBS | RFBS | SRA | XCRC | RCRC | 0 | ITF | RD/WR (23) |

**XFBS … Transmit FIFO Block Size**

0 … Block size for the transmit FIFO data is 32 byte
1 … Block size for the transmit FIFO data is 16 byte

*Note: A change of XFBS will take effect after a receiver command (CMDRD.XME, CMDRD.XRES, CMDRD.XTF) has been written.*

**RFBS … Receive FIFO Block Size**

| RFBS | | Block Size Receive FIFO |
|---|---|---|
| Bit 6 | Bit5 | |
| 0 | 0 | 32 byte |
| 0 | 1 | 16 byte |
| 1 | 0 | 8 byte |
| 1 | 1 | 4 byte |

*Note: A change of RFBS will take effect after a transmitter command (CMDR.RMC, CMDR.RRES,) has been written*

**SRA … Store Receive Address**

0 … Receive Address isn't stored in the RFIFOD
1 … Receive Address is stored in the RFIFOD

**XCRC … Transmit CRC**

0 … CRC is transmitted
1 … CRC isn't transmitted

**RCRC… Receive CRC**

0 … CRC isn't stored in the RFIFOD
1 … CRC is stored in the RFIFOD

**ITF… Interframe Time Fill**

Selects the inter-frame time fill signal which is transmitted between HDLC-frames.

0 … idle (continuous '1')
1 … flags (sequence of patterns: '0111 1110')

*Note: ITF must be set to '0' for power down mode.*
*In applications with D-channel access handling (collision resolution), the only possible inter-frame time fill is idle* (continuous '1'). *Otherwise the D-channel on the S/T-bus cannot be accessed*

### 4.1.9 TIMR1 - Timer 1 Register

Value after reset: $00_H$

| | 7 5 | 4 0 | |
|---|---|---|---|
| TIMR1 | CNT | VALUE | RD/WR (24) |

**CNT ... Timer Counter**

CNT together with VALUE determines the time period T after which a AUXI.TIN1 interrupt will be generated:

CNT=0...6:T = CNT x 2.048 sec + T1 with T1 = ( VALUE+1 ) x 0.064 sec

CNT=7:T = T1 = ( VALUE+1 ) x 0.064 sec (generated periodically)

The timer can be started by setting the STI-bit in CMDRD and will be stopped when a TIN1 interrupt is generated or the TIMR1 register is written.

*Note: If CNT is set to 7, a TIN interrupt is indefinitely generated after every expiration of T1 (i.e. T = T1).*

**VALUE ... Timer Value**

Determines the value of the timer value **T1 = ( VALUE + 1 ) x 0.064 sec**.

### 4.1.10 SAP1 - SAPI1 Register

Value after reset: $FC_H$

| | 7 | | | 0 | |
|---|---|---|---|---|---|
| SAP1 | SAPI1 | | 0 | MHA | WR (25) |

**SAPI1 ... SAPI1 value**

Value of the first programmable Service Access Point Identifier (SAPI) according to the ISDN LAPD protocol.

**MHA... Mask High Address**

0 … The SAPI address of an incomming frame is compared with SAP1, SAP2, SAPG.
1 … The SAPI address of an incomming frame is compared with SAP1 and SAPG. SAP1 can be masked with SAP2 thereby bit positions of SAP1 are not compared if they are set to ’1’ in SAP2.

### 4.1.11 SAP2 - SAPI2 Register

Value after reset: $FC_H$

| | 7 | | | 0 | |
|---|---|---|---|---|---|
| SAP2 | SAPI2 | | 0 | MLA | WR (26) |

**SAPI2 ... SAPI2 value**

Value of the second programmable Service Access Point Identifier (SAPI) according to the ISDN LAPD-protocol.

**MLA... Mask Low Address**

0 … The TEI address of an incomming frame is compared with TEI1, TEI2 and TEIG.
1 … The TEI address of an incomming frame is compared with TEI1 and TEIG. TEI1 can be masked with TEI2 thereby bit positions of TEI1 are not compared if they are set to ’1’ in TEI2.

### 4.1.12 RBCLD - Receive Frame Byte Count Low D-Channel

Value after reset: $00_H$

| | 7 | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|
| RBCLD | RBC7 | | | | | | RBC0 | RD (26) |

**RBC7-0 ... Receive Byte Count**

Eight least significant bits of the total number of bytes in a received message (see RBCHD register).

### 4.1.13 RBCHD - Receive Frame Byte Count High D-Channel

Value after reset: $00_H$.

| | 7 | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|
| RBCHD | 0 | 0 | 0 | OV | RBC11 | | RBC8 | RD (27) |

**OV ... Overflow**

A ’1’ in this bit position indicates a message longer than $(2^{12} - 1) = 4095$ bytes .

**RBC8-11 ... Receive Byte Count**

Four most significant bits of the total number of bytes in a received message (see RBCLD register).

*Note: Normally RBCHD and RBCLD should be read by the microcontroller after an RME-interrupt in order to determine the number of bytes to be read from the RFIFOD, and the total message length. The contents of the registers are valid only after an RME or RPF interrupt, and remain so until the frame is acknowledged via the RMC bit or RRES.*

### 4.1.14 TEI1 - TEI1 Register 1

Value after reset: $FF_H$

| | 7 | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|
| TEI1 | TEI1 | | | | | | EA1 | WR (27) |

**TEI1 ... Terminal Endpoint Identifier**

In all message transfer modes except in transparent modes 0, 1 and extended transparent mode, TEI1 is used by the IPAC-X for address recognition. In the case of a two-byte address field, it contains the value of the first programmable Terminal Endpoint Identifier according to the ISDN LAPD-protocol.
In non-automodes with one-byte address field, TEI1 is a command address, according to X.25 LAPB.

**EA1 ... Address field Extension bit**

This bit is set to ’1’ according to HDLC/LAPD.

## 4.1.15 TEI2 - TEI2 Register

Value after reset: $FF_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| TEI2 | TEI2 | | | | | | | EA2 | WR (28) |

**TEI2 ... Terminal Endpoint Identifier**

In all message transfer modes except in transparent modes 0, 1 and extended transparent mode, TEI2 is used by the IPAC-X for address recognition. In the case of a two-byte address field, it contains the value of the second programmable Terminal Endpoint Identifier according of the ISDN LAPD-protocol.
In non-auto-modes with one-byte address field, TEI2 is a response address, according to X.25 LAPD.

**EA2 ... Address field Extension bit**

This bit is to be set to ’1’ according to HDLC/LAPD.

## 4.1.16 RSTAD - Receive Status Register D-Channel

Value after reset: $0F_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| RSTAD | VFR | RDO | CRC | RAB | SA1 | SA0 | C/R | TA | RD (28) |

For general information please refer to **Chapter 3.9**.

### VFR... Valid Frame

Determines whether a valid frame has been received.
The frame is valid (1) or invalid (0).
A frame is invalid when there is not a multiple of 8 bits between flag and frame end (flag, abort).

### RDO ... Receive Data Overflow

If RDO=1, at least one byte of the frame has been lost, because it could not be stored in RFIFOD. As opposed to the ISTAD.RFO an RDO indicates that the beginning of a frame has been received but not all bytes could be stored as the RFIFOD was temporarily full.

### CRC ... CRC Check

The CRC is correct (1) or incorrect (0).

### RAB ... Receive Message Aborted

The receive message was aborted by the remote station (1), i.e. a sequence of seven 1’s was detected before a closing flag.

### SA1-0 ... SAPI Address Identification

### TA ... TEI Address Identification

SA1-0 are significant in non-automode with a two-byte address field, as well as in transparent mode 3. TA is significant in all modes except in transparent modes 0 and 1.

Two programmable SAPI values (SAP1, SAP2) plus a fixed group SAPI (SAPG of value $FC_H$/$FE_H$), and two programmable TEI values (TEI1, TEI2) plus a fixed group TEI (TEIG of value $FF_H$), are available for address comparison.

The result of the address comparison is given by SA1-0 and TA, as follows:

| MDS2-0 | SA1 | SA0 | TA | Address Match with 1st Byte | Address Match with 2nd Byte |
|---|---|---|---|---|---|
| **010 (Non-Auto/8 Mode)** | x<br>x | x<br>x | 0<br>1 | TEI2<br>TEI1 | -<br>- |
| **011 (Non-Auto/16 Mode)** | 0<br>0<br>0<br>0<br>1<br>1 | 0<br>0<br>1<br>1<br>0<br>0 | 0<br>1<br>0<br>1<br>0<br>1 | SAP2<br>SAP2<br>SAPG<br>SAPG<br>SAP1<br>SAP1 | TEIG<br>TEI2<br>TEIG<br>TEI1 or TEI2<br>TEIG<br>TEI1 |
| **111 (Transparent Mode1)** | 0<br>0<br>1 | 0<br>1<br>0 | x<br>x<br>x | SAP2<br>SAPG<br>SAP1 | -<br>-<br>- |
| **101 (Transparent Mode 2)** | -<br>- | -<br>- | 0<br>1 | -<br>- | TEIG<br>TEI1 or TEI2 |
| | 1 | 1 | x | reserved | |

*Note: If SAP1 and SAP2 contain identical values, the combination SAP1,2-TEIG will only be indicated by SA1,0 = ’10’ (i.e. the value ’00’ will not occur in this case).*

**C/R ... Command/Response**

The C/R bit contains the C/R bit of the received frame (Bit1 in the SAPI address)

*Note: The contents of RSTAD corresponds to the last received HDLC frame; it is duplicated into RFIFOD for every frame (last byte of frame)*

### 4.1.17 TMD -Test Mode Register D-Channel

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| TMD | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TLP | RD/WR (29) |

For general information please refer to **Chapter 3.10**.

**TLP ... Test Loop**

The TX path of layer-2 is internally connected with the RX path of layer-2. Data coming from the layer 1 controller will not be forwarded to the layer 2 controller.
The setting of TLP is only valid if the IOM interface is active.

## 4.1.18 CIR0 - Command/Indication Receive 0

Value after reset: $F3_H$

| | 7 | | | | 0 | |
|---|---|---|---|---|---|---|
| CIR0 | CODR0 | CIC0 | CIC1 | S/G | BAS | RD (2E) |

**CODR0 ... C/I Code 0 Receive**

Value of the received Command/Indication code. A C/I-code is loaded in CODR0 only after being the same in two consecutive IOM-frames and the previous code has been read from CIR0.

**CIC0 ... C/I Code 0 Change**

A change in the received Command/Indication code has been recognized. This bit is set only when a new code is detected in two consecutive IOM-frames. It is reset by a read of CIR0.

**CIC1 ... C/I Code 1 Change**

A change in the received Command/Indication code in IOM-channel 1 has been recognized. This bit is set when a new code is detected in one IOM-frame. It is reset by a read of CIR0.

**S/G ... Stop/Go Bit Monitoring**

Indicates the availability of the upstream D-channel on the S/T interface.
1: Stop
0: Go

**BAS ... Bus Access Status**

Indicates the state of the TIC-bus:
0: the IPAC-X itself occupies the D- and C/I-channel
1: another device occupies the D- and C/I-channel

*Note: The CODR0 bits are updated every time a new C/I-code is detected in two consecutive IOM-frames. If several consecutive valid new codes are detected and*

*CIR0 is not read, only the first and the last C/I code is made available in CIR0 at the first and second read of that register, respectively.*

### 4.1.19 CIX0 - Command/Indication Transmit 0

Value after reset: $FE_H$

| | 7 | | | | 0 | |
|---|---|---|---|---|---|---|
| CIX0 | CODX0 | TBA2 | TBA1 | TBA0 | BAC | WR (2E) |

**CODX0 ... C/I-Code 0 Transmit**

Code to be transmitted in the C/I-channel 0. The code is only transmitted if the TIC bus is occupied. If TIC bus is enabled but occupied by another device, only “1s” are transmitted.

**TBA2-0 ... TIC Bus Address**

Defines the individual address for the IPAC-X on the IOM bus.This address is used to access the C/I- and D-channel on the IOM interface.

*Note: If only one device is liable to transmit in the C/I- and D-channels of the IOM it should always be given the address value ’7’.*

**BAC ... Bus Access Control**

Only valid if the TIC-bus feature is enabled (MODED.DIM2-0).

If this bit is set, the IPAC-X will try to access the TIC-bus to occupy the C/I-channel even if no D-channel frame has to be transmitted. It should be reset when the access has been completed to grant a similar access to other devices transmitting in that IOM-channel.

*Note: Access is always granted by default to the IPAC-X with TIC-Bus Address (TBA2-0, STCR register) ’7’, which has the lowest priority in a bus configuration.*

### 4.1.20 CIR1 - Command/Indication Receive 1

Value after reset: $FE_H$

| | 7 | | | 0 | |
|---|---|---|---|---|---|
| CIR1 | CODR1 | CICW | CI1E | | RD (2F) |

**CODR1 ... C/I-Code 1 Receive**

**CICW, CI1E ... C/I-Channel Width, C/I-Channel 1 Interrupt Enable**

These two bits contain the read back values from CIX1 register (see below).

## 4.1.21 CIX1 - Command/Indication Transmit 1

Value after reset: $FE_H$

| | 7 | | | 0 | |
|---|---|---|---|---|---|
| CIX1 | CODX1 | | CICW | CI1E | WR (2F) |

**CODX1 ... C/I-Code 1 Transmit**

Bits 7-2 of C/I-channel 1.

**CICW... C/I-Channel Width**

CICW selects between a 4 bit (’0’) and 6 bit (’1’) C/I1 channel width.

The C/I1 handler always reads and writes 6-bit values but if 4-bit is selected, the higher two bits are ignored for interrupt generation. However in write direction the full CODX1 code is transmitted, i.e. the host must write the higher two bits to “1”.

**CI1E ... C/I-Channel 1 Interrupt Enable**

Interrupt generation ISTA.CIC of CIR0.CIC1 is enabled (1) or masked (0).

## 4.2 Transceiver Registers

### 4.2.1 TR_CONF0 - Transceiver Configuration Register 0

Value after reset: $01_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| TR_CONF0 | DIS_TR | BUS | EN_ICV | 0 | L1SW | 0 | EXLP | LDD | RD/WR (30) |

**DIS_TR ... Disable Transceiver**

Setting DIS_TR to “1” disables the transceiver. In order to reenable the transceiver again, a transceiver reset must be issued (SRES.RES_TR=1). The transceiver must not be reenabled by setting DIS_TR from “1” to “0”.

For general information please refer to **Chapter 3.3.10**.

**BUS ... Point-to-Point / Bus Selection (NT / Int. NT / LT-S mode only)**

0: Adaptive Timing (Point-t-Point, extended passive bus).
1: Fixed Timing (Short passive bus).

**EN_ICV ... Enable Illegal Code Violation**

0:normal operation

1:ICV enabled. The receipt of at least one illegal code violation within one multi-frame is indicated by the C/I indication ’1011’ (CVR) in two consecutive IOM frames.

**L1SW ... Enable Layer 1 State Machine in Software**

0:Layer 1 state machine of the IPAC-X is used

1:Layer 1 state machine is disabled. The functionality can be realized in software. The commands can be written to register TR_CMD and the status can be read from TR_STA.

For general information please refer to **Chapter 3.5**.

**EXLP ... External loop**

In case the analog loopback is activated with C/I = ARL or with the LP_A bit in the TR_CMD register the loop is a

0: internal loop next to the line pins

1: external loop which has to be closed between SR1/2 and SX1/SX2

*Note: The external loop is only useful if bit DIS_TX of register TR_CONF2 is set to '0'.*

For general information please refer to **Chapter 3.3.11**.

**LDD ... Level Detection Discard**

0: Automatic clock generation after detection of any signal on the line in power down state

1: No clock generation after detection of any signal on the line in power down state

*Note: If an interrupt by the level detect circuitry is generated, the microcontroller has to set this bit to '0' for an activation of the S/T interface.*

For general information please refer to **Chapter 3.3.9** and **Chapter 3.7.6**.

## 4.2.2 TR_CONF1 - Transceiver Configuration Register 1

Value after reset: $0x_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| TR_CONF1 | 0 | RPLL_ADJ | EN_SFSC | 0 | 0 | x | x | x | RD/WR (31) |

**RPLL_ADJ ... Receive PLL Adjustment**

0: DPLL tracking step is 0.5 XTAL period per S-frame

1: DPLL tracking step is 1 XTAL period per S-frame

**EN_SFSC ... Enable Short FSC**

0: No short FSC is generated

1: A short FSC is generated once per multi-frame (every 40th IOM frame)

**x ... Undefined**

The value of these bits depends on the selected mode. It is important to note that these bits must not be overwritten to a different value when accessing this register.

### 4.2.3 TR_CONF2 - Transmitter Configuration Register 2

Value after reset: $80_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| TR_CONF2 | DIS_TX | PDS | 0 | RLP | 0 | 0 | SGP | SGD | RD/WR (32) |

**DIS_TX ... Disable Line Driver**

0: Transmitter is enabled
1: Transmitter is disabled

For general information please refer to **Chapter 3.3.10**.

**PDS ... Phase Deviation Select**

Defines the phase deviation of the S-transmitter.
0: The phase deviation is 2 S-bits minus 7 oscillator periods plus analog delay plus delay of the external circuitry.
1: The phase deviation is 2 S-bits minus 9 oscillator periods plus analog delay plus delay of the external circuitry.

For general information please refer to **Chapter 3.3.8**.

**RLP ... Remote Line Loop**

0: Remote Line Loop open
1: Remote Line Loop closed

For general information please refer to **Chapter 3.3.11**.

**SGP ... Stop/Go Bit Polarity**

Defines the polarity of the S/G bit output on pin SGO.
0: low active (SGO=0 means “go”; SGO=1 means “stop”)
1: high active (SGO=1 means “go”; SGO=0 means “stop”)

**SGD ... Stop/Go Bit Duration**

Defines the duration of the S/G bit output on pin SGO.

0: active during the D-channel timeslot
1: active during the whole corresponding IOM frame (starts and ends with the beginning of the D-channel timeslot)

Outside the active window of SGO (defined in SGD) the level on pin SGO remains in the “stop”-state depending on the selected polarity (SGP), i.e. SGO=1 (if SGP=0) or SGO=0 (if SGP=1) outside the active window.

### 4.2.4 TR_STA - Transceiver Status Register

Value after reset: $00_H$

| | 7 | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|
| TR_STA | RINF | SLIP | ICV | 0 | FSYN | 0 | LD | RD (33) |

Important: This register is used only if the Layer 1 state machine of the IPAC-X is disabled (TR_CONF0.L1SW = 1) and implemented in software! With the IPAC layer 1 state machine enabled, the signals from this register are automatically evaluated.

For general information please refer to **Chapter 3.5**.

**RINF ... Receiver INFO**

00: Received INFO 0
01: Received any signal except INFO 0,2,3,4
10: Reserved (NT mode) or INFO 2 (TE mode)
11: Received INFO 3 (NT mode) or INFO 4 (TE mode)

**SLIP ... SLIP Detected**

A ’1’ in this bit position indicates that a SLIP is detected in the receive or transmit path.

**ICV ... Illegal Code Violation**

0:No illegal code violation is detected
1:Illegal code violation (ANSI T1.605) in data stream is detected

**FSYN ... Frame Synchronization State**

0: The S/T receiver is not synchronized
1: The S/T receiver has synchronized to the framing bit F

**LD ... Level Detection**

0:No receive signal has been detected on the line.
1:Any receive signal has been detected on the line.

### 4.2.5 TR_CMD - Transceiver Command Register

Value after reset: $08_H$

| | 7 | | | | | 0 | |
|---|---|---|---|---|---|---|---|
| TR_CMD | XINF | DPRIO | TDDIS | PD | LP_A | 0 | RD/WR (34) |

Important: This register is only writable if the Layer 1 state machine of the IPAC-X is disabled (TR_CONF0.L1SW = 1)! With the IPAC layer 1 state machine enabled, the signals from this register are automatically generated but nevertheless this register can always be read. DPRIO can also be written in Intelligent NT mode.

**XINF ... Transmit INFO**

000: Transmit INFO 0
001: reserved
010: Transmit INFO 1 (TE mode) or INFO 2 (NT mode)
011: Transmit INFO 3 (TE mode) or INFO 4 (NT mode)
100: Send continous pulses at 192 kbit/s alternating or 96 kHz rectangular, respectively (SCP)
101: Send single pulses at 4 kbit/s with alternating polarity corresponding to 2 kHz fundamental mode (SSP)
11x: reserved

**DPRIO ... D-Channel Priority (always writable in Int. NT mode)**

0: Priority Class 1for D channel access on IOM (Int. NT) or on S interface (TE/LT-T)
1: Priority Class 2 for D channel access on IOM (Int. NT) or on S interface (TE/LT-T)

**TDDIS ... Transmit Data Disabled (TE mode)**

0: The B and D channel data are transparently transmitted on the S/T interface if INFO 3 is being transmitted
1: The B and D channel data are set to logical ’1’ on the S/T interface if INFO 3 is being transmitted

**PD ... Power Down**

0: The transceiver is set to operational mode
1: The transceiver is set to power down mode

For general information please refer to **Chapter 3.5.1.2**.

**LP_A ... Loop Analog**

The setting of this bit corresponds to the C/I command ARL.

0: Analog loop is open

1: Analog loop is closed internally or externally according to the EXLP bit in the TR_CONF0 register

For general information please refer to **Chapter 3.3.11**.

## 4.2.6 SQRR1 - S/Q-Channel Receive Register 1

Value after reset: $40_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| SQRR | MSYN | MFEN | 0 | 0 | SQR1 | SQR2 | SQR3 | SQR4 | RD (35) |

For general information please refer to **Chapter 3.3.2**.

**MSYN ... Multi-frame Synchronization State**

0: The S/T receiver has not synchronized to the received $F_A$ and M bits

1: The S/T receiver has synchronized to the received $F_A$ and M bits

**MFEN ... Multiframe Enable**

Read-back of the MFEN bit of the SQXR register

**SQR11-14 ... Received S Bits**

Received S bits in frames 1, 6, 11 and 16 (TE mode)
received Q bits in frames 1, 6, 11 and 16 (NT mode).

### 4.2.7 SQXR1- S/Q-Channel TX Register 1

Value after reset: $4F_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| SQXR1 | 0 | MFEN | 0 | 0 | SQX1 | SQX2 | SQX3 | SQX4 | WR (35) |

**MFEN ... Multiframe Enable**

Used to enable or disable the multiframe structure (see **Chapter 3.3.2**)

0: S/T multiframe is disabled
1: S/T multiframe is enabled
Readback value in SQRR1.

**SQX1-4 ... Transmitted S/Q Bits**

Transmitted Q bits ($F_A$ bit position) in frames 1, 6, 11 and 16 (TE mode), transmitted S bits ($F_A$ bit position) in frames 1, 6, 11 and 16 (NT mode).

### 4.2.8 SQRR2 - S/Q-Channel Receive Register 2

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| SQRR2 | SQR21 | SQR22 | SQR23 | SQR24 | SQR31 | SQR32 | SQR33 | SQR34 | RD (36) |

**SQR21-24, SQR31-34... Received S Bits (TE mode only)**

Received S bits in frames 2, 7, 12 and 17 (SQR21-24, subchannel 2), and in frames 3, 8, 13 and 18 (SQR31-34, subchannel 3).

### 4.2.9 SQXR2 - S/Q-Channel TX Register 2

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| SQXR2 | SQX21 | SQX22 | SQX23 | SQX24 | SQX31 | SQX32 | SQX33 | SQX34 | WR (36) |

**SQX21-24, SQX31-34... Transmitted S Bits (NT mode only)**

Transmitted S bits in frames 2, 7, 12 and 17 (SQX21-24, subchannel 2), and in frames 3, 8, 13 and 18 (SQX31-34, subchannel 3).

### 4.2.10 SQRR3 - S/Q-Channel Receive Register 3

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| SQRR3 | SQR41 | SQR42 | SQR43 | SQR44 | SQR51 | SQR52 | SQR53 | SQR54 | RD (37) |

**SQR41-44, SQR51-54... Received S Bits (TE mode only)**

Received S bits in frames 4, 9, 14 and 19 (SQR41-44, subchannel 4), and in frames 5, 10, 15 and 20 (SQR51-54, subchannel 5).

### 4.2.11 SQXR3 - S/Q-Channel TX Register 3

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| SQXR3 | SQX41 | SQX42 | SQX43 | SQX44 | SQX51 | SQX52 | SQX53 | SQX54 | WR (37) |

**SQX41-44, SQX51-54... Transmitted S Bits (NT mode only)**

Transmitted S bits in frames 4, 9, 14 and 19 (SQX41-44, subchannel 4), and in frames 5, 10, 15 and 20 (SQX51-54, subchannel 5).

### 4.2.12 ISTATR - Interrupt Status Register Transceiver

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| ISTATR | x | x | x | x | LD | RIC | SQC | SQW | RD (38) |

For all interrupts in the ISTATR register the following logical states are defined:

0: Interrupt is not acitvated
1: Interrupt is acitvated

**x ... Reserved**

Bits set to “1” in this bit position must be ignored.

**LD ... Level Detection**

Any receive signal has been detected on the line. This bit is set to “1” (i.e. an interrupt is generated if not masked) as long as any receiver signal is detected on the line.

**RIC ... Receiver INFO Change**

RIC is activated if one of the TR_STA bits RINF or ICV has changed. This bit is reset by reading the TR_STA register.

**SQC ... S/Q-Channel Change**

A change in the received S-channel (TE) or Q-channel (NT) has been detected. The new code can be read from the SQRxx bits of registers SQRR1-3 within the next multiframe (5 ms). This bit is reset by a read access to the corresponding SQRRx register.

**SQW ... S/Q-Channel Writable**

The S/Q channel data for the next multiframe is writable.
The register for the Q (S) bits to be transmitted (received) has to be written (read) within the next multiframe (5 ms). This bit is reset by writing register SQXRx.

### 4.2.13 MASKTR - Mask Transceiver Interrupt

Value after reset: $FF_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| MASKTR | 1 | 1 | 1 | 1 | LD | RIC | SQC | SQW | RD/WR (39) |

The transceiver interrupts LD, RIC, SQC and SQW are enabled (0) or disabled (1).

### 4.2.14 TR_MODE - Transceiver Mode Register 1

Value after reset: $000000xx_B$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| TR_ MODE | 0 | 0 | 0 | 0 | DCH_ INH | MODE 2 | MODE 1 | MODE 0 | RD/WR (3A) |

For general information please refer also to **Chapter 3.7.5.4**.

**DCH_INH ... D-Channel Inhibit (NT, LT-S and Int. NT modes only)**

Setting this bit to ’1’ has the effect that the S-transceiver blocks the access to the D-channel on S by inverting the E-bits.

**MODE2-0 ... Transceiver Mode**

000: TE mode
001: LT-T mode
010: NT mode (without D-channel handler)
011: LT-S mode (without D-channel handler)
110: Intelligent NT mode (with NT state machine and with D-channel handler)
111: Intelligent NT mode (with LT-S state machine and with D-channel handler)
100: reserved
101: reserved

*Note: The three modes TE, LT-T and LT-S can be selected by pin strapping (reset values for bits TR_MODE.MODE0,1 loaded from pins MODE0,1), all other modes are programmable only.*

## 4.3 Auxiliary Interface Registers

### 4.3.1 ACFG1 - Auxiliary Configuration Register 1

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| ACFG1 | OD7 | OD6 | OD5 | OD4 | OD3 | OD2 | OD1 | OD0 | RD/WR (3C) |

For general information please refer to **Chapter 3.8.1**.

**OD7-0 ... Output Driver Select for AUX7 - AUX0**

0: output is open drain

1: output is push/pull

*Note: The ODx configuration is only valid if the corresponding output is enabled in the AOE register.*
*AUX0-2 are only available in TE and Int. NT mode and not in all other modes (used as channel select).*
*AUX7 and AUX6 provide internal pull up resistors which are only available as inputs and in output/open drain mode, but disabled in output / push/pull mode.*

### 4.3.2 ACFG2 - Auxiliary Configuration Register 2

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| ACFG2 | A7SEL | A5SEL | FBS | A4SEL | ACL | LED | EL1 | EL0 | RD/WR (3D) |

**A7SEL ... AUX7 Function Select**

0: pin AUX7 provides normal I/O functionality.

1: pin AUX7 provides the S/G bit output (SGO) from the IOM DD-line. Bit AOE.OE7 is don't care, the output characteristic (push pull or open drain) can be selected via ACFG1.OD7.

**A5SEL ... AUX5 Function Select**

0: pin AUX5 provides normal I/O functionality.

1: pin AUX5 provides an FSC or BCL signal output (FBOUT) which is selected in ACFG2.FBS. Bit AOE.OE5 is don't care, the output characteristic (push pull or open drain) can be selected via ACFG1.OD5.

For general information please refer to **Chapter 3.4**.

**FBS ... FSC/BCL Output Select**

0: FSC is output on pin AUX5.

1: BCL (single bit clock) is output on pin AUX5.

*Note: This selection has only effect on pin AUX5 if FBOUT is enabled (A5SEL=1). In LT-T mode pin SCLK provides an 1.536 MHz output clock which can be used as DCL input. This is necessary for BCL generation.*

For general information please refer to **Chapter 3.4**.

**A4SEL ... AUX4 Function Select**

0: pin AUX4 provides normal I/O functionality.

1: pin AUX4 supports multiframe synchronization and is used as M-bit input in Int. NT/ NT/LT-S modes or as M-bit output in TE/LT-T modes (input/output is automatically selected with the mode). Bit AOE.OE4 is don't care, the output characteristic (push pull or open drain) can be selected via ACFG1.OD4.

For general information please refer to **Chapter 3.3.3**.

**ACL ... $\overline{\text{ACL}}$ Function Select**

0: Pin $\overline{\text{ACL}}$ automatically indicates the S-bus activation status by a LOW level.

1: The output state of $\overline{\text{ACL}}$ is programmable by the host in bit LED.

*Note: An LED with preresistance may directly be connected to $\overline{\text{ACL}}$.*

**LED ... LED Control**

If enabled ($\overline{\text{ACL}}$=1) the LED with preresistance connected between VDD and $\overline{\text{ACL}}$ is switched ...

0: Off (high level on pin $\overline{\text{ACL}}$)

1: On (low level on pin $\overline{\text{ACL}}$)

**EL0, 1 ... Edge/Level Triggered Interrupt Input for $\overline{\text{INT0}}$, $\overline{\text{INT1}}$**

0: A negative level ...

1: A negative edge ... on $\overline{\text{INT0/1}}$ (pins AUX6/7) generates an interrupt to the IPAC-X.

*Note: An interrupt is only generated if the corresponding mask bit in AUXM is reset. This configuration is only valid if the corresponding output enable bit in AOE is disabled.*

For general information please refer to **Chapter 3.8.1**.

### 4.3.3 AOE - Auxiliary Output Enable Register

Value after reset: $FF_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| AOE | OE7 | OE6 | OE5 | OE4 | OE3 | OE2 | OE1 | OE0 | RD/WR (3E) |

For general information please refer to **Chapter 3.8.1**.

**OE7-0 ... Output Enable for AUX7 - AUX0**

0: Pin AUX7-0 is configured as output. The value of the corresponding bit in the ATX register is driven on AUX7-0.

1: Pin AUX7-0 is configured as input. The value of the corresponding bit can be read from the ARX register.

*Note: In NT and LT modes the pins AUX0-2 are not available as I/O pins. If pins AUX7, AUX6 are to be used as interrupt input, OE7, OE6 must be set to 1. If pins AUX7, AUX5 and AUX4 are not used as I/O pins (see ACFG2), the corresponding OEx bit cannot be set, but delivers the mode dependent direction (input/output) in that function upon a read access. If the secondary function is disabled, the direction of the pin as I/O pin is valid again.*

### 4.3.4 ARX - Auxiliary Interface Receive Register

Value after reset: (not defined)

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| ARX | AR7 | AR6 | AR5 | AR4 | AR3 | AR2 | AR1 | AR0 | RD (3F) |

**AR7-0 ... Auxiliary Receive**

The value of AR7-0 always reflects the level at pin AUX7-0 at the time when ARX is read by the host even if a pin is configured as output. If the mask bit for AUX7, 6 is set in the MASKA register, no interrupt is generated to the IPAC-X, however, the current state at pin AUX7,6 can be read from AR7,6

*Note: In NT and LT modes the pins AUX0-2 are not available as I/O pins.*

### 4.3.5 ATX - Auxiliary Interface Transmit Register

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| ATX | AT7 | AT6 | AT5 | AT4 | AT3 | AT2 | AT1 | AT0 | WR (3F) |

**AT7-0 ... Auxiliary Transmit**

A ’0’ or ’1’ in AT7-0 will drive a low or a high level at pin AUX7-0 if the corresponding output is enabled in the AOE register.

*Note: In NT and LT modes the pins AUX0-2 are not available as I/O pins.*

## 4.4 IOM-2 and MONITOR Handler

### 4.4.1 CDAxy - Controller Data Access Register xy

| | 7 | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|
| CDAxy | Controller Data Access Register | | | | | | | RD/WR (40-43) |

Data registers CDAxy which can be accessed from the controller.

| Register | Register Address | Value after Reset |
|---|---|---|
| CDA10 | $40_H$ | $FF_H$ |
| CDA11 | $41_H$ | $FF_H$ |
| CDA20 | $42_H$ | $FF_H$ |
| CDA21 | $43_H$ | $FF_H$ |

### 4.4.2 XXX_TSDPxy - Time Slot and Data Port Selection for CHxy

| | 7 | | | | 0 | |
|---|---|---|---|---|---|---|
| XXX_ TSDPxy | DPS | 0 | 0 | TSS | | RD/WR (44-4D) |

| Register | Register Address | Value after Reset |
|---|---|---|
| CDA_TSDP10 | $44_H$ | $00_H$ ( = output on B1-DD) |
| CDA_TSDP11 | $45_H$ | $01_H$ ( = output on B2-DD) |
| CDA_TSDP20 | $46_H$ | $80_H$ ( = output on B1-DU) |
| CDA_TSDP21 | $47_H$ | $81_H$ ( = output on B2-DU) |
| BCHA_TSDP_BC1 | $48_H$ | $80_H$ ( = output on B1-DU) |
| BCHA_TSDP_BC2 | $49_H$ | $81_H$ ( = output on B2-DU) |
| BCHB_TSDP_BC1 | $4A_H$ | $81_H$ ( = output on B2-DU) |
| BCHB_TSDP_BC2 | $4B_H$ | $85_H$ ( = output on IC2-DU) |
| TR_TSDP_BC1 | $4C_H$ | $00_H$ ( = transceiver output on B1-DD), see note |
| TR_TSDP_BC2 | $4D_H$ | $01_H$ ( = transceiver output on B2-DD), see note |

This register determines the time slots and the data ports on the IOM-2 interface for the data channels 'xy' of the functional units 'XXX' which are Controller Data Access (CDA), B-channel controllers (BCHA, BCHB) and Transceiver (TR).

Each of the two B-channel controllers (BCHA, BCHB) can access any combination of two 8-bit timeslots and one 2-bit timeslot (e.g. 16-bit access to B1+B2 or 18-bit IDSL in 2B+D). The position of the two 8-bit timeslots is programmed in BCHx_TSDP_BC1 and BCHx_TSDP_BC2. The position of the 2-bit timeslot is programmed in BCHA_CR and BCHB_CR. In the same registers each of the three timeslots is enabled/disabled.

The position of B-channel data from the S-interface is programmed in TR_TSDP_BC1 and TR_TSDP_BC2.

*Note: The reset values for TR_TSDP_BC1/2 are depending on the mode selection (MODE0/1) and channel selection (CH0-2).*

**DPS ... Data Port Selection**

0: The data channel xy of the functional unit XXX is output on DD.
The data channel xy of the functional unit XXX is input from DU.
1: The data channel xy of the functional unit XXX is output on DU.
The data channel xy of the functional unit XXX is input from DD.

*Note: For the CDA (controller data access) data the input is determined by the CDA_CRx.SWAP bit. If SWAP = '0' the input for the CDAxy data is vice versa to the output setting for CDAxy. If the SWAP = '1' the input from CDAx0 is vice versa to the output setting of CDAx1 and the input from CDAx1 is vice versa to the output setting of CDAx0. See controller data access description in* ***Chapter 3.7.1.1***

**TSS ... Timeslot Selection**

Selects one of 32 timeslots (0...31) on the IOM-2 interface for the data channels.

*Note: The TSS reset values for TR_TSDP_BC1/2 are determined by the channel select pins CH2-0 which are mapped to the corresponding bits TSS4-2.*

## 4.4.3 CDAx_CR - Control Register Controller Data Access CH1x

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| CDAx_CR | 0 | 0 | EN_TBM | EN_I1 | EN_I0 | EN_O1 | EN_O0 | SWAP | RD/WR (4E-4F) |

| Register | Register Address | Value after Reset |
|---|---|---|
| CDA1_CR | $4E_H$ | $00_H$ |
| CDA2_CR | $4F_H$ | $00_H$ |

For general information please refer to ***Chapter 3.7.1.1***.

**EN_TBM ... Enable TIC Bus Monitoring**

0: The TIC bus monitoring is disabled

1: The TIC bus monitoring with the CDAx0 register is enabled. The TSDPx0 register must be set to $08_H$ for monitoring from DU or $88_H$ for monitoring from DD, respectively. (This selection is only valid if IOM_CR.TIC_DIS = 0).

**EN_I1, EN_I0 ... Enable Input CDAx0, CDAx1**

0: The input of the CDAx0, CDAx1 register is disabled

1: The input of the CDAx0, CDAx1 register is enabled

**EN_O1, EN_O0 ... Enable Output CDAx0, CDAx1**

0: The output of the CDAx0, CDAx1 register is disabled

1: The output of the CDAx0, CDAx1 register is enabled

**SWAP ... Swap Inputs**

0: The time slot and data port for the input of the CDAxy register is defined by its own TSDPxy register. The data port for the CDAxy input is vice versa to the output setting for CDAxy.

1: The input (time slot and data port) of the CDAx0 is defined by the TSDP register of CDAx1 and the input of CDAx1 is defined by the TSDP register of CDAx0. The data port for the CDAx0 input is vice versa to the output setting for CDAx1. The data port for the CDAx1 input is vice versa to the output setting for CDAx0. The input definition for time slot and data port CDAx0 are thus swapped to CDAx1 and for CDAx1 to CDAx0. The outputs are not affected by the SWAP bit.

### 4.4.4 TR_CR - Control Register Transceiver Data (IOM_CR.CI_CS=0)

Value after reset: $F8_H$

| | 7 | | | | | 0 | |
|---|---|---|---|---|---|---|---|
| TR_CR | EN_D | EN_B2R | EN_B1R | EN_B2X | EN_B1X | CS2-0 | RD/WR (50) |

Read and write access to this register is only possible if IOM_CR.CI_CS = 0.

**EN_D ... Enable Transceiver D-Channel Data**
**EN_B2R ... Enable Transceiver B2 Receive Data**
**EN_B1R ... Enable Transceiver B1 Receive Data**
**EN_B2X ... Enable Transceiver B2 Transmit Data**
**EN_B1X ... Enable Transceiver B1 Transmit Data**

This register is used to individually enable/disable the D-channel (both RX and TX direction) and the receive/transmit paths for the B-channels of the S-transceiver.

0: The corresponding data path to the transceiver is disabled.
1: The corresponding data path to the transceiver is enabled.

*Note: Receive data corresponds to downstream direction, and transmit data corresponds to upstream direction.*

**CS2-0 ... Channel Select for Transceiver D-channel**

This register is used to select one of eight IOM channels to which the transceiver D-channel data is related to.

*Note: The reset value is determined by the channel select pins CH2-0 which are directly mapped to CS2-0. It should be noted that writing TR_CR.CS2-0 will also write to TRC_CR.CS2-0 and therefore modify the channel selection for the transceiver C/I0 data.*

### 4.4.5 TRC_CR - Control Register Transceiver C/I0 (IOM_CR.CI_CS=1)

Value after reset: $00_H$

| | 7 | | | | | 0 | |
|---|---|---|---|---|---|---|---|
| TRC_CR | 0 | 0 | 0 | 0 | 0 | CS2-0 | RD/WR (50) |

Write access to this register is possible if IOM_CR.CI_CS = 0 or IOM_CR.CI_CS = 1.
Read access to this register is possible only if IOM_CR.CI_CS = 1.

**CS2-0 ... Channel Select for the Transceiver C/I0 Channel**

This register is used to select one of eight IOM channels to which the transceiver C/I0 channel data is related to. The reset value is determined by the MODE2-bit and the channel select pins CH2-0 which are mapped to CS2-0.

### 4.4.6 BCHx_CR - Control Register B-Channel Controller Data

| | 7 | | | | | 0 | |
|---|---|---|---|---|---|---|---|
| BCHx_CR | DPS_D | 0 | EN_D | EN_ BC2 | EN_ BC1 | CS2-0 | RD/WR (51,52) |

| Register | Register Address | Value after Reset |
|---|---|---|
| BCHA_CR | $51_H$ | $08_H$ |
| BCHB_CR | $52_H$ | $81_H$ |

The registers BCHA_TSDP_BC1/2 and BCHB_TSDP_BC1/2 (see above) select the IOM-2 timeslots for B-channel controller access. For each of the B-channel controllers (BCHA, BCHB) two 8-bit timeslots can be selected (position and direction).

This register BCHx_CR is used to select the position (CS2-0) and direction (DPS_D) of the 2-bit timeslot for each of the two B-channel controllers, and each of the three selected timeslots (2 x 8-bit and 2-bit) is individually enabled/disabled (EN_BC1, EN_BC2, EN_D).

**DPS_D ... Data Port Selection for D-Channel Timeslot access**

0: The B-channel controller data is output on DD.
The B-channel controller data is input from DU.
1: The B-channel controller data is output on DU.
The B-channel controller data is input from DD.

**EN_D ... Enable D-Channel Timeslot (2-bit) for B-Channel controller access**
**EN_BC2 ... Enable B2-Channel Timeslot (8-bit) for B-Channel controller access**
**EN_BC1 ... Enable B1-Channel Timeslot (8-bit) for B-Channel controller access**

These bits individually enable/disable the B-channel access to the 2-bit and the two 8-bit timeslots.

0: B-channel B/A does not access timeslot data B1, B2 or D, respectively.

1: B-channel B/A does access timeslot data B1, B2 or D, respectively.

*Note: The terms B1/B2 should not imply that the 8-bit timeslots must be located in the first/second IOM-2 timeslots, it's simply a placeholder for the 8-bit timeslot position selected in the registers BCHA_TSDP_BC1/2 and BCHB_TSDP_BC1/2.*

**CS2-0 ... Channel Select for D-Channel Timeslot access**

This register is used to select one of eight IOM channels. If enabled (EN_D=1), the B-channel controller is connected to the 2-bit D-channel timeslot of that IOM channel.

*Note: The reset value is determined by the channel select pins CH2-0 which are directly mapped to CS2-0.*

## 4.4.7 DCI_CR - Control Register for D and CI1 Handler (IOM_CR.CI_CS=0)

Value after reset: $A0_H$

| | 7 | | | | | 0 | |
|---|---|---|---|---|---|---|---|
| DCI_CR | DPS_ CI1 | EN_ CI1 | D_ EN_D | D_ EN_B2 | D_ EN_B1 | CS2-0 | RD/WR (53) |

Read and write access to this register is only possible if IOM_CR.CI_CS = 0.

**DPS_CI1 ... Data Port Selection CI1 Handler Data**

0: The CI1 handler data is output on DD and input from DU
1: The CI1 handler data is output on DU and input from DD

**EN_CI1 ... Enable CI1 Handler Data**

0: CI1 handler data access is disabled
1: CI1 handler data access is enabled

*Note: The timeslot for the C/I1 handler cannot be programmed but is fixed to IOM channel 1.*

**D_EN_D ... Enable D-timeslot for D-channel controller**
**D_EN_B2 ... Enable B2-timeslot for D-channel controller**
**D_EN_B1 ... Enable B1-timeslot for D-channel controller**

These bits are used to select the timeslot length for the D-channel HDLC controller access as it is capable to access not only the D-channel timeslot. The host can individually enable two 8-bit timeslots B1- and B2-channel (D_EN_B1, D_EN_B2) and one 2-bit timeslot D-channel (D_EN_D) on IOM-2. The position is selected via CS2-0.

0: D-channel controller does not access timeslot data B1, B2 or D, respectively

1: D-channel controller does access timeslot data B1, B2 or D, respectively

**CS2-0 ... Channel Select for D-channel controller**

This register is used to select one of eight IOM channels. If enabled, the D-channel data is connected to the corresponding timeslots of that IOM channel.

*Note: The reset value is determined by the channel select pins CH2-0 which are directly mapped to CS2-0. It should be noted that writing DCI_CR.CS2-0 will also write to DCIC_CR.CS2-0 and therefore modify the channel selection for the data of the C/I0 handler.*

## 4.4.8 DCIC_CR - Control Register for CI0 Handler (IOM_CR.CI_CS=1)

Value after reset: $00_H$

| | 7 | | | | | 0 | |
|---|---|---|---|---|---|---|---|
| DCIC_CR | 0 | 0 | 0 | 0 | 0 | CS2-0 | RD/WR (13) |

Write access to this register is possible if IOM_CR.CI_CS = 0 or IOM_CR.CI_CS = 1.
Read access to this register is possible only if IOM_CR.CI_CS = 1.

**CS2-0 ... Channel Select for C/I0 Handler**

This register is used to select one of eight IOM channels. If enabled, the data of the C/I0 handler is connected to the corresponding C/I0 timeslots of that IOM channel.

The reset value is determined by the channel select pins CH2-0 which are mapped to CS2-0.

### 4.4.9 MON_CR - Control Register Monitor Data

Value after reset: $40_H$

| | 7 | | | | | 0 | |
|---|---|---|---|---|---|---|---|
| MON_CR | DPS | EN_ MON | 0 | 0 | 0 | CS2-0 | RD/WR (54) |

For general information please refer to **Chapter 3.7.3**.

**DPS ... Data Port Selection**

0: The Monitor data is output on DD and input from DU

1: The Monitor data is output on DU and input from DD

**EN_MON ... Enable Output**

0: The Monitor data input and output is disabled

1: The Monitor data input and output is enabled

**CS2-0 ... MONITOR Channel Selection**

000: The MONITOR data is input/output on MON0 (3rd timeslot on IOM-2)

001: The MONITOR data is input/output on MON1 (7th timeslot on IOM-2)

010: The MONITOR data is input/output on MON2 (11th timeslot on IOM-2)

:

111: The MONITOR data is input/output on MON7 (31st timeslot on IOM-2)

*Note: The reset value is determined by the channel select pins CH2-0 which are directly mapped to CS2-0.*

### 4.4.10 SDSx_CR - Control Register Serial Data Strobe x

Value after reset: $00_H$

| | 7 | | | | 0 | |
|---|---|---|---|---|---|---|
| SDSx_CR | ENS_ TSS | ENS_ TSS+1 | ENS_ TSS+3 | TSS | | RD/WR (55-56) |

| Register | Register Address | Value after Reset |
|---|---|---|
| SDS1_CR | $55_H$ | $00_H$ |
| SDS2_CR | $56_H$ | $00_H$ |

This register is used to select position and length of the strobe signals. The length can be any combination of two 8-bit timeslot (ENS_TSS, ENS_TSS+1) and one 2-bit timeslot (ENS_TSS+3).

For general information please refer to **Chapter 3.7.2** and **Chapter 3.7.2.2**.

**ENS_TSS ... Enable Serial Data Strobe of timeslot TSS**
**ENS_TSS+1 ... Enable Serial Data Strobe of timeslot TSS+1**

0: The serial data strobe signal SDSx is inactive during TSS, TSS+1

1: The serial data strobe signal SDSx is active during TSS, TSS+1

**ENS_TSS+3 ... Enable Serial Data Strobe of timeslot TSS+3 (D-Channel)**

0: The serial data strobe signal SDSx is inactive during the D-channel (bit7, 6) of TSS+3

1: The serial data strobe signal SDSx is active during the D-channel (bit7, 6) of TSS+3

**TSS ... Timeslot Selection**

Selects one of 32 timeslots on the IOM-2 interface (with respect to FSC) during which SDSx is active high or provides a strobed BCL clock output (see SDS_CONF.SDS1/2_BCL). The data strobe signal allows standard data devices to access a programmable channel.

### 4.4.11 IOM_CR - Control Register IOM Data

Value after reset: $08_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| IOM_CR | SPU | DIS_ AW | CI_CS | TIC_ DIS | EN_ BCL | CLKM | DIS_ OD | DIS_ IOM | RD/WR (57) |

**SPU ... Software Power Up**

0: The DU line is normally used for transmitting data

1: Setting this bit to ’1’ will pull the DU line to low. This will enforce connected layer 1 devices to deliver IOM-clocking.

After a subsequent ISTA.CIC-interrupt (C/I-code change) and reception of the C/I-code ”PU” (Power Up indication in TE-mode) the microcontroller writes an AR or TIM command as C/I-code in the CIX0-register, resets the SPU bit and waits for the following CIC-interrupt.

For general information please refer to **Chapter 3.7.6**.

**DIS_AW ... Disable Asynchronous Awake (NT, LT-S, Int. NT mode only)**

Setting this bit to “1” disables the Asynchronous Awake function of the transceiver.

**CI_CS ... C/I Channel Selection**

The channel selection for D-channel and C/I-channel is done in the channel select bits CH2-0 of register TR_CR (for the transceiver) and DCI_CR (for the D-channel controller and C/I-channel controller).

0: A write access to CS2-0 has effect on the configuration of D- and C/I-channel, whereas a read access delivers the D-channel configuration only.

1: A write access to CS2-0 has effect on the configuration of the C/I-channel only, whereas a read access delivers the C/I-channel configuration only.

**TIC_DIS ... TIC Bus Disable**

0: The last octet of IOM channel 2 (12th timeslot) is used as TIC bus (in a frame timing with 12 timeslots only).

1: The TIC bus is disabled. The last octet of the last IOM time slot (TS 11) can be used as every time slot.

**EN_BCL ... Enable Bit Clock BCL/SCLK**

0: The BCL/SCLK clock is disabled
1: The BCL/SCLK clock is enabled.

**CLKM ... Clock Mode**

If the transceiver is disabled (DIS_TR = ’1’) or in NT, LT-S and Int. NT mode the DCL from the IOM-2 interface is an input.

0: A double bit clock is connected to DCL

1: A single bit clock is connected to DCL

For general information please refer to **Chapter 3.7**.

**DIS_OD ... Disable Open Drain Drivers**

0: DU/DD are open drain drivers

1: DU/DD are push pull drivers

**DIS_IOM ... Disable IOM**

DIS_IOM should be set to ’1’ if external devices connected to the IOM interface should be “disconnected“ e.g. for power saving purposes or for not disturbing the internal IOM connection between layer 1 and layer 2. However, the IPAC-X internal operation between S-transceiver, B-channel and D-channel controller is independent of the DIS_IOM bit.

0: The IOM interface is enabled

1: The IOM interface is disabled. The FSC, DCL clock outputs have high impedance; clock inputs are active; DU, DD data line inputs are switched off and outputs have high impedance; except in TE/LT-T mode the DU line is input (’0’-level causes activation), so the DU pin must be terminated (pull up resistor).

### 4.4.12 STI - Synchronous Transfer Interrupt

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| STI | STOV 21 | STOV 20 | STOV 11 | STOV 10 | STI 21 | STI 20 | STI 11 | STI 10 | RD (58) |

For all interrupts in the STI register the following logical states are applied:

0: Interrupt is not activated

1: Interrupt is activated

The interrupts are automatically reset by reading the STI register. For general information please refer to **Chapter 3.7.1.1**.

**STOVxy ... Synchronous Transfer Overflow Interrupt**

Enabled STOV interrupts for a certain STIxy interrupt are generated when the STIxy has not been acknowledged in time via the ACKxy bit in the ASTI register. This must be one (for DPS='0') or zero (for DPS='1') BCL clocks before the time slot which is selected for the STOV.

**STIxy ... Synchronous Transfer Interrupt**

Depending on the DPS bit in the corresponding TSDPxy register the Synchronous Transfer Interrupt STIxy is generated two (for DPS='0') or one (for DPS='1') BCL clock after the selected time slot (TSDPxy.TSS).

*Note: ST0Vxy and ACKxy are useful for synchronizing microcontroller accesses and receive/transmit operations. One BCL clock is equivalent to two DCL clock cycles.*

### 4.4.13 ASTI - Acknowledge Synchronous Transfer Interrupt

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| ASTI | 0 | 0 | 0 | 0 | ACK 21 | ACK 20 | ACK 11 | ACK 10 | WR (58) |

For general information please refer to **Chapter 3.7.1.1**.

**ACKxy ... Acknowledge Synchronous Transfer Interrupt**

After an STIxy interrupt the microcontroller has to acknowledge the interrupt by setting the corresponding ACKxy bit to “1”.

### 4.4.14 MSTI - Mask Synchronous Transfer Interrupt

Value after reset: $FF_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| MSTI | STOV 21 | STOV 20 | STOV 11 | STOV 10 | STI 21 | STI 20 | STI 11 | STI 10 | RD/WR (59) |

For the MSTI register the following logical states are applied:

0: Interrupt is not masked
1: Interrupt is masked

For general information please refer to **Chapter 3.7.1.1**.

**STOVxy ... Synchronous Transfer Overflow for STIxy**

Mask bits for the corresponding STOVxy interrupt bits.

**STIxy ... Synchronous Transfer Interrupt xy**

Mask bits for the corresponding STIxy interrupt bits.

### 4.4.15 SDS_CONF - Configuration Register for Serial Data Strobes

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| SDS_CONF | 0 | 0 | 0 | 0 | DIOM_INV | DIOM_SDS | SDS2_BCL | SDS1_BCL | RD/WR (5A) |

For general information on SDS1/2_BCL please refer to **Chapter 3.7.2**.

**DIOM_INV ... DU/DD on IOM Timeslot Inverted**

0: DU/DD are active during SDS1 HIGH phase and inactive during the LOW phase.
1: DU/DD are active during SDS1 LOW phase and inactive during the HIGH phase.
This bit has only effect if DIOM_SDS is set to ’1’ otherwise DIOM_INV is don’t care.

**DIOM_SDS ... DU/DD on IOM Controlled via SDS1**

0: The pin SDS1 and its configuration settings are used for serial data strobe only. The IOM-2 data lines are not affected.
1: The DU/DD lines are deactivated during the during High/Low phase (selected via DIOM_INV) of the SDS1 signal. The SDS1 timeslot is selected in SDS1_CR.

**SDSx_BCL ... Enable IOM Bit Clock for SDSx**

0: The serial data strobe is generated in the programmed timeslot.
1: The IOM bit clock is generated in the programmed timeslot.

### 4.4.16 MCDA - Monitoring CDA Bits

Value after reset: $FF_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| MCDA | MCDA21 | | MCDA20 | | MCDA11 | | MCDA10 | | RD (5B) |
| | Bit7 | Bit6 | Bit7 | Bit6 | Bit7 | Bit6 | Bit7 | Bit6 | |

**MCDAxy ... Monitoring CDAxy Bits**

Bit 7 and Bit 6 of the CDAxy registers are mapped into the MCDA register.

This can be used for monitoring the D-channel bits on DU and DD and the ’Echo bits’ on the TIC bus with the same register

### 4.4.17 MOR - MONITOR Receive Channel

Value after reset: $FF_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| MOR | Monitor Receiver Data | | | | | | | | RD (5C) |

Contains the MONITOR data received in the IOM-2 MONITOR channel according to the MONITOR channel protocol. The MONITOR channel (0-7) can be selected by setting the monitor channel select bit MON_CR.MCS.

### 4.4.18 MOX - MONITOR Transmit Channel

Value after reset: $FF_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| MOX | Monitor Transmit Data | | | | | | | | WR (5C) |

Contains the MONITOR data to be transmitted in IOM-2 MONITOR channel according to the MONITOR channel protocol.The MONITOR channel (0-7) can be selected by setting the monitor channel select bit MON_CR.MCS

### 4.4.19 MOSR - MONITOR Interrupt Status Register

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| MOSR | MDR | MER | MDA | MAB | 0 | 0 | 0 | 0 | RD (5D) |

**MDR ... MONITOR channel Data Received**

**MER ... MONITOR channel End of Reception**

**MDA ... MONITOR channel Data Acknowledged**

The remote end has acknowledged the MONITOR byte being transmitted.

**MAB ... MONITOR channel Data Abort**

### 4.4.20 MOCR - MONITOR Control Register

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| MOCR | MRE | MRC | MIE | MXC | 0 | 0 | 0 | 0 | RD/WR (5E) |

**MRE ... MONITOR Receive Interrupt Enable**

0: MONITOR interrupt status MDR generation is masked

1: MONITOR interrupt status MDR generation is enabled

**MRC ... MR Bit Control**

Determines the value of the MR bit:

0:MR is always ’1’. In addition, the MDR interrupt is blocked, except for the first byte of a packet (if MRE = 1).

1:MR is internally controlled by the IPAC-X according to MONITOR channel protocol. In addition, the MDR interrupt is enabled for all received bytes according to the MONITOR channel protocol (if MRE = 1).

**MIE ... MONITOR Interrupt Enable**

MONITOR interrupt status MER, MDA, MAB generation is enabled (1) or masked (0).

**MXC ... MX Bit Control**

Determines the value of the MX bit:
0:The MX bit is always ’1’.

1:The MX bit is internally controlled by the IPAC-X according to MONITOR channel protocol.

### 4.4.21 MSTA - MONITOR Status Register

Value after reset: $00_H$

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| MSTA | 0 | 0 | 0 | 0 | 0 | MAC | 0 | TOUT | RD (5F) |

**MAC ... MONITOR Transmit Channel Active**

The data transmisson in the MONITOR channel is in progress.

**TOUT ... Time-Out**

Read-back value of the TOUT bit.

### 4.4.22 MCONF - MONITOR Configuration Register

Value after reset: $00_H$

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| MCONF | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TOUT | WR (5F) |

**TOUT... Time-Out**

0: The monitor time-out function is disabled

1: The monitor time-out function is enabled

## 4.5 Interrupt and General Configuration

### 4.5.1 ISTA - Interrupt Status Register

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| ISTA | ICA | ICB | ST | CIC | AUX | TRAN | MOS | ICD | RD (60) |

For all interrupts in the ISTA register following logical states are applied:

0: Interrupt is not acitvated
1: Interrupt is acitvated

**ICA, ICB, ICD ... HDLC Interrupt from B-channel A, B or D-channel**

An interrupt originated from the HDLC controllers of B-channel A, B or of the D-channel has been recognized.

**ST ... Synchronous Transfer**

This interrupt is generated to enable the microcontroller to lock on to the IOM timing for synchronous transfers. The source can be read from the STI register.

**CIC ... C/I Channel Change**

A change in C/I channel 0 or C/I channel 1 has been recognized. The actual value can be read from CIR0 or CIR1.

**AUX ... Auxiliary Interrupts**

Signals an interrupt generated from external awake (pin $\overline{\text{EAW}}$), watchdog timer overflow, timer1, timer2 or from one of the interrupt input pins ($\overline{\text{INT0}}$, $\overline{\text{INT1}}$). The source can be read from the auxiliary interrupt register AUXI.

**TRAN ... Transceiver Interrupt**

An interrupt originated in the transceiver interrupt status register (ISTATR) has been recognized.

**MOS ... MONITOR Status**

A change in the MONITOR Status Register (MOSR) has occured.

*Note: A read of the ISTA register clears none of the interrupts. They are only cleared by reading the corresponding status register.*

### 4.5.2 MASK - Mask Register

Value after reset: $FF_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| MASK | ICA | ICB | ST | CIC | AUX | TRAN | MOS | ICD | WR (60) |

For the MASK register following logical states are applied:

0: Interrupt is enabled
1: Interrupt is disabled

Each interrupt source in the ISTA register can selectively be masked/disabled by setting the corresponding bit in MASK to ’1’. Masked interrupt status bits are not indicated when ISTA is read. Instead, they remain internally stored and pending, until the mask bit is reset to ’0’.

*Note: In the event of a C/I channel change, CIC is set in ISTA even if the corresponding mask bit in MASK is set, but no interrupt is generated.*

### 4.5.3 AUXI - Auxiliary Interrupt Status Register

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| AUXI | 0 | 0 | EAW | WOV | TIN2 | TIN1 | INT1 | INT0 | RD (61) |

For all interrupts in the ISTA register following logical states are applied:

0: Interrupt is not acitvated
1: Interrupt is acitvated

**EAW ... External Awake Interrupt**

An interrupt from the $\overline{\text{EAW}}$ pin has been detected.

**WOV ... Watchdog Timer Overflow**

Signals the expiration of the watchdog timer, which means that the microcontroller has failed to set the watchdog timer control bits WTC1 and WTC2 (MODE1 register) in the correct manner. A reset pulse has been generated by the IPAC-X.

**TIN2, 1 ... Timer Interrupt 1, 2**

An interrupt originated from timer 1 or timer 2 is recognized, i.e the timer has expired.

**INT1, 0 ... Auxiliary Interrupt from external devices 1, 0**

A low level or a negative state transition (programmable in ACFG2.EL1/0) is detected at pin AUX7 or AUX6, respectively.

### 4.5.4 AUXM - Auxiliary Mask Register

Value after reset: $FF_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| AUXM | 1 | 1 | EAW | WOV | TIN2 | TIN1 | INT1 | INT0 | WR (61) |

For the MASK register following logical states are applied:

0: Interrupt is enabled
1: Interrupt is disabled

Each interrupt source in the AUXI register can selectively be masked/disabled by setting the corresponding bit in AUXM to ’1’. Masked interrupt status bits are not indicated when AUXI is read. Instead, they remain internally stored and pending, until the mask bit is reset to ’0’.

### 4.5.5 MODE1 - Mode1 Register

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| MODE1 | 0 | 0 | 0 | WTC1 | WTC2 | CFS | RSS2 | RSS1 | RD/WR (62) |

**WTC1, 2 ... Watchdog Timer Control 1, 2**

After the watchdog timer mode has been selected (RSS = ’11’) the watchdog timer is started. During every time period of 128 ms the microcontroller has to program the WTC1 and WTC2 bit in the following sequence

| | WTC1 | WTC2 |
|---|---|---|
| 1. | 1 | 0 |
| 2. | 0 | 1 |

to reset and restart the watchdog timer.
If WTC1/2 is not written fast enough in this way, the timer expires and a WOV-interrupt (AUXI register) together with a reset pulse is generated.

**CFS ... Configuration Select**

This bit determines clock relations and recovery on S/T and IOM interfaces.

0: The IOM interface clock and frame signals are always active, "Power Down" state included.
The states "Power Down" and "Power Up" are thus functionally identical except for the indication: PD = 1111 and PU = 0111.
With the C/I command Timing (TIM) the microcontroller can enforce the "Power Up" state and with C/I command Deactivation Indication (DI) the "Power Down" state is reached again.
However, it is also possible to activate the S-interface directly with the C/I command Activate Request (AR 8/10/L) without the TIM command.

1: The IOM interface clock and frame signals are normally inactive ("Power Down").
For activating the IOM-2 clocks the "Power Up" state can be induced by software (IOM_CR.SPU) or by resetting CFS again.
After that the S-interface can be activated with the C/I command Activate Request (AR 8/10/L). The "Power Down" state can be reached again with the C/I command Deactivation Indication (DI).

*Note: After reset the IOM interface is always active. To reach the "Power Down" state the CFS-bit has to be set.*

For general information please refer to **Chapter 3.3.9**.

### RSS2, RSS1... Reset Source Selection 2,1

The IPAC-X reset sources for the $\overline{\text{RSTO}}$ output pin can be selected according to the table below.

| RSS | | C/I Code Change | EAW | Watchdog Timer |
|---|---|---|---|---|
| Bit 1 | Bit 0 | | | |
| 0 | 0 | -- | -- | -- |
| 0 | 1 | (reserved) | | |
| 1 | 0 | x | x | -- |
| 1 | 1 | -- | -- | x |

- If RSS = ’00’ no above listed reset source is selected and therefore no reset is generated at $\overline{\text{RSTO}}$.
- **Watchdog Timer**
  After the selection of the watchdog timer (RSS = ’11’) the timer is reset and started. During every time period of 128 ms the microcontroller has to program the WTC1 and WTC2 bits in two consecutive bit pattern (see description of the WTC1, 2 bits) otherwise the watchdog timer expires and a reset pulse of 125 µs ≤ t≤ 250 µs is generated. Deactivation of the watchdog timer is only possible with a hardware reset.
- If RSS = ’10’ is selected the following two reset sources generate a reset pulse of 125 µs ≤ t ≤ 250 µs at the $\overline{\text{RSTO}}$ pin:
  **- External (Subscriber) Awake ($\overline{\text{EAW}}$)**
  The **$\overline{\text{EAW}}$** input pin serves as a request signal from the subscriber to initiate the awake function in a terminal and generates a reset pulse (in TE mode only).
  **- Exchange Awake (C/I Code)**
  A C/I Code change generates a reset pulse.

After a reset pulse generated by the IPAC-X and the corresponding interrupt (WOV or CIC) the actual reset source can be read from the ISTA.

## 4.5.6 MODE2 - Mode2 Register

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| MODE2 | 0 | 0 | 0 | 0 | INT_ POL | 0 | 0 | PPSDX | RD/WR (63) |

**INT_POL ... Interrupt Polarity**

Selects the polarity of the interrupt pin $\overline{\text{INT}}$.
0: low active with open drain characteristic (default)
1: high active with push pull characteristic

**PPSDX ... Push/Pull Output for SDX (SCI Interface)**

0: The SDX pin has open drain characteristic
1: The SDX pin has push/pull characteristic

## 4.5.7 ID - Identification Register

Value after reset: $01_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| ID | 0 | 0 | DESIGN | | | | | | RD (64) |

**DESIGN ... Design Number**

The design number allows to identify different hardware designs of the IPAC-X by software.

$01_H$: V 1.4

(all other codes reserved)

## 4.5.8 SRES - Software Reset Register

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| SRES | RES_ CI | RES_ BCHA | RES_ BCHB | RES_ MON | RES_ DCH | RES_ IOM | RES_ TR | RES_ RSTO | WR (64) |

**RES_xx ... Reset Functional Block xx**

A reset can be activated on the functional block C/I-handler, B-channel A and B, Monitor channel, D-channel, IOM handler, S-transceiver and to pin $\overline{\text{RSTO}}$.

Setting one of these bits to “1” causes the corresponding block to be reset for a duration of 4 BCL clock cycles, except RES_RSTO which is activated for a duration of 125 ... 250µs. The bits are automatically reset to “0” again.

### 4.5.9 TIMR2 - Timer 2 Register

Value after reset: $00_H$

| | 7 | | | 0 | |
|---|---|---|---|---|---|
| TIMR2 | TMD | 0 | CNT | | RD/WR (65) |

**TMD ... Timer Mode**

Timer 2 can be used in two different modes of operation.

0: Count Down Timer.
An interrupt is generated only once after a time period of 1 ... 63 ms.

1: Periodic Timer.
An interrupt is periodically generated every 1 ... 63 ms (see CNT).

**CNT ... Timer Counter**

0: Timer off.

1 ... 63:Timer period = 1 ... 63 ms

By writing ’0’ to CNT the timer is immediately stopped. A value different from that determines the time period after which an interrupt will be generated.
If the timer is already started with a certain CNT value and is written again before an interrupt has been released, the timer will be reset to the new value and restarted again. An interrupt is indicated to the host in AUXI.TIN2.

*Note: Reading back this value delivers back the current counter value which may differ from the programmed value if the counter is running.*

## 4.6 B-Channel Registers

The registers for B-channel A are contained in the address space $70_H$ - $7A_H$ and for B-channel B in the address space $80_H$ - $8A_H$.

### 4.6.1 ISTAB - Interrupt Status Register B-Channels

Value after reset: $10_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| ISTAB | RME | RPF | RFO | XPR | 0 | XDU | 0 | 0 | RD (70/80) |

For general information please refer to **Chapter 3.9.6**.

**RME ... Receive Message End**

One complete frame of length less than or equal to the defined block size (EXMB.RFBS) or the last part of a frame of length greater than the defined block size has been received. The contents are available in the RFIFOB. The message length and additional information may be obtained from RBCHB and RBCLB and the RSTAB register.

**RPF ... Receive Pool Full**

A data block of a frame longer than the defined block size (EXMB.RFBS) has been received and is available in the RFIFOB. The frame is not yet complete.

**RFO ... Receive Frame Overflow**

The received data of a frame could not be stored, because the RFIFOB is occupied. The whole message is lost.

This interrupt can be used for statistical purposes and indicates that the microcontroller does not respond quickly enough to an RPF or RME interrupt (ISTAB).

**XPR ... Transmit Pool Ready**

A data block of up to the defined block size 32 or 64 (EXMB.XFBS) can be written to the XFIFOB.

An XPR interrupt will be generated in the following cases:

- after an XTF or XME command as soon as the 32 or 64 bytes in the XFIFOB are available and the frame is not yet complete
- after an XTF together with an XME command is issued, when the whole frame has been transmitted
- after a reset of the transmitter (XRES)

- after a device reset

**XDU ... Transmit Data Underrun**

The current transmission of a frame is aborted by transmitting seven ’1’s because the XFIFOB holds no further data. This interrupt occurs whenever the microcontroller has failed to respond to an XPR interrupt (ISTAB register) quickly enough, after having initiated a transmission and the message to be transmitted is not yet complete.

### 4.6.2 MASKB - Mask Register B-Channels

Value after reset: $FF_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| MASKB | RME | RPF | RFO | XPR | 1 | XDU | 1 | 1 | WR (70/80) |

Each interrupt source in the ISTAB register can selectively be masked by setting the corresponding bit in MASKB to ’1’. Masked interrupt status bits are not indicated when ISTAB is read. Instead, they remain internally stored and pending until the mask bit is reset to ’0’.

For general information please refer to **Chapter 3.9.6**.

### 4.6.3 STARB - Status Register B-Channels

Value after reset: $40_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| STARB | XDOV | XFW | 0 | 0 | RACI | 0 | XACI | 0 | RD (71/81) |

**XDOV ... Transmit Data Overflow**

More than 16 or 32 bytes (according to selected block size) have been written to the XFIFOB, i.e. data has been overwritten.

**XFW ... Transmit FIFO Write Enable**

Data can be written to the XFIFOB. This bit may be polled instead of (or in addition to) using the XPR interrupt.

### RACI ... Receiver Active Indication

The B-channel HDLC receiver is active when RACI = ’1’. This bit may be polled. The RACI bit is set active after a begin flag has been received and is reset after receiving an abort sequence.

### XACI ... Transmitter Active Indication

The B-channel HDLC-transmitter is active when XACI = ’1’. This bit may be polled. The XACI-bit is active when an XTF-command is issued and the frame has not been completely transmitted

## 4.6.4 CMDRB - Command Register B-channels

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| CMDRB | RMC | RRES | 0 | 0 | XTF | 0 | XME | XRES | WR (71/81) |

### RMC ... Receive Message Complete

Reaction to RPF (Receive Pool Full) or RME (Receive Message End) interrupt. By setting this bit, the microcontroller confirms that it has fetched the data, and indicates that the corresponding space in the RFIFOB may be released.

### RRES ... Receiver Reset

HDLC receiver is reset, the RFIFOB is cleared of any data.

### XTF ... Transmit Transparent Frame

After having written up to 32 or 64 bytes (EXMB.XFBS) to the XFIFOB, the microcontroller initiates the transmission of a transparent frame by setting this bit to ’1’. The opening flag is automatically added to the message by the IPAC-X.

### XME ... Transmit Message End

By setting this bit to ’1’ the microcontroller indicates that the data block written last to the XFIFOB completes the corresponding frame. The IPAC-X terminates the transmission by appending the CRC and the closing flag sequence to the data.

### XRES ... Transmitter Reset

The B-channel HDLC transmitter is reset and the XFIFOB is cleared of any data. This command can be used by the microcontroller to abort a frame currently in transmission.

*Note: After an XPR interrupt further data has to be written to the XFIFOB and the appropriate Transmit Command (XTF) has to be written to the CMDRB register again to continue transmission, when the current frame is not yet complete (see also XPR in ISTAB).*
*During frame transmission, the 0-bit insertion according to the HDLC bit-stuffing mechanism is done automatically.*

### 4.6.5 MODEB - Mode Register

Value after reset: $C0_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| MODEB | MDS2 | MDS1 | MDS0 | 0 | RAC | 0 | 0 | 0 | RD/WR (72/82) |

**MDS2-0 ... Mode Select**

Determines the message transfer mode of the HDLC controller, as follows:

| MDS2-0 | Mode | Number of Address Bytes | Address Comparison | | Remark |
|---|---|---|---|---|---|
| | | | 1.Byte | 2.Byte | |
| 0 0 0 | Reserved | | | | |
| 0 0 1 | Reserved | | | | |
| 0 1 0 | Non-Auto mode | 1 | RAL1,RAL2 | – | One-byte address compare. |
| 0 1 1 | Non-Auto mode | 2 | RAH1,RAH2, Group Address | RAL1,RAL2, Group Address | Two-byte address compare. |
| 1 0 0 | Extended transparent mode | | | | |
| 1 1 0 | Transparent mode 0 | – | – | – | No address compare. All frames accepted. |

| MDS2-0 | Mode | Number of Address Bytes | Address Comparison | | Remark |
|---|---|---|---|---|---|
| | | | 1.Byte | 2.Byte | |
| 1 1 1 | Transparent mode 1 | > 1 | RAH1,RAH2, Group Address | – | High-byte address compare. |
| 1 0 1 | Transparent mode 2 | > 1 | – | RAL1,RAL2, Group Address | Low-byte address compare. |

*Note: - RAH1, RAH2: two programmable address values for the first received address byte (in the case of an address field longer than 1 byte);*
*Group Address= fixed value FC / $FE_H$.*
*- RAL1, RAL2: two programmable address values for the second (or the only, in the case of a one-byte address) received address byte;*
*Group Address= fixed value $FF_H$.*

**RAC ... Receiver Active**

The B-channel HDLC receiver is activated when this bit is set to ’1’. If set to ’0’ the HDLC data is not evaluated in the receiver.

## 4.6.6 EXMB - Extended Mode Register B-Channels

Value after reset: $00_H$

| | 7 | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|
| EXMB | XFBS | RFBS | SRA | XCRC | RCRC | 0 | ITF | RD/WR (73/83) |

**XFBS … Transmit FIFO Block Size**

0 … Block size for the transmit FIFO data is 64 byte
1 … Block size for the transmit FIFO data is 32 byte

*Note: A change of XFBS will take effect after a receiver command (CMDRB.XME, CMDRB.XRES, CMDRB.XTF) has been written.*

### RFBS … Receive FIFO Block Size

| RFBS | | Block Size Receive FIFO |
|---|---|---|
| Bit 6 | Bit5 | |
| 0 | 0 | 64 byte |
| 0 | 1 | 32 byte |
| 1 | 0 | 16 byte |
| 1 | 1 | 8 byte |

*Note: A change of RFBS will take effect after a transmitter command (CMDRB.RMC, CMDRB.RRES,) has been written*

### SRA … Store Receive Address

0 … Receive Address is not stored in the RFIFOB
1 … Receive Address is stored in the RFIFOB

### XCRC … Transmit CRC

0 … CRC is transmitted
1 … CRC is not transmitted

### RCRC… Receive CRC

0 … CRC is not stored in the RFIFOB
1 … CRC is stored in the RFIFOB

### ITF… Interframe Time Fill

Selects the inter-frame time fill signal which is transmitted between HDLC-frames.

0 … idle (continuous ’1’)
1 … flags (sequence of patterns: ‘0111 1110’)

### 4.6.7 RAH1 - RAH1 Register

Value after reset: $00_H$

| | 7 | | | 0 | |
|---|---|---|---|---|---|
| RAH1 | RAH1 | | 0 | MHA | WR (75/85) |

**RAH1 ... Value of the First individual Programmable High Address Byte**

In operating modes that provide high byte address recognition, the high byte of the received address is compared with the individual programmable values in RAH1, RAH2 or group address $FC_H$/$FE_H$.

**MHA ... Mask High Address**

0: The RAH1 address of an incoming frame is compared with RAH1, RAH2 and Group Address.
1: The RAH1 address of an incoming frame is compared with RAH1 and Group Address. RAH1 can be masked with RAH2 thereby bitpositions of RAH1 are not compared if they are set to ’1’ in RAH2.

### 4.6.8 RAH2 - RAH2 Register

Value after reset: $00_H$

| | 7 | | | 0 | |
|---|---|---|---|---|---|
| RAH2 | RAH2 | | 0 | MLA | WR (76/86) |

**RAH2 ... Value of the second individual programmable high address byte**

See RAH1 register above. RAH1 and RAH2 are used in non-auto mode when a 2-byte address field has been selected and in the transparent mode 1.

**MLA ... Mask Low Address**

0:The address of an incoming frame is compared with RAL1, RAL2 and Group Address.
1:The address of an incoming frame is compared with RAL1 and Group Address. RAL1 can be masked with RAL2 thereby bitpositions of RAL1 are not compared if they are set to ’1’ in RAL2.

### 4.6.9 RBCLB - Receive Frame Byte Count Low B-Channels

Value after reset: $00_H$

| | 7 | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|
| RBCLB | RBC7 | | | | | | RBC0 | RD (76/86) |

**RBC7-0 ... Receive Byte Count**

Eight least significant bits of the total number of bytes in a received message (see RBCHB register).

### 4.6.10 RBCHB - Receive Frame Byte Count High B-Channels

Value after reset: $00_H$.

| | 7 | | | | | 0 | |
|---|---|---|---|---|---|---|---|
| RBCHB | 0 | 0 | 0 | OV | RBC11 | RBC8 | RD (77/87) |

**OV ... Overflow**

A ’1’ in this bit position indicates a message longer than ($2^{12}$ - 1) = 4095 bytes .

**RBC8-11 ... Receive Byte Count**

Four most significant bits of the total number of bytes in a received message (see RBCLB register).

*Note: Normally RBCHB and RBCLB should be read by the microcontroller after an RME-interrupt in order to determine the number of bytes to be read from the RFIFOB, and the total message length. The contents of the registers are valid only after an RME or RPF interrupt, and remain so until the frame is acknowledged via the RMC bit or RRES.*

### 4.6.11 RAL1 - RAL1 Register 1

Value after reset: $00_H$

| | 7 | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|
| RAL1 | RAL1 | | | | | | | WR (77/87) |

RAL1 ... Receive Address Byte Low Register 1

The general function (READ/WRITE) and the meaning or contents of this register depends on the selected operating mode:

– Non-auto mode (16-bit address):
  RAL1 can be programmed with the value of the first individual low address byte.
– Non-auto mode (8-bit address):
  According to X.25 LAPB protocol, the address in RAL1 is recognized as COMMAND address.

### 4.6.12 RAL2 - RAL2 Register

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| RAL2 | RAL2 | | | | | | | | WR (78/88) |

RAL2 ... Receive Address Byte Low Register 2

Value of the second individual programmable low address byte. If a one byte address field is selected, RAL2 is recognized as RESPONSE according to X.25 LAPB protocol.

### 4.6.13 RSTAB - Receive Status Register B-Channels

Value after reset: $0E_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| RSTAB | VFR | RDO | CRC | RAB | HA1 | HA0 | C/R | LA | RD (78/88) |

**VFR... Valid Frame**

Determines whether a valid frame has been received.
The frame is valid (1) or invalid (0).
A frame is invalid when there is not a multiple of 8 bits between flag and frame end (flag, abort).

**RDO ... Receive Data Overflow**

If RDO=1, at least one byte of the frame has been lost, because it could not be stored in RFIFOB. As opposed to ISTAB.RFO an RDO indicates that the beginning of a frame has been received but not all bytes could be stored as the RFIFOB was temporarily full.

**CRC ... CRC Check**

The CRC is correct (1) or incorrect (0).

**RAB ... Receive Message Aborted**

The receive message was aborted by the remote station (1), i.e. a sequence of seven 1's was detected before a closing flag.

**HA1, HA0 … High Byte Address Compare; significant only in non automode 16 and in transparent mode 1**

In operating modes which provide high byte address recognition, the IPAC-X compares the high byte of a 2-bytes address with the contents of two individual programmable registers (RAH1, RAH2) and the fixed values $FE_H$ and $FC_H$ (group address).

Depending on the result of this comparison, the following bit combinations are possible:

10 … RAH1 has been recognized
00 … RAH2 has been recognized
01 … group address has been recognized

**C/R ... Command/Response**

The C/R bit contains the C/R bit of the received frame (Bit1 in the SAPI address, LAPD)

**LA … Low Byte Address Compare; significant only in non automodes 8 and 16 and in transparent mode 2**

The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared with two programmable registers (RAL1, RAL2) and with the group address (fixed value $FF_H$)
0 … Group address has been recognized
1 … RAL1 or RAL2 has been recognized

*Note: RSTAB corresponds to the last received HDLC frame; it is duplicated into RFIFOB for every frame (last byte of frame).*
*If several frames are contained in the RFIFOB the corresponding status information for each frame should be evaluated from the FIFO contents (last byte) as RSTAB only refers to last frame in the FIFO.*

### 4.6.14 TMB -Test Mode Register B-Channels

Value after reset: $00_H$

| | 7 | | | | | | | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| TMB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TLP | RD/WR (79/89) |

**TLP ... Test Loop**

The TX path of layer-2 is internally connected with the RX path of layer-2. Data coming from the layer 1 controller will not be forwarded to the layer 2 controller.

### 4.6.15 RFIFOB - Receive FIFO B-Channels

| | 7 | | 0 | |
|---|---|---|---|---|
| RFIFOB | Receive data | | | RD (7A/8A) |

A read access to this register gives access to the “current” FIFO location selected by an internal pointer which is automatically incremented after each read access.

The RFIFOB contains up to 128 bytes of received data.

After an ISTAB.RPF interrupt, a complete data block is available. The block size can be 8, 16, 32 or 64 bytes depending on the EXMB.RFBS setting.

After an ISTAB.RME interrupt, the number of received bytes can be obtained by reading the RBCLB register.

### 4.6.16 XFIFOB - Transmit FIFO B-Channels

| | 7 | | 0 | |
|---|---|---|---|---|
| XFIFOB | Transmit data | | | WR (7A/8A) |

A write access to this register gives access to the “current” FIFO location selected by an internal pointer which is automatically incremented after each write access.

Depending on EXMB.XFBS up to 32 or 64 bytes of transmit data can be written to the XFIFOB following an ISTAB.XPR interrupt.

# 5 Electrical Characteristics

## 5.1 Absolute Maximum Ratings

| Parameter | Symbol | Limit Values | | Unit |
|---|---|---|---|---|
| | | min. | max. | |
| Ambient temperature under bias<br>PEB<br>PEF | $T_A$ | <br>0<br>-45 | <br>+70<br>+85 | °C |
| Storage temperature | $T_{STG}$ | – 55 | 150 | °C |
| Input/output voltage on any pin with respect to ground | $V_S$ | – 0.3 | 5.25 | V |
| Maximum voltage on any pin with respect to ground | $V_{max}$ | | 5.5 | V |

*Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
*Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.*
*The supply voltage must show a monotonic rise.*

## 5.2 DC Characteristics

$V_{DD}/V_{SS}$ = 3.3 V ± 5%; $T_A$ = 0 to 70 °C

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| H-input level (except pin SR1/2) | $V_{IH}$ | 2.0 | | 5.5 | V | |
| L-input level (except pin SR1/2) | $V_{IL}$ | – 0.3 | | 0.8 | V | |
| H-output level (except pin XTAL2, SX1/2) | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = - 4.5 mA (AD0-7)<br>$I_{OH}$ = - 400 µA (all others) |
| L-output level (except pin XTAL2, SX1/2) | $V_{OL}$ | | | 0.45 | V | $I_{OL}$ = 6 mA (DU, DD, C768)<br>$I_{OL}$ = 4.5 mA ($\overline{ACL}$, AUX7, AUX6, AD0-7)<br>$I_{OL}$ = 2 mA (all others) |
| Input leakage current<br>Output leakage current (all pins except SX1/2,SR1/2,XTAL1/2, AUX7/6) | $I_{LI}$<br>$I_{LO}$ | | | ± 1<br>± 1 | µA<br>µA | 0 V< $V_{IN}$<$V_{DD}$<br>0 V< $V_{OUT}$<$V_{DD}$ |
| Input leakage current<br>Output leakage current (AUX7/6) | $I_{LI}$<br>$I_{LO}$ | 50<br>50 | | 200<br>200 | µA<br>µA | 0 V< $V_{IN}$<$V_{DD}$<br>0 V< $V_{OUT}$<$V_{DD}$<br>(only if AUX7/6 is input or output/open-drain; not relevant if output/push-pull) |
| Power supply current-Power Down<br>- Clocks Off<br><br>- Clocks On | <br>$I_{PD1}$<br><br>$I_{PD2}$ | | | <br>300<br><br>3 | <br>µA<br><br>mA | Inputs at $V_{SS}$ / $V_{DD}$<br>No output loads<br>except SX1,2 (50 Ω) |
| Power supply current<br>- Operational (96 kHz)<br><br><br>- B1=$00_H$,B2=$FF_H$, D=0 | <br>$I_{OP1}$<br><br>$I_{OP2}$<br><br>$I_{OP3}$ | | | <br>30<br><br>30<br><br>25 | <br>mA<br><br>mA<br><br>mA | <br>DCL=1536 kHz<br><br>DCL= 4096 kHz<br><br>DCL=1536 kHz |

## 5.3 Capacitances

$T_A$ = 25 °C, $V_{DD}$ = 3.3 V ± 5% $V_{SSA}$ = 0 V, $V_{SS}$ = 0 V, $f_c$ = 1 MHz, unmeasured pins grounded.

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Input Capacitance<br>I/O Capacitance | $C_{IN}$<br>$C_{I/O}$ | | 7<br>7 | pF<br>pF | All pins except SX1,2 and XTAL1,2 |
| Output Capacitance against $V_{SS}$ | $C_{OUT}$ | | 10 | pF | pins SX1,2 |

## 5.4 Oscillator Specification

### Recommended Oscillator Circuits

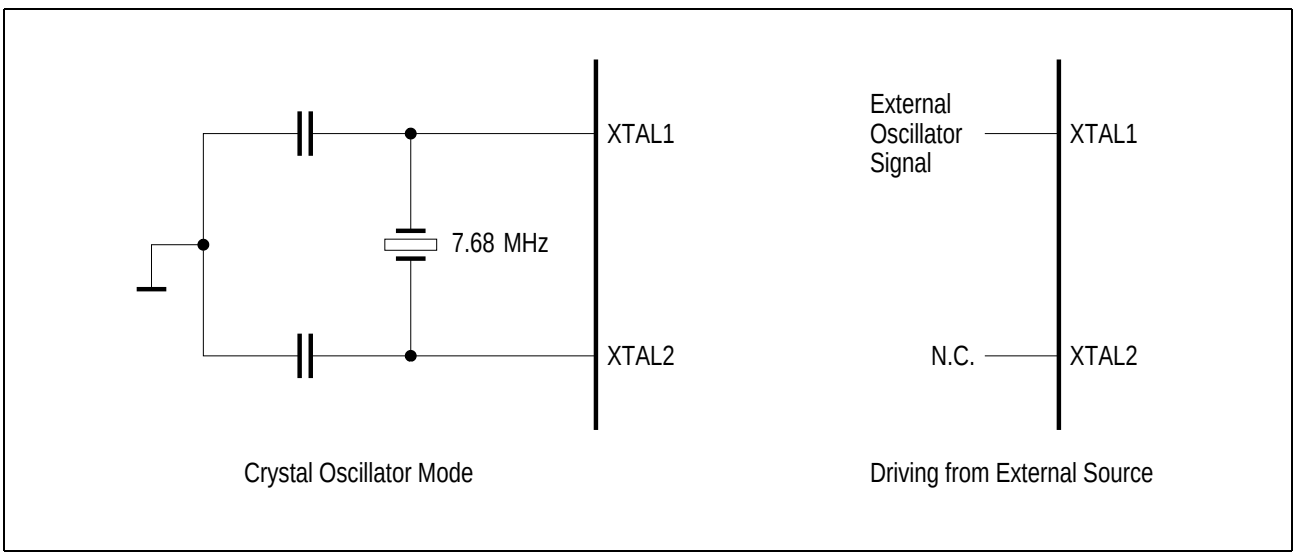



**Figure 89 Oscillator Circuits**

| Parameter | Symbol | Limit Values | Unit |
|---|---|---|---|
| Frequency | f | 7.680 | MHz |
| Frequency calibration tolerance | | max. 100 | ppm |
| Load capacitance | $C_L$ | max. 40 | pF |
| Oscillator mode | | fundamental | |

*Note: It is important to note that the load capacitance depends on the recommendation of the crystal specification. Typical values are 22 ... 33 pF.*

### XTAL1 Clock Characteristics (external oscillator input)

| Parameter | Limit Values | |
|---|---|---|
| | min. | max. |
| Duty cycle | 1:2 | 2:1 |

## 5.5 AC Characteristics

$T_A$ = 0 to 70 °C, $V_{DD}$ = 3.3 V ± 5%

Inputs are driven to 2.4 V for a logical "1" and to 0.45 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC testing input/output waveforms are shown in **Figure 90.**

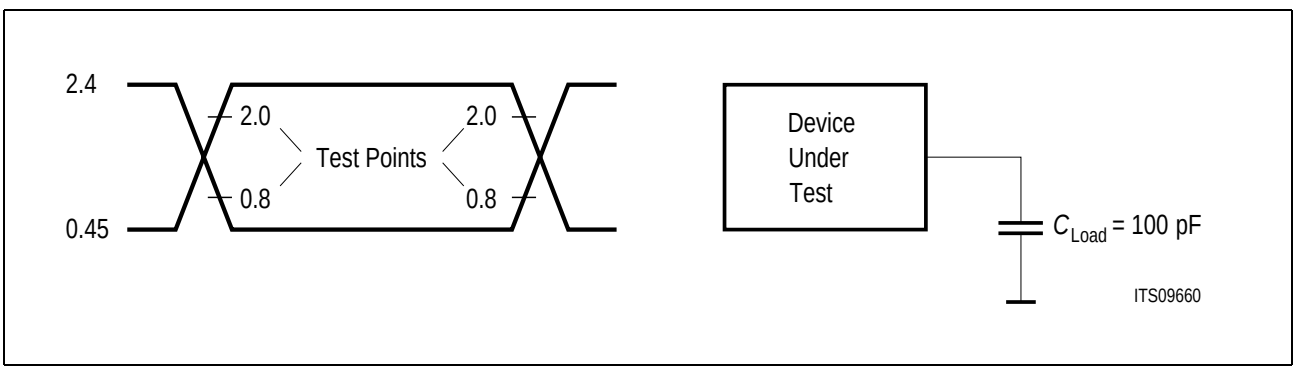



**Figure 90 Input/Output Waveform for AC Tests**

## 5.6 IOM-2 Interface Timing

Data is transmitted with the rising edge of DCL and sampled with its falling edge. Below figure shows double clock mode timing (the length of a timeslot is 2 DCL cycles), however, the timing parameters are valid both in single and double clock mode. For the direction of DU,DD (input or output) please refer to **Chapter 3.4**.

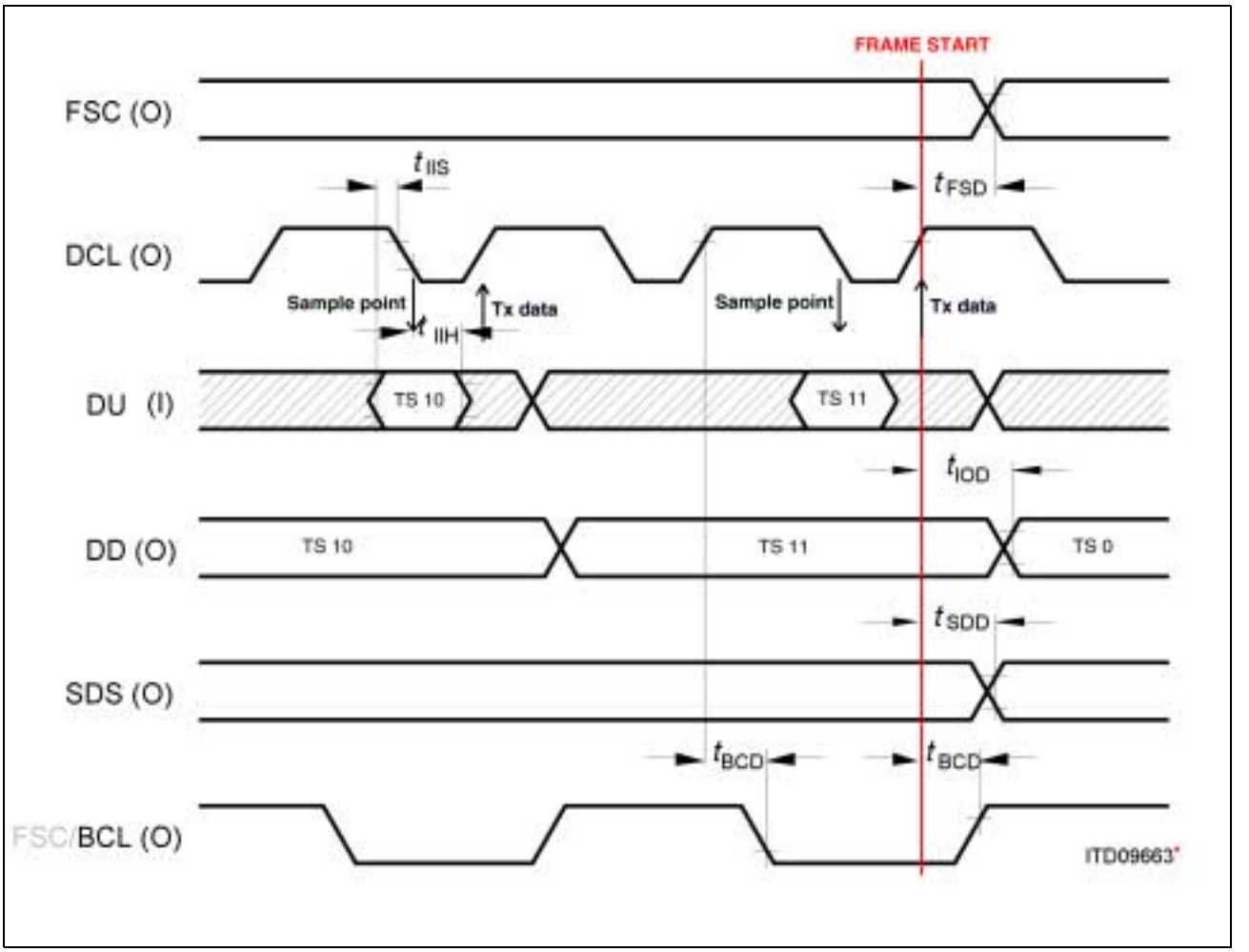



**Figure 91 IOM-2 Timing (TE mode)**

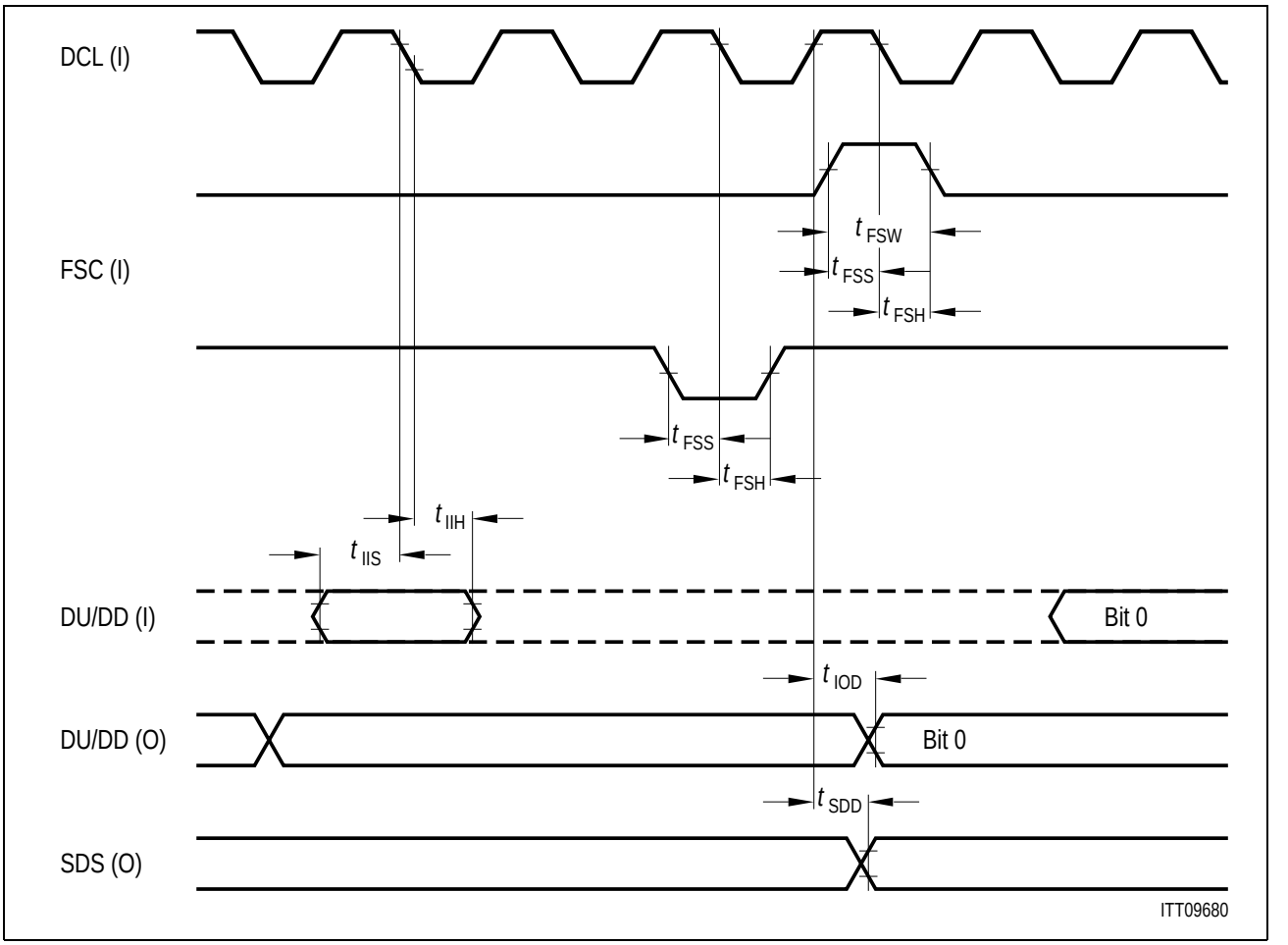



**Figure 92 IOM-2 Timing (LT-S, LT-T, NT mode)**

| Parameter | Symbol | Limit Values | | Unit |
|---|---|---|---|---|
| | | min. | max. | |
| IOM output data delay | $t_{IOD}$ | | 60 | ns |
| IOM input data setup | $t_{IIS}$ | 4 | | ns |
| IOM input data hold | $t_{IIH}$ | 3 | | ns |
| FSC strobe delay (see note) | $t_{FSD}$ | -135 | 15 | ns |
| Strobe signal delay | $t_{SDD}$ | | 50 | ns |
| BCL / FSC delay | $t_{BCD}$ | | 30 | ns |
| Frame sync setup | $t_{FSS}$ | 20 | | ns |
| Frame sync hold | $t_{FSH}$ | 30 | | ns |
| Frame sync width | $t_{FSW}$ | 40 | | ns |

***Note: Min. value in synchronous state, max. value in non-synchronous state. This results in a phase shift of FSC when the S-Bus gets activated, this is the FSC signal is shifted by 135 ns. This applies only to TE mode.***

## DCL Clock Output Characteristics

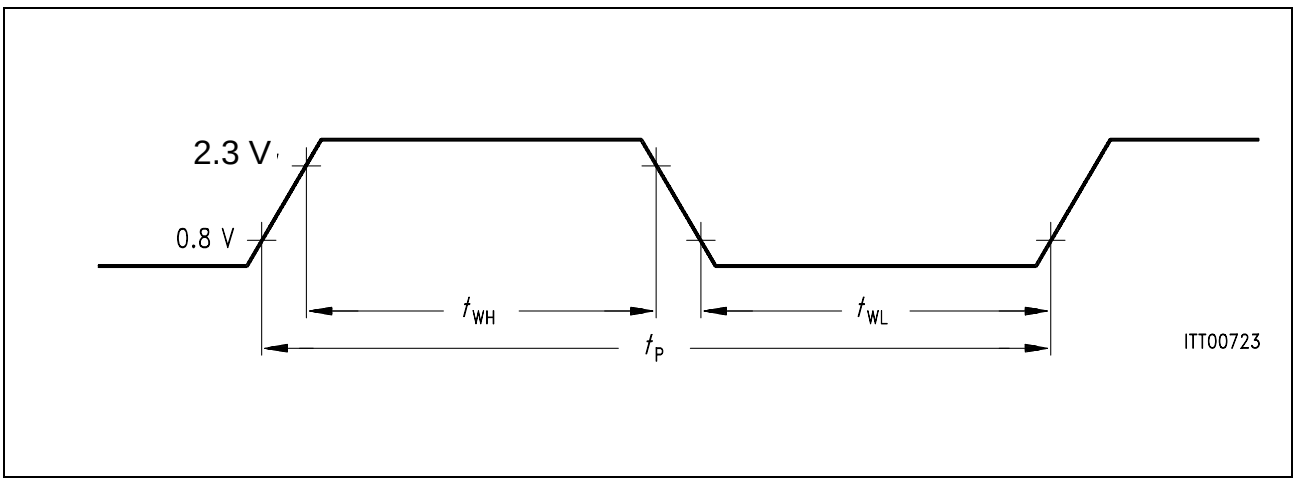



**Figure 93 Definition of Clock Period and Width**

| Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|
| | min. | typ. | max. | | |
| $t_P$ | 585 | 651 | 717 | ns | osc ± 100 ppm |
| $t_{WH}$ | 260 | 325 | 391 | ns | osc ± 100 ppm |
| $t_{WL}$ | 260 | 325 | 391 | ns | osc ± 100 ppm |

## DCL Clock Input Characteristics

| Parameter | Limit Values | | Unit |
|---|---|---|---|
| | min. | max. | |
| Duty cycle | 40 | 60 | % |

## 5.7 Microcontroller Interface Timing

### 5.7.1 Serial Control Interface (SCI) Timing

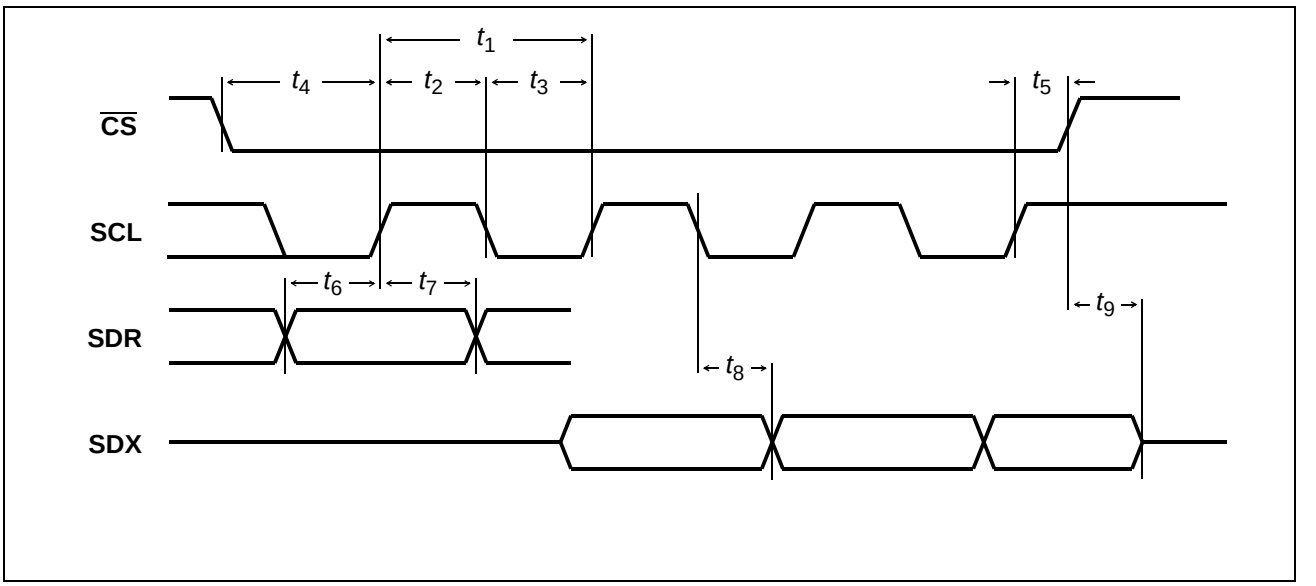



**Figure 94 SCI Interface**

| Parameter<br>SCI Interface | Symbol | Limit values | | Unit |
|---|---|---|---|---|
| | | min. | max. | |
| SCL cycle time | $t_1$ | 200 | | ns |
| SCL high time | $t_2$ | 100 | | ns |
| SCL low time | $t_3$ | 100 | | ns |
| $\overline{CS}$ setup time | $t_4$ | 2 | | ns |
| $\overline{CS}$ hold time | $t_5$ | 10 | | ns |
| SDR setup time | $t_6$ | 10 | | ns |
| SDR hold time | $t_7$ | 6 | | ns |
| SDX data out delay | $t_8$ | | 30 | ns |
| $\overline{CS}$ high to SDX tristate | $t_9$ | | 40 | ns |

## 5.7.2 Parallel Microcontroller Interface Timing

### Siemens/Intel Bus Mode

The data read and write timing is the same for multiplexed and non multiplexed bus operation (**Figure 95** and **Figure 96**). **Figure 97** shows the corresponding address timing in multiplexed mode and **Figure 98** in non multiplexed mode.

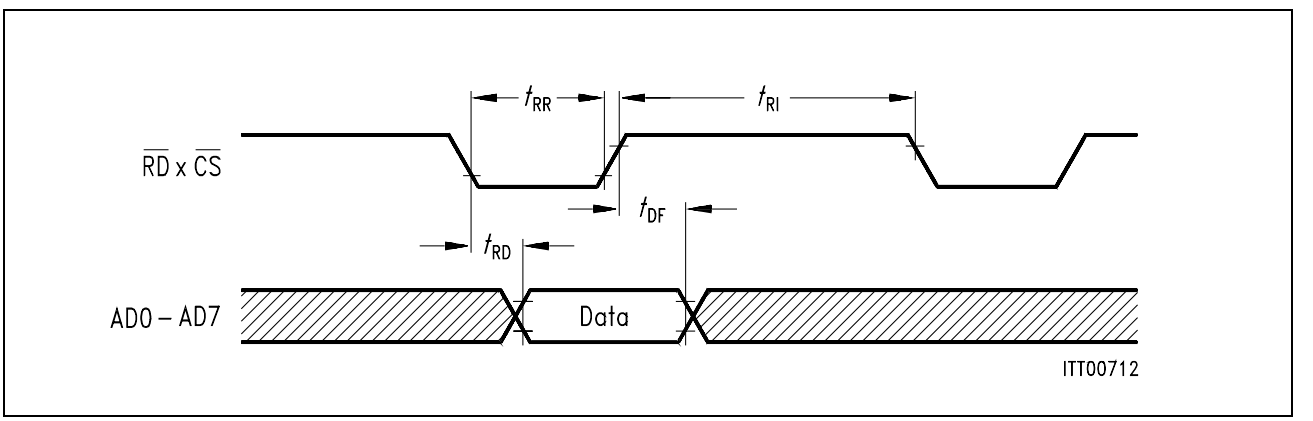



**Figure 95 Microprocessor Read Cycle**

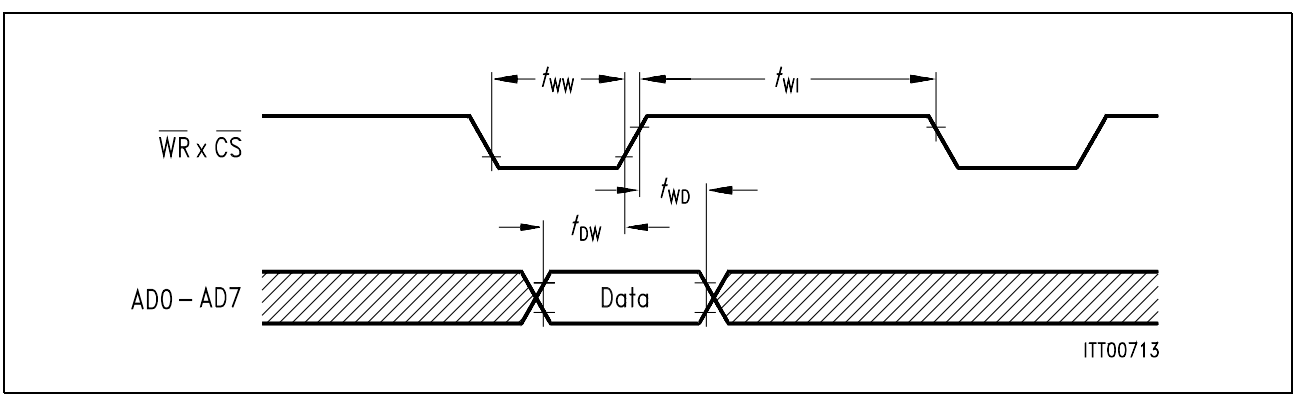



**Figure 96 Microprocessor Write Cycle**

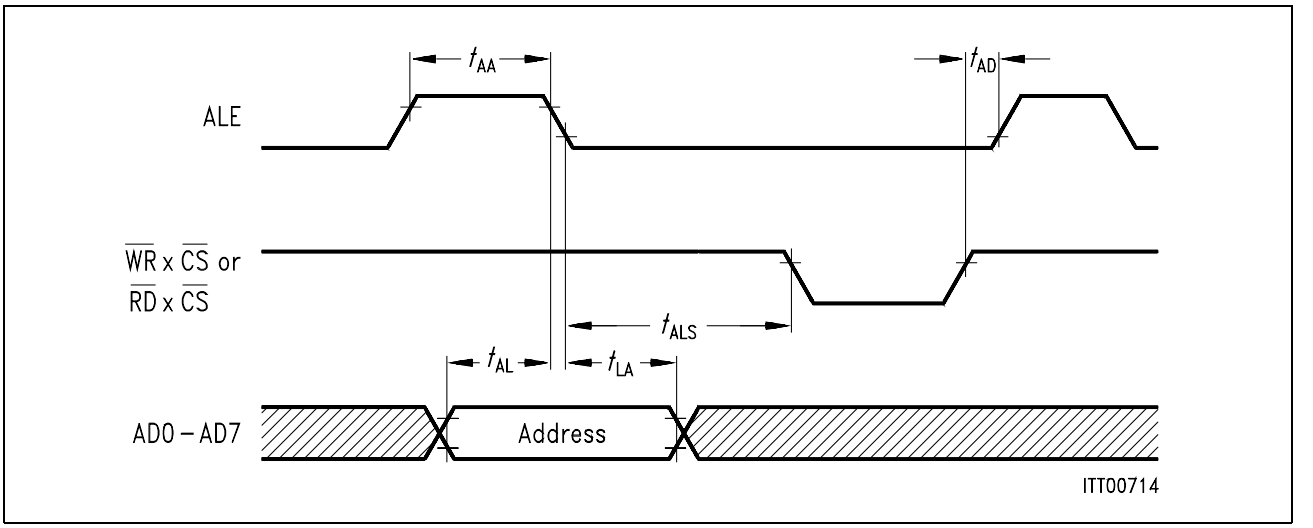



**Figure 97 Multiplexed Address Timing**

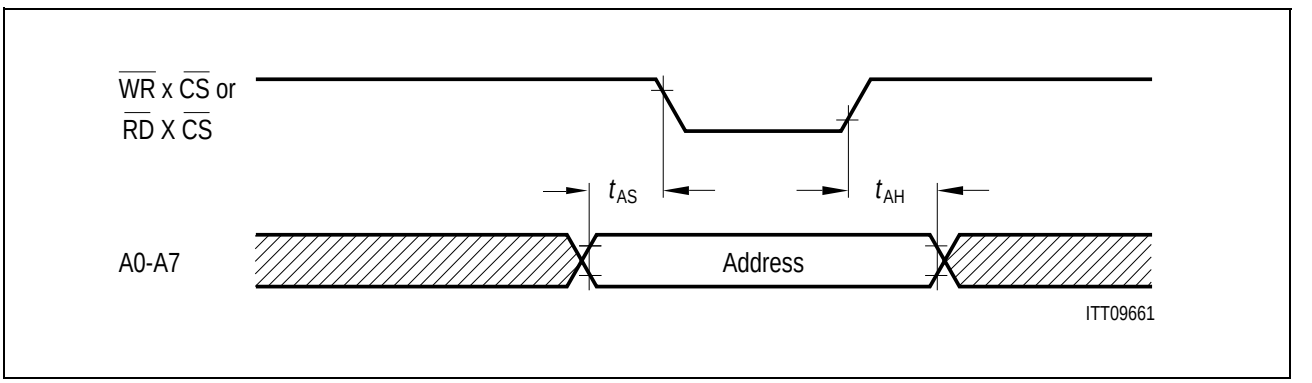



**Figure 98 Non-Multiplexed Address Timing**

### Motorola Bus Mode

The Motorola Bus is non multiplexed. The data timing is shown in **Figure 99** (read) and **Figure 100** (write). The corresponding address timing (for both read and write) is shown in **Figure 101**.

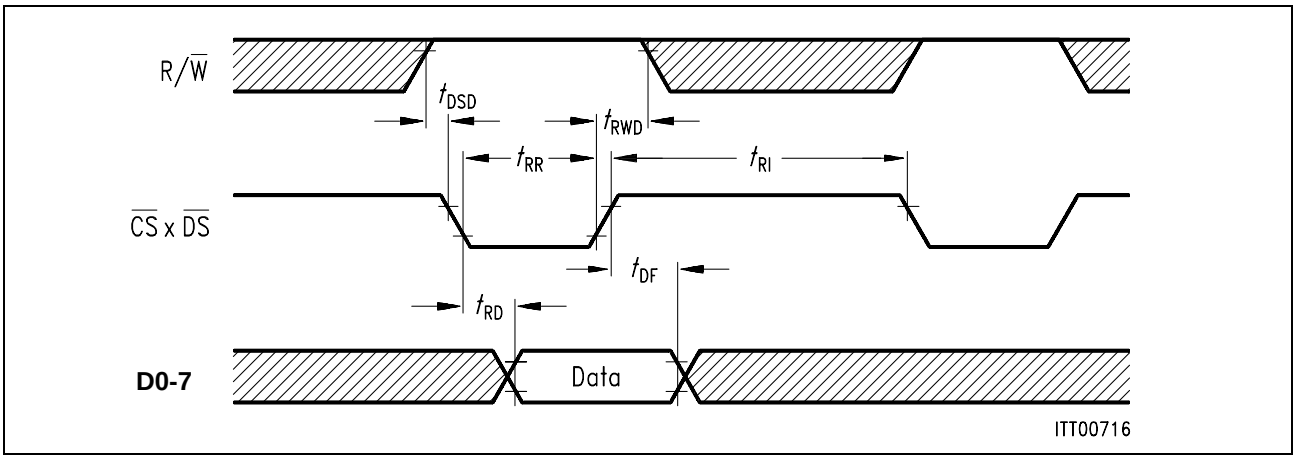



**Figure 99 Microprocessor Read Timing**

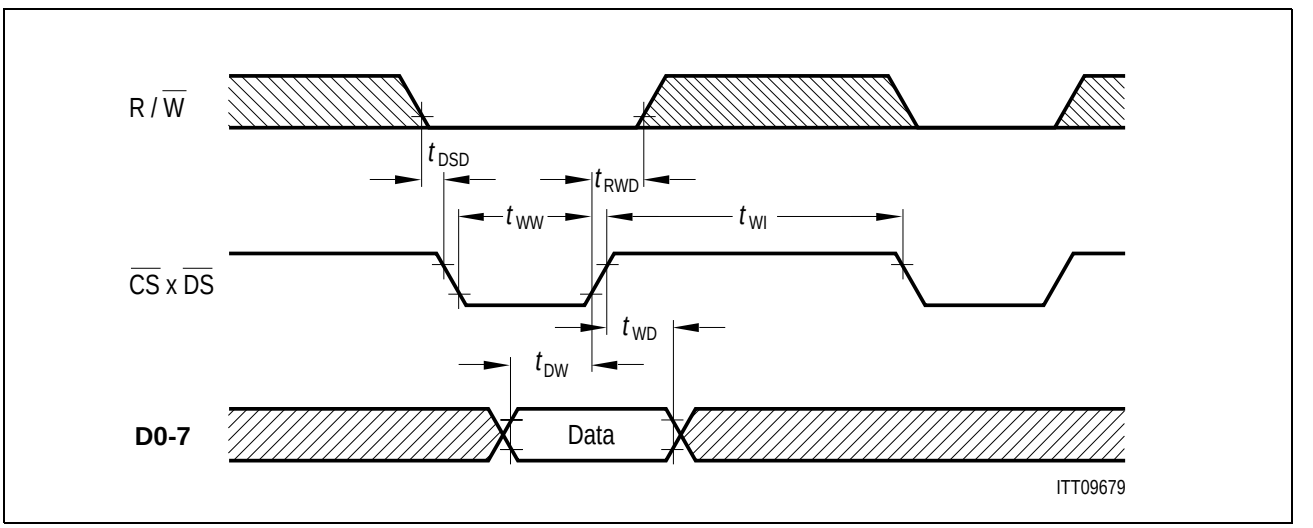



**Figure 100 Microprocessor Write Cycle**

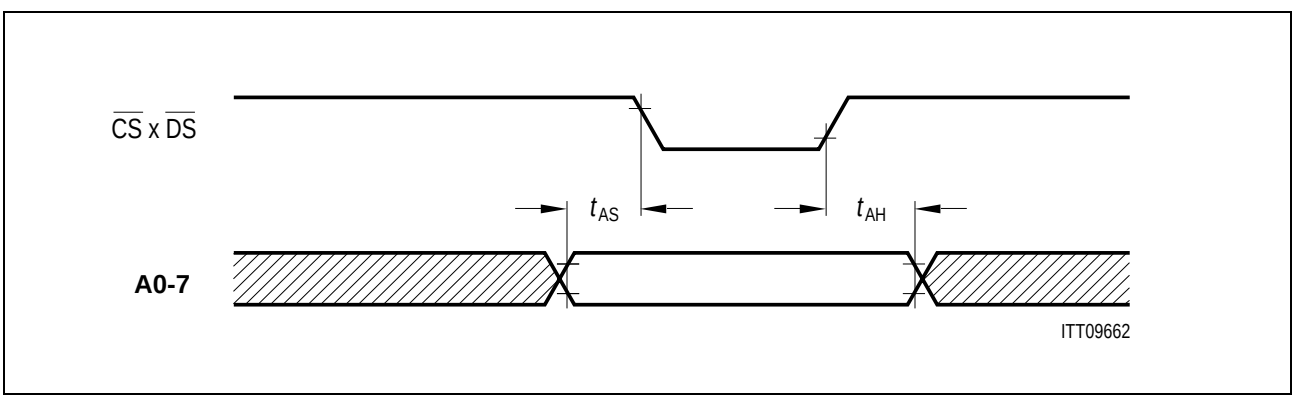



**Figure 101 Non-Multiplexed Address Timing**

## Microprocessor Interface Timing

| Parameter | Symbol | Limit Values | | Unit |
|---|---|---|---|---|
| | | min. | max. | |
| ALE pulse width | $t_{AA}$ | 20 | | ns |
| Address setup time to ALE | $t_{AL}$ | 5 | | ns |
| Address hold time from ALE | $t_{LA}$ | 3 | | ns |
| Address latch setup time to $\overline{WR}$, $\overline{RD}$ | $t_{ALS}$ | 10 | | ns |
| Address setup time | $t_{AS}$ | 10 | | ns |
| Address hold time | $t_{AH}$ | 3 | | ns |
| ALE guard time | $t_{AD}$ | 15 | | ns |
| $\overline{DS}$ delay after R/$\overline{W}$ setup | $t_{DSD}$ | 3 | | ns |
| $\overline{RD}$ pulse width | $t_{RR}$ | 100 | | ns |
| Data output delay from $\overline{RD}$ | $t_{RD}$ | | 80 | ns |
| Data float from $\overline{RD}$ | $t_{DF}$ | | 25 | ns |
| $\overline{RD}$ control interval | $t_{RI}$ | 70 | | ns |
| $\overline{W}$ pulse width | $t_{WW}$ | 10 | | ns |
| Data setup time to $\overline{W}$ x $\overline{CS}$ | $t_{DW}$ | 10 | | ns |
| Data hold time $\overline{W}$ x $\overline{CS}$ | $t_{WD}$ | 2 | | ns |
| $\overline{W}$ control interval | $t_{WI}$ | 70 | | ns |
| R/$\overline{W}$ hold from $\overline{CS}$ x $\overline{DS}$ inactive | $t_{RWD}$ | 2 | | ns |

## 5.8 Multiframe Synchronisation Timing

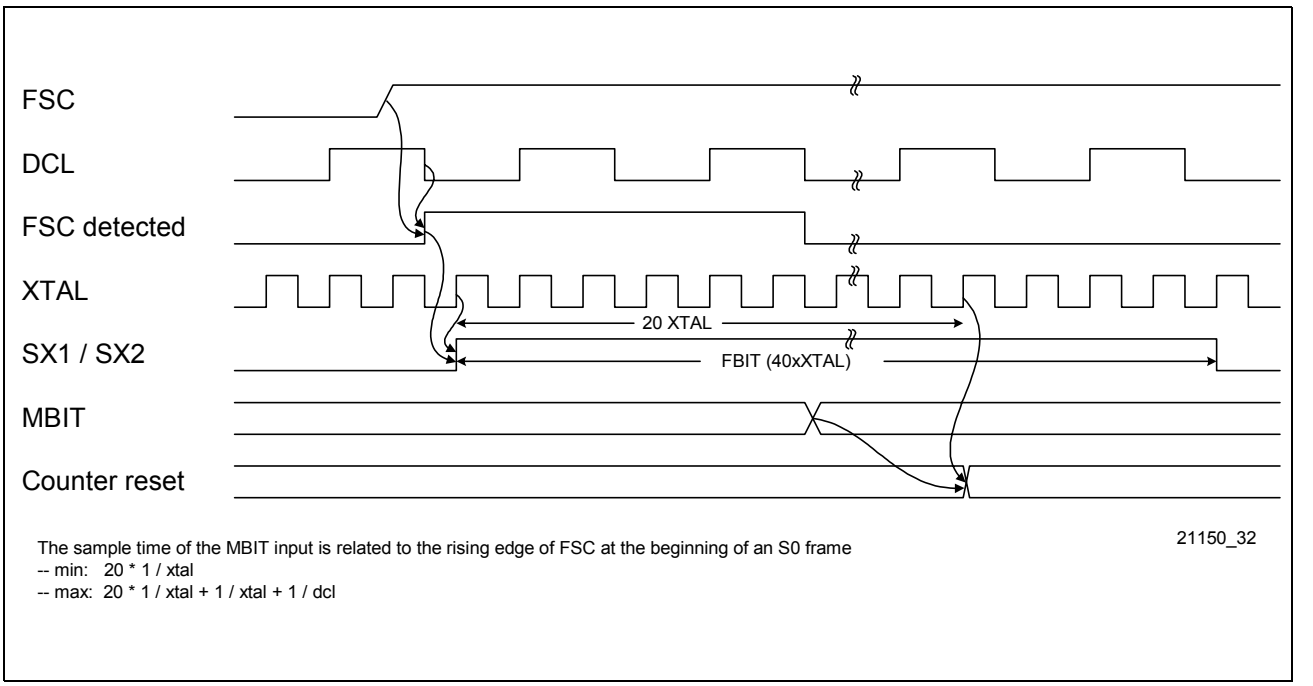



**Figure 102 Sampling Time in LT-S/NT Mode (M-Bit Input)**

## 5.9 Reset

| Parameter | Symbol | Limit Values | Unit | Test Conditions |
|---|---|---|---|---|
| | | min. | | |
| Length of active low state | $t_{RES}$ | 4 | ms | Power On/Power Down to Power Up (Standby) |
| | | 2 x DCL clock cycles | | During Power Up (Standby) |

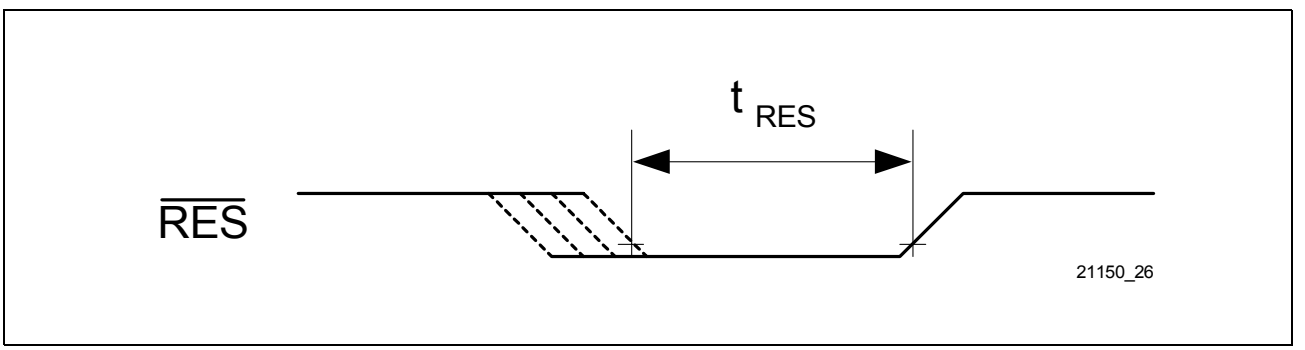



**Figure 103 Reset Signal $\overline{RES}$**

## 5.10 S-Transceiver

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| $V_{DD}$= 3.3 V ± 5%; $V_{SS}$= 0 V; $T_A$ = 0 to 70 °C | | | | | | |
| Absolute value of output pulse amplitude \| VSX2 – VSX1 \| | VX | | | 1.17 | V | $R_L = \infty$ |
| Transmitter output current | IX | | | 26 | mA | $R_L$ = 5.6 Ω |
| Transmitter output impedance (SX1,2) | $Z_X$ | 10<br><br>0 | | | kΩ<br><br>Ω | Inactive or during binary one;<br>during binary zero<br>$R_L$ = 50 Ω |
| Receiver Input impedance (SR1,2) | $Z_R$ | 30 | | | kΩ | $V_{DD}$ = 3.3 V |

## 5.11 Recommended Transformer Specification

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Transformer ratio | | | 1:1 | | | |
| Main inductance | L | 25<br><br>20 | | | mH<br><br>mH | no DC current, 10 kHz<br>2.5 mA DC current, 10 kHz |
| Leakage inductance | $L_L$ | | | 8<br>6 | µH<br>µH | NT/LT-S mode, 10 kHz<br>TE/LT-T mode, 10 kHz |
| Capacitance between primary and secondary side | C | | | 80 | pF | 1 kHz |
| Copper resistance | R | 1.7 | 2.0 | 2.3 | W | |

*Note: In TE/LT-T mode, at the pulse shape measurement with a load of 400 Ω (e.g. K 1403 approval test "Pulse shape") overshots might occur with a leakage inductance greater than 6 µH.*

## 5.12 Line Overload Protection

The maximum input current for the S-transceiver lines (under overvoltage conditions) is given as a function of the width of a rectangular input current pulse. The desctruction limits are shown in **Figure 104**.

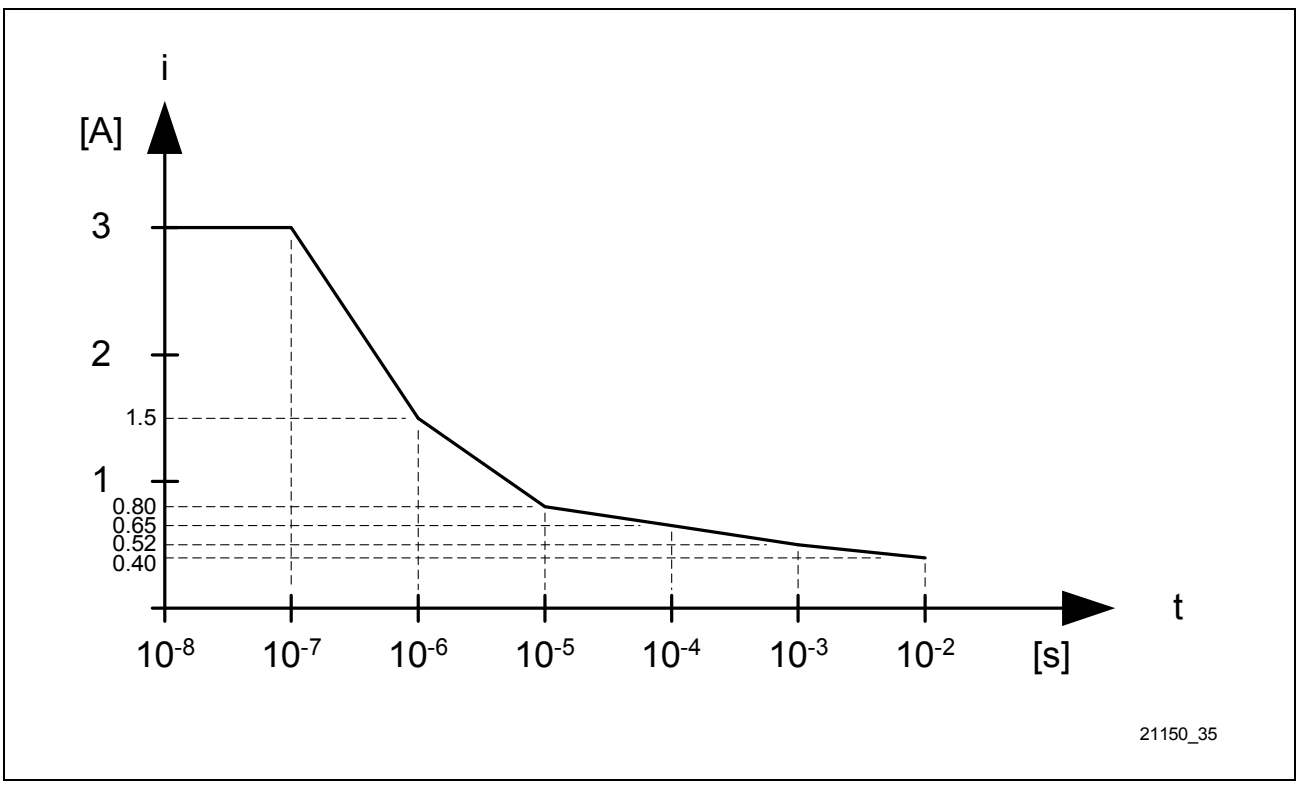



**Figure 104 Maximum Line Input Current**

## 5.13 EMC / ESD Aspects

To improve performance with respect to EMC and ESD requirements it is recommended to provide additional capacitors in the middle tap of the transformers (see **Figure 105** below). The values for C1 and C2 should be in the range 1 ... 10 nF. They can be located either on the chip side of the transformer (option 1) or on the S bus side (option 2), but not on both sides.

This improves EMC immunity acording to EN55024 which is mandatory since 2001-07-01.

*Note: The figure does not show any other components required for protection circuit in receive and transmit direction as this is not affected by including C1 and C2.*

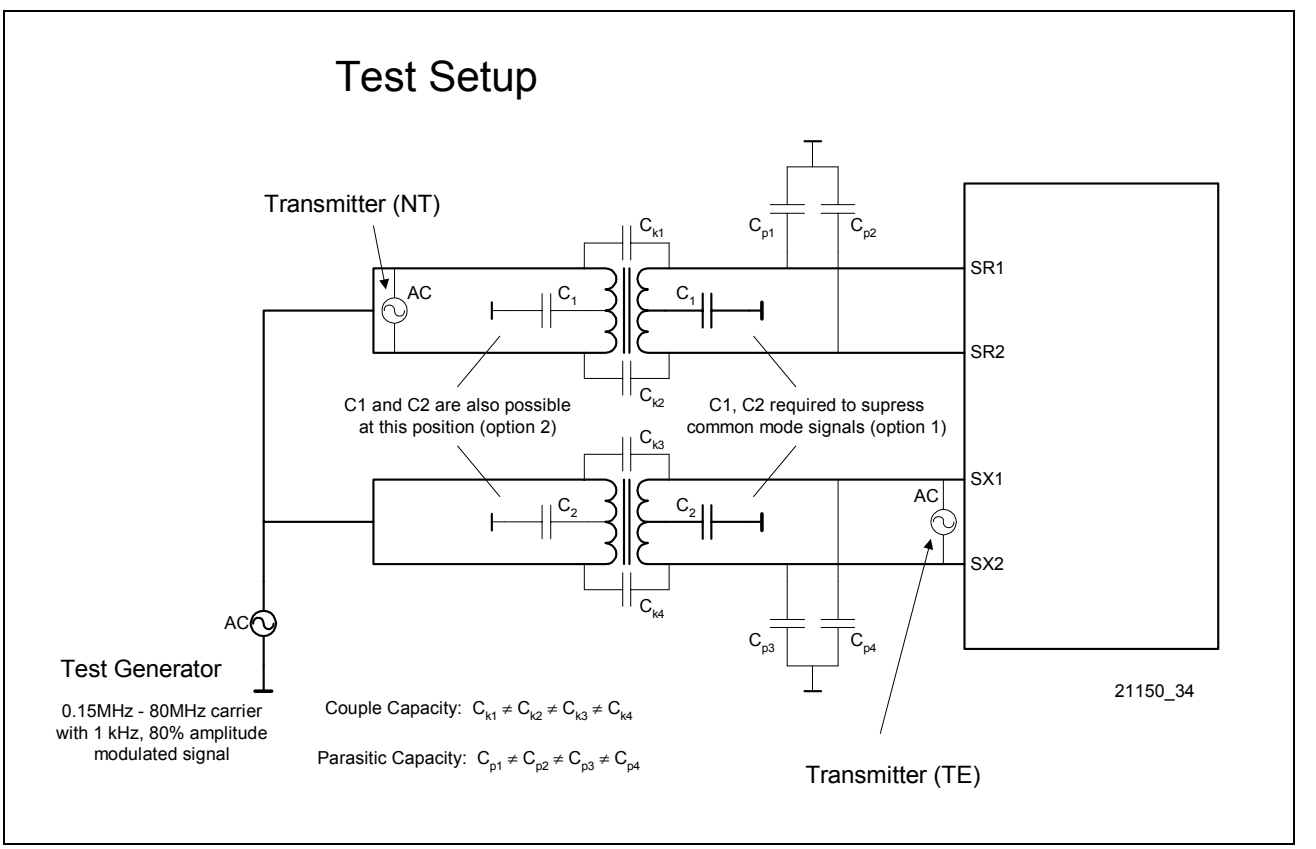
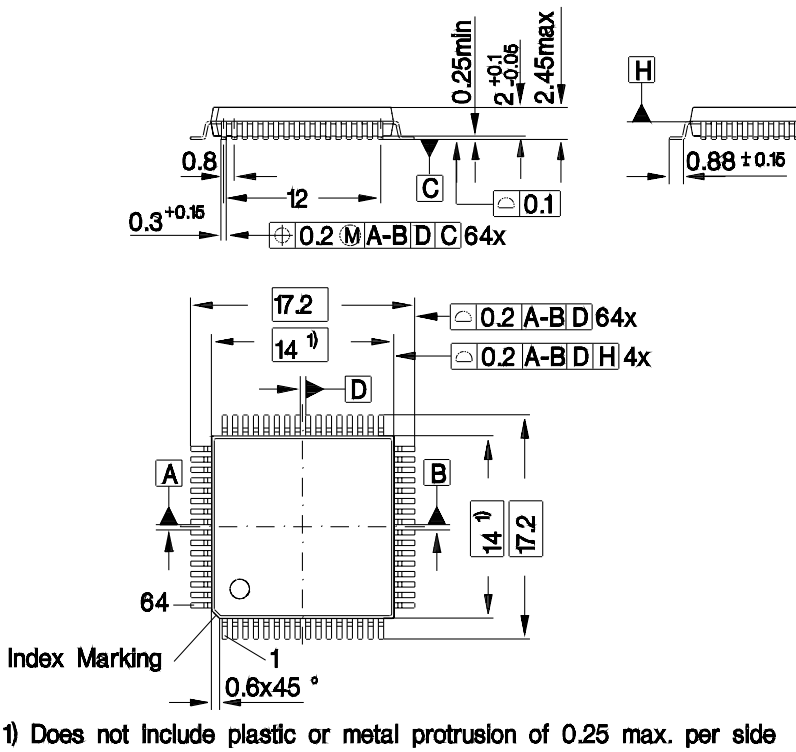



**Figure 105 Transformer Circuitry**

# 6 Package Outlines

**P-MQFP-64-1**
(Plastic Metric Quad Flat Package)



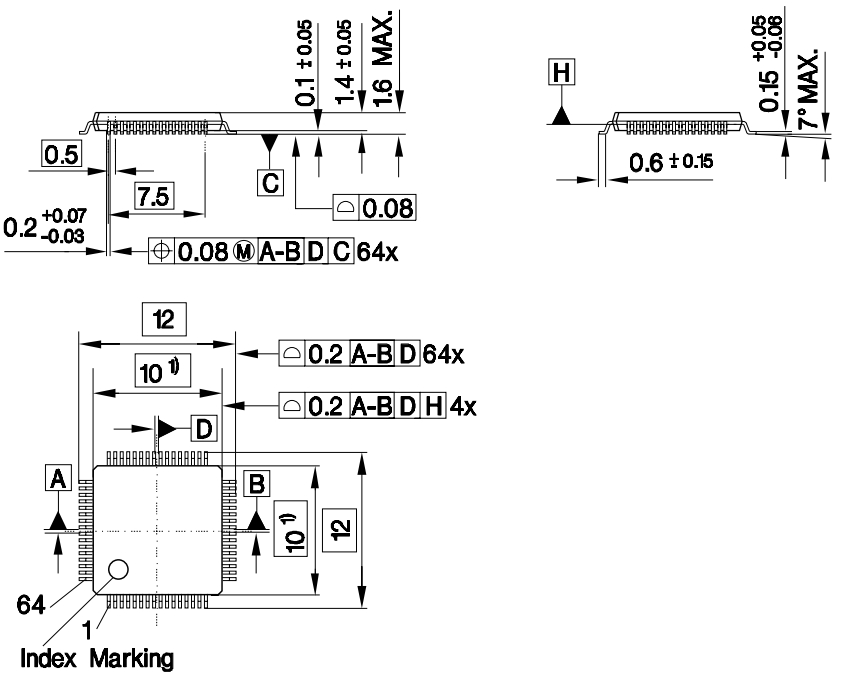

GPM05220

You can find all of the current packages, types of packing, and others on the Infineon Internet Page "Products": **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

**P-TQFP-64-1**
(Plastic Thin Quad Flat Package)




1) Does not include plastic or metal protrusion of 0.25 max. per side

GPM05613

You can find all of the current packages, types of packing, and others on the Infineon Internet Page "Products": **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

# 7 Appendix

### D-channel HDLC, C/I-channel Handler

| Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDR | R/W | RES |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RFIFOD | D-Channel Receive FIFO | | | | | | | | $00_H$-$1F_H$ | R | |
| XFIFOD | D-Channel Transmit FIFO | | | | | | | | $00_H$-$1F_H$ | W | |
| ISTAD | RME | RPF | RFO | XPR | XMR | XDU | 0 | 0 | $20_H$ | R | $10_H$ |
| MASKD | RME | RPF | RFO | XPR | XMR | XDU | 1 | 1 | $20_H$ | W | $FF_H$ |
| STARD | XDOV | XFW | 0 | 0 | RACI | 0 | XACI | 0 | $21_H$ | R | $40_H$ |
| CMDRD | RMC | RRES | 0 | STI | XTF | 0 | XME | XRES | $21_H$ | W | $00_H$ |
| MODED | MDS2 | MDS1 | MDS0 | 0 | RAC | DIM2 | DIM1 | DIM0 | $22_H$ | R/W | $C0_H$ |
| EXMD1 | XFBS | RFBS | | SRA | XCRC | RCRC | 0 | ITF | $23_H$ | R/W | $00_H$ |
| TIMR1 | CNT | | | VALUE | | | | | $24_H$ | R/W | $00_H$ |
| SAP1 | SAPI1 | | | | | | 0 | MHA | $25_H$ | W | $FC_H$ |
| SAP2 | SAPI2 | | | | | | 0 | MLA | $26_H$ | W | $FC_H$ |
| RBCLD | RBC7 | | | | | | | RBC0 | $26_H$ | R | $00_H$ |
| RBCHD | 0 | 0 | 0 | OV | RBC11 | | | RBC8 | $27_H$ | R | $00_H$ |
| TEI1 | TEI1 | | | | | | | EA1 | $27_H$ | W | $FF_H$ |
| TEI2 | TEI2 | | | | | | | EA2 | $28_H$ | W | $FF_H$ |
| RSTAD | VFR | RDO | CRC | RAB | SA1 | SA0 | C/R | TA | $28_H$ | R | $0F_H$ |
| TMD | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TLP | $29_H$ | R/W | $00_H$ |
| | reserved | | | | | | | | $2A$-$2D_H$ | | |
| CIR0 | CODR0 | | | | CIC0 | CIC1 | S/G | BAS | $2E_H$ | R | $F3_H$ |
| CIX0 | CODX0 | | | | TBA2 | TBA1 | TBA0 | BAC | $2E_H$ | W | $FE_H$ |

| | | | | | | |
|---|---|---|---|---|---|---|
| CIR1 | CODR1 | CICW | CI1E | $2F_H$ | R | $FE_H$ |
| CIX1 | CODX1 | CICW | CI1E | $2F_H$ | W | $FE_H$ |

**Transceiver, Auxiliary Interface**

| NAME | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDR | R/W | RES |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TR_CONF0 | DIS_TR | BUS | EN_ICV | 0 | L1SW | 0 | EXLP | LDD | $30_H$ | R/W | $01_H$ |
| TR_CONF1 | 0 | RPLL_ADJ | EN_SFSC | 0 | 0 | x | x | x | $31_H$ | R/W | |
| TR_CONF2 | DIS_TX | PDS | 0 | RLP | 0 | 0 | SGP | SGD | $32_H$ | R/W | $80_H$ |
| TR_STA | RINF | | SLIP | ICV | 0 | FSYN | 0 | LD | $33_H$ | R | $00_H$ |
| TR_CMD | XINF | | | DPRIO | TDDIS | PD | LP_A | 0 | $34_H$ | R/W | $08_H$ |
| SQRR1 | MSYN | MFEN | 0 | 0 | SQR11 | SQR12 | SQR13 | SQR14 | $35_H$ | R | $40_H$ |
| SQXR1 | 0 | MFEN | 0 | 0 | SQX11 | SQX12 | SQX13 | SQX14 | $35_H$ | W | $4F_H$ |
| SQRR2 | SQR21 | SQR22 | SQR23 | SQR24 | SQR31 | SQR32 | SQR33 | SQR34 | $36_H$ | R | $00_H$ |
| SQXR2 | SQX21 | SQX22 | SQX23 | SQX24 | SQX31 | SQX32 | SQX33 | SQX34 | $36_H$ | W | $00_H$ |
| SQRR3 | SQR41 | SQR42 | SQR43 | SQR44 | SQR51 | SQR52 | SQR53 | SQR54 | $37_H$ | R | $00_H$ |
| SQXR3 | SQX41 | SQX42 | SQX43 | SQX44 | SQX51 | SQX52 | SQX53 | SQX54 | $37_H$ | W | $00_H$ |
| ISTATR | 0 | x | x | x | LD | RIC | SQC | SQW | $38_H$ | R | $00_H$ |
| MASKTR | 1 | 1 | 1 | 1 | LD | RIC | SQC | SQW | $39_H$ | R/W | $FF_H$ |
| TR_MODE | 0 | 0 | 0 | 0 | DCH_INH | MODE 2 | MODE 1 | MODE 0 | $3A_H$ | R/W | $00_H$ |
| | reserved | | | | | | | | $3B_H$ | | |
| ACFG1 | OD7 | OD6 | OD5 | OD4 | OD3 | OD2 | OD1 | OD0 | $3C_H$ | R/W | $00_H$ |
| ACFG2 | A7SEL | A5SEL | FBS | A4SEL | ACL | LED | EL1 | EL0 | $3D_H$ | R/W | $00_H$ |

### Transceiver, Auxiliary Interface

| NAME | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDR | R/W | RES |
|---|---|---|---|---|---|---|---|---|---|---|---|
| AOE | OE7 | OE6 | OE5 | OE4 | OE3 | OE2 | OE1 | OE0 | $3E_H$ | R/W | $FF_H$ |
| ARX | AR7 | AR6 | AR5 | AR4 | AR3 | AR2 | AR1 | AR0 | $3F_H$ | R | |
| ATX | AT7 | AT6 | AT5 | AT4 | AT3 | AT2 | AT1 | AT0 | $3F_H$ | W | $00_H$ |

### IOM Handler (Timeslot , Data Port Selection, CDA Data and CDA Control Register)

| Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDR | R/W | RES |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CDA10 | Controller Data Access Register (CH10) | | | | | | | | 40H | R/W | FFH |
| CDA11 | Controller Data Access Register (CH11) | | | | | | | | 41H | R/W | FFH |
| CDA20 | Controller Data Access Register (CH20) | | | | | | | | 42H | R/W | FFH |
| CDA21 | Controller Data Access Register (CH21) | | | | | | | | 43H | R/W | FFH |
| CDA_ TSDP10 | DPS | 0 | 0 | TSS | | | | | 44H | R/W | 00H |
| CDA_ TSDP11 | DPS | 0 | 0 | TSS | | | | | 45H | R/W | 01H |
| CDA_ TSDP20 | DPS | 0 | 0 | TSS | | | | | 46H | R/W | 80H |
| CDA_ TSDP21 | DPS | 0 | 0 | TSS | | | | | 47H | R/W | 81H |
| BCHA_ TSDP_ BC1 | DPS | 0 | 0 | TSS | | | | | 48H | R/W | 80H |
| BCHA_ TSDP_ BC2 | DPS | 0 | 0 | TSS | | | | | 49H | R/W | 81H |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| BCHB_TSDP_BC1 | DPS | 0 | 0 | TSS | | | | | 4AH | R/W | 81H |
| BCHB_TSDP_BC2 | DPS | 0 | 0 | TSS | | | | | 4BH | R/W | 85H |
| TR_TSDP_BC1 | DPS | 0 | 0 | TSS | | | | | 4CH | R/W | |
| TR_TSDP_BC2 | DPS | 0 | 0 | TSS | | | | | 4DH | R/W | |
| CDA1_CR | 0 | 0 | EN_TBM | EN_I1 | EN_I0 | EN_O1 | EN_O0 | SWAP | 4EH | R/W | 00H |
| CDA2_CR | 0 | 0 | EN_TBM | EN_I1 | EN_I0 | EN_O1 | EN_O0 | SWAP | 4FH | R/W | 00H |

**IOM Handler (Control Registers, Synchronous Transfer Interrupt Control), MONITOR Handler**

| Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDR | R/W | RES |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TR_CR (CI_CS=0) | EN_D | EN_B2R | EN_B1R | EN_B2X | EN_B1X | CS2-0 | | | $50_H$ | R/W | |
| TRC_CR (CI_CS=1) | 0 | 0 | 0 | 0 | 0 | CS2-0 | | | $50_H$ | R/W | |
| BCHA_CR | DPS_D | 0 | EN_D | EN_BC2 | EN_BC1 | CS2-0 | | | $51_H$ | R/W | $80_H$ |
| BCHB_CR | DPS_D | 0 | EN_D | EN_BC2 | EN_BC1 | CS2-0 | | | $52_H$ | R/W | $81_H$ |
| DCI_CR (CI_CS=0) | DPS_CI1 | EN_CI1 | D_EN_D | D_EN_B2 | D_EN_B1 | CS2-0 | | | $53_H$ | R/W | |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DCIC_CR (CI_CS=1) | 0 | 0 | 0 | 0 | 0 | CS2-0 | | | $53_H$ | R/W | 00H |
| MON_CR | DPS | EN_ MON | 0 | 0 | 0 | CS2-0 | | | $54_H$ | R/W | |
| SDS1_CR | ENS_ TSS | ENS_ TSS+1 | ENS_ TSS+3 | TSS | | | | | $55_H$ | R/W | $00_H$ |
| SDS2_CR | ENS_ TSS | ENS_ TSS+1 | ENS_ TSS+3 | TSS | | | | | $56_H$ | R/W | $00_H$ |
| IOM_CR | SPU | DIS_ AW | CI_CS | TIC_ DIS | EN_ BCL | CLKM | DIS_ OD | DIS_ IOM | $57_H$ | R/W | $08_H$ |
| STI | STOV 21 | STOV 20 | STOV 11 | STOV 10 | STI 21 | STI 20 | STI 11 | STI 10 | $58_H$ | R | $00_H$ |
| ASTI | 0 | 0 | 0 | 0 | ACK 21 | ACK 20 | ACK 11 | ACK 10 | $58_H$ | W | $00_H$ |
| MSTI | STOV 21 | STOV 20 | STOV 11 | STOV 10 | STI 21 | STI 20 | STI 11 | STI 10 | $59_H$ | R/W | $FF_H$ |
| SDS_ CONF | 0 | 0 | 0 | 0 | DIOM_ INV | DIOM_ SDS | SDS2_ BCL | SDS1_ BCL | $5A_H$ | R/W | $00_H$ |
| MCDA | MCDA21 | | MCDA20 | | MCDA11 | | MCDA10 | | $5B_H$ | R | $FF_H$ |
| MOR | MONITOR Receive Data | | | | | | | | $5C_H$ | R | $FF_H$ |
| MOX | MONITOR Transmit Data | | | | | | | | $5C_H$ | W | $FF_H$ |
| MOSR | MDR | MER | MDA | MAB | 0 | 0 | 0 | 0 | $5D_H$ | R | $00_H$ |
| MOCR | MRE | MRC | MIE | MXC | 0 | 0 | 0 | 0 | $5E_H$ | R/W | $00_H$ |
| MSTA | 0 | 0 | 0 | 0 | 0 | MAC | 0 | TOUT | $5F_H$ | R | $00_H$ |
| MCONF | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TOUT | $5F_H$ | W | $00_H$ |

### Interrupt, General Configuration Registers

| NAME | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDR | R/W | RES |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISTA | ICA | ICB | ST | CIC | AUX | TRAN | MOS | ICD | $60_H$ | R | $00_H$ |
| MASK | ICA | ICB | ST | CIC | AUX | TRAN | MOS | ICD | $60_H$ | W | $FF_H$ |
| AUXI | 0 | 0 | EAW | WOV | TIN2 | TIN1 | INT1 | INT0 | $61_H$ | R | $00_H$ |
| AUXM | 1 | 1 | EAW | WOV | TIN2 | TIN1 | INT1 | INT0 | $61_H$ | W | $FF_H$ |
| MODE1 | 0 | 0 | 0 | WTC1 | WTC2 | CFS | RSS2 | RSS1 | $62_H$ | R/W | $00_H$ |
| MODE2 | 0 | 0 | 0 | 0 | INT_ POL | 0 | 0 | PPSDX | $63_H$ | R/W | $00_H$ |
| ID | 0 | 0 | DESIGN | | | | | | $64_H$ | R | $01_H$ |
| SRES | RES_ CI | RES_ BCHA | RES_ BCHB | RES_ MON | RES_ DCH | RES_ IOM | RES_ TR | RES_ RSTO | $64_H$ | W | $00_H$ |
| TIMR2 | TMD | 0 | CNT | | | | | | $65_H$ | R/W | $00_H$ |
| | reserved | | | | | | | | $66_H$- $6F_H$ | | |

### B-channel HDLC Control Registers (channel A / B)

| Name | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | ADDR | R/W | RES |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISTAB | RME | RPF | RFO | XPR | 0 | XDU | 0 | 0 | $70_H/80_H$ | R | $10_H$ |
| MASKB | RME | RPF | RFO | XPR | 1 | XDU | 1 | 1 | $70_H/80_H$ | W | $FF_H$ |
| STARB | XDOV | XFW | 0 | 0 | RACI | 0 | XACI | 0 | $71_H/81_H$ | R | $40_H$ |
| CMDRB | RMC | RRES | 0 | 0 | XTF | 0 | XME | XRES | $71_H/81_H$ | W | $00_H$ |
| MODEB | MDS2 | MDS1 | MDS0 | 0 | RAC | 0 | 0 | 0 | $72_H/82_H$ | R/W | $C0_H$ |
| EXMB | XFBS | RFBS | | SRA | XCRC | RCRC | 0 | ITF | $73_H/83_H$ | R/W | $00_H$ |
| | reserved | | | | | | | | $74_H/84_H$ | | |

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RAH1 | RAH1 | | | | | | 0 | MHA | $75_H/85_H$ | W | $00_H$ |
| RAH2 | RAH2 | | | | | | 0 | MLA | $76_H/86_H$ | W | $00_H$ |
| RBCLB | RBC7 | | | | | | | RBC0 | $76_H/86_H$ | R | $00_H$ |
| RBCHB | 0 | 0 | 0 | OV | RBC11 | | | RBC8 | $77_H/87_H$ | R | $00_H$ |
| RAL1 | RAL1 | | | | | | | | $77_H/87_H$ | W | $00_H$ |
| RAL2 | RAL2 | | | | | | | | $78_H/88_H$ | W | $00_H$ |
| RSTAB | VFR | RDO | CRC | RAB | HA1 | HA0 | C/R | LA | $78_H/88_H$ | R | $0E_H$ |
| TMB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | TLP | $79_H/89_H$ | R/W | $00_H$ |
| RFIFOB | B-Channel Receive FIFO | | | | | | | | $7A_H/8A_H$ | R | |
| XFIFOB | B-Channel Transmit FIFO | | | | | | | | $7A_H/8A_H$ | W | |
| | reserved | | | | | | | | $7B_H$-$7F_H$ $8B_H$-$8F_H$ | | |

## A

A4SEL bit 202
A5SEL bit 202
A7SEL bit 202
Absolute maximum ratings 245
AC characteristics 250
ACFG1 register 202
ACFG2 register 202
ACKxy bits 218
ACL bit 202
Activation 94
Activation indication - pin ACL 49
Activation LED 49
Activation/deactivation of IOM-2 interface 138
AOE register 204
Appendix 265
Applications 20
AR7-0 bits 204
Architecture 33
ARX register 204
ASTI register 218
Asynchronous awake 140
AT7-0 bits 205
ATX register 205
AUX bit 224
AUXI register 225
Auxiliary interface 141
AUXM register 226

## B

BAC bit 188
BAS bit 187
BCHx_CR registers 211
BCHx_TSDP_BC1/2 registers 207
Block diagram 34
BUS bit 191
Bus operation modes 40

## C

C/I channel 128
C/R bit 185, 242
Capacitances 248
CDA_TSDPxy registers 207
CDAx_CR register 208
CDAxy registers 206
CFS bit 227
CI_CS bit 216
CI1E bit 189
CIC bit 224
CIC1/0 bits 187
CICW bit 189
CIR0 register 187
CIR1 register 189
CIX0 register 188
CIX1 register 190
CLKM bit 216
Clock generation 70
CMDR register 178
CMDRB register 234
CNT bits 182, 230
CODR0 bits 187
CODR1 bits 189
CODX0 bits 188
CODX1 bits 190
Control of layer-1 75
Controller data access 102
CRC bit 185, 242

## D

D_EN_B2/1 bits 212
D_EN_D bit 212
DC characteristics 246
DCH_INH bit 200
D-channel access control
Intelligent NT 134
S-bus D-channel control in LT-T 134
S-bus priority mechanism 131
TIC bus 129
DCI_CR register 212
Deactivation 94
Delay between IOM-2 and S 59
DESIGN bits 229
Device architecture 33

DIM2-0 bits 179
Direct address mode 40
DIS_AW bit 216
DIS_IOM bit 216
DIS_OD bit 216
DIS_TR bit 191
DIS_TX bit 193
DPRIO bit 195
DPS bit 207, 214
DPS_CI1 bit 212
DPS_D bit 211

## E

EA1 bit 184
EA2 bit 185
EAW bit 225
EL1/0 bits 202
Electrical characteristics 245
EN_B2/1R bits 209
EN_B2/1X bits 209
EN_BC2/1 bits 211
EN_BCL bit 216
EN_CI1 bit 212
EN_D bit 209, 211
EN_I0 bit 208
EN_I1 bit 208
EN_ICV bit 191
EN_MON bit 214
EN_O0 bit 208
EN_O1 bit 208
EN_SFSC bit 192
EN_TBM bit 208
ENS_TSSx bits 215
Exchange awake 45
EXLP bit 191
EXMB register 237
EXMD1 register 180
Extended transparent mode 161
External reset input 45

## F

FBS bit 202
Features 18
FSYN bit 194
Functional blocks 33

## H

HA1/0 bits 242
HDLC controllers
Access to IOM channels 160
Data reception 147
Data transmission 155
Extended transparent mode 161
Interrupts 162
Receive frame structure 153
Test functions 163
Transmit frame structure 160

## I

I/O lines 141
ICA/B bits 224
ICD bit 224
ICV bit 194
ID register 229
IDSL 111
Indirect address mode 40
INT_POL bit 229
INT1/0 bits 225
Intelligent NT 134
Interrupt input 142
Interrupt structure 42
IOM_CR register 216
IOM-2 97
Frame structure (LT) 99
Frame structure (NT) 99
Frame structure (TE) 98
Handler 100
Interface Timing 251
LT-S, LT-T, NT modes 97
Monitor channel 117
TE mode 97
ISTA register 224
ISTAB register 232
ISTAD register 175
ISTATR register 199

ITF bit 180, 237

## J

Jitter 73

## L

L1SW bit 191
LA bit 242
LD bit 194, 199
LDD bit 191
LED bit 202
LED output 49
Level detection 67
Logic symbol 19
Looping data 103
LP_A bit 195
LT-T mode 134

## M

MAB bit 221
MAC bit 223
MASK register 225
MASKB register 233
MASKD register 176
MASKTR register 200
M-Bit synchronisation 56
MCDA register 220
MCDAxy bits 220
MCONF register 223
MDA bit 221
MDR bit 221
MDS2-0 bits 179, 236
MER bit 221
MFEN bit 196, 197
MHA bit 182, 238
Microcontroller interface timing 254
Microcontroller interfaces 35
MIE bit 222
MLA bit 183, 240
MOCR register 222
MODE1 register 227
MODE2 register 229
MODE2-0 bits 200
MODEB register 236
MODED register 179
MON_CR register 214
Monitor channel
- Error treatment 122
- Handshake procedure 118
- Interrupt logic 127
- Master device 124
- Slave device 125
- Time-out procedure 126

Monitoring data 107
Monitoring TIC bus 107
MOR register 220
MOS bit 224
MOSR register 221
MOX register 221
MRC bit 222
MRE bit 222
MSTA register 223
MSTI register 219
MSYN bit 196
Multiframe sync timing 258
Multiframe synchronization 56
Multiframing 54
MXC bit 222

## O

OD7-0 bits 202
OE7-0 bits 204
Oscillator 249
Oscillator clock output 74
OV bit 184, 241
Overview 14

## P

Package Outlines 262
Parallel microcontroller interface 40
PD bit 195
PDS bit 193
Pin configuration 24
PPSDX bit 229

## R

RAB bit 185, 242
RAC bit 179, 236
RACI bit 177, 233
RAH1 register 238
RAH2 register 240
RAL1 register 241
RAL2 register 242
RBC11-8 bits 184, 241
RBC7-0 bits 183, 240
RBCHB register 241
RBCHD register 184
RBCLB register 240
RBCLD register 183
RCRC bit 180, 237
RDO bit 185, 242
Receive PLL 73
Register description 165
RES_xxx bits 230
Reset generation 44
Reset source selection 44
Reset timing 259
RFBS bits 180, 237
RFIFOB register 244
RFIFOD register 174
RFO bit 175, 232
RIC bit 199
RINF bits 194
RLP bit 193
RMC bit 178, 234
RME bit 175, 232
RPF bit 175, 232
RPLL_ADJ bit 192
RRES bit 178, 234
RSS2/1 bits 227
RSTAB register 242
RSTAD register 185

## S

S/G bit 136, 187
S/T-Interface 50
Circuitry 64
Coding 52
Delay compensation 66
External protection circuitry 64
Multiframe synchronization 56
Multiframing 54
Receiver characteristics 63
Transceiver enable/disable 67
Transmitter characteristics 62
SA1/0 bits 185
SAP1 register 182
SAP2 register 183
S-bus priority mechanism 131
SCI - serial control interface 36
SCI interface timing 254
SDS 114
SDS_CONF register 219
SDS2/1_BCL bits 219
SDSx_CR registers 215
Serial data strobe 114
SGD bit 193
SGP bit 193
Shifting data 103
SLIP bit 194
Software reset 45
SPU bit 216
SQC bit 199
SQR1-4 bits 196
SQR21-24 bits 197
SQR31-34 bits 197
SQR41-44 bits 198
SQR51-54 bits 198
SQRR1 register 196
SQRR2 register 197
SQRR3 register 198
SQW bit 199
SQX1-4 bits 197
SQX21-24 198
SQX31-34 bits 198
SQX41-44 bits 198
SQX51-54 bits 198
SQXR1 register 197
SQXR2 register 198
SQXR3 register 198

SRA bit 180, 237
SRES register 230
ST bit 224
STARB register 233
STARD register 177
State machine
LT-S mode 84
NT mode 89
TE and LT-T mode 77
STI bit 178
STI register 217
STIxy bits 217, 219
Stop/Go bit 136, 187
STOVxy bits 217, 219
Strobed data clock 114
Subscriber awake 45
SWAP bit 208
Synchronous transfer 108

## T

TA bit 185
TBA2-0 bits 188
TDDIS bit 195
TEI1 register 184
TEI2 register 185
Test functions 68
Test signals 164
TIC bus 129
TIC_DIS bit 216
Timer 46
Timer 1 47
Timer 2 47
TIMR1 register 182
TIMR2 register 230
TIN2/1 bits 225
TLP bit 187, 244
TMB register 244
TMD bit 230
TMD register 187
TOUT bit 223
TR_CMD register 195
TR_CONF0 register 191
TR_CONF1 register 192
TR_CONF2 register 193
TR_CR register 209
TR_MODE register 200
TR_STA register 194
TR_TSDP_BC1/2 registers 207
TRAN bit 224
Transceiver enable/disable 67
Transformer specification 261
TSS bits 207, 215
Typical applications 20

## V

VALUE bits 182
VFR bit 185, 242

## W

Watchdog timer 45
WOV bit 225
WTC1/2 bits 227

## X

XACI bit 177, 233
XCRC bit 180, 237
XDOV bit 177, 233
XDU bit 175, 232
XFBS bit 180, 237
XFIFOB register 244
XFIFOD register 174
XFW bit 177, 233
XINF bits 195
XME bit 178, 234
XMR bit 175
XPR bit 175, 232
XRES bit 178, 234
XTF bit 178, 234

http://www.infineon.com

Published by Infineon Technologies AG