ISZ-2510
Product Specification
Revision 1.0

CONTENTS

1 Document Information

1.1 Revision History

Revision Date	Revision	Description
12/24/2013	1.0	Initial Release

1.2 Purpose and Scope

This document is a preliminary product specification, providing a description, specifications, and design related information for the single axis ISZ-2510™ gyroscope. The device is housed in a small 3x3x0.9mm QFN package.

1.3 Product Overview

The ISZ-2510 is a single-chip, digital output, single axis MEMS gyroscope IC which features a 512-byte FIFO. The FIFO can lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode.

The gyroscope includes a programmable full-scale range of ±250, ±500, ±1000, and ±2000 degrees/sec, very low Rate noise at 0.01 dps/√Hz and extremely low power consumption at 2.8mA. Factory-calibrated initial sensitivity reduces production-line calibration requirements.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, a precision clock with 1% drift from -40°C to 85°C, an embedded temperature sensor, and programmable interrupts. The device features I^2C and SPI serial interfaces, a VDD operating range of 1.71 to 3.6V, and a separate digital IO supply, VDDIO from 1.71V to 3.6V.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the gyro package size down to a footprint and thickness of 3x3x0.9mm (16-pin QFN), to provide a very small yet high performance low cost package. The device provides high robustness by supporting 10,000 *g* shock reliability.

1.4 Applications

- Toys
- Tools
- Industrial

2 Features

The ISZ-2510 MEMS gyroscope includes a wide range of features:

2.1 Sensors

- Monolithic Z- Axis angular rate sensor (gyros) integrated circuit
- Digital-output temperature sensor
- External sync signal connected to the FSYNC pin supports image, video and GPS synchronization
- Factory calibrated scale factor
- High cross-axis isolation via proprietary MEMS design
- 10,000*g* shock tolerant

2.2 Digital Output

- Fast Mode (400kHz) I^2C serial interface
- 1 MHz SPI serial interface for full read/write capability
- 20 MHz SPI to read gyro sensor & temp sensor data.
- 16-bit ADCs for digitizing sensor outputs
- User-programmable full-scale-range of ±250, ±500, ±1000, and ±2000 °/sec

2.3 Data Processing

- The total data set obtained by the device includes gyroscope data, temperature data, and the one bit external sync signal connected to the FSYNC pin.
- FIFO allows burst read, reduces serial bus traffic and saves power on the system processor.
- FIFO can be accessed through both I^2C and SPI interfaces.
- Programmable interrupt
- Programmable low-pass filters

2.4 Clocking

- On-chip timing generator clock frequency ±1% drift over full temperature range

2.5 Power

- VDD supply voltage range of 1.71V to 3.6V
- Flexible VDDIO reference voltage allows for multiple I^2C and SPI interface voltage levels
- Power consumption with both axes active: 2.8mA
- Sleep mode: 8µA
- Each axis can be individually powered down

2.6 Package

- 3x3x0.9mm footprint and maximum thickness 16-pin QFN plastic package
- MEMS structure hermetically sealed at wafer level
- RoHS and Green compliant

3 Electrical Characteristics

3.1 Sensor Specifications

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VDDIO = 1.8V, T_A=25°C.

Parameter	Conditions	Min	Typical	Max	Unit	Notes
GYRO SENSITIVITY						
Full-Scale Range	FS_SEL=0		±250		º/s	
	FS_SEL=1		±500		º/s	
	FS_SEL=2		±1000		º/s	
	FS_SEL=3		±2000		º/s	
Sensitivity Scale Factor	FS_SEL=0		131		LSB/(º/s)	
	FS_SEL=1		65.5		LSB/(º/s)	
	FS_SEL=2		32.8		LSB/(º/s)	
	FS_SEL=3		16.4		LSB/(º/s)	
Gyro ADC Word Length			16		bits	
Sensitivity Scale Factor Tolerance	25°C		±4.5		%	
Sensitivity Scale Factor Variation Over Temperature	-10°C to +75°		±4		%	
Nonlinearity	Best fit straight line; 25°C		±0.2		%	
Cross-Axis Sensitivity			±2		%	
GYRO ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	25°C		±15		º/s	
ZRO Variation Over Temperature	-10°C to +75°C		±15		º/s	
GYRO NOISE PERFORMANCE	**FS_SEL=0**					
Total RMS Noise	DLPFCFG=2 (92 Hz)		0.1		º/s-rms	
Rate Noise Spectral Density	At 10Hz		0.01		º/s/√Hz	
GYRO MECHANICAL						
Mechanical Frequency		25	27	29	kHz	
GYRO START-UP TIME	DLPFCFG=0, to ±1º/s of Final					
ZRO Settling	From Sleep Mode to ready		35		ms	
	From Power On to ready		50		ms	
TEMPERATURE SENSOR						
Range	Untrimmed		-10 to +75		ºC	
Sensitivity			321.4		LSB/ºC	
Room-Temperature Offset	21°C		0		LSB	
Linearity			±0.2		°C	
TEMPERATURE RANGE						
Specification Temperature Range		-10		+75	ºC	

3.2 Electrical Specifications

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VDDIO = 1.8V, T_A = 25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
VDD POWER SUPPLY						
Operating Voltage Range		1.71		3.6	V	
Power-Supply Ramp Rate	Monotonic ramp. Ramp rate is 10% to 90% of the final value	1		100	ms	
Normal Operating Current	Z Axis Active		2.8		mA	
Sleep Mode Current			8		µA	
VDDIO REFERENCE VOLTAGE (must be regulated)						
Voltage Range		1.71		3.6	V	
Power-Supply Ramp Rate	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.1		100	ms	
Normal Operating Current	10pF load, 5MHz data rate. Does not include pull up resistor current draw as that is system dependent		300		µA	
START-UP TIME FOR REGISTER READ/WRITE			12		ms	
I^2C ADDRESS	AD0 = 0 AD0 = 1		1101000 1101001			
DIGITAL INPUTS (FSYNC, AD0, SCLK, SDI, /CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	
C_I, Input Capacitance			< 5		pF	
DIGITAL OUTPUT (INT, SDO)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1MΩ	0.9*VDDIO			V	
V_{OL1}, LOW-Level Output Voltage	R_{LOAD}=1MΩ			0.1*VDDIO	V	
$V_{OL.INT1}$, INT Low-Level Output Voltage	OPEN=1, 0.3mA sink current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t_{INT}, INT Pulse Width	LATCH_INT_EN=0		50		µs	

Note: Power-Supply Ramp Rates are defined as the time it takes for the voltage to rise from 10% to 90% of the final value. VDD and VDDIO must be monotonic ramps.

3.3 Electrical Specifications, continued

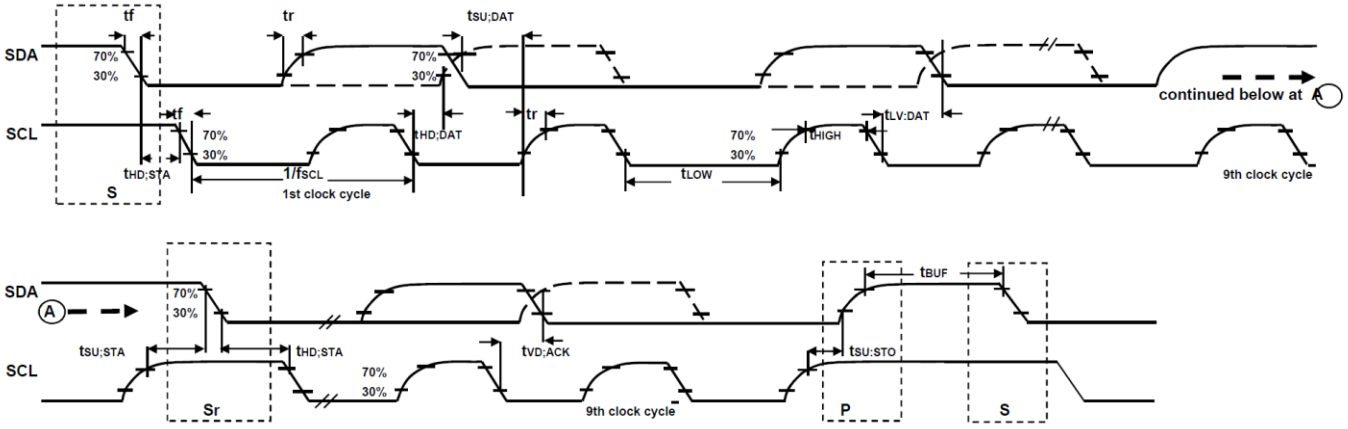
Typical Operating Circuit of Section 4.2, VDD = 2.5V, VDDIO = 1.8V, T_A = 25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
I^2C I/O (SCL, SDA)						
V_{IL}, LOW Level Input Voltage			-0.5V to 0.3*VDDIO		V	
V_{IH}, HIGH-Level Input Voltage			0.7*VDDIO to VDDIO + 0.5V		V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL1}, LOW-Level Output Voltage	3mA sink current		0 to 0.4		V	
I_{OL}, LOW-Level Output Current	V_{OL} = 0.4V V_{OL} = 0.6V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf		20+0.1C_b to 250		ns	
C_I, Capacitance for Each I/O pin			< 10		pF	
INTERNAL CLOCK SOURCE						
	Fchoice=0,1,2 SMPLRT_DIV=0		32		kHz	
Sample Rate	Fchoice=3; DLPFCFG=0 or 7 SMPLRT_DIV=0		8		kHz	
	Fchoice=3; DLPFCFG=1,2,3,4,5,6; SMPLRT_DIV=0		1		kHz	
Clock Frequency Initial Tolerance	CLK_SEL=0, 6; 25°C	-2		+2	%	
	CLK_SEL=1,2,3,4,5; 25°C	-1		+1	%	
Frequency Variation over Temperature	CLK_SEL=0,6		-10 to +10		%	
	CLK_SEL=1,2,3,4,5		±1		%	
PLL Settling Time	CLK_SEL=1,2,3,4,5		4		ms	

3.4 I²C Timing Characterization

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VDDIO = 1.8V, T_A=25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
I²C TIMING	**I²C FAST-MODE**					
f_{SCL}, SCL Clock Frequency		0		400	kHz	
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.6			µs	
t_{LOW}, SCL Low Period		1.3			µs	
t_{HIGH}, SCL High Period		0.6			µs	
$t_{SU.STA}$, Repeated START Condition Setup Time		0.6			µs	
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	
$t_{SU.DAT}$, SDA Data Setup Time		100			ns	
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400pF	20+0.1 C_b		300	ns	
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400pF	20+0.1 C_b		300	ns	
$t_{SU.STO}$, STOP Condition Setup Time		0.6			µs	
t_{BUF}, Bus Free Time Between STOP and START Condition		1.3			µs	
C_b, Capacitive Load for each Bus Line			< 400		pF	
$t_{VD.DAT}$, Data Valid Time				0.9	µs	
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.9	µs	



I²C Bus Timing Diagram

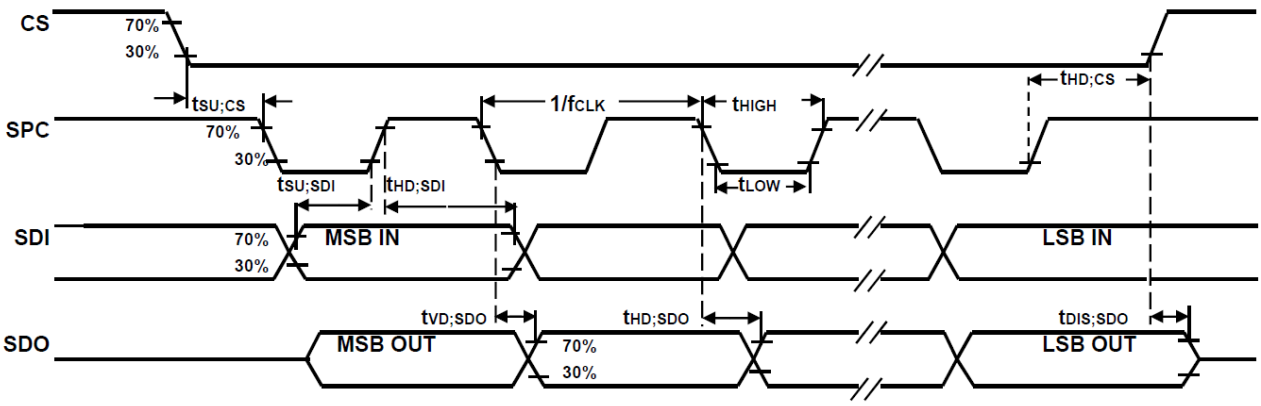
3.5 SPI Timing Characterization

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VDDIO = 1.8V, T_A = 25°C,

Parameters	Conditions	Min	Typical	Max	Units
SPI TIMING					
f_{SCLK}, SCLK Clock Frequency				1[1]	MHz
				20[2]	MHz
t_{LOW}, SCLK Low Period		400			ns
t_{HIGH}, SCLK High Period		400			ns
$t_{SU.CS}$, CS Setup Time		8			ns
$t_{HD.CS}$, CS Hold Time		500			ns
$t_{SU.SDI}$, SDI Setup Time		11			ns
$t_{HD.SDI}$, SDI Hold Time		7			ns
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20pF			100	ns
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 20pF	4			ns
$t_{DIS.SDO}$, SDO Output Disable Time				10	ns

Notes:

1. R/W of all Registers
2. Read of Sensor Registers only



SPI Bus Timing Diagram

3.6 Absolute Maximum Ratings

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

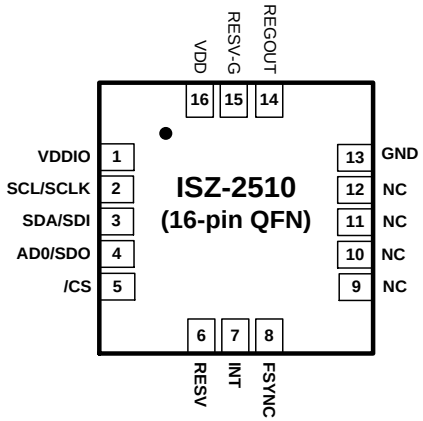
Absolute Maximum Ratings

Parameter	Rating
Supply Voltage, VDD	-0.5V to +4.0V
VDDIO Input Voltage Level	-0.5V to 4.0V
REGOUT	-0.5V to 2V
Input Voltage Level (AD0, FSYNC)	-0.5V to VDD
SCL, SDA, INT (SPI enable)	-0.5V to VDD
SCL, SDA, INT (SPI disable)	-0.5V to VDD
Acceleration (Any Axis, unpowered)	10,000*g* for 0.2ms
Operating Temperature Range	-40°C to +85°
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2kV (HBM); 200V (MM)
Latch-up	JEDEC Class II (2),125°C, ±100mA

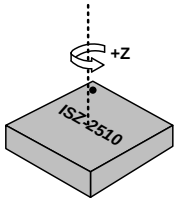
4 Applications Information

4.1 Pin Out and Signal Description

Pin Number 3x3x0.9mm	Pin Name	Pin Description
1	VDDIO	Digital I/O supply voltage
2	SCL/SCLK	I^2C serial clock (SCL); SPI serial clock (SCLK)
3	SDA/SDI	I^2C serial data (SDA); SPI serial data input (SDI)
4	AD0 / SDO	I^2C Slave Address LSB (AD0); SPI serial data output (SDO)
5	/CS	SPI chip select (0=SPI mode, 1= I^2C mode)
6	RESV	Reserved. Connect to Ground.
7	INT	Interrupt digital output (totem pole or open-drain)
8	FSYNC	Frame synchronization digital input. Connect to GND if not used.
13	GND	Power supply ground
14	REGOUT	Regulator filter capacitor connection
15	RESV-G	Reserved. Connect to Ground.
16	VDD	Power supply voltage
9, 10, 11, 12	NC	Not internally connected. May be used for PCB trace routing.

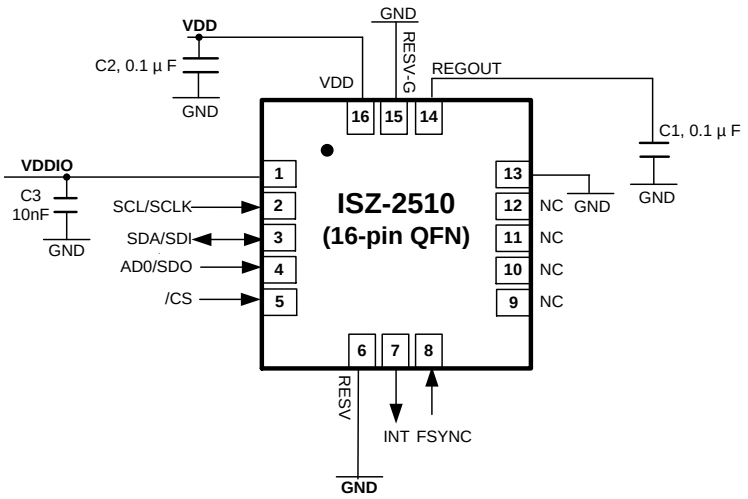


QFN Package (Top View)
16-pin, 3mm x 3mm x 0.90mm
Footprint and maximum thickness



Orientation of Axes of Sensitivity and Polarity of Rotation

4.2 Typical Operating Circuit



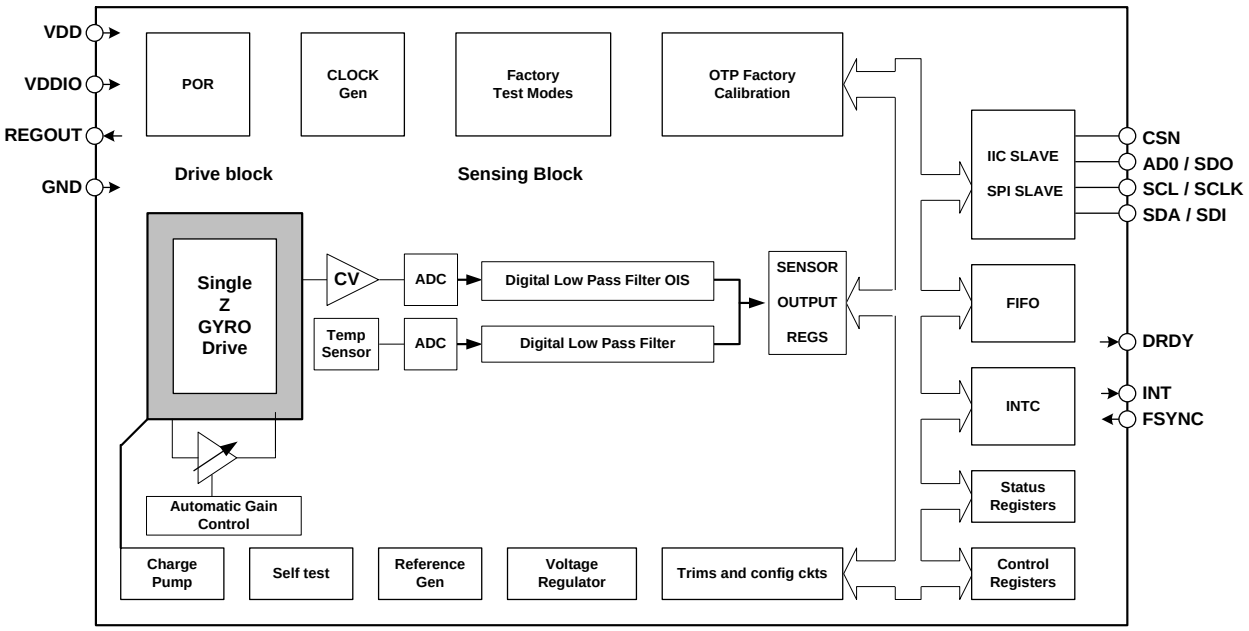
Typical Operating Circuit

4.3 Bill of Materials for External Components

Component	Label	Specification	Quantity
Regulator Filter Capacitor	C1	Ceramic, X7R, 0.1µF ±10%, 2V	1
VDD Bypass Capacitor	C2	Ceramic, X7R, 0.1µF ±10%, 4V	1
VDDIO Bypass Capacitor	C3	Ceramic, X7R, 10nF ±10%, 4V	1

5 Functional Overview

5.1 Block Diagram



5.2 Overview

The ISZ-2510 is comprised of the following key blocks / functions:

- Single-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- I^2C and SPI serial communications interfaces
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDO

5.3 Single-Axis MEMS Gyroscope with 16-bit ADCs and Signal Conditioning

The ISZ-2510 consists of a single structure vibratory MEMS rate gyroscope, which detects rotation about the Z axis. When the gyro is rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pick off. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The chip features a programmable full-scale range of the gyro sensors of ±250, ±500, ±1000, and ±2000 dps. User-selectable low-pass filters enable a wide range of cut-off frequencies. The ADC sample rate can be programmed to 32 kHz, 8 kHz, 1 kHz, 500 Hz, 333.3 Hz, 250 Hz, 200 Hz, 166.7 Hz, 142.9 Hz, or 125 Hz.

5.4 I^2C and SPI Serial Communications Interface

The ISZ-2510 has both I^2C and SPI serial interfaces. The device always acts as a slave when communicating to the system processor. The logic level for communications to the master is set by the voltage on the VDDIO pin. The LSB of the of the I^2C slave address is set by the AD0 pin. The I^2C and SPI protocols are described in more detail in Section 6.

5.5 Internal Clock Generation

The ISZ-2510 has a flexible clocking scheme, allowing for a variety of internal clock sources for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, various control circuits, and registers.

Allowable internal sources for generating the internal clock are:

- An internal relaxation oscillator
- PLL (gyroscope based clock)

In order for the gyroscope to perform to spec, the PLL must be selected as the clock source. When the internal 20MHz oscillator is chosen as the clock source, the device can operate while having the gyroscopes disabled. However, this is only recommended if the user wishes to use the internal temperature sensor in this mode.

5.6 Sensor Data Registers

The sensor data registers contain the latest gyro and temperature data. They are read-only registers, and are accessed via the Serial Interface. Data from these registers may be read anytime, however, the interrupt function may be used to determine when new data is available.

5.7 FIFO

The ISZ-2510 contains a 512-byte FIFO register that is accessible via the both the I^2C and SPI Serial Interfaces. The FIFO configuration register determines what data goes into it, with possible choices being gyro data, temperature readings and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.

5.8 Interrupts

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources), (2) new data is available to be read (from the FIFO and Data registers), and (3) FIFO overflow. The interrupt status can be read from the Interrupt Status register.

5.9 Digital-Output Temperature Sensor

An on-chip temperature sensor and ADC are used to measure the device's die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

5.10 Bias and LDO

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ISZ-2510. Its two inputs are unregulated VDD of 1.71V to 3.6V and a VDDIO logic reference supply voltage of 1.71V to 3.6V. The LDO output is bypassed by a 0.1µF capacitor at REGOUT.

6 Digital Interface

6.1 I²C Serial Interface

The internal registers and memory of the ISZ-2510 can be accessed using the I²C interface.

Serial Interface

Pin Number	Pin Name	Pin Description
1	VDDIO	Digital I/O supply voltage.
4	AD0 / SDO	I²C Slave Address LSB (AD0); SPI serial data output (SDO)
2	SCL / SCLK	I²C serial clock (SCL); SPI serial clock (SCLK)
3	SDA / SDI	I²C serial data (SDA); SPI serial data input (SDI)

6.1.1 I²C Interface

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ISZ-2510 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

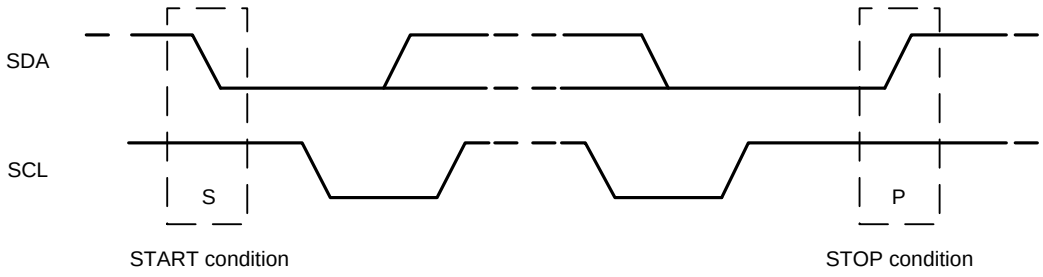
The slave address of the device is b110100X which is 7 bits long. The LSB bit of the 7 bit address is determined by the logic level on pin AD0. This allows two ISZ-2510 devices to be connected to the same I²C bus. When used in this configuration, the address of the one of the devices should be b1101000 (pin AD0 is logic low) and the address of the other should be b1101001 (pin AD0 is logic high). The I²C address is stored in WHO_AM_I register.

I²C Communications Protocol

START (S) and STOP (P) Conditions

Communication on the I²C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

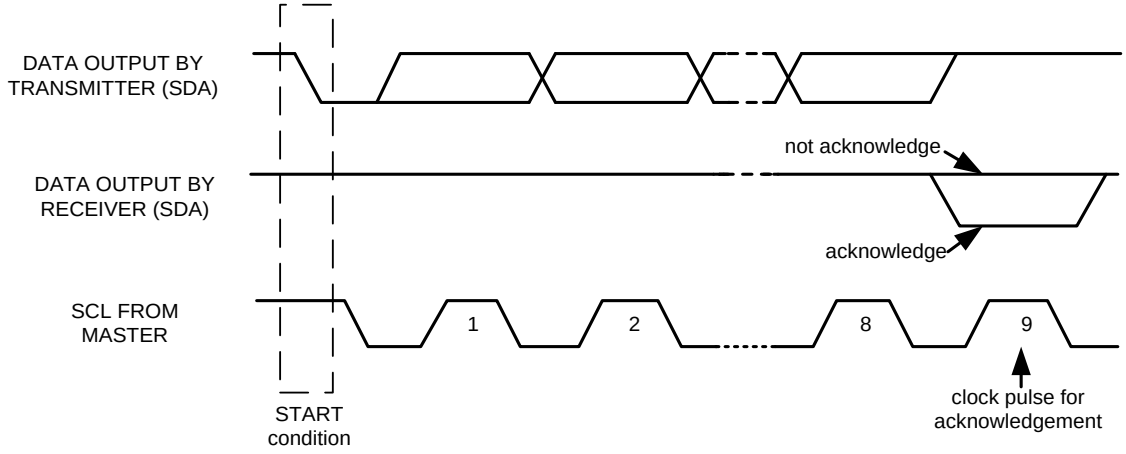


START and STOP Conditions

Data Format / Acknowledge

I²C data bytes are defined to be 8 bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

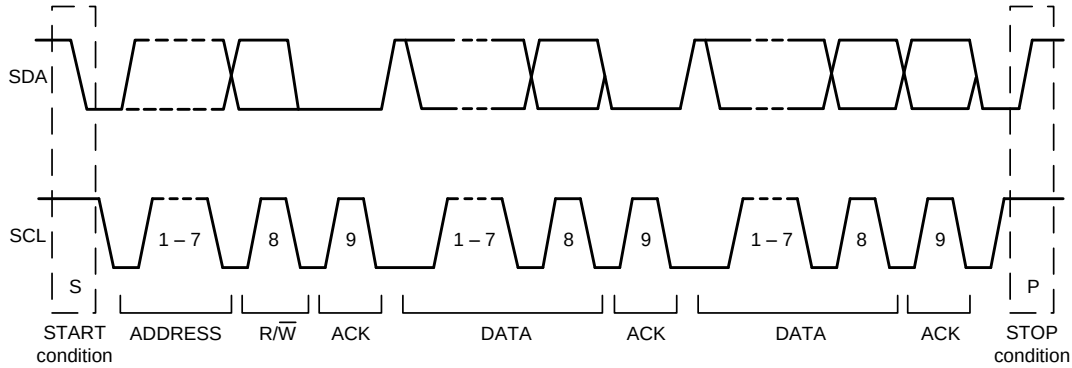
If a slave is busy and is unable to transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).



Acknowledge on the I²C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.



Complete I²C Data Transfer

To write the internal ISZ-2510 registers, the master transmits the start condition (S), followed by the I^2C address and the write bit (0). At the 9th clock cycle (when the clock is high), the device acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the device acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the device automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

Single-Byte Write Sequence

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

Burst Write Sequence

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal device registers, the master sends a start condition, followed by the I^2C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the device, the master transmits a start signal followed by the slave address and read bit. As a result, the device sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9th clock cycle. The following figures show single and two-byte read sequences.

Single-Byte Read Sequence

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Burst Read Sequence

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

I²C Terms

Signal	Description
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I²C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9th clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9th clock cycle
RA	The internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

6.1.2 SPI interface

SPI is a 4-wire synchronous serial interface that uses two control and two data lines. The ISZ-2510 always operates as a Slave device during standard Master-Slave SPI operation. With respect to the Master, the Serial Clock output (SCLK), the Data Output (SDO) and the Data Input (SDI) are shared among the Slave devices. The Master generates an independent Chip Select (/CS) for each Slave device; /CS goes low at the start of transmission and goes back high at the end. The Serial Data Output (SDO) line, remains in a high-impedance (high-z) state when the device is not selected, so it does not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. SCLK frequency is 1MHz max for SPI in full read/write capability mode. When the SPI frequency is set to 20MHz, its operation is limited to reading sensor registers only.
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Read/Writes, data is two or more bytes:

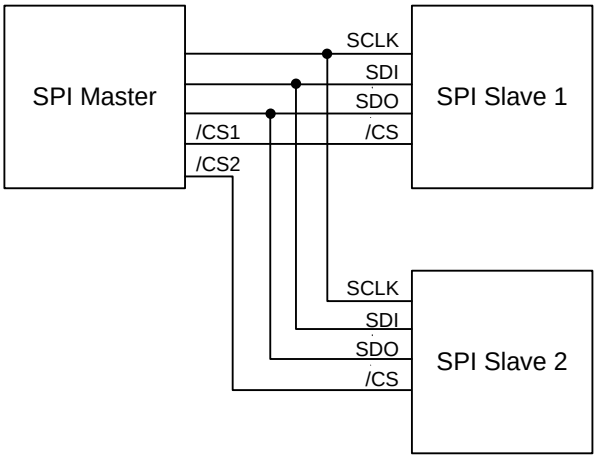
SPI Address format

MSB							LSB
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.



Typical SPI Master / Slave Configuration

Each SPI slave requires its own Chip Select (/CS) line. SDO, SDI and SCLK lines are shared. Only one /CS line is active (low) at a time ensuring that only one slave is selected at a time. The /CS lines of other slaves are held high which causes their respective SDO pins to be high-Z.

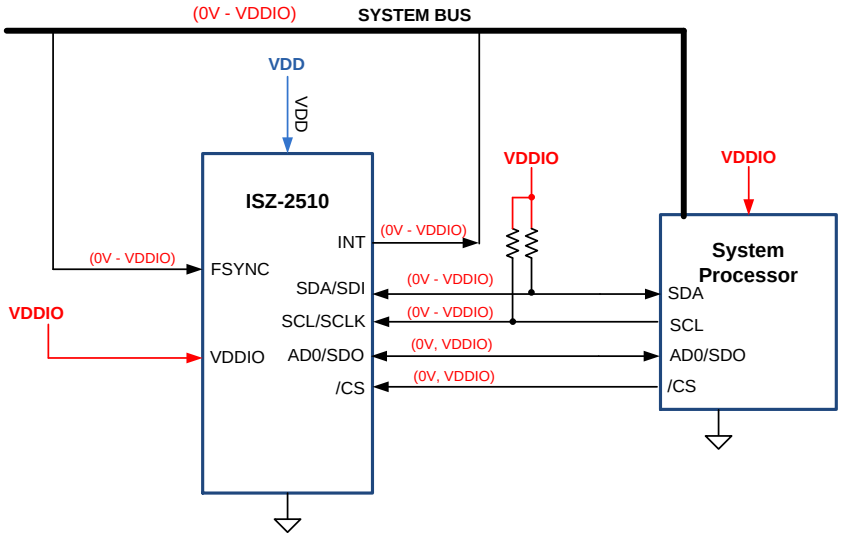
7 Serial Interface Considerations

7.1 Supported Interfaces

The ISZ-2510 supports I^2C and SPI communication.

7.2 Logic Levels

The I/O logic levels are set to VDDIO. VDDIO may be set to be equal to VDD or to another voltage, such that it is between 1.71 V and 3.6V at all times. Both I^2C and SPI communication support VDDIO.



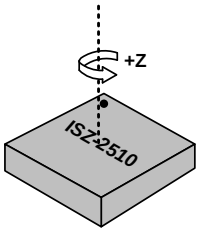
8 Assembly

This section provides general guidelines for assembling InvenSense Micro Electro-Mechanical Systems (MEMS) gyros packaged in Quad Flat No leads package (QFN) surface mount integrated circuits.

This preliminary datasheet only provides limited information with respect to ISZ-2510 Assembly. Additional information will be supplied in subsequent versions of the document.

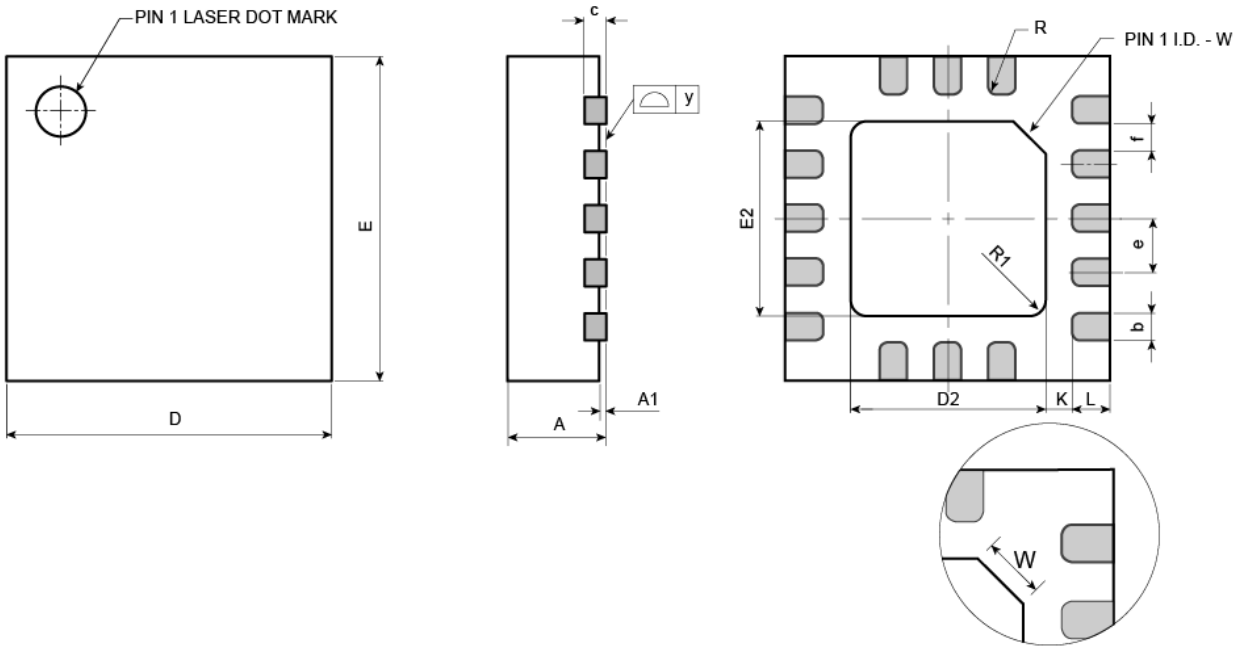
8.1 Orientation of Axes

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier in the figure.



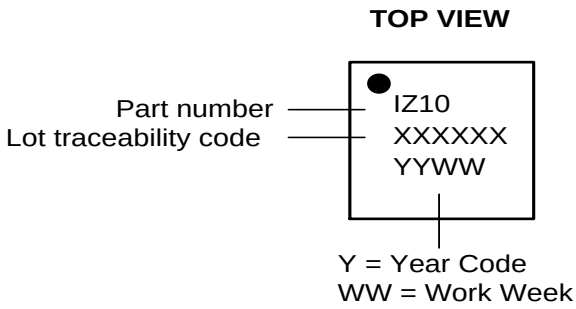
Orientation of Axes of Sensitivity and Polarity of Rotation

8.2 Package Dimensions



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.85	0.90	0.95
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	---	0.20 REF	---
D	2.90	3.00	3.10
D2	1.75	1.80	1.85
E	2.90	3.00	3.10
E2	1.75	1.80	1.85
e	---	0.50	---
f (e-b)			
K	---	0.25 REF	---
L	0.30	0.35	0.40
R	0.08	REF.	---
R1	---	0.15	---
W	---	0.30	---
y	0.00	---	0.075

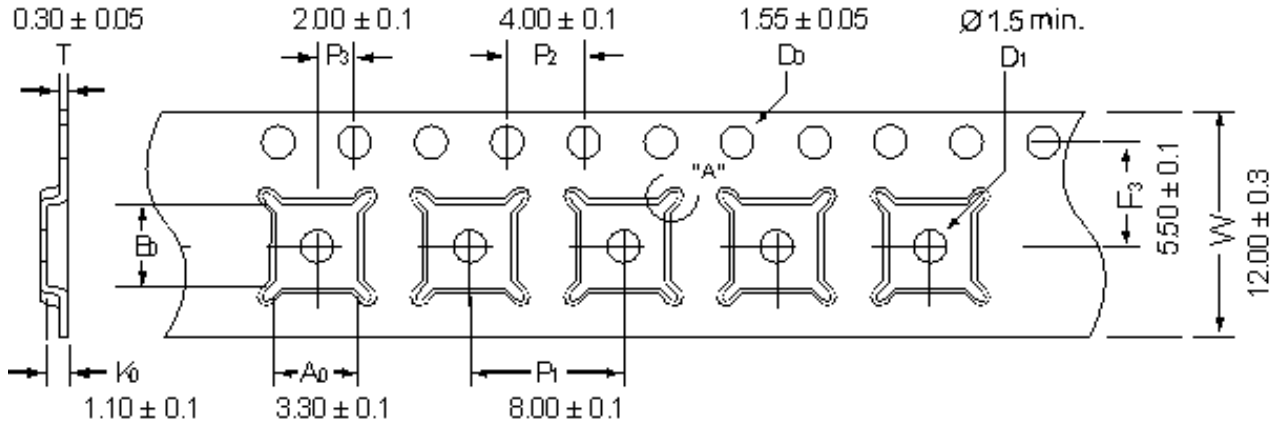
8.3 Package Marking Specification

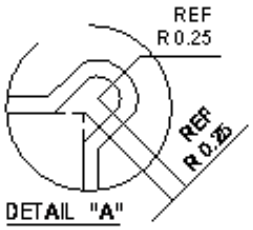


Part number:

Product	Top Mark
ISZ-2510	IZ10

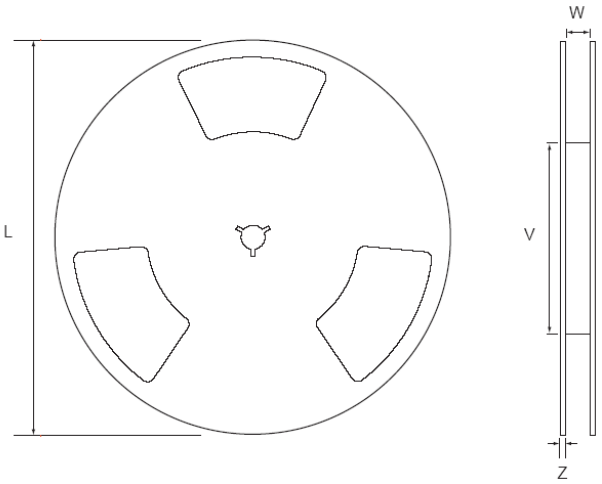
8.4 Tape & Reel Specification





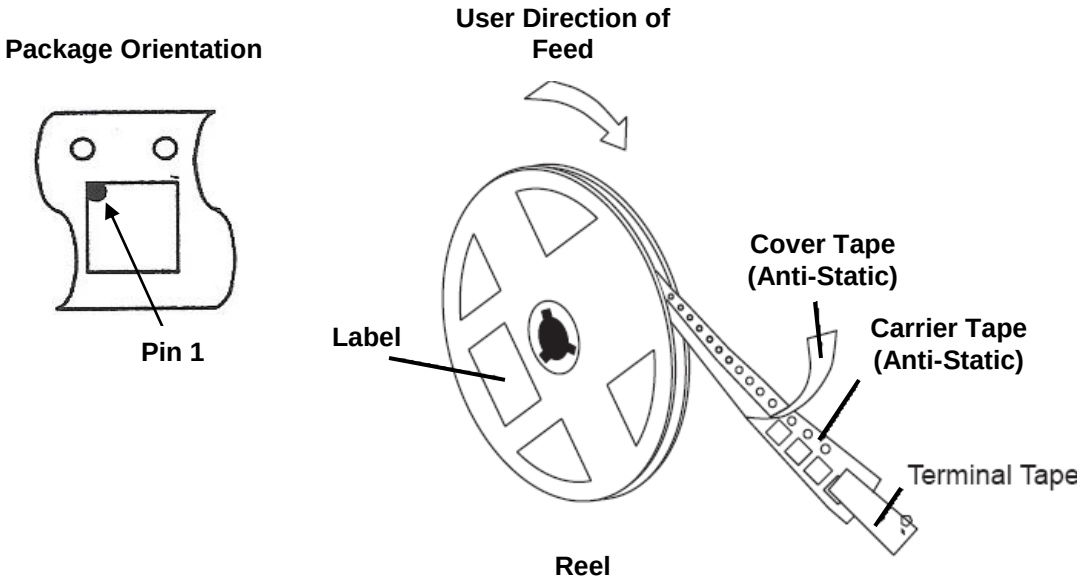
(1) Measured from centerline of pocket to centerline of pocket.
(2) Cummulative tolerance of 10 sprocket holes is ± 0.20
(3) Measured from centerline of sprocket hole to centerline of pocket

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED



Reel Dimensions and Package Size

PKG SIZE	REEL (mm)			
	L	V	W	Z
3x3	330	102	12.8	2.3



Tape and Reel Specification

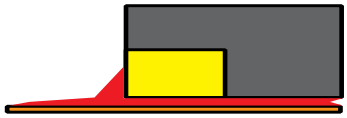
Reel Specifications

Quantity Per Reel	5,000
Reels per Pizza Box	1
Pizza Boxes Per Carton (max)	5
Pcs/Carton (max)	25,000

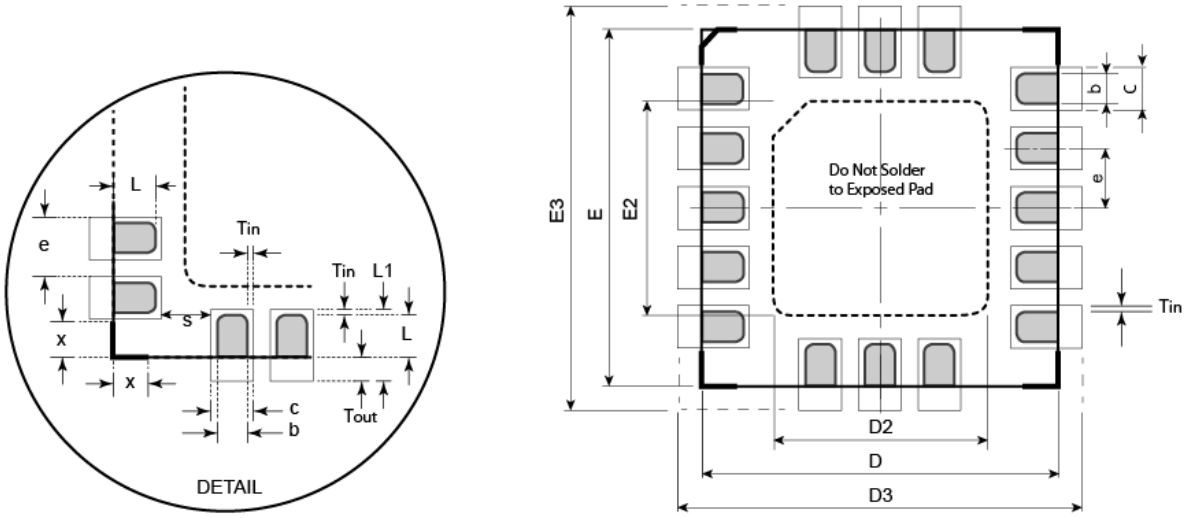
Note: empty pizza boxes are included to ensure that pizza boxes don't shift.

8.5 PCB Design Guidelines

The Pad Diagram using a JEDEC type extension with solder rising on the outer edge is shown below. The Pad Dimensions Table shows pad sizing (mean dimensions) recommended for the product.



JEDEC type extension with solder rising on outer edge



SYMBOLS	DIMENSIONS IN MILLIMETERS	NOM
Nominal Package I/O Pad Dimensions		
e	Lead Finger (Pad) Pitch, (Land Pitch)	0.50
b	Lead Finger (Pad) Width	0.25
L	Lead Finger (Pad) Length	0.35
D	Package Width	3.00
E	Package Length	3.00
D2	Exposed Pad Width	1.80
E2	Exposed Pad Length	1.80
I/O Land Design Dimensions (Guidelines)		
D3	PCB Land Extent Width	3.70
E3	PCB Land Extent Length	3.70
c	PCB Land Width	0.30
Tout	Outward Extension (Land beyond Pad)	0.35
Tin	Inward Extension (Land beyond Pad)	0.05
L1	Land Length	0.75
x	Silkscreen Corner Marker Length	0.30

9 Register Map

The register map listed below covers all the 1, 2 and 3 axis members of the family. Please note that the register values are relevant per specific part number.

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
04	04	XG_OFFS_TC_H	R/W	-	-	-	-	-	-	XG_OFFS_TC_H [9]	XG_OFFS_TC_H [8]
05	05	XG_OFFS_TC_L	R/W	XG_OFFS_TC_L [7:0]							
07	07	YG_OFFS_TC_H	R/W	-	-	-	-	-	-	YG_OFFS_TC_H [9]	YG_OFFS_TC_H [8]
08	08	YG_OFFS_TC_L	R/W	YG_OFFS_TC_L [7:0]							
0A	10	ZG_OFFS_TC_H	R/W	-	-	-	-	-	-	ZG_OFFS_TC_H [9]	ZG_OFFS_TC_H [8]
0B	11	ZG_OFFS_TC_L	R/W	ZG_OFFS_TC_L [7:0]							
13	19	XG_OFFS_USRH	R/W	X_OFFS_USR[15:8]							
14	20	XG_OFFS_USRL	R/W	X_OFFS_USR[7:0]							
15	21	YG_OFFS_USRH	R/W	Y_OFFS_USR[15:8]							
16	22	YG_OFFS_USRL	R/W	Y_OFFS_USR[7:0]							
17	23	ZG_OFFS_USRH	R/W	Z_OFFS_USR[15:8]							
18	24	G_OFFS_USRL	R/W	Z_OFFS_USR[7:0]							
19	25	SMPLRT_DIV	R/W	SMPLRT_DIV[7:0]							
1A	26	CONFIG	R/W	-	FIFO _MODE	EXT_SYNC_SET[2:0]			DLPF_CFG[2:0]		
1B	27	GYRO_CONFIG	R/W	XG_ST	YG_ST	ZG_ST	FS_SEL [1:0]		-	FCHOICE_B[1:0]	
23	35	FIFO_EN	R/W	TEMP _FIFO_EN	XG _FIFO_EN	YG _FIFO_EN	ZG _FIFO_EN	-	-	-	-
37	55	INT_PIN_CFG	R/W	INT_LEVEL	INT_OPEN	LATCH _INT_EN	INT_RD _CLEAR	FSYNC_ INT_LEVEL	FSYNC _INT _MODE_EN	-	-
38	56	INT_ENABLE	R/W	-	-	-	FIFO _OFLOW _EN	FSYNC_INT _EN	-	-	DATA _RDY_EN
3A	58	INT_STATUS	R	-	-	-	FIFO _OFLOW _INT	FSYNC_INT	-	-	DATA _RDY_INT
41	65	TEMP_OUT_H	R	TEMP_OUT[15:8]							
42	66	TEMP_OUT_L	R	TEMP_OUT[7:0]							
43	67	GYRO_XOUT_H	R	GYRO_XOUT[15:8]							
44	68	GYRO_XOUT_L	R	GYRO_XOUT[7:0]							
45	69	GYRO_YOUT_H	R	GYRO_YOUT[15:8]							
46	70	GYRO_YOUT_L	R	GYRO_YOUT[7:0]							
47	71	GYRO_ZOUT_H	R	GYRO_ZOUT[15:8]							
48	72	GYRO_ZOUT_L	R	GYRO_ZOUT[7:0]							
6A	106	USER_CTRL	R/W	-	FIFO_EN	-	I2C_IF _DIS	-	FIFO _RESET	-	SIG_COND _RESET
6B	107	PWR_MGMT_1	R/W	DEVICE _RESET	SLEEP	-	-	TEMP_DIS	CLKSEL[2:0]		
6C	108	PWR_MGMT_2	R/W	-		-	-	-	STBY_XG	STBY_YG	STBY_ZG
72	114	FIFO_COUNTH	R/W	-	-	-	-	-	-	FIFO_COUNT[9:8]	
73	115	FIFO_COUNTL	R/W	FIFO_COUNT[7:0]							
74	116	FIFO_R_W	R/W	FIFO_DATA[7:0]							
75	117	WHO_AM_I	R	-	WHO_AM_I[6:1]						-

Note: Register Names ending in _H and _L contain the high and low bytes, respectively, of an internal register value.

In the detailed register tables that follow, register names are in capital letters, while register values are in capital letters and italicized. For example, the GYRO_XOUT_H register (Register 67) contains the 8 most significant bits, *GYRO_XOUT*[15:8], of the 16-bit X-Axis gyroscope measurement, *GYRO_XOUT*.

The reset value is 0x00 for all registers other than the WHO_AM_I register (Register 117), which resets to 0x68.

10 Register Descriptions

This section describes the function and contents of each register.

Note: The device will come up in full power mode upon power-up. (i.e. not sleep mode)

10.1 Registers 04-05, 07-08, 10-11- Gyroscope offset Temperature Compensation (TC)

XG_OFFS_TC_H, XG_OFFS_TC_L, YG_OFFS_TC_H, YG_OFFS_TC_L, ZG_OFFS_TC_H, and ZG_OFFS_TC_L

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
04	04							XG_OFFS_TC_H [9]	XG_OFFS_TC_H [8]
05	05	XG_OFFS_TC_L [7:0]							
07	07							YG_OFFS_TC_H [9]	YG_OFFS_TC_H [8]
08	08	YG_OFFS_TC_L [7:0]							
0A	10							ZG_OFFS_TC_H [9]	ZG_OFFS_TC_H [8]
0B	11	ZG_OFFS_TC_L [7:0]							

Description:

The temperature compensation (TC) registers are used to reduce gyro offset variation due to temperature change. The TC feature is always enabled. However the compensation only happens when a non-zero TC coefficient is programed during factory trim which gets loaded into these registers at power up or after a *DEVICE_RESET*. If these registers contain a value of zero, temperature compensation has no effect on the offset of the chip. The TC registers are 10-bit signed values in 2's complement format with a resolution of 2.52 mdps/C steps.

If these registers contain a non-zero value after power up, the user may write zeroes to them to see the offset values without TC with temperature variation. Note that doing so may result in offset values that exceed data sheet "Initial ZRO Tolerance" in other than normal ambient temperature (~21 °C). The TC coefficients maybe restored by the user with a power up or a *DEVICE_RESET*.

Parameters:

XG_OFFS_TC_H/L: 10-bit offset of X gyroscope (2's complement)
YG_OFFS_TC_H/L: 10-bit offset of Y gyroscope (2's complement)
ZG_OFFS_TC_H/L: 10-bit offset of Z gyroscope (2's complement)

10.2 Registers 19 to 24 – Gyroscope offset adjustment

XG_OFFS_USRH, XG_OFFS_USRL, YG_OFFS_USRH, YG_OFFS_USRL, ZG_OFFS_USRH, and ZG_OFFS_USRL

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
13	19	X_OFFS_USR[15:8]							
14	20	X_OFFS_USR[7:0]							
15	21	Y_OFFS_USR[15:8]							
16	22	Y_OFFS_USR[7:0]							

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
17	23	Z_OFFS_USR[15:8]							
18	24	Z_OFFS_USR[7:0]							

Description:
These registers are used to remove DC bias from the sensor outputs. The values in these registers are subtracted from the gyroscope sensor values before going into the sensor registers (see registers 67 to 72).
Parameters:
XG_OFFS_USR_H/L: 16-bit offset of X gyroscope (2's complement)
YG_OFFS_USR_H/L: 16-bit offset of Y gyroscope (2's complement)
ZG_OFFS_USR_H/L: 16-bit offset of Z gyroscope (2's complement)

10.3 Register 25 – Sample Rate Divider

SMPRT_DIV
Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
19	25	SMPLRT_DIV[7:0]							

Description:
This register specifies the divider from the gyroscope output rate that can be used to generate a reduced Sample Rate. Please note that this register is only effective when *FCHOICE_B*[1:0] = 2'b00 (Register 27) and *DLPF_CFG* = 1, 2, 3, 4, 5, or 6 (Register 26).
When *FCOICE_B*[1:0] = 2'b00 but *DLPF_CFG* = 0 or 7, the Sample Rate is fixed at 8kHz and the divider in this register does not apply. When *FCHOICE_B*[1:0] = 2'b01, 2'b10, or 2'b11, the Sample Rate is fixed at 32kHz and the divider in this register does not apply.
The sensor register output and FIFO output are both based on the Sample Rate.
When this register is effective under the *FCOICE_B* and *DLPF_CFG* settings, the reduced Sample Rate is generated by the formula below:

Sample Rate = Gyroscope Output Rate / (1 + *SMPLRT_DIV*)

Where Gyroscope Output Rate = 1kHz.

Parameters:

SMPLRT_DIV 8-bit unsigned value. The Sample Rate is determined by dividing the gyroscope output rate by this value.

10.4 Register 26 – Configuration

CONFIG
Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1A	26	-	FIFO_MODE	EXT_SYNC_SET[2:0]			DLPF_CFG[2:0]		

Description:
This register configures the FIFO's mode of operation, the external Frame Synchronization (FSYNC) pin sampling and the Digital Low Pass Filter (DLPF) setting. Please note that the DLPF can only be used when *FCHOICE_B*[1:0] =2b'00 (Register 27).
When *FIFO_MODE* is set to 1 and the FIFO is full, additional writes will not be written to the FIFO. When this bit is equal to 0 and the FIFO is full, additional writes will be written to the FIFO, replacing the oldest data. In order to enable and disable writing to the FIFO, use the enable bits in Register 35. For further information regarding the FIFO's operation, please refer to Register 116.
An external signal connected to the FSYNC pin can be sampled by configuring *EXT_SYNC_SET*. Signal changes to the FSYNC pin are latched so that short strobes may be captured. The latched

FSYNC signal will be sampled at the Sampling Rate, as defined in register 25. After sampling, the latch will reset to the current FSYNC signal state.
The sampled value will be reported in place of the least significant bit in a sensor data register determined by the value of *EXT_SYNC_SET* according to the following table.

EXT_SYNC_SET	FSYNC Bit Location
0	Input disabled
1	TEMP_OUT_L[0]
2	GYRO_XOUT_L[0]
3	GYRO_YOUT_L[0]
4	GYRO_ZOUT_L[0]

The DLPF is configured by *DLPF_CFG,* when *FCHOICE_B*[1:0] = 2b'00. The gyroscope and temperature sensor are filtered according to the value of *DLPF_CFG* and *FCHOICE_B* as shown in the table below.

FCHOICE_B		DLPF_CFG	Gyroscope			Temperature Sensor	
<1>	<0>		Bandwidth (Hz)	Delay (ms)	Fs (kHz)	Bandwidth (Hz)	Delay (ms)
0	0	0	250	0.97	8	4000	0.04
0	0	1	184	2.9	1	188	1.9
0	0	2	92	3.9	1	98	2.8
0	0	3	41	5.9	1	42	4.8
0	0	4	20	9.9	1	20	8.3
0	0	5	10	17.85	1	10	13.4
0	0	6	5	33.48	1	5	18.6
0	0	7	3600	0.17	8	4000	0.04
x	1	x	8800	0.064	32	4000	0.04
1	0	x	3600	0.11	32	4000	0.04

Bit 7 is reserved.

Parameters:

FIFO_MODE When set to 1 and the FIFO is full, additional writes will not be written to the FIFO.
When equal to 0 and the FIFO is full, additional writes will be written to the FIFO, replacing the oldest data.
In order to disable writing to the FIFO, use the enable bits in Register 35.

EXT_SYNC_SET 3-bit unsigned value. Configures the FSYNC pin sampling.

DLPF_CFG 3-bit unsigned value. Configures the DLPF setting.

10.5 Register 27 – Gyroscope Configuration

GYRO_CONFIG

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1B	27	XG_ST	YG_ST	ZG_ST	FS_SEL[1:0]		-	FCHOICE_B[1:0]	

Description:

This register is used to trigger gyroscope self test and configure the gyroscopes' full scale range. Gyroscope self-test permits users to test the mechanical and electrical portions of the gyroscope. When self-test is activated by setting XG_ST, YG_ST, ZG_ST bits in register 27, the on-board electronics will actuate the appropriate sensor. This actuation will move the sensor's proof masses over a distance equivalent to a pre-defined Coriolis force. This proof mass displacement results in a change in the sensor output, which is reflected in the output signal. The output signal is used to observe the self-test response. The self-test response (STR) is stored in the sensor data output

registers 67 – 72. This self-test-response is used to determine whether the part has passed or failed self-test
This self-test response must be within the limits provided in product specification document for the part to pass self-test. Otherwise, the part is deemed to have failed self-test.
FS_SEL selects the full scale range of the gyroscope outputs according to the following table.

FS_SEL	Full Scale Range
0	± 250 °/s
1	± 500 °/s
2	± 1000 °/s
3	± 2000 °/s

FCHOICE_B, in conjunction with *DLPF_CFG* (Register 26), is used to choose the gyroscope output setting. For further information regarding the operation of *FCHOICE_B*, please refer to Section 4.2.
Bit 2 is reserved.

Parameters:

XG_ST	Setting this bit causes the X axis gyroscope to perform self test.
YG_ST	Setting this bit causes the Y axis gyroscope to perform self test.
ZG_ST	Setting this bit causes the Z axis gyroscope to perform self test.
FS_SEL	2-bit unsigned value. Selects the full scale range of gyroscopes.
FCHOICE_B	2-bit unsigned value used to choose the gyroscope output setting.

10.6 Register 35 – FIFO Enable

FIFO_EN

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
23	35	TEMP_ FIFO_EN	XG_ FIFO_EN	YG_ FIFO_EN	ZG_ FIFO_EN	-	-	-	-

Description:

This register determines which sensor measurements are loaded into the FIFO buffer.
Data stored inside the sensor data registers (Registers 65 to 72) will be loaded into the FIFO buffer if a sensor's respective FIFO_EN bit is set to 1 in this register. The behavior of FIFO writes when the FIFO buffer is full can be configured with the *FIFO_MODE* bit (Register 26). In order to read the data in the FIFO buffer, the *FIFO_EN* bit (Register 106) must be enabled.
When a sensor's FIFO_EN bit is enabled in this register, data from the sensor data registers will be loaded into the FIFO buffer. The sensors are sampled at the Sample Rate as defined in Register 25.
For further information regarding sensor data registers, please refer to Registers 65 to 72
Bits 3 through 0 are reserved.

Parameters:

TEMP_FIFO_EN	When set to 1, this bit enables TEMP_OUT_H and TEMP_OUT_L (Registers 65 and 66) to be written into the FIFO buffer.
XG_ FIFO_EN	When set to 1, this bit enables GYRO_XOUT_H and GYRO_XOUT_L (Registers 67 and 68) to be written into the FIFO buffer.
YG_ FIFO_EN	When set to 1, this bit enables GYRO_YOUT_H and GYRO_YOUT_L (Registers 69 and 70) to be written into the FIFO buffer.
ZG_ FIFO_EN	When set to 1, this bit enables GYRO_ZOUT_H and GYRO_ZOUT_L (Registers 71 and 72) to be written into the FIFO buffer.

10.7 Register 55 – INT Pin / Bypass Enable Configuration

INT_PIN_CFG

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
37	55	INT_LEVEL	INT_OPEN	LATCH _INT_EN	INT_RD _CLEAR	FSYNC_ INT_LEVEL	FSYNC _INT_ MODE_EN	-	-

Description:

This register configures the behavior of the interrupt signals at the INT pins. This register is also used to enable the FSYNC Pin to be used as an interrupt to the host application processor.
Bits 1 and 0 are reserved.

Parameters:

INT_LEVEL
When this bit is equal to 0, the logic level for the INT pin is active high.
When this bit is equal to 1, the logic level for the INT pin is active low.

INT_OPEN
When this bit is equal to 0, the INT pin is configured as push-pull.
When this bit is equal to 1, the INT pin is configured as open drain.

LATCH_INT_EN
When this bit is equal to 0, the INT pin emits a 50us long pulse.
When this bit is equal to 1, the INT pin is held high until the interrupt is cleared.

INT_RD_CLEAR
When this bit is equal to 0, interrupt status bits are cleared only by reading INT_STATUS (Register 58)
When this bit is equal to 1, interrupt status bits are cleared on any read operation.

FSYNC_INT_LEVEL
When this bit is equal to 0, the logic level for the FSYNC pin (when used as an interrupt to the host processor) is active high.
When this bit is equal to 1, the logic level for the FSYNC pin (when used as an interrupt to the host processor) is active low.

FSYNC_INT_MODE_EN
When this bit is equal to 1, the FSYNC pin will trigger an interrupt when it transitions to the level specified by *FSYNC_INT_LEVEL*. When a FSYNC interrupt is triggered, the *FSYNC_INT* bit in Register 58 will be set to 1. An interrupt is sent to the host processor if the FSYNC interrupt is enabled by the *FSYNC_INT_EN* bit in Register 56.
When this bit is equal to 0, the FSYNC pin is disabled from causing an interrupt.

10.8 Register 56 – Interrupt Enable

INT_ENABLE

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
38	56	-	-	-	FIFO _OFLOW _EN	FSYNC _INT_EN	-	-	DATA _RDY_EN

Description:

This register enables interrupt generation by interrupt sources.
For information regarding the interrupt status for of each interrupt generation source, please refer to Register 58.
Bits 7 through 5, 2, and 1 are reserved.

Parameters:

FIFO_OFLOW_EN When set to 1, this bit enables a FIFO buffer overflow to generate an interrupt.

FSYNC_INT_EN When equal to 0, this bit disables the FSYNC pin from causing an interrupt to the host processor.
When set to 1, this bit enables the FSYNC pin to be used as an interrupt to the host processor.

DATA_RDY_EN When set to 1, this bit enables the Data Ready interrupt. The Data Ready interrupt is triggered when all the sensor registers have been written with the latest gyro sensor data.

10.9 Register 58 – Interrupt Status

INT_STATUS

Type: Read Only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3A	58	-	-	-	FIFO _OFLOW _INT	FSYNC _INT	-	-	DATA _RDY_INT

Description:

This register shows the interrupt status of each interrupt generation source. Each bit will clear after the register is read.

For information regarding the corresponding interrupt enable bits, please refer to Register 56.

Bits 7 through 5, 2, and 1 are reserved.

Parameters:

FIFO_OFLOW_INT This bit automatically sets to 1 when a FIFO buffer overflow interrupt has been generated.
The bit clears to 0 after the register has been read.

FSYNC_INT This bit automatically sets to 1 when an FSYNC interrupt has been generated.
The bit clears to 0 after the registers has been read.

DATA_RDY_INT This bit automatically sets to 1 when a Data Ready interrupt is generated.
The bit clears to 0 after the register has been read.

10.10 Registers 65 and 66 – Temperature Measurement

TEMP_OUT_H and TEMP_OUT_L

Type: Read Only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
41	65	TEMP_OUT[15:8]							
42	66	TEMP_OUT[7:0]							

Description:

These registers store the most recent temperature sensor measurement.

Temperature measurements are written to these registers at the Sample Rate as defined in Register 25.

These temperature measurement registers, along with the gyroscope measurement registers, are composed of two sets of registers: an internal register set and a user-facing read register set.

The data within the temperature sensor's internal register set is always updated at the Sample Rate. Meanwhile, the user-facing read register set duplicates the internal register set's data values whenever the serial interface is idle. This guarantees that a burst read of sensor registers will read measurements from the same sampling instant. Note that if burst reads are not used, the user is responsible for ensuring a set of single byte reads correspond to a single sampling instant by checking the Data Ready interrupt.

The scale factor and offset for the temperature sensor are found in the Electrical Specifications table in Product Specification document.

Parameters:

TEMP_OUT 16-bit signed value.
Stores the most recent temperature sensor measurement.

10.11 Registers 67 to 72 – Gyroscope Measurements

GYRO_XOUT_H, GYRO_XOUT_L, GYRO_YOUT_H, GYRO_YOUT_L, GYRO_ZOUT_H, and GYRO_ZOUT_L

Type: Read Only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
43	67	GYRO_XOUT[15:8]							
44	68	GYRO_XOUT[7:0]							
45	69	GYRO_YOUT[15:8]							
46	70	GYRO_YOUT[7:0]							
47	71	GYRO_ZOUT[15:8]							
48	72	GYRO_ZOUT[7:0]							

Description:

These registers store the most recent gyroscope measurements. Gyroscope measurements are written to these registers at the Sample Rate as defined in Register 25.

The gyroscope sensor registers continuously update at the user selectable ODR sample rate whenever the serial interface is idle. It is recommended to use burst reads on host interface to guarantee a read of sensor registers will read measurements from the same sampling instant. Note that if burst reads are not used, the user is responsible for ensuring a set of single byte reads correspond to a single sampling instant by checking the Data Ready interrupt. Failing to do so, may result in reading the low and high byte of the same sensor from different samples which could appear as noise peaks to the user for example. The following should be considered for single byte read mode:

1. Data_RDY_INT gets generated any time the sensor registers get updated with the sensor data. The frequency of this interrupt is the same as the ODR which is user selectable. The INT Configurations, INT status register and INT pin can be configured using the user register 37h, 38h and 3Ah.
2. The sensor register outputs are 16 bits (2 bytes). Both bytes should be read at the same time in order to get reliable data using burst mode. If a single byte read is used, the host needs to read the bytes back to back after Data_RDY_INT is set to ensure both bytes are from same sample.
3. The sensor registers should be read at a faster rate than the selected ODR with the read cycle preferably completed for all the sensors to get consistent and reliable output.

Each 16-bit gyroscope measurement has a full scale defined in *FS_SEL* (Register 27). For each full scale setting, the gyroscopes' sensitivity per LSB in *GYRO_xOUT* is shown in the table below:

FS_SEL	Full Scale Range	LSB Sensitivity
0	0	± 250 °/s
1	1	± 500 °/s
2	2	± 1000 °/s
3	3	± 2000 °/s

Parameters:

GYRO_XOUT 16-bit 2's complement value.
Stores the most recent X axis gyroscope measurement.

GYRO_YOUT 16-bit 2's complement value.
Stores the most recent Y axis gyroscope measurement.

GYRO_ZOUT 16-bit 2's complement value.
Stores the most recent Z axis gyroscope measurement.

10.12 Register 106 – User Control

USER_CTRL

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6A	106	-	FIFO_EN	-	I2C_IF _DIS	-	FIFO _RESET	-	SIG_COND _RESET

Description:

This register allows the user to enable and disable the FIFO buffer and choose the primary I^2C interface. The FIFO buffer, sensor signal paths and sensor registers can also be reset using this register.

The primary SPI interface will be enabled in place of the disabled primary I^2C interface when *I2C_IF_DIS* is set to 1.

When the reset bits (*FIFO_RESET* and *SIG_COND_RESET*) are set to 1, these reset bits will trigger a reset and then clear to 0.

Bits 7, 5, 3, and 1 are reserved.

Parameters:

FIFO_EN — When set to 1, this bit enables FIFO operations.
When this bit is cleared to 0, the FIFO buffer is disabled. The FIFO buffer cannot be read from while disabled. However, it can still be written to. In order to disable writing to the FIFO, please use the enable bits in Register 35.
The FIFO buffer's data will not be lost unless the FIFO is reset, or unless the device is power cycled or soft reset.

I2C_IF_DIS — When set to 1, this bit disables the primary I^2C interface and enables the SPI interface instead.

FIFO_RESET — This bit resets the FIFO buffer *w*hen set to 1. It is recommended that *FIFO_EN* be 0 when this is done. This bit automatically clears to 0 after the reset has been triggered.

SIG_COND_RESET — When set to 1, this bit resets the signal paths for all sensors (gyroscopes and temperature sensor). This operation will also clear the sensor registers. This bit automatically clears to 0 after the reset has been triggered.

10.13 Register 107 – Power Management 1

PWR_MGMT_1
Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6B	107	DEVICE _RESET	SLEEP	-	-	TEMP_DIS	CLKSEL[2:0]		

Description:
This register allows the user to configure the power mode and clock source. It also provides a bit for resetting the entire device, and a bit for disabling the temperature sensor.
By setting *SLEEP* to 1, the device can be put into low power sleep mode.
An internal 20MHz oscillator or the gyroscope based clock (PLL) can be selected as the device clock source. The PLL is the default clock source upon power up. In order for the gyroscope to perform to spec, the PLL must be selected as the clock source.
When the internal 20MHz oscillator is chosen as the clock source, the device can operate while having the gyroscopes disabled. However, this is only recommended if the user wishes to use the internal temperature sensor in this mode.
The clock source can be selected according to the following table.

CLKSEL	Clock Source
0	Internal 20MHz oscillator
1	PLL
2	PLL
3	PLL
4	PLL
5	PLL
6	Internal 20MHz oscillator
7	Reserved

For further information regarding the device clock source, please refer to the relevant Product Specification document and the Power Mode Transition Descriptions section in the Appendix.

Bits 5 and 4 are reserved.

Parameters:

DEVICE_RESET	When set to 1, this bit resets all internal registers to their default values. The bit automatically clears to 0 once the reset is done. The default values for each register can be found in Section 3.
SLEEP	When set to 1, this bit puts the device into sleep mode.
TEMP_DIS	When set to 1, this bit disables the temperature sensor.
CLKSEL	3-bit unsigned value. Specifies the clock source of the device.

10.14 Register 108 – Power Management 2

PWR_MGMT_2

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6C	108	-	-	-	-	-	STBY_XG	STBY_YG	STBY_ZG

Description:

This register allows the user to put individual axes of the gyroscope into standby mode. Note that in order to activate any gyro axis again, all gyro axes must first be put into standby mode, and then be turned on simultaneously.

If the user wishes to put all three gyro axes into standby mode, the internal oscillator must be selected as the clock source (Register 107).

If all three gyro axes are put into standby mode while the clock source of the device is set to the PLL (with the gyro drive generating the reference clock), the chip will hang due to an absence of a clock. As long as one gyro axis is enabled, the drive circuit will remain active and the PLL will provide a clock.

Bits 7 through 3 are reserved.

Parameters:

STBY_XG When set to 1, this bit puts the X axis gyroscope into standby mode. When cleared to 0 after all three gyro axes have been but into standby mode, the gyroscope turns on.

STBY_YG When set to 1, this bit puts the Y axis gyroscope into standby mode. When cleared to 0 after all three gyro axes have been but into standby mode, the gyroscope turns on.

STBY_ZG When set to 1, this bit puts the Z axis gyroscope into standby mode. When cleared to 0 after all three gyro axes have been but into standby mode, the gyroscope turns on.

10.15 Register 114 and 115 – FIFO Count Registers

FIFO_COUNT_H and FIFO_COUNT_L

Type: Read Only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
72	114	-	-	-	-	-	-	FIFO_COUNT[9:8]	
73	115	FIFO_COUNT[7:0]							

Description:

These registers keep track of the number of samples currently in the FIFO buffer in terms of the number of bytes stored.

These registers shadow the FIFO Count value. Both registers are loaded with the current sample count when FIFO_COUNT_H (Register 114) is read.

Note: Reading only FIFO_COUNT_L will not update the registers to the current FIFO COUNT value. FIFO_COUNT_H must be accessed first to update the contents of both these registers.

FIFO_COUNT should always be read in high-low order in order to guarantee that the most current FIFO Count value is read.

Bits 7 through 2 of Register 114 are reserved.

Parameters:

FIFO_COUNT 16-bit unsigned value. Indicates the number of bytes stored in the FIFO buffer. This number is in turn the number of bytes that can be read from the FIFO buffer and it is directly proportional to the number of samples available given the set of sensor data bound to be stored in the FIFO (register 35).

10.16 Register 116 – FIFO Read Write

FIFO_R_W

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
74	116	FIFO_DATA[7:0]							

Description:

This register is used to read and write data from the FIFO buffer.

Data is written to the FIFO in order of register number (from lowest to highest). If all the FIFO enable flags (see below) are enabled, the contents of registers 65 through 72 will be written in order at the Sample Rate, based on the description for *SMPLRT_DIV*, located in Register 25.

The contents of the sensor data registers (Registers 65 to 72) are written into the FIFO buffer when their corresponding FIFO enable flags are set to 1 in FIFO_EN (Register 35).

If the FIFO buffer has overflowed, the status bit *FIFO_OFLOW_INT* is automatically set to 1. This bit is located in INT_STATUS (Register 58). When the FIFO buffer has overflowed, the treatment of the new data is determined by the *FIFO_MODE* bit in Register 26.

The user should check *FIFO_COUNT* to ensure that the FIFO buffer is not read when empty, and that more data than available is not read from the FIFO.

Parameters:

FIFO_DATA 8-bit data transferred to and from the FIFO buffer.

10.17 Register 117 – Who Am I

WHO_AM_I

Type: Read Only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
75	117	-	WHO_AM_I[5:0]						-

Description:

This register is used to verify the identity of the device. The contents of *WHO_AM_I* are the upper 6 bits of the device's 7-bit I^2C address. The least significant bit of the IT devices's I^2C address is determined by the value of the AD0 pin. The value of the AD0 pin is not reflected in this register.
The default value of the register is 0x68.
Bits 0 and 7 are reserved. (Hard coded to 0)

Parameters:

WHO_AM_I Contains the 6-bit I^2C address of the gyroscope device
The Power-On-Reset value of Bit6:Bit1 is 110 100.

11 Environmental Compliance

The ISZ-2510 is RoHS Green and environmental compliant.

Environmental Declaration Disclaimer:
InvenSense believes this environmental information to be correct but cannot guarantee accuracy or completeness. Conformity documents for the above component constitutes are on file. InvenSense subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by InvenSense.