



# LC74781, 74781M

## On-Screen Display Controller LSI for VCR Products

An ON Semiconductor Company

### Overview

The LC74781 and LC74781M are on-screen display CMOS LSIs that display characters and patterns on a TV screen under microprocessor control. The LC74781 and LC74781M display up to 12 lines of 24 characters, each in a 12 × 18 dot matrix.

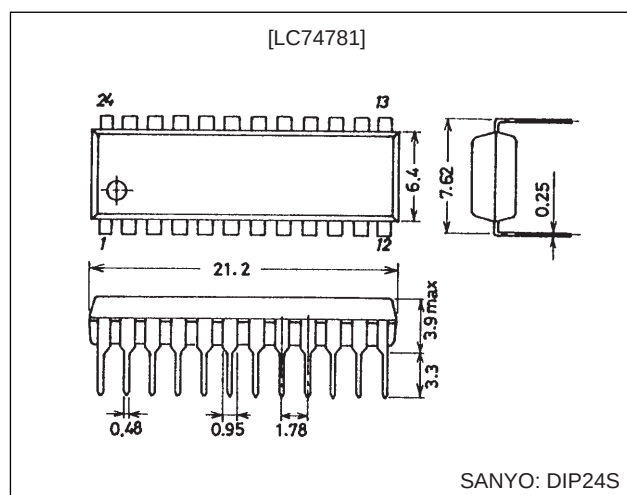
### Features

- Display structure: 12 lines × 24 characters (up to 288 characters)
- Character structure: 12 (horizontal) × 18 (vertical) dots
- Character sizes: Three size settings each in the vertical and horizontal directions
- Character set: 128 characters
- Display start position: 64 position settings each in the vertical and horizontal directions
- Blinking: In individual character units
- Blinking types: Two types with periods of about 0.5 and 1.0 second
- Blanking: Whole font area blanking (12 × 18 dots)
- Background colors: 8 colors (in internal synchronization mode): 4fSC (NTSC/PAL/PAL-M/PAL-N)  
Background colors: 4 colors (in internal synchronization mode): 2fSC (NTSC)  
Background colors: 1 color (blue) (in internal synchronization mode): 2fSC (PAL/PAL-M/PAL-N)
- External control input: 8-bit serial input format
- Built-in sync separator circuit
- Character blanked data output
- Video output: Compound NTSC, PAL, PAL-N and PAL-M output

### Package Dimensions

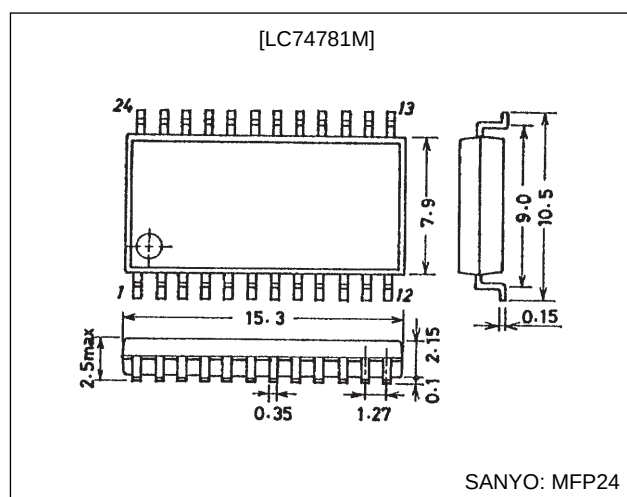
unit: mm

#### 3067-DIP24S



unit: mm

#### 3045B-MFP24

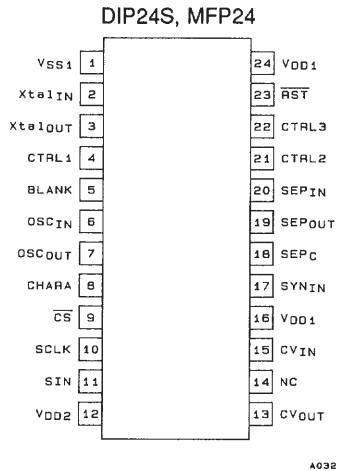


## LC74781, 74781M

### Pin Functions

| Pin No. | Symbol                 | Function                              | Description                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|---------|------------------------|---------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | V <sub>SS1</sub>       | Ground                                | Ground connection (digital system ground)                                                                                                                                                                                                                                                                                                                                                                                                   |
| 2       | Xtal <sub>IN</sub>     | Crystal oscillator connection         | Used to connect the crystal oscillator and capacitor used to generate the internal synchronization signal, or to input an external clock (2fsc or 4fsc).                                                                                                                                                                                                                                                                                    |
| 3       | Xtal <sub>OUT</sub>    |                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 4       | CTRL1                  | Crystal oscillator input switching    | Switches between external clock input mode and crystal oscillator mode.<br>Low = crystal oscillator mode, high = external clock mode                                                                                                                                                                                                                                                                                                        |
| 5       | BLANK                  | Blanking output                       | Outputs the blank signal (the OR of the character and border signals). (Outputs a composite sync signal when MOD0 is high.) Outputs the crystal oscillator clock during reset (when the RST pin is low), but can be set up to not output this signal by microprocessor command.                                                                                                                                                             |
| 6       | OSC <sub>IN</sub>      | LC oscillator connection              | Connections for the coil and capacitor that form the oscillator that generates the character output dot clock.                                                                                                                                                                                                                                                                                                                              |
| 7       | OSC <sub>OUT</sub>     |                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 8       | CHARA                  | Character output                      | Outputs the character signal. (Functions as the external synchronization signal discrimination signal output pin when MOD0 is high, and outputs the state of the judgment as to whether the external synchronization signal is present or not. Outputs a high level when the synchronization signal is present.) Outputs the dot clock (LC oscillator) during reset, but can be set up to not output this signal by microprocessor command. |
| 9       | $\overline{\text{CS}}$ | Enable input                          | Serial data input enable input. Serial data input is enabled when low. A pull-up resistor is built in (hysteresis input).                                                                                                                                                                                                                                                                                                                   |
| 10      | SCLK                   | Clock input                           | Serial data input clock input.<br>A pull-up resistor is built in (hysteresis input).                                                                                                                                                                                                                                                                                                                                                        |
| 11      | SIN                    | Data input                            | Serial data input. A pull-up resistor is built in (hysteresis input).                                                                                                                                                                                                                                                                                                                                                                       |
| 12      | V <sub>DD2</sub>       | Power supply                          | Composite video signal level adjustment power supply pin (analog system power supply).                                                                                                                                                                                                                                                                                                                                                      |
| 13      | CV <sub>OUT</sub>      | Video signal output                   | Composite video signal output                                                                                                                                                                                                                                                                                                                                                                                                               |
| 14      | NC                     |                                       | Must be either connected to ground or left open.                                                                                                                                                                                                                                                                                                                                                                                            |
| 15      | CV <sub>IN</sub>       | Video signal input                    | Composite video signal input                                                                                                                                                                                                                                                                                                                                                                                                                |
| 16      | V <sub>DD1</sub>       | Power supply                          | Power supply (+5 V: digital system power supply)                                                                                                                                                                                                                                                                                                                                                                                            |
| 17      | SYN <sub>IN</sub>      | Sync separator circuit input          | Video signal input for the built-in sync separator circuit (Used for either horizontal synchronization signal or composite sync signal input when the built-in sync separator circuit is not used.)                                                                                                                                                                                                                                         |
| 18      | SEP <sub>C</sub>       | Sync separator circuit bias voltage   | Built-in sync separator circuit bias voltage monitor pin                                                                                                                                                                                                                                                                                                                                                                                    |
| 19      | SEP <sub>OUT</sub>     | Composite sync signal output          | Built-in sync separator circuit composite sync signal output. (When MOD1 is high, outputs a high level during internal synchronization and a low level during external synchronization.) (Outputs the SYN <sub>IN</sub> input signal when the internal sync separator circuit is not used.)                                                                                                                                                 |
| 20      | SEP <sub>IN</sub>      | Vertical synchronization signal input | Inputs a vertical synchronization signal created by integrating the SEP <sub>OUT</sub> pin output signal. An integrator must be attached at the SEP <sub>OUT</sub> pin. This pin must be tied to V <sub>DD1</sub> if unused.                                                                                                                                                                                                                |
| 21      | CTRL2                  | NTSC/PAL-M switching input            | The setting indicated by this pin takes priority in switching between the NTSC, PAL, PAL-M and PAL-N formats. A low level selects NTSC after a reset. The microprocessor command NTSC, PAL, PAL-M, or PAL-N setting is valid. High = PAL-M format.                                                                                                                                                                                          |
| 22      | CTRL3                  | SEP <sub>IN</sub> input control       | Controls whether or not the $\overline{\text{VSYNC}}$ signal is input to the SEP <sub>IN</sub> input. Low = $\overline{\text{VSYNC}}$ input, high = $\overline{\text{VSYNC}}$ not input.                                                                                                                                                                                                                                                    |
| 23      | RST                    | Reset input                           | System reset input. A pull-up resistor is built in (hysteresis input).                                                                                                                                                                                                                                                                                                                                                                      |
| 24      | V <sub>DD1</sub>       | Power supply (+5 V)                   | Power supply (+5 V: digital system power supply)                                                                                                                                                                                                                                                                                                                                                                                            |

## Pin Assignment



## Specifications

### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter                   | Symbol               | Conditions                        | Ratings                          | Unit             |
|-----------------------------|----------------------|-----------------------------------|----------------------------------|------------------|
| Maximum supply voltage      | $V_{DD\text{ max}}$  | $V_{DD1}$ and $V_{DD2}$ pins      | $V_{SS} - 0.3$ to $V_{SS} + 7.0$ | V                |
| Maximum input voltage       | $V_{IN\text{ max}}$  | All pins                          | $V_{SS} - 0.3$ to $V_{DD} + 0.3$ | V                |
| Maximum output voltage      | $V_{OUT\text{ max}}$ | BLANK, CHARA and $SEP_{OUT}$ pins | $V_{SS} - 0.3$ to $V_{DD} + 0.3$ | V                |
| Allowable power dissipation | $P_{d\text{ max}}$   | $T_a = 25^\circ\text{C}$          | 350                              | mW               |
| Operating temperature       | $T_{opr}$            |                                   | $-30$ to $+70$                   | $^\circ\text{C}$ |
| Storage temperature         | $T_{stg}$            |                                   | $-40$ to $+125$                  | $^\circ\text{C}$ |

### Allowable Operating Ranges at $T_a = -30$ to $+70^\circ\text{C}$

| Parameter                     | Symbol     | Conditions                                                                                                              | min            | typ    | max             | Unit       |
|-------------------------------|------------|-------------------------------------------------------------------------------------------------------------------------|----------------|--------|-----------------|------------|
| Supply voltage                | $V_{DD1}$  | $V_{DD1}$ pin                                                                                                           | 4.5            | 5.0    | 5.5             | V          |
|                               | $V_{DD2}$  | $V_{DD2}$ pin                                                                                                           | 4.5            | 5.0    | $1.27 V_{DD1}$  | V          |
| Input high level voltage      | $V_{IH1}$  | $\overline{RST}$ , $\overline{CS}$ , SIN and SCLK pins                                                                  | $0.8 V_{DD1}$  |        | $V_{DD1} + 0.3$ | V          |
|                               | $V_{IH2}$  | CTRL1, CTRL2, CTRL3 and $SEP_{IN}$ pins                                                                                 | $0.7 V_{DD1}$  |        | $V_{DD1} + 0.3$ | V          |
| Input low level voltage       | $V_{IL1}$  | $\overline{RST}$ , $\overline{CS}$ , SIN and SCLK pins                                                                  | $V_{SS} - 0.3$ |        | $0.2 V_{DD1}$   | V          |
|                               | $V_{IL2}$  | CTRL1, CTRL2, CTRL3 and $SEP_{IN}$ pins                                                                                 | $V_{SS} - 0.3$ |        | $0.3 V_{DD1}$   | V          |
| Pull-up resistance            | $R_{PU}$   | $\overline{RST}$ , $\overline{CS}$ , SIN and SCLK pins, applies to pins set by options.                                 | 25             | 50     | 90              | k $\Omega$ |
| Composite video input voltage | $V_{IN1}$  | CV <sub>IN</sub> pin: $V_{DD1} = 5\text{ V}$                                                                            |                | 2.0    |                 | Vp-p       |
|                               | $V_{IN2}$  | SYN <sub>IN</sub> pin: $V_{DD1} = 5\text{ V}$                                                                           |                | 2.0    | 2.5             | Vp-p       |
| Input voltage                 | $V_{IN3}$  | Xtal <sub>IN</sub> pin (in external clock input mode), $f_{in} = 2\text{fsc}$ or $4\text{fsc}$ : $V_{DD1} = 5\text{ V}$ | 0.10           |        | 5.0             | Vp-p       |
| Oscillator frequency          | $F_{OSC1}$ | Xtal <sub>IN</sub> and Xtal <sub>OUT</sub> oscillator pins (2fsc: NTSC)                                                 |                | 7.159  |                 | MHz        |
|                               | $F_{OSC1}$ | Xtal <sub>IN</sub> and Xtal <sub>OUT</sub> oscillator pins (4fsc: NTSC)                                                 |                | 14.318 |                 | MHz        |
|                               | $F_{OSC1}$ | Xtal <sub>IN</sub> and Xtal <sub>OUT</sub> oscillator pins (2fsc: PAL)                                                  |                | 8.867  |                 | MHz        |
|                               | $F_{OSC1}$ | Xtal <sub>IN</sub> and Xtal <sub>OUT</sub> oscillator pins (4fsc: PAL)                                                  |                | 17.734 |                 | MHz        |
|                               | $F_{OSC1}$ | Xtal <sub>IN</sub> and Xtal <sub>OUT</sub> oscillator pins (2fsc: PAL-M)                                                |                | 7.151  |                 | MHz        |
|                               | $F_{OSC1}$ | Xtal <sub>IN</sub> and Xtal <sub>OUT</sub> oscillator pins (4fsc: PAL-M)                                                |                | 14.302 |                 | MHz        |
|                               | $F_{OSC1}$ | Xtal <sub>IN</sub> and Xtal <sub>OUT</sub> oscillator pins (2fsc: PAL-N)                                                |                | 7.164  |                 | MHz        |
|                               | $F_{OSC1}$ | Xtal <sub>IN</sub> and Xtal <sub>OUT</sub> oscillator pins (4fsc: PAL-N)                                                |                | 14.328 |                 | MHz        |
|                               | $F_{OSC2}$ | OSC <sub>IN</sub> and OSC <sub>OUT</sub> oscillator pins (LC oscillator)                                                | 5              |        | 10              | MHz        |

Note: If the Xtal<sub>IN</sub> pin is used in clock input mode, be sure to prevent input noise from becoming a problem.

# LC74781, 74781M

## Electrical Characteristics at Ta = -30 to +70°C, V<sub>DD1</sub> = 5 V unless otherwise specified

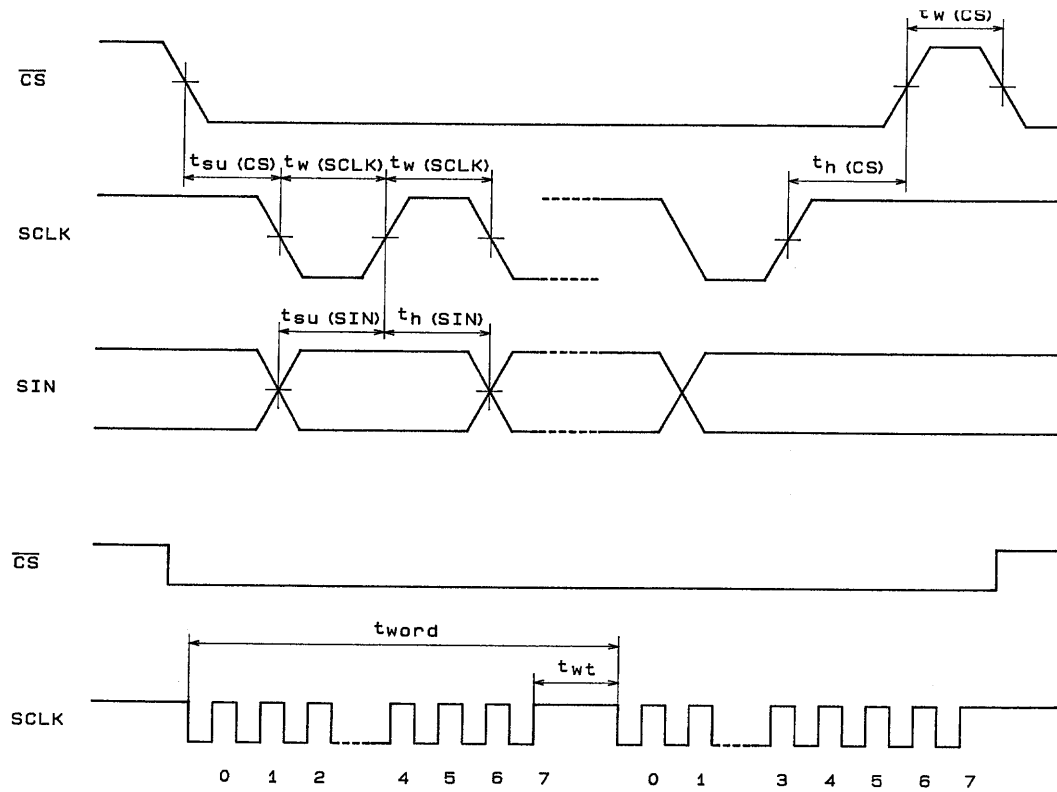
| Parameter                   | Symbol             | Conditions                                                                                      |                                                    |    | min  | typ  | max  | Unit |
|-----------------------------|--------------------|-------------------------------------------------------------------------------------------------|----------------------------------------------------|----|------|------|------|------|
| Input off leakage current   | I <sub>leak1</sub> | CV <sub>IN</sub> pin                                                                            |                                                    |    |      |      | 1    | μA   |
| Output off leakage current  | I <sub>leak2</sub> | CV <sub>OUT</sub> pin                                                                           |                                                    |    |      |      | 1    | μA   |
| Output high level voltage   | V <sub>OH1</sub>   | BLANK, CHARA and SEP <sub>OUT</sub> pins: V <sub>DD1</sub> = 4.5 V, I <sub>OH</sub> = −1.0 mA   |                                                    |    | 3.5  |      |      | V    |
| Output low level voltage    | V <sub>OL1</sub>   | BLANK, CHARA and SEP <sub>OUT</sub> pins: V <sub>DD1</sub> = 4.5 V, I <sub>OH</sub> = 1.0 mA    |                                                    |    |      |      | 1.0  | V    |
| Input current               | I <sub>IH</sub>    | RST, CS, SIN, SCLK, CTRL1, CTRL3 and SEP <sub>IN</sub> pins: V <sub>IN</sub> = V <sub>DD1</sub> |                                                    |    |      |      | 1    | μA   |
|                             | I <sub>IL</sub>    | CTRL1, CTRL2, CTRL3 and OSC <sub>IN</sub> pins: V <sub>IN</sub> = V <sub>SS1</sub>              |                                                    |    | −1   |      |      | μA   |
| Operating current drain     | I <sub>DD1</sub>   | V <sub>DD1</sub> pin; all outputs: open, Xtal: 7.159 MHz, LC: 8 MHz                             |                                                    |    |      |      | 15   | mA   |
|                             | I <sub>DD2</sub>   | V <sub>DD2</sub> pin: V <sub>DD2</sub> = 5 V                                                    |                                                    |    |      |      | 20   | mA   |
| Sync level                  | V <sub>SN</sub>    | CV <sub>OUT</sub> pin                                                                           | V <sub>DD1</sub> = 5.0 V, V <sub>DD2</sub> = 5.0 V | *1 | 0.70 | 0.82 | 0.94 | V    |
|                             |                    |                                                                                                 |                                                    | *2 | 0.91 | 1.03 | 1.15 | V    |
| Pedestal level              | V <sub>PD</sub>    | CV <sub>OUT</sub> pin                                                                           | V <sub>DD1</sub> = 5.0 V, V <sub>DD2</sub> = 5.0 V | *1 | 1.31 | 1.43 | 1.55 | V    |
|                             |                    |                                                                                                 |                                                    | *2 | 1.53 | 1.65 | 1.77 | V    |
| Color burst low level       | V <sub>CBL</sub>   | CV <sub>OUT</sub> pin                                                                           | V <sub>DD1</sub> = 5.0 V, V <sub>DD2</sub> = 5.0 V | *1 | 1.00 | 1.12 | 1.24 | V    |
|                             |                    |                                                                                                 |                                                    | *2 | 1.21 | 1.33 | 1.45 | V    |
| Color burst high level      | V <sub>CBH</sub>   | CV <sub>OUT</sub> pin                                                                           | V <sub>DD1</sub> = 5.0 V, V <sub>DD2</sub> = 5.0 V | *1 | 1.63 | 1.75 | 1.87 | V    |
|                             |                    |                                                                                                 |                                                    | *2 | 1.84 | 1.96 | 2.08 | V    |
| Background color low level  | V <sub>RSL</sub>   | CV <sub>OUT</sub> pin                                                                           | V <sub>DD1</sub> = 5.0 V, V <sub>DD2</sub> = 5.0 V | *1 | 1.47 | 1.59 | 1.71 | V    |
|                             |                    |                                                                                                 |                                                    | *2 | 1.68 | 1.80 | 1.92 | V    |
| Background color high level | V <sub>RSH</sub>   | CV <sub>OUT</sub> pin                                                                           | V <sub>DD1</sub> = 5.0 V, V <sub>DD2</sub> = 5.0 V | *1 | 1.99 | 2.11 | 2.23 | V    |
|                             |                    |                                                                                                 |                                                    | *2 | 2.19 | 2.31 | 2.43 | V    |
| Border level 0              | V <sub>BK0</sub>   | CV <sub>OUT</sub> pin                                                                           | V <sub>DD1</sub> = 5.0 V, V <sub>DD2</sub> = 5.0 V | *1 | 1.42 | 1.54 | 1.66 | V    |
|                             |                    |                                                                                                 |                                                    | *2 | 1.63 | 1.75 | 1.87 | V    |
| Border level 1              | V <sub>BK1</sub>   | CV <sub>OUT</sub> pin                                                                           | V <sub>DD1</sub> = 5.0 V, V <sub>DD2</sub> = 5.0 V | *1 | 1.99 | 2.11 | 2.23 | V    |
|                             |                    |                                                                                                 |                                                    | *2 | 2.19 | 2.31 | 2.43 | V    |
| Character level             | V <sub>CHA</sub>   | CV <sub>OUT</sub> pin                                                                           | V <sub>DD1</sub> = 5.0 V, V <sub>DD2</sub> = 5.0 V | *1 | 2.58 | 2.70 | 2.82 | V    |
|                             |                    |                                                                                                 |                                                    | *2 | 2.78 | 2.90 | 3.02 | V    |

Note: 1. When the sync level is 0.8 V.  
2. When the sync level is 1.0 V.

## Timing Characteristics at Ta = -30 to +70°C, V<sub>DD1</sub> = 5 ± 0.5 V

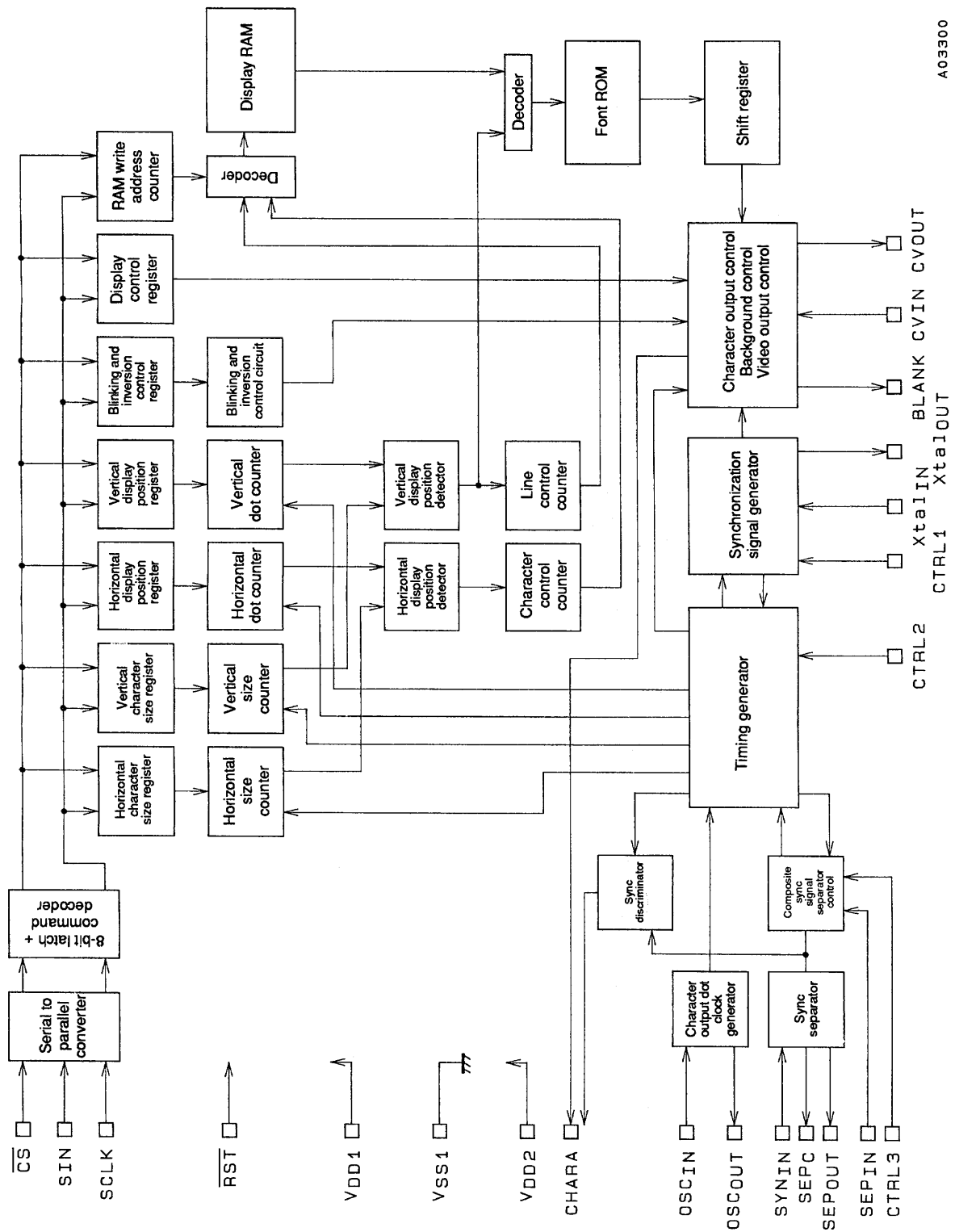
| Parameter                 | Symbol                | Conditions                          | min | typ | max | Unit |
|---------------------------|-----------------------|-------------------------------------|-----|-----|-----|------|
| Minimum input pulse width | t <sub>W</sub> (SCLK) | SCLK pin                            | 200 |     |     | ns   |
|                           | t <sub>W</sub> (CS)   | CS pin (the period when CS is high) | 1   |     |     | μs   |
| Data setup time           | t <sub>SU</sub> (CS)  | CS pin                              | 200 |     |     | ns   |
|                           | t <sub>SU</sub> (SIN) | SIN pin                             | 200 |     |     | ns   |
| Data hold time            | t <sub>H</sub> (CS)   | CS pin                              | 2   |     |     | μs   |
|                           | t <sub>H</sub> (SIN)  | SIN pin                             | 200 |     |     | ns   |
| One word write time       | t <sub>word</sub>     | 8-bit data write time               | 4.2 |     |     | μs   |
|                           | t <sub>wt</sub>       | RAM data write time                 | 1   |     |     | μs   |

## Serial Data Input Timing



A03299

## System Block Diagram



A03300

## Display Control Commands

The display control commands have a serial input format with 8-bit units. A command consists of a command identifier code in the first byte and data in the second and subsequent bytes. There are eight commands as listed below.

- ① COMMAND0: Display memory (VRAM) write address setup command
- ② COMMAND1: Display character data write command
- ③ COMMAND2: Vertical display start position and vertical character size setup command
- ④ COMMAND3: Horizontal display start position and horizontal character size setup command
- ⑤ COMMAND4: Display control setup command
- ⑥ COMMAND5: Display control setup command
- ⑦ COMMAND6: Synchronization signal detection setup command
- ⑧ COMMAND7: Display control setup command

**Display Control Command Table**

| Command                                                                           | First byte                  |   |   |   |            |            |            |            | Second byte |          |          |            |            |            |            |           |
|-----------------------------------------------------------------------------------|-----------------------------|---|---|---|------------|------------|------------|------------|-------------|----------|----------|------------|------------|------------|------------|-----------|
|                                                                                   | Command identification code |   |   |   | Data       |            |            |            | Data        |          |          |            |            |            |            |           |
|                                                                                   | 7                           | 6 | 5 | 4 | 3          | 2          | 1          | 0          | 7           | 6        | 5        | 4          | 3          | 2          | 1          | 0         |
| COMMAND0<br>(Set write address)                                                   | 1                           | 0 | 0 | 0 | V3         | V2         | V1         | V0         | 0           | 0        | 0        | H4         | H3         | H2         | H1         | H0        |
| COMMAND1<br>(Write character)                                                     | 1                           | 0 | 0 | 1 | 0          | 0          | 0          | at         | 0           | c6       | c5       | c4         | c3         | c2         | c1         | c0        |
| COMMAND2<br>(Set vertical display start position and vertical character size)     | 1                           | 0 | 1 | 0 | VS<br>21   | VS<br>20   | VS<br>11   | VS<br>10   | 0           | FS       | VP<br>5  | VP<br>4    | VP<br>3    | VP<br>2    | VP<br>1    | VP<br>0   |
| COMMAND3<br>(Set horizontal display start position and horizontal character size) | 1                           | 0 | 1 | 1 | HS<br>21   | HS<br>20   | HS<br>11   | HS<br>10   | 0           | LC       | HP<br>5  | HP<br>4    | HP<br>3    | HP<br>2    | HP<br>1    | HP<br>0   |
| COMMAND4<br>(Display control)                                                     | 1                           | 1 | 0 | 0 | TST<br>MOD | RAM<br>ERS | OSC<br>STP | SYS<br>RST | 0           | BLK<br>2 | BLK<br>1 | BLK<br>0   | BK<br>1    | BK<br>0    | RV         | DSP<br>ON |
| COMMAND5<br>(Display control)                                                     | 1                           | 1 | 0 | 1 | NP<br>1    | NP<br>0    | NON        | INT        | 0           | 0        | 0        | BCL        | CB         | PH<br>2    | PH<br>1    | PH<br>0   |
| COMMAND6<br>(Synchronization signal detection)                                    | 1                           | 1 | 1 | 0 | MOD<br>1   | MOD<br>0   | DIS<br>LIN | MUT        | 0           | RN<br>2  | RN<br>1  | RN<br>0    | SN<br>3    | SN<br>2    | SN<br>1    | SN<br>0   |
| COMMAND7<br>(Display control)                                                     | 1                           | 1 | 1 | 1 | EX<br>1    | PD<br>1    | EX<br>0    | PD<br>0    | 0           | 0        | 0        | VNP<br>SEL | VSP<br>SEL | MSK<br>ERS | MSK<br>SEL | EGL       |

Once written, the command identifier code in the first byte is stored until the next first byte is written. However, when the display character data write command (COMMAND1) is written, the LC74781/M locks into the display character data write mode, and another first byte cannot be written.

When a high level is input to the  $\overline{CS}$  pin, the LC74781/M is set to COMMAND0 (display memory write address setup mode).

## LC74781, 74781M

### ① COMMAND0 (Display memory write address setup command)

First byte

| DA0 to DA7 | Register name | Register content |                                                                        | Note |
|------------|---------------|------------------|------------------------------------------------------------------------|------|
|            |               | State            | Function                                                               |      |
| 7          | —             | 1                | Command 0 identification code<br>Set the display memory write address. |      |
| 6          | —             | 0                |                                                                        |      |
| 5          | —             | 0                |                                                                        |      |
| 4          | —             | 0                |                                                                        |      |
| 3          | V3            | 0                | Display memory address (0 to B hexadecimal)                            |      |
|            |               | 1                |                                                                        |      |
| 2          | V2            | 0                |                                                                        |      |
|            |               | 1                |                                                                        |      |
| 1          | V1            | 0                |                                                                        |      |
|            |               | 1                |                                                                        |      |
| 0          | V0            | 0                |                                                                        |      |
|            |               | 1                |                                                                        |      |

Second byte

| DA0 to DA7 | Register name | Register content |                                              | Note |
|------------|---------------|------------------|----------------------------------------------|------|
|            |               | State            | Function                                     |      |
| 7          | —             | 0                | Second byte identification bit               |      |
| 6          | —             | 0                |                                              |      |
| 5          | —             | 0                |                                              |      |
| 4          | H4            | 0                | Display memory address (0 to 17 hexadecimal) |      |
|            |               | 1                |                                              |      |
| 3          | H3            | 0                |                                              |      |
|            |               | 1                |                                              |      |
| 2          | H2            | 0                |                                              |      |
|            |               | 1                |                                              |      |
| 1          | H1            | 0                |                                              |      |
|            |               | 1                |                                              |      |
| 0          | H0            | 0                |                                              |      |
|            |               | 1                |                                              |      |

Note: The register states are all set to zero when the LC74781/M is reset with the  $\overline{\text{RST}}$  pin.

### ② COMMAND1 (Display character data write setup command)

First byte

| DA0 to DA7 | Register name | Register content |                                                                       | Note                                                                                                                   |
|------------|---------------|------------------|-----------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|
|            |               | State            | Function                                                              |                                                                                                                        |
| 7          | —             | 1                | Command 1 identification code<br>Set up display character data write. | When this command is input, the LC74781/M locks into the display character data write mode until the CS pin goes high. |
| 6          | —             | 0                |                                                                       |                                                                                                                        |
| 5          | —             | 0                |                                                                       |                                                                                                                        |
| 4          | —             | 1                |                                                                       |                                                                                                                        |
| 3          | —             | 0                |                                                                       |                                                                                                                        |
| 2          | —             | 0                |                                                                       |                                                                                                                        |
| 1          | —             | 0                |                                                                       |                                                                                                                        |
| 0          | at            | 0                | Character attribute off                                               |                                                                                                                        |
|            |               | 1                | Character attribute on                                                |                                                                                                                        |



# LC74781, 74781M

## Second byte

| DA0 to DA7 | Register name | Register content |                                       | Note |
|------------|---------------|------------------|---------------------------------------|------|
|            |               | State            | Function                              |      |
| 7          | —             | 0                | Character code (00 to 7F hexadecimal) |      |
| 6          | c6            | 0                |                                       |      |
|            |               | 1                |                                       |      |
| 5          | c5            | 0                |                                       |      |
|            |               | 1                |                                       |      |
| 4          | c4            | 0                |                                       |      |
|            |               | 1                |                                       |      |
| 3          | c3            | 0                |                                       |      |
|            |               | 1                |                                       |      |
| 2          | c2            | 0                |                                       |      |
|            |               | 1                |                                       |      |
| 1          | c1            | 0                |                                       |      |
|            |               | 1                |                                       |      |
| 0          | c0            | 0                |                                       |      |
|            |               | 1                |                                       |      |

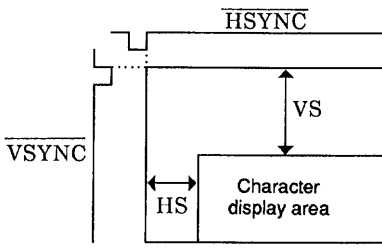
Note: The register states are all set to zero when the LC74781/M is reset with the  $\overline{\text{RST}}$  pin.

## ③ COMMAND2 (Vertical display start position and vertical character size setup command)

### First byte

| DA0 to DA7 | Register name | Register content |                                                                                                                                                                                    |  |  | Note        |   |   |   |            |            |   |            |            |                                     |
|------------|---------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|-------------|---|---|---|------------|------------|---|------------|------------|-------------------------------------|
|            |               | State            | Function                                                                                                                                                                           |  |  |             |   |   |   |            |            |   |            |            |                                     |
| 7          | —             | 1                | Command 2 identification code<br>Set the vertical display start position and vertical character size.                                                                              |  |  |             |   |   |   |            |            |   |            |            |                                     |
| 6          | —             | 0                |                                                                                                                                                                                    |  |  |             |   |   |   |            |            |   |            |            |                                     |
| 5          | —             | 1                |                                                                                                                                                                                    |  |  |             |   |   |   |            |            |   |            |            |                                     |
| 4          | —             | 0                |                                                                                                                                                                                    |  |  |             |   |   |   |            |            |   |            |            |                                     |
| 3          | VS21          | 0                | <table><tr><td>VS21 \ VS20</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1H per dot</td><td>2H per dot</td></tr><tr><td>1</td><td>3H per dot</td><td>1H per dot</td></tr></table> |  |  | VS21 \ VS20 | 0 | 1 | 0 | 1H per dot | 2H per dot | 1 | 3H per dot | 1H per dot | Second line vertical character size |
|            |               | VS21 \ VS20      |                                                                                                                                                                                    |  |  | 0           | 1 |   |   |            |            |   |            |            |                                     |
| 0          | 1H per dot    | 2H per dot       |                                                                                                                                                                                    |  |  |             |   |   |   |            |            |   |            |            |                                     |
| 1          | 3H per dot    | 1H per dot       |                                                                                                                                                                                    |  |  |             |   |   |   |            |            |   |            |            |                                     |
| 1          | 1             |                  |                                                                                                                                                                                    |  |  |             |   |   |   |            |            |   |            |            |                                     |
| 2          | VS20          | 0                | <table><tr><td>VS11 \ VS10</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1H per dot</td><td>2H per dot</td></tr><tr><td>1</td><td>3H per dot</td><td>1H per dot</td></tr></table> |  |  | VS11 \ VS10 | 0 | 1 | 0 | 1H per dot | 2H per dot | 1 | 3H per dot | 1H per dot | First line vertical character size  |
|            |               | VS11 \ VS10      |                                                                                                                                                                                    |  |  | 0           | 1 |   |   |            |            |   |            |            |                                     |
| 0          | 1H per dot    | 2H per dot       |                                                                                                                                                                                    |  |  |             |   |   |   |            |            |   |            |            |                                     |
| 1          | 3H per dot    | 1H per dot       |                                                                                                                                                                                    |  |  |             |   |   |   |            |            |   |            |            |                                     |
| 1          | 1             |                  |                                                                                                                                                                                    |  |  |             |   |   |   |            |            |   |            |            |                                     |
| 1          | VS11          | 0                | <table><tr><td>VS11 \ VS10</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1H per dot</td><td>2H per dot</td></tr><tr><td>1</td><td>3H per dot</td><td>1H per dot</td></tr></table> |  |  | VS11 \ VS10 | 0 | 1 | 0 | 1H per dot | 2H per dot | 1 | 3H per dot | 1H per dot | First line vertical character size  |
|            |               | VS11 \ VS10      |                                                                                                                                                                                    |  |  | 0           | 1 |   |   |            |            |   |            |            |                                     |
| 0          | 1H per dot    | 2H per dot       |                                                                                                                                                                                    |  |  |             |   |   |   |            |            |   |            |            |                                     |
| 1          | 3H per dot    | 1H per dot       |                                                                                                                                                                                    |  |  |             |   |   |   |            |            |   |            |            |                                     |
| 1          | 1             |                  |                                                                                                                                                                                    |  |  |             |   |   |   |            |            |   |            |            |                                     |
| 0          | VS10          | 0                | <table><tr><td>VS11 \ VS10</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1H per dot</td><td>2H per dot</td></tr><tr><td>1</td><td>3H per dot</td><td>1H per dot</td></tr></table> |  |  | VS11 \ VS10 | 0 | 1 | 0 | 1H per dot | 2H per dot | 1 | 3H per dot | 1H per dot | First line vertical character size  |
|            |               | VS11 \ VS10      |                                                                                                                                                                                    |  |  | 0           | 1 |   |   |            |            |   |            |            |                                     |
| 0          | 1H per dot    | 2H per dot       |                                                                                                                                                                                    |  |  |             |   |   |   |            |            |   |            |            |                                     |
| 1          | 3H per dot    | 1H per dot       |                                                                                                                                                                                    |  |  |             |   |   |   |            |            |   |            |            |                                     |
| 1          | 1             |                  |                                                                                                                                                                                    |  |  |             |   |   |   |            |            |   |            |            |                                     |

### Second byte

| DA0 to DA7 | Register name | Register content |                                                                                                                                                                                                                                                       | Note                                                                                            |
|------------|---------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|
|            |               | State            | Function                                                                                                                                                                                                                                              |                                                                                                 |
| 7          | —             | 0                | Second byte identification bit                                                                                                                                                                                                                        |                                                                                                 |
| 6          | FS            | 0                | Crystal oscillator frequency: 2fsc                                                                                                                                                                                                                    |                                                                                                 |
|            |               | 1                | Crystal oscillator frequency: 4fsc                                                                                                                                                                                                                    |                                                                                                 |
| 5          | VP5 (MSB)     | 0                | If VS is the vertical display start position then:<br>$VS = H \times \left( 2 \sum_{n=0}^5 2^n VP_n \right)$<br>H: the horizontal synchronization pulse period<br> | The vertical display start position is set by the 6 bits VP0 to VP5. The weight of bit 1 is 2H. |
|            |               | 1                |                                                                                                                                                                                                                                                       |                                                                                                 |
| 4          | VP4           | 0                |                                                                                                                                                                                                                                                       |                                                                                                 |
|            |               | 1                |                                                                                                                                                                                                                                                       |                                                                                                 |
| 3          | VP3           | 0                |                                                                                                                                                                                                                                                       |                                                                                                 |
|            |               | 1                |                                                                                                                                                                                                                                                       |                                                                                                 |
| 2          | VP2           | 0                |                                                                                                                                                                                                                                                       |                                                                                                 |
|            |               | 1                |                                                                                                                                                                                                                                                       |                                                                                                 |
| 1          | VP1           | 0                |                                                                                                                                                                                                                                                       |                                                                                                 |
|            |               | 1                |                                                                                                                                                                                                                                                       |                                                                                                 |
| 0          | VP0 (LSB)     | 0                |                                                                                                                                                                                                                                                       |                                                                                                 |
|            |               | 1                |                                                                                                                                                                                                                                                       |                                                                                                 |

Note: The register states are all set to zero when the LC74781/M is reset with the  $\overline{\text{RST}}$  pin.

## ④ COMMAND3 (Horizontal display start position and horizontal character size setup command)

First byte

| DA0 to DA7 | Register name | Register content |                                                                                                                                                                                            |  |  | Note        |   |   |   |              |              |   |              |              |                                       |
|------------|---------------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|-------------|---|---|---|--------------|--------------|---|--------------|--------------|---------------------------------------|
|            |               | State            | Function                                                                                                                                                                                   |  |  |             |   |   |   |              |              |   |              |              |                                       |
| 7          | —             | 1                | Command 3 identification code<br>Set the horizontal display start position and horizontal character size.                                                                                  |  |  |             |   |   |   |              |              |   |              |              |                                       |
| 6          | —             | 0                |                                                                                                                                                                                            |  |  |             |   |   |   |              |              |   |              |              |                                       |
| 5          | —             | 1                |                                                                                                                                                                                            |  |  |             |   |   |   |              |              |   |              |              |                                       |
| 4          | —             | 1                |                                                                                                                                                                                            |  |  |             |   |   |   |              |              |   |              |              |                                       |
| 3          | HS21          | 0                | <table><tr><td>HS21 \ HS20</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1 Tc per dot</td><td>2 Tc per dot</td></tr><tr><td>1</td><td>3 Tc per dot</td><td>1 Tc per dot</td></tr></table> |  |  | HS21 \ HS20 | 0 | 1 | 0 | 1 Tc per dot | 2 Tc per dot | 1 | 3 Tc per dot | 1 Tc per dot | Second line horizontal character size |
|            |               | HS21 \ HS20      |                                                                                                                                                                                            |  |  | 0           | 1 |   |   |              |              |   |              |              |                                       |
| 0          | 1 Tc per dot  | 2 Tc per dot     |                                                                                                                                                                                            |  |  |             |   |   |   |              |              |   |              |              |                                       |
| 1          | 3 Tc per dot  | 1 Tc per dot     |                                                                                                                                                                                            |  |  |             |   |   |   |              |              |   |              |              |                                       |
| 1          | 1             |                  |                                                                                                                                                                                            |  |  |             |   |   |   |              |              |   |              |              |                                       |
| 2          | HS20          | 0                | <table><tr><td>HS21 \ HS20</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1 Tc per dot</td><td>2 Tc per dot</td></tr><tr><td>1</td><td>3 Tc per dot</td><td>1 Tc per dot</td></tr></table> |  |  | HS21 \ HS20 | 0 | 1 | 0 | 1 Tc per dot | 2 Tc per dot | 1 | 3 Tc per dot | 1 Tc per dot | Second line horizontal character size |
|            |               | HS21 \ HS20      |                                                                                                                                                                                            |  |  | 0           | 1 |   |   |              |              |   |              |              |                                       |
| 0          | 1 Tc per dot  | 2 Tc per dot     |                                                                                                                                                                                            |  |  |             |   |   |   |              |              |   |              |              |                                       |
| 1          | 3 Tc per dot  | 1 Tc per dot     |                                                                                                                                                                                            |  |  |             |   |   |   |              |              |   |              |              |                                       |
| 1          | 1             |                  |                                                                                                                                                                                            |  |  |             |   |   |   |              |              |   |              |              |                                       |
| 1          | HS11          | 0                | <table><tr><td>HS11 \ HS10</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1 Tc per dot</td><td>2 Tc per dot</td></tr><tr><td>1</td><td>3 Tc per dot</td><td>1 Tc per dot</td></tr></table> |  |  | HS11 \ HS10 | 0 | 1 | 0 | 1 Tc per dot | 2 Tc per dot | 1 | 3 Tc per dot | 1 Tc per dot | First line horizontal character size  |
|            |               | HS11 \ HS10      |                                                                                                                                                                                            |  |  | 0           | 1 |   |   |              |              |   |              |              |                                       |
| 0          | 1 Tc per dot  | 2 Tc per dot     |                                                                                                                                                                                            |  |  |             |   |   |   |              |              |   |              |              |                                       |
| 1          | 3 Tc per dot  | 1 Tc per dot     |                                                                                                                                                                                            |  |  |             |   |   |   |              |              |   |              |              |                                       |
| 1          | 1             |                  |                                                                                                                                                                                            |  |  |             |   |   |   |              |              |   |              |              |                                       |
| 0          | HS10          | 0                | <table><tr><td>HS11 \ HS10</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1 Tc per dot</td><td>2 Tc per dot</td></tr><tr><td>1</td><td>3 Tc per dot</td><td>1 Tc per dot</td></tr></table> |  |  | HS11 \ HS10 | 0 | 1 | 0 | 1 Tc per dot | 2 Tc per dot | 1 | 3 Tc per dot | 1 Tc per dot | First line horizontal character size  |
|            |               | HS11 \ HS10      |                                                                                                                                                                                            |  |  | 0           | 1 |   |   |              |              |   |              |              |                                       |
| 0          | 1 Tc per dot  | 2 Tc per dot     |                                                                                                                                                                                            |  |  |             |   |   |   |              |              |   |              |              |                                       |
| 1          | 3 Tc per dot  | 1 Tc per dot     |                                                                                                                                                                                            |  |  |             |   |   |   |              |              |   |              |              |                                       |
| 1          | 1             |                  |                                                                                                                                                                                            |  |  |             |   |   |   |              |              |   |              |              |                                       |

Second byte

| DA0 to DA7 | Register name | Register content |                                                                                                                                                                        | Note                                                                                                    |
|------------|---------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------|
|            |               | State            | Function                                                                                                                                                               |                                                                                                         |
| 7          | —             | 0                | Second byte identification bit                                                                                                                                         |                                                                                                         |
| 6          | LC            | 0                | An LC oscillator is used for the dot clock.                                                                                                                            | Selects the dot clock used in horizontal character display.                                             |
|            |               | 1                | A crystal oscillator is used for the dot clock.                                                                                                                        |                                                                                                         |
| 5          | HP5 (MSB)     | 0                | If HS is the horizontal start position then:<br>$HS = Tc \times (2 \sum_{n=0}^5 2^n HP_n)$<br>Tc: Period of the oscillator connected to OSCIN/OSCOU in operating mode. | The horizontal display start position is set by the six bits HP5 to HP0.<br>The weight of bit 1 is 2Tc. |
|            |               | 1                |                                                                                                                                                                        |                                                                                                         |
| 4          | HP4           | 0                |                                                                                                                                                                        |                                                                                                         |
|            |               | 1                |                                                                                                                                                                        |                                                                                                         |
| 3          | HP3           | 0                |                                                                                                                                                                        |                                                                                                         |
|            |               | 1                |                                                                                                                                                                        |                                                                                                         |
| 2          | HP2           | 0                |                                                                                                                                                                        |                                                                                                         |
|            |               | 1                |                                                                                                                                                                        |                                                                                                         |
| 1          | HP1           | 0                |                                                                                                                                                                        |                                                                                                         |
|            |               | 1                |                                                                                                                                                                        |                                                                                                         |
| 0          | HP0 (LSB)     | 0                |                                                                                                                                                                        |                                                                                                         |
|            |               | 1                |                                                                                                                                                                        |                                                                                                         |

Note: The register states are all set to zero when the LC74781/M is reset with the  $\overline{RST}$  pin.

## ⑤ COMMAND4 (Display control setup command)

First byte

| DA0 to DA7 | Register name | Register content |                                                                | Note                                                                                                       |
|------------|---------------|------------------|----------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|
|            |               | State            | Function                                                       |                                                                                                            |
| 7          | —             | 1                | Command 4 identification code<br>Display control               |                                                                                                            |
| 6          | —             | 1                |                                                                |                                                                                                            |
| 5          | —             | 0                |                                                                |                                                                                                            |
| 4          | —             | 0                |                                                                |                                                                                                            |
| 3          | TSTMOD        | 0                | Normal operating mode                                          | This bit must be zero.                                                                                     |
|            |               | 1                | Test mode                                                      |                                                                                                            |
| 2          | RAMERS        | 0                |                                                                | The RAM erase operation requires about 500 $\mu$ s (It is executed in the DSPOFF state.)                   |
|            |               | 1                | Erase display RAM (set to 7F hexadecimal)                      |                                                                                                            |
| 1          | OSCSTP        | 0                | Do not stop the crystal oscillator and LC oscillator circuits. | Valid when character display is off in external synchronization mode.                                      |
|            |               | 1                | Stop the crystal oscillator and LC oscillator circuits.        |                                                                                                            |
| 0          | SYSRST        | 0                |                                                                | Reset occurs when the $\overline{CS}$ pin is low, and the reset is cleared when $\overline{CS}$ goes high. |
|            |               | 1                | Reset all registers and turn the display off.                  |                                                                                                            |

## LC74781, 74781M

### Second byte

| DA0 to DA7  | Register name | Register content    |                                                                                                                                                                                                    |  | Note                                                                                                                              |   |   |   |              |                |   |             |                     |                            |  |
|-------------|---------------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|-----------------------------------------------------------------------------------------------------------------------------------|---|---|---|--------------|----------------|---|-------------|---------------------|----------------------------|--|
|             |               | State               | Function                                                                                                                                                                                           |  |                                                                                                                                   |   |   |   |              |                |   |             |                     |                            |  |
| 7           | —             | 0                   | Second byte identification bit                                                                                                                                                                     |  |                                                                                                                                   |   |   |   |              |                |   |             |                     |                            |  |
| 6           | BLK2          | 0                   | Character display block                                                                                                                                                                            |  | Full character size specification                                                                                                 |   |   |   |              |                |   |             |                     |                            |  |
|             |               | 1                   | Video display block                                                                                                                                                                                |  |                                                                                                                                   |   |   |   |              |                |   |             |                     |                            |  |
| 5           | BLK1          | 0                   | <table><tr><td>BLK1 \ BLK0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>Blanking off</td><td>Character size</td></tr><tr><td>1</td><td>Border size</td><td>Full character size</td></tr></table> |  | BLK1 \ BLK0                                                                                                                       | 0 | 1 | 0 | Blanking off | Character size | 1 | Border size | Full character size | Changes the blanking size. |  |
| BLK1 \ BLK0 | 0             | 1                   |                                                                                                                                                                                                    |  |                                                                                                                                   |   |   |   |              |                |   |             |                     |                            |  |
| 0           | Blanking off  | Character size      |                                                                                                                                                                                                    |  |                                                                                                                                   |   |   |   |              |                |   |             |                     |                            |  |
| 1           | Border size   | Full character size |                                                                                                                                                                                                    |  |                                                                                                                                   |   |   |   |              |                |   |             |                     |                            |  |
| 4           | BLK0          | 0                   |                                                                                                                                                                                                    |  |                                                                                                                                   |   |   |   |              |                |   |             |                     |                            |  |
|             |               | 1                   |                                                                                                                                                                                                    |  |                                                                                                                                   |   |   |   |              |                |   |             |                     |                            |  |
| 3           | BK1           | 0                   | Blinking period: about 0.5 s                                                                                                                                                                       |  | Switches the blinking period.                                                                                                     |   |   |   |              |                |   |             |                     |                            |  |
|             |               | 1                   | Blinking period: about 1.0 s                                                                                                                                                                       |  |                                                                                                                                   |   |   |   |              |                |   |             |                     |                            |  |
| 2           | BK0           | 0                   | Blinking off                                                                                                                                                                                       |  | When blinking is specified for reversed characters, the blinking will be between normal character and reversed character display. |   |   |   |              |                |   |             |                     |                            |  |
|             |               | 1                   | Blinking on                                                                                                                                                                                        |  |                                                                                                                                   |   |   |   |              |                |   |             |                     |                            |  |
| 1           | RV            | 0                   | Reverse (character reversing) off                                                                                                                                                                  |  |                                                                                                                                   |   |   |   |              |                |   |             |                     |                            |  |
|             |               | 1                   | Reverse (character reversing) on                                                                                                                                                                   |  |                                                                                                                                   |   |   |   |              |                |   |             |                     |                            |  |
| 0           | DSPON         | 0                   | Character display off                                                                                                                                                                              |  |                                                                                                                                   |   |   |   |              |                |   |             |                     |                            |  |
|             |               | 1                   | Character display on                                                                                                                                                                               |  |                                                                                                                                   |   |   |   |              |                |   |             |                     |                            |  |

Note: The register states are all set to zero when the LC74781/M is reset with the  $\overline{\text{RST}}$  pin.

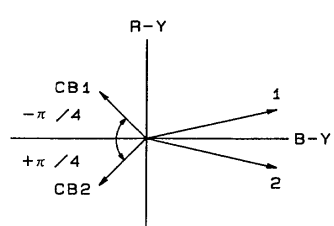
### ⑥ COMMAND5 (Display control setup command)

#### First byte

| DA0 to DA7 | Register name | Register content |                                                                                                                                                           |  |  | Note                                                    |   |   |   |      |       |   |     |       |                                             |  |  |
|------------|---------------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|---------------------------------------------------------|---|---|---|------|-------|---|-----|-------|---------------------------------------------|--|--|
|            |               | State            | Function                                                                                                                                                  |  |  |                                                         |   |   |   |      |       |   |     |       |                                             |  |  |
| 7          | —             | 1                | Command 5 identification code<br>Display control                                                                                                          |  |  |                                                         |   |   |   |      |       |   |     |       |                                             |  |  |
| 6          | —             | 1                |                                                                                                                                                           |  |  |                                                         |   |   |   |      |       |   |     |       |                                             |  |  |
| 5          | —             | 0                |                                                                                                                                                           |  |  |                                                         |   |   |   |      |       |   |     |       |                                             |  |  |
| 4          | —             | 1                |                                                                                                                                                           |  |  |                                                         |   |   |   |      |       |   |     |       |                                             |  |  |
| 3          | NP1           | 0                | <table><tr><td>NP1 / NP0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>NTSC</td><td>PAL-M</td></tr><tr><td>1</td><td>PAL</td><td>PAL-N</td></tr></table> |  |  | NP1 / NP0                                               | 0 | 1 | 0 | NTSC | PAL-M | 1 | PAL | PAL-N | Switches between NTSC, PAL, PAL-M and PAL-N |  |  |
|            |               | NP1 / NP0        |                                                                                                                                                           |  |  | 0                                                       | 1 |   |   |      |       |   |     |       |                                             |  |  |
| 0          | NTSC          | PAL-M            |                                                                                                                                                           |  |  |                                                         |   |   |   |      |       |   |     |       |                                             |  |  |
| 1          | PAL           | PAL-N            |                                                                                                                                                           |  |  |                                                         |   |   |   |      |       |   |     |       |                                             |  |  |
| 1          |               |                  |                                                                                                                                                           |  |  |                                                         |   |   |   |      |       |   |     |       |                                             |  |  |
| 2          | NP0           | 0                |                                                                                                                                                           |  |  |                                                         |   |   |   |      |       |   |     |       |                                             |  |  |
|            |               | 1                |                                                                                                                                                           |  |  |                                                         |   |   |   |      |       |   |     |       |                                             |  |  |
| 1          | NON           | 0                | Interlaced                                                                                                                                                |  |  | Switches between interlaced and non-interlaced displays |   |   |   |      |       |   |     |       |                                             |  |  |
|            |               | 1                | Non-interlaced                                                                                                                                            |  |  |                                                         |   |   |   |      |       |   |     |       |                                             |  |  |
| 0          | INT           | 0                | External synchronization                                                                                                                                  |  |  | Switches between external and internal synchronization  |   |   |   |      |       |   |     |       |                                             |  |  |
|            |               | 1                | Internal synchronization                                                                                                                                  |  |  |                                                         |   |   |   |      |       |   |     |       |                                             |  |  |

# LC74781, 74781M

## Second byte

| DA0 to DA7 | Register name | Register content |                                                        |         |         |                          |          | Note                                                                                                                                                          |                                           |
|------------|---------------|------------------|--------------------------------------------------------|---------|---------|--------------------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------|
|            |               | State            | Function                                               |         |         |                          |          |                                                                                                                                                               |                                           |
| 7          | —             | 0                | Second byte identification bit                         |         |         |                          |          |                                                                                                                                                               |                                           |
| 6          | —             | 0                |                                                        |         |         |                          |          |                                                                                                                                                               |                                           |
| 5          | —             | 0                |                                                        |         |         |                          |          |                                                                                                                                                               |                                           |
| 4          | BCL           | 0                | Background color present                               |         |         |                          |          |                                                                                                                                                               | Only valid with internal synchronization. |
|            |               | 1                | No background color (only the background level is set) |         |         |                          |          |                                                                                                                                                               |                                           |
| 3          | CB            | 0                | Outputs a color burst signal.                          |         |         |                          |          |                                                                                                                                                               | Only valid when BCL is high.              |
|            |               | 1                | Stops color burst signal output.                       |         |         |                          |          |                                                                                                                                                               |                                           |
| 2          | PH2           | 0                |                                                        |         |         |                          |          | <div>Sample background color phase diagram for PAL mode color burst</div>  |                                           |
|            |               | 1                |                                                        |         |         |                          |          |                                                                                                                                                               |                                           |
| 1          | PH1           | 0                | Phase 2                                                | Phase 1 | Phase 0 | Background color (phase) |          |                                                                                                                                                               |                                           |
|            |               |                  | 0                                                      | 0       | 0       | NTSC                     | PAL      |                                                                                                                                                               |                                           |
|            |               | 1                | 0                                                      | 0       | 1       | In phase*                | In phase |                                                                                                                                                               |                                           |
|            |               |                  | 0                                                      | 1       | 0       | 3π/2*                    | ∓ π/2    |                                                                                                                                                               |                                           |
| 0          | PH0           | 0                | 0                                                      | 1       | 1       | π*                       | ± π      |                                                                                                                                                               |                                           |
|            |               |                  | 1                                                      | 0       | 0       | 3π/4                     | ± 3π/4   |                                                                                                                                                               |                                           |
|            |               | 1                | 1                                                      | 0       | 1       | π/4                      | ± π/4    |                                                                                                                                                               |                                           |
|            |               |                  | 1                                                      | 1       | 0       | 7π/4                     | ∓ π/4    |                                                                                                                                                               |                                           |
|            |               | 1                | 1                                                      | 1       | 5π/4    | ∓ 3π/4                   |          |                                                                                                                                                               |                                           |

Note: The register states are all set to zero when the LC74781/M is reset with the  $\overline{\text{RST}}$  pin.

## ⑦ COMMAND6 (Synchronization signal detection setup command)

### First byte

| DA0 to DA7 | Register name | Register content |                                                                                                                | Note                                                 |
|------------|---------------|------------------|----------------------------------------------------------------------------------------------------------------|------------------------------------------------------|
|            |               | State            | Function                                                                                                       |                                                      |
| 7          | —             | 1                | Command 6 identification code<br>Synchronization signal control settings                                       |                                                      |
| 6          | —             | 1                |                                                                                                                |                                                      |
| 5          | —             | 1                |                                                                                                                |                                                      |
| 4          | —             | 0                |                                                                                                                |                                                      |
| 3          | MOD1          | 0                | Sync separator circuit signal                                                                                  | Switches the SEP <sub>OUT</sub> (pin 19) output      |
|            |               | 1                | High level output during internal synchronization                                                              |                                                      |
| 2          | MOD0          | 0                | Pin 5: Blank signal<br>Pin 8: Character signal                                                                 | Switches the BLANK (pin 5) and CHARA (pin 8) outputs |
|            |               | 1                | Pin 5: Composite synchronization signal<br>Pin 8: External synchronization signal discrimination output signal |                                                      |
| 1          | DISLIN        | 0                | 12 lines                                                                                                       | Switches the number of display lines.                |
|            |               | 1                | 10 lines                                                                                                       |                                                      |
| 0          | MUT           | 0                | Normal output                                                                                                  | Switches CV <sub>OUT</sub>                           |
|            |               | 1                | CV <sub>IN</sub> is cut and CV <sub>OUT</sub> is fixed at the pedestal level.                                  |                                                      |

# LC74781, 74781M

## Second byte

| DA0 to DA7 | Register name | Register content |                                                                                                                                                                                       |              |         |              | Note      |     |                                |                                |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |
|------------|---------------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|---------|--------------|-----------|-----|--------------------------------|--------------------------------|--------------------------------|---|---|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|            |               | State            | Function                                                                                                                                                                              |              |         |              |           |     |                                |                                |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |
| 7          | —             | 0                | Second byte identification bit                                                                                                                                                        |              |         |              |           |     |                                |                                |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |
| 6          | RN2           | 0                | <table><tr><td>RN2</td><td>RN1</td><td>RN0</td><td>Number of times HSYNC detected</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0 times</td></tr></table>                            |              |         |              | RN2       | RN1 | RN0                            | Number of times HSYNC detected | 0                              | 0 | 0 | 0 times | External synchronization signal detection control<br>Signal absent to present transition recognition<br>Setting for the sampling period when SYNC can be detected consecutively in the horizontal synchronization signal period (1H). |              |                                                                                                                                                                                                                                           |
|            |               | RN2              |                                                                                                                                                                                       |              |         |              | RN1       | RN0 | Number of times HSYNC detected |                                |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |
| 0          | 0             | 0                | 0 times                                                                                                                                                                               |              |         |              |           |     |                                |                                |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |
| 1          |               |                  |                                                                                                                                                                                       |              |         |              |           |     |                                |                                |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |
| 5          | RN1           | 0                | 0                                                                                                                                                                                     | 0            | 0 times |              |           |     |                                |                                |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |
|            |               | 1                | 0                                                                                                                                                                                     | 0            | 1       | 4 times      |           |     |                                |                                |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |
| 4          | RN0           | 0                | 0                                                                                                                                                                                     | 1            | 0       | 8 times      |           |     |                                |                                |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |
|            |               | 1                | 1                                                                                                                                                                                     | 0            | 0       | 16 times     |           |     |                                |                                |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |
| 3          | SN3           | 0                | <table><tr><td>SN3</td><td>SN2</td><td>SN1</td><td>SN0</td><td>Number of times HSYNC detected</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Not detected</td></tr></table> |              |         |              | SN3       | SN2 | SN1                            | SN0                            | Number of times HSYNC detected | 0 | 0 | 0       | 0                                                                                                                                                                                                                                     | Not detected | External synchronization signal detection control<br>Signal present to absent transition recognition<br>Setting for the sampling period when SYNC can not be detected consecutively in the horizontal synchronization signal period (1H). |
|            |               | SN3              |                                                                                                                                                                                       |              |         |              | SN2       | SN1 | SN0                            | Number of times HSYNC detected |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |
| 0          | 0             | 0                | 0                                                                                                                                                                                     | Not detected |         |              |           |     |                                |                                |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |
| 1          |               |                  |                                                                                                                                                                                       |              |         |              |           |     |                                |                                |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |
| 2          | SN2           | 0                | 0                                                                                                                                                                                     | 0            | 0       | Not detected |           |     |                                |                                |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |
|            |               | 1                | 0                                                                                                                                                                                     | 0            | 0       | 1            | 32 times  |     |                                |                                |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |
| 1          | SN1           | 0                | 0                                                                                                                                                                                     | 0            | 1       | 0            | 64 times  |     |                                |                                |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |
|            |               | 1                | 0                                                                                                                                                                                     | 1            | 0       | 0            | 128 times |     |                                |                                |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |
| 0          | SN0           | 0                | 1                                                                                                                                                                                     | 0            | 0       | 0            | 256 times |     |                                |                                |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |
|            |               | 1                |                                                                                                                                                                                       |              |         |              |           |     |                                |                                |                                |   |   |         |                                                                                                                                                                                                                                       |              |                                                                                                                                                                                                                                           |

Note: The register states are all set to zero when the LC74781/M is reset with the  $\overline{\text{RST}}$  pin.

## ⑧ COMMAND7 (Display control setup command)

### First byte

| DA0 to DA7 | Register name | Register content |                                                        | Note                                            |
|------------|---------------|------------------|--------------------------------------------------------|-------------------------------------------------|
|            |               | State            | Function                                               |                                                 |
| 7          | —             | 1                | Command 7 identification code<br>Display control setup |                                                 |
| 6          | —             | 1                |                                                        |                                                 |
| 5          | —             | 1                |                                                        |                                                 |
| 4          | —             | 1                |                                                        |                                                 |
| 3          | EX1           | 0                | MODE1 setting output                                   | Switches the SEP <sub>OUT</sub> (pin 19) output |
|            |               | 1                | PORT DATA1 setting output                              |                                                 |
| 2          | PD1           | 0                | The output is set low.                                 |                                                 |
|            |               | 1                | The output is set high.                                |                                                 |
| 1          | EX0           | 0                | MODE0 setting output                                   | Switches the BLANK (pin 5) output               |
|            |               | 1                | PORT DATA0 setting output                              |                                                 |
| 0          | PD0           | 0                | The output is set low.                                 |                                                 |
|            |               | 1                | The output is set high.                                |                                                 |

### Second byte

| DA0 to DA7 | Register name | Register content |                                          | Note                                                                                 |
|------------|---------------|------------------|------------------------------------------|--------------------------------------------------------------------------------------|
|            |               | State            | Function                                 |                                                                                      |
| 7          | —             | 0                | Second byte identification bit           |                                                                                      |
| 6          | —             | 0                |                                          |                                                                                      |
| 5          | —             | 0                |                                          |                                                                                      |
| 4          | VNPSEL        | 0                | V falling edge detection                 | Switches V acquisition polarity when internal V separation is used in external mode. |
|            |               | 1                | V rising edge detection                  |                                                                                      |
| 3          | VSPSEL        | 0                | VSEP: about 8.9 μs (for NTSC)            | Switches the internal V separation time.                                             |
|            |               | 1                | VSEP: about 17.8 μs (for NTSC)           |                                                                                      |
| 2          | MSKERS        | 0                | Mask valid                               | HSYNC and VSYNC mask release                                                         |
|            |               | 1                | Mask invalid                             |                                                                                      |
| 1          | MSKSEL        | 0                | 3H (for NTSC)                            | Switches the VSYNC mask.                                                             |
|            |               | 1                | 20H (for NTSC)                           |                                                                                      |
| 0          | EGL           | 0                | Border level 0 only (VBK0)               | Switches the border level<br>(Only valid for BLK0 = 0 and BLK1 = 1)                  |
|            |               | 1                | Border level has two stages (VBK0, VBK1) |                                                                                      |

Note: The register states are all set to zero when the LC74781/M is reset with the  $\overline{\text{RST}}$  pin.

## Display Screen Structure

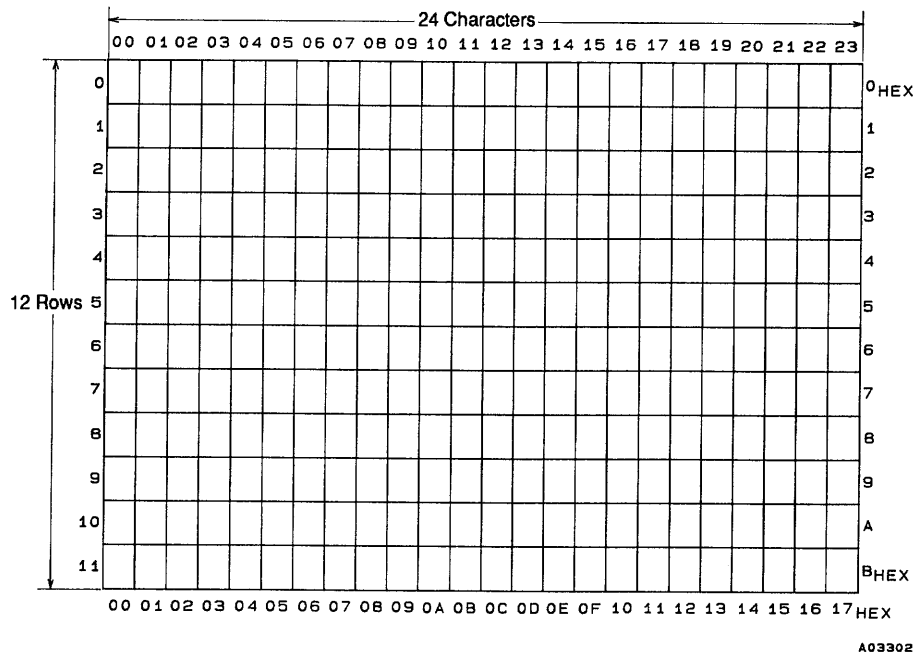
The display consists of 24 characters × 12 rows.

The maximum number of displayed character is 288.

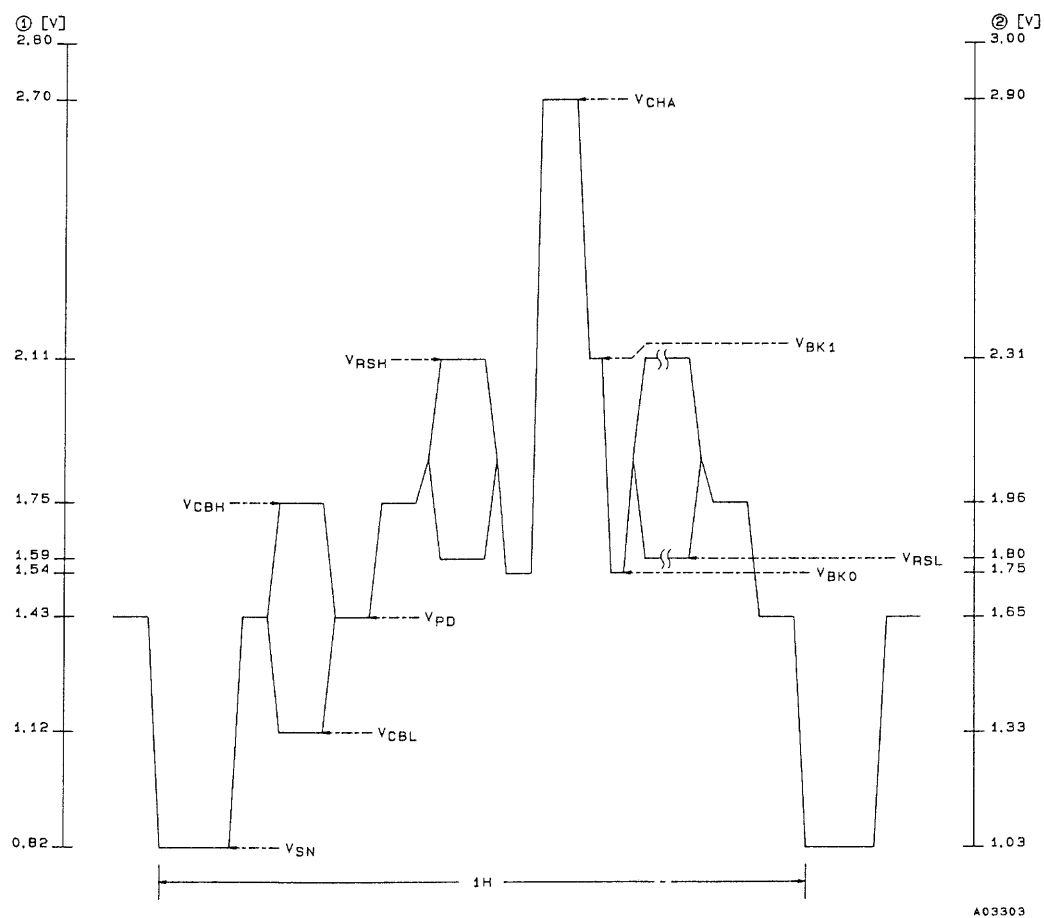
The maximum number of characters is reduced to less than 288 when the character size is enlarged.

Display memory addresses are specified as row (0 to 11 decimal) and column (0 to 23 decimal) addresses.

### Display Screen Structure (display memory addresses)



## Composite Video Signal Output Level (internally generated level)

CV<sub>OUT</sub> output level waveform ( $V_{DD2} = 5.00$  V)

| Output level                      | Output voltage ① [V] | Output voltage ② [V] |
|-----------------------------------|----------------------|----------------------|
| $V_{CHA}$ : Character             | 2.70                 | 2.90                 |
| $V_{BK1}$ : Border                | 2.11                 | 2.31                 |
| $V_{RSH}$ : Background color high | 2.11                 | 2.31                 |
| $V_{CBH}$ : Color burst high      | 1.75                 | 1.96                 |
| $V_{RSL}$ : Background color low  | 1.59                 | 1.80                 |
| $V_{BK0}$ : Border                | 1.54                 | 1.75                 |
| $V_{PD}$ : Pedestal               | 1.43                 | 1.65                 |
| $V_{CBL}$ : Color burst low       | 1.12                 | 1.33                 |
| $V_{SN}$ : Sync                   | 0.82                 | 1.03                 |

 $V_{DD2} = 5.00$  V

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