

FEATURES

isoPower integrated, isolated dc-to-dc converter
100 mA output current for ADuM5020
60 mA output current for ADuM5028
 Meets CISPR22 Class B emissions limits at full load on a 2-layer PCB
16-lead SOIC_W package with 7.8 mm minimum creepage
8-lead SOIC_IC package with 8.3 mm minimum creepage
High temperature operation: 125°C maximum
Safety and regulatory approvals
 UL recognition (pending)
 3000 V rms for 1 minute per UL 1577
 CSA Component Acceptance Notice 5A (pending)
 VDE certificate of conformity (pending)
 VDE V 0884-10
 $V_{IORM} = 565$ V peak
 CQC certification per GB4943.1-2011

APPLICATIONS

RS-485/RS-422/CAN transceiver power
 Power supply start-up bias and gate drives
 Isolated sensor interfaces
 Industrial PLCs

GENERAL DESCRIPTION

The ADuM5020 and ADuM5028¹ are *isoPower*®, integrated, isolated dc-to-dc converters. Based on the Analog Devices, Inc., *iCoupler*® technology, these dc-to-dc converters provide regulated, isolated power that is below CISPR22 Class B limits at full load on a 2-layer printed circuit board (PCB) with ferrites. Common voltage combinations and the associated current output levels are shown in Table 1 through Table 4.

The ADuM5020 and ADuM5028 eliminate the need to design and build isolated dc-to-dc converters in applications up to 500 mW. The *iCoupler* chip scale transformer technology is used

FUNCTIONAL BLOCK DIAGRAMS

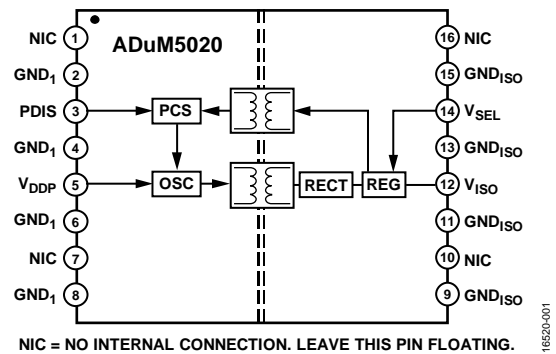


Figure 1. ADuM5020 Functional Block Diagram

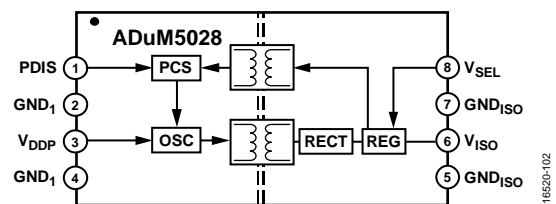


Figure 2. ADuM5028 Functional Block Diagram

for the magnetic components of the dc-to-dc converter. The result is a small form factor, isolated solution.

The ADuM5020 and ADuM5028 isolated dc-to-dc converters provide two different package variants: the ADuM5020 in a wide body, 16-lead SOIC_W package, and the ADuM5028 in the space saving, 8-lead, wide body SOIC_IC. See the Pin Configuration and Function Descriptions section and the Ordering Guide for more information.

¹ Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

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REVISION HISTORY

6/2018—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/5 V SECONDARY ISOLATED SUPPLY

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DDP} = V_{ISO} = 5\text{ V}$. Minimum and maximum specifications apply over the entire recommended operation range, which is $4.5\text{ V} \leq V_{DDP} \leq 5.5\text{ V}$, $4.5\text{ V} \leq V_{ISO} \leq 5.5\text{ V}$, and $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted.

Table 1. ADuM5020 DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V_{ISO}	4.75	5.0	5.25	V	V_{ISO} output current (I_{ISO}) = 10 mA
Line Regulation	V_{ISO} (LINE)		2		mV/V	$I_{ISO} = 50\text{ mA}$, $V_{DDP} = 4.5\text{ V}$ to 5.5 V
Load Regulation ¹	V_{ISO} (LOAD)		1	5	%	$I_{ISO} = 10\text{ mA}$ to 90 mA
Output Ripple ¹	V_{ISO} (RIP)		75		mV p-p	20 MHz bandwidth, bypass output capacitance (C_{BO}) = $0.1\text{ }\mu\text{F} 10\text{ }\mu\text{F}$, $I_{ISO} = 90\text{ mA}$
Output Noise ¹	V_{ISO} (NOISE)		200		mV p-p	$C_{BO} = 0.1\text{ }\mu\text{F} 10\text{ }\mu\text{F}$, $I_{ISO} = 90\text{ mA}$
Switching Frequency	f_{OSC}		180		MHz	
Pulse-Width Modulation (PWM) Frequency	f_{PWM}		625		kHz	
Output Supply Current ¹	I_{ISO} (MAX)	50			mA	$4.75\text{ V} < V_{ISO} < 5.25\text{ V}$
		100			mA	$4.5\text{ V} < V_{ISO} < 5.25\text{ V}$
Efficiency at I_{ISO} (MAX) ¹			33		%	$I_{ISO} = 100\text{ mA}$
V_{DDP} Supply Current						
No V_{ISO} Load	I_{DDP} (Q)		8	25	mA	
Full V_{ISO} Load	I_{DDP} (MAX)		310		mA	
Thermal Shutdown						
Shutdown Temperature			154		$^\circ\text{C}$	
Thermal Hysteresis			10		$^\circ\text{C}$	

¹ Maximum V_{ISO} output current is derated by $1.75\text{ mA}/^\circ\text{C}$ for $T_A > 85^\circ\text{C}$.

Table 2. ADuM5028 DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V _{ISO}	4.75	5.0	5.25	V	I _{ISO} = 10 mA
Line Regulation	V _{ISO} (LINE)		2		mV/V	I _{ISO} = 30 mA, V _{DDP} = 4.5 V to 5.5 V
Load Regulation ¹	V _{ISO} (LOAD)		1	5	%	I _{ISO} = 10 mA to 54 mA
Output Ripple ¹	V _{ISO} (RIP)		75		mV p-p	20 MHz bandwidth, C _{BO} = 0.1 μF 10 μF, I _{ISO} = 54 mA
Output Noise ¹	V _{ISO} (NOISE)		200		mV p-p	C _{BO} = 0.1 μF 10 μF, I _{ISO} = 54 mA
Switching Frequency	f _{OSC}		180		MHz	
PWM Frequency	f _{PWM}		625		kHz	
Output Supply Current ¹	I _{ISO} (MAX)	60			mA	4.75 V < V _{ISO} < 5.25 V
Efficiency at I _{ISO} (MAX) ¹			33		%	I _{ISO} = 60 mA
V _{DDP} Supply Current						
No V _{ISO} Load	I _{DDP} (Q)		8	25	mA	
Full V _{ISO} Load	I _{DDP} (MAX)		310		mA	
Thermal Shutdown						
Shutdown Temperature			154		°C	
Thermal Hysteresis			10		°C	

¹ Maximum V_{ISO} output current is derated by $1\text{ mA}/^\circ\text{C}$ for $T_A > 85^\circ\text{C}$.

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DDP} = 5.0\text{ V}$, $V_{ISO} = 3.3\text{ V}$. Minimum/maximum specifications apply over the entire recommended operation range, which is $4.5\text{ V} \leq V_{DDP} \leq 5.5\text{ V}$, $3.0\text{ V} \leq V_{ISO} \leq 3.6\text{ V}$, and $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted.

Table 3. ADuM5020 DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V_{ISO}	3.135	3.3	3.465	V	$I_{ISO} = 10\text{ mA}$
Line Regulation	$V_{ISO}(\text{LINE})$		2		mV/V	$I_{ISO} = 50\text{ mA}$, $V_{DDP} = 3.0\text{ V to }3.6\text{ V}$
Load Regulation ¹	$V_{ISO}(\text{LOAD})$		1	5	%	$I_{ISO} = 10\text{ mA to }90\text{ mA}$
Output Ripple ¹	$V_{ISO}(\text{RIP})$		50		mV p-p	20 MHz bandwidth, $C_{BO} = 0.1\text{ }\mu\text{F} 10\text{ }\mu\text{F}$, $I_{ISO} = 90\text{ mA}$
Output Noise ¹	$V_{ISO}(\text{NOISE})$		130		mV p-p	$C_{BO} = 0.1\text{ }\mu\text{F} 10\text{ }\mu\text{F}$, $I_{ISO} = 90\text{ mA}$
Switching Frequency	f_{OSC}		180		MHz	
PWM Frequency	f_{PWM}		625		kHz	
Output Supply Current ¹	$I_{ISO}(\text{MAX})$	50			mA	$3.135\text{ V} < V_{ISO} < 3.465\text{ V}$
		100			mA	$3.0\text{ V} < V_{ISO} < 3.465\text{ V}$
Efficiency at $I_{ISO}(\text{MAX})$ ¹			27		%	$I_{ISO} = 100\text{ mA}$
V_{DDP} Supply Current						
No V_{ISO} Load	$I_{DDP}(\text{Q})$		5	18	mA	
Full V_{ISO} Load	$I_{DDP}(\text{MAX})$		250		mA	
Thermal Shutdown						
Shutdown Temperature			154		$^\circ\text{C}$	
Thermal Hysteresis			10		$^\circ\text{C}$	

¹ Maximum V_{ISO} output current is derated by $1.75\text{ mA}/^\circ\text{C}$ for $T_A > 85^\circ\text{C}$.

Table 4. ADuM5028 DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V _{ISO}	3.135	3.3	3.465	V	I _{ISO} = 10 mA
Line Regulation	V _{ISO} (LINE)		2		mV/V	I _{ISO} = 30 mA, V _{DDP} = 3.0 V to 3.6 V
Load Regulation ¹	V _{ISO} (LOAD)		1	5	%	I _{ISO} = 10 mA to 54 mA
Output Ripple ¹	V _{ISO} (RIP)		50		mV p-p	20 MHz bandwidth, C _{BO} = 0.1 μF 10 μF, I _{ISO} = 54 mA
Output Noise ¹	V _{ISO} (NOISE)		130		mV p-p	C _{BO} = 0.1 μF 10 μF, I _{ISO} = 54 mA
Switching Frequency	f _{OSC}		180		MHz	
PWM Frequency	f _{PWM}		625		kHz	
Output Supply Current ¹	I _{ISO} (MAX)	60			mA	3.135 V < V _{ISO} < 3.465 V
Efficiency at I _{ISO} (MAX) ¹			27		%	I _{ISO} = 60 mA
V _{DDP} Supply Current						
No V _{ISO} Load	I _{DDP} (Q)		5	18	mA	
Full V _{ISO} Load	I _{DDP} (MAX)		250		mA	
Thermal Shutdown						
Shutdown Temperature			154		°C	
Thermal Hysteresis			10		°C	

¹ Maximum V_{ISO} output current is derated by $1\text{ mA}/^\circ\text{C}$ for $T_A > 85^\circ\text{C}$.

REGULATORY APPROVALS

Table 5.

UL (Pending) ¹	CSA (Pending)	VDE (Pending) ²	CQC (Pending)
Recognized Under 1577 Component Recognition Program ¹ Single Protection, 3000 V rms Isolation Voltage	Approved under CSA Component Acceptance Notice 5A CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2 Basic insulation at 780 V rms (1103 V peak) Reinforced insulation at 390 V rms (552 V peak) IEC 60601-1 Edition 3.1: Basic insulation (1 means of patient protection (1 MOPP)), 585 V rms (827 V peak) CSA 61010-1-12 and IEC 61010-1 third edition: Basic insulation at 300 V rms mains, 780 V rms (1103 V peak) Reinforced insulation at 300 V rms mains, 390 V rms (552 V peak)	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 Reinforced insulation 565 V peak, surge isolation voltage (V_{IOSM}) = 6000 V peak Transient voltage (V_{IOTM}) = 4242 V peak	Certified under CQC11-471543-2012 GB4943.1-2011: Basic insulation at 780 V rms (1103 V peak) Reinforced insulation at 390 V rms (552 V peak)
File E214100	File 205078	File 2471900-4880-0001	File (pending)

¹ In accordance with UL 1577, each ADuM5020 and ADuM5028 are proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec.

² In accordance with DIN V VDE V 0884-10, each ADuM5020 and ADuM5028 are proof tested by applying an insulation test voltage ≥ 1059 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 6. ADuM5020 Insulation and Safety

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	7.8	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	7.8	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		25.5	μm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN IEC 112/VDE 0303 Part 1
Material Group		I		Material Group (DIN VDE 0110, 1/89, Table 1)

Table 7. ADuM5028 Insulation and Safety

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	8.3	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		25.5	μm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN IEC 112/VDE 0303 Part 1
Material Group		I		Material Group (DIN VDE 0110, 1/89, Table 1)

PACKAGE CHARACTERISTICS

Table 8. ADuM5020 Package Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output) ¹	R _{I-O}		10 ¹³		Ω	f = 1 MHz
Capacitance (Input to Output) ¹	C _{I-O}		2.2		pF	
Input Capacitance ²	C _I		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ _{JA}		45		°C/W	Thermocouple located at center of package underside ³

¹ This device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

² Input capacitance is from any input data pin to ground.

³ The value of θ_{JA} is based on devices mounted on a JEDEC JESD-51 standard 2s2p board and still air.

Table 9. ADuM5028 Package Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output) ¹	R _{I-O}		10 ¹³		Ω	f = 1 MHz
Capacitance (Input to Output) ¹	C _{I-O}		2.2		pF	
Input Capacitance ²	C _I		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ _{JA}		80		°C/W	Thermocouple located at center of package underside ³

¹ This device is considered a 2-terminal device: Pin 1 through Pin 4 are shorted together, and Pin 5 through Pin 8 are shorted together.

² Input capacitance is from any input data pin to ground.

³ The value of θ_{JA} is based on devices mounted on a JEDEC JESD-51 standard 2s2p board and still air.

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by the protective circuits. The asterisk (*) marking on packages denotes DIN V VDE V 0884-10 approval.

Table 10. ADuM5020 VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110			I to IV	
For Rated Mains Voltage ≤ 150 V rms			I to III	
For Rated Mains Voltage ≤ 300 V rms			I to II	
For Rated Mains Voltage ≤ 400 V rms			40/125/21	
Climatic Classification			2	
Pollution Degree per DIN VDE 0110, Table 1				
Maximum Working Insulation Voltage		V _{IORM}	565	V peak
Input to Output Test Voltage, Method b1	V _{IORM} × 1.875 = V _{PR} , 100% production test, t _m = 1 sec, partial discharge < 5 pC	V _{PR}	1059	V peak
Input to Output Test Voltage, Method a		V _{PR}		
After Environmental Tests Subgroup 1	V _{IORM} × 1.5 = V _{pd(m)} , t _{ini} = 60 sec, t _m = 10 sec, partial discharge < 5 pC	V _{pd(m)}	848	V peak
After Input or Safety Test Subgroup 2 and Subgroup 3	V _{IORM} × 1.2 = V _{pd(m)} , t _{ini} = 60 sec, t _m = 10 sec, partial discharge < 5 pC	V _{pd(m)}	678	V peak
Highest Allowable Overvoltage	Transient overvoltage, t _{TR} = 10 sec	V _{IOTM}	4242	V peak
Withstand Isolation Voltage	1 minute withstand rating	V _{ISO}	3000	V rms
Surge Isolation Voltage Reinforced	V _{IOSM(TEST)} = 10 kV; 1.2 μs rise time; 50 μs, 50% fall time	V _{IOSM}	6000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Case Temperature		T _S	150	°C
Total Power Dissipation at 25°C		I _{S1}	2.78	W
Insulation Resistance at T _S	V _{IO} = 500 V	R _S	>10 ⁹	Ω

Table 11. ADuM5028 VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms			I to IV I to III I to II	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	565	V peak
Input to Output Test Voltage, Method b1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, $t_m = 1$ sec, partial discharge < 5 pC	V_{PR}	1059	V peak
Input to Output Test Voltage, Method a		V_{PR}		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	848	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	678	V peak
Highest Allowable Overvoltage	Transient overvoltage, $t_{TR} = 10$ sec	V_{IOTM}	4242	V peak
Withstand Isolation Voltage	1 minute withstand rating	V_{ISO}	3000	V rms
Surge Isolation Voltage Reinforced	$V_{IOSM(TEST)} = 10$ kV; 1.2 μ s rise time; 50 μ s, 50% fall time	V_{IOSM}	6000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 4)			
Case Temperature		T_S	150	$^{\circ}\text{C}$
Total Power Dissipation at 25 $^{\circ}\text{C}$		I_{S1}	1.56	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

RECOMMENDED OPERATING CONDITIONS

Table 12.

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature ¹	T _A	−40		+125	°C
Supply Voltages ²	V _{DDP}				
V _{DDP} at V _{ISO} = 3.135 V to 3.465 V		4.5		5.5	V
V _{DDP} at V _{ISO} = 4.75 V to 5.25 V		4.5		5.5	V

¹ Operation at >85°C requires reduction of the maximum load current.
² Each voltage is relative to its respective ground.

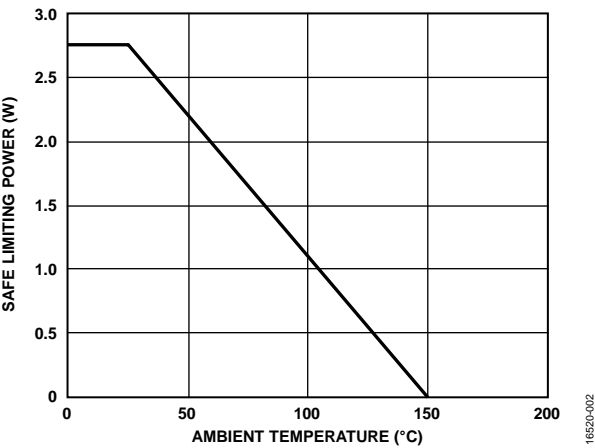


Figure 3. ADuM5020 Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

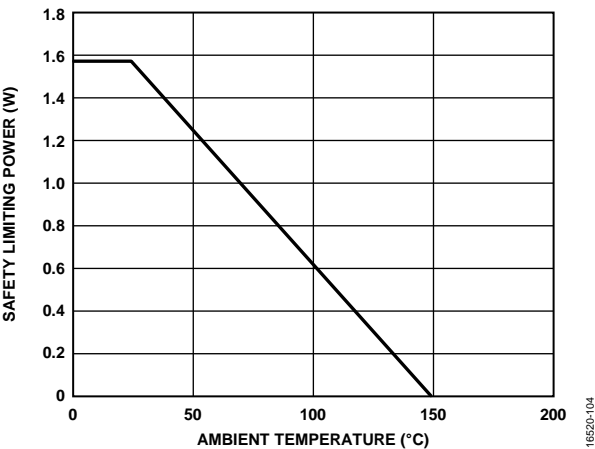


Figure 4. ADuM5028 Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 13.

Parameter	Rating
Storage Temperature (T_{ST})	-55°C to $+150^\circ\text{C}$
Ambient Operating Temperature (T_A)	-40°C to $+125^\circ\text{C}$
Supply Voltages (V_{DDP} , V_{ISO}) ¹	-0.5 V to $+7.0\text{ V}$
V_{ISO} Supply Current	
ADuM5020	100 mA
ADuM5028	60 mA
Input Voltage ($PDIS$, V_{SEL}) ^{1, 2}	-0.5 V to $V_{DDI} + 0.5\text{ V}$
Common-Mode Transients ³	$-200\text{ kV}/\mu\text{s}$ to $+200\text{ kV}/\mu\text{s}$

¹ All voltages are relative to their respective ground.

² V_{DDI} is the input side supply voltage.

³ Common-mode transients refer to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 14. Maximum Continuous Working Voltage Supporting 50-Year Minimum Lifetime¹

Parameter	Max	Unit	Applicable Certification
AC Voltage			
Bipolar Waveform	560	V peak	50-year operation
Unipolar Waveform			
Basic Insulation	560	V peak	50-year operation
DC Voltage			
Basic Insulation	1000	V peak	50-year operation

¹ Maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

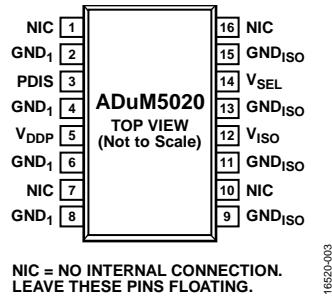


Figure 5. Pin Configuration

Table 15. ADuM5020 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7, 10, 16	NIC	No Internal Connection. Leave these pins floating.
2, 4, 6, 8	GND ₁	Ground 1. Ground reference for the primary. It is recommended that these pins be connected to a common ground.
3	PDIS	Power Disable. When tied to any GND ₁ pin, the V _{ISO} output voltage is active. When a logic high voltage is applied, the V _{ISO} output voltage is shut down. Do not leave this pin floating.
5	V _{DDP}	Primary Supply Voltage, 4.5 V to 5.5 V.
9, 11, 13, 15	GND _{ISO}	Ground Reference for V _{ISO} on Side 2. It is recommended that these pins be connected to a common ground.
12	V _{ISO}	Secondary Supply Voltage Output for External Loads.
14	V _{SEL}	Output Voltage Selection.

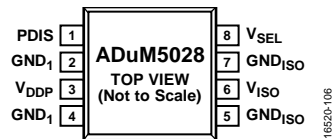


Figure 6. ADuM5028 Pin Configuration

Table 16. ADuM5028 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PDIS	Power Disable. When tied to any GND ₁ pin, the V _{ISO} output voltage is active. When a logic high voltage is applied, the V _{ISO} output voltage is shut down. Do not leave this pin floating.
2, 4	GND ₁	Ground 1. Ground reference for the primary. It is recommended that these pins be connected to a common ground.
3	V _{DDP}	Primary Supply Voltage, 4.5 V to 5.5 V.
5, 7	GND _{ISO}	Ground Reference for V _{ISO} on Side 2. It is recommended that these pins be connected together.
6	V _{ISO}	Secondary Supply Voltage Output for External Loads.
8	V _{SEL}	Output Voltage Selection. Connect V _{SEL} to V _{ISO} for 5 V output or connect V _{SEL} to GND _{ISO} for 3.3 V output. This pin has a weak internal pull-up; therefore, do not leave this pin floating.

TRUTH TABLE

Table 17. Truth Table (Positive Logic)

V _{DDP} (V)	V _{SEL} Input	PDIS Input	V _{ISO} Output (V)
5	High	Low	5
5	Don't care	High	0
5	Low	Low	3.3
5	Don't care	High	0

TYPICAL PERFORMANCE CHARACTERISTICS

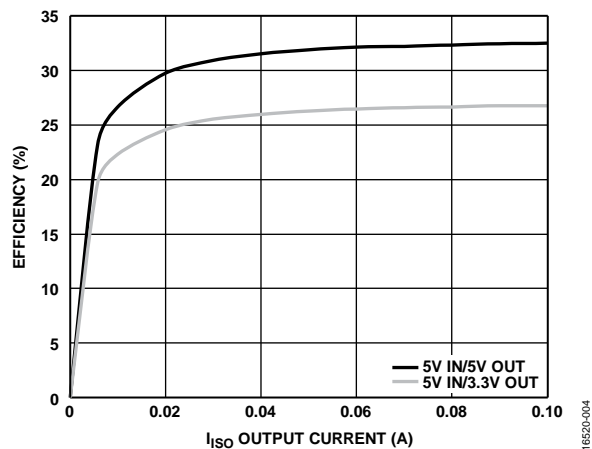
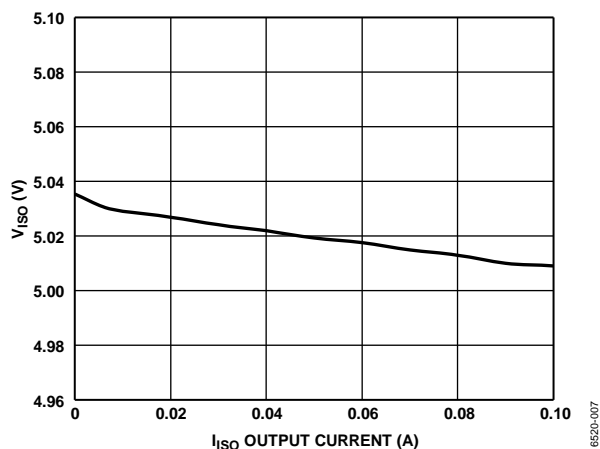
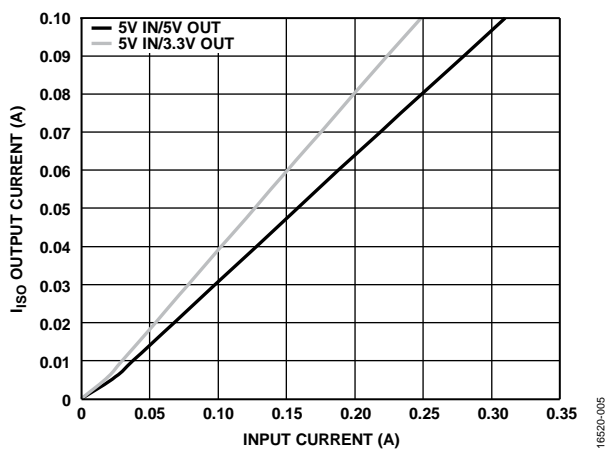
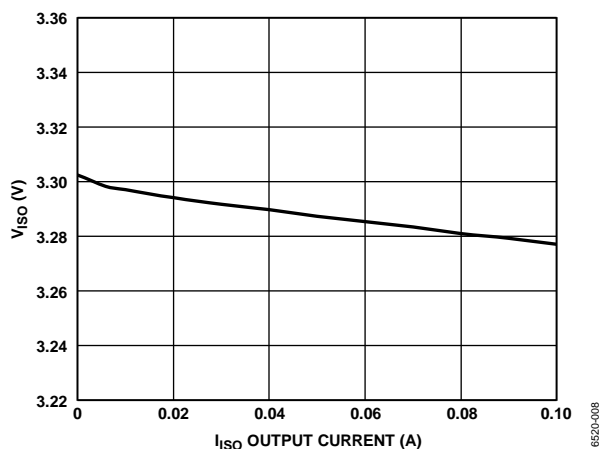
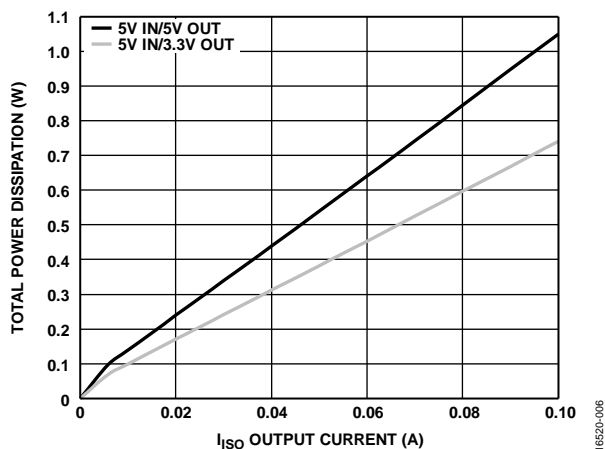
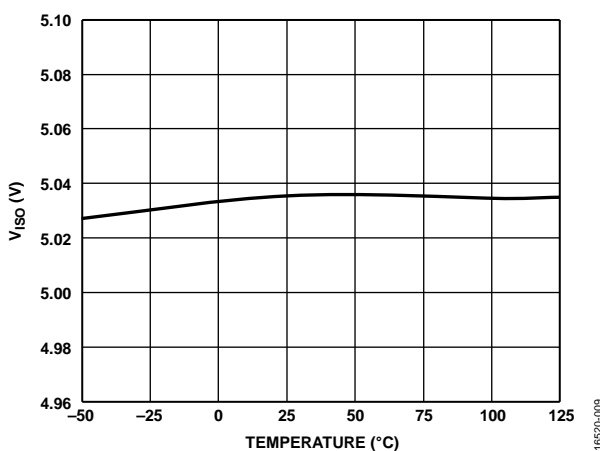


Figure 7. Typical Power Supply Efficiency in Supported Supply Configurations

Figure 10. V_{ISO} vs. I_{ISO} Output Current, Input = 5 V, V_{ISO} = 5 VFigure 8. I_{ISO} Output Current vs. Input Current in Supported Power ConfigurationsFigure 11. V_{ISO} vs. I_{ISO} Output Current, Input = 5 V, V_{ISO} = 3.3 VFigure 9. Total Power Dissipation vs. I_{ISO} Output Current in Supported Power ConfigurationsFigure 12. V_{ISO} vs. Temperature, Input = 5 V, V_{ISO} Output = 5 V

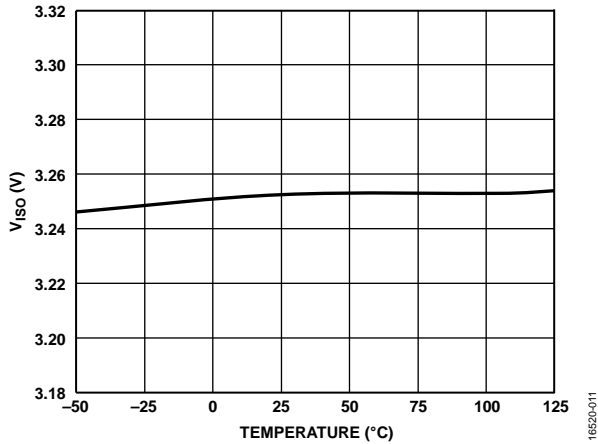


Figure 13. V_{ISO} vs. Temperature, Input = 3.3 V, V_{ISO} Output = 3.3 V

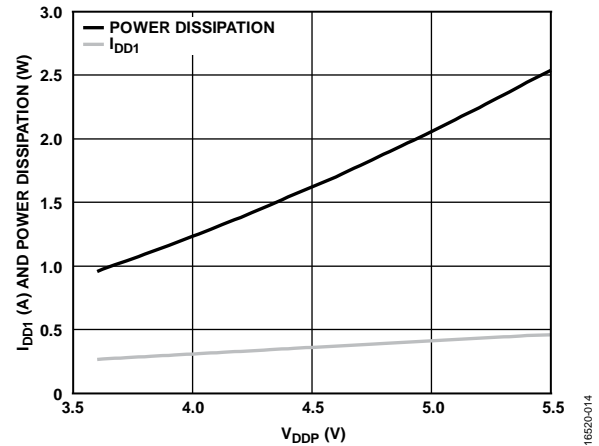


Figure 16. Short-Circuit Input Current (I_{DD1}) and Power Dissipation vs. V_{DDP}

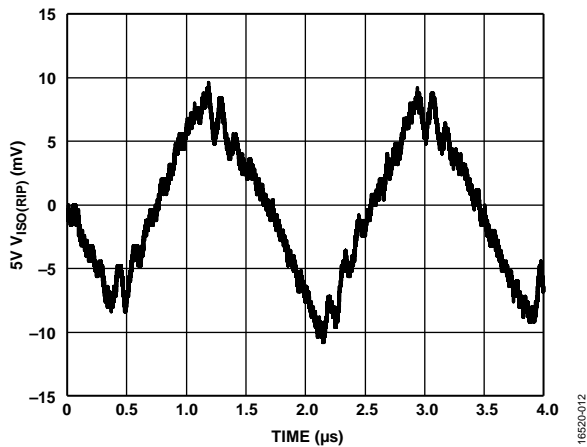


Figure 14. V_{ISO} Ripple, 5 V Input to 5 V Output at 90% Load, Bandwidth = 20 MHz

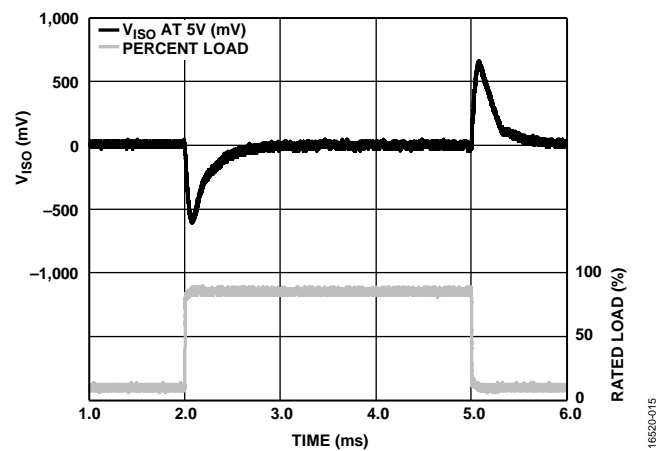


Figure 17. V_{ISO} Transient Load Response 5 V Input to 5 V Output 10% to 90% Load Step

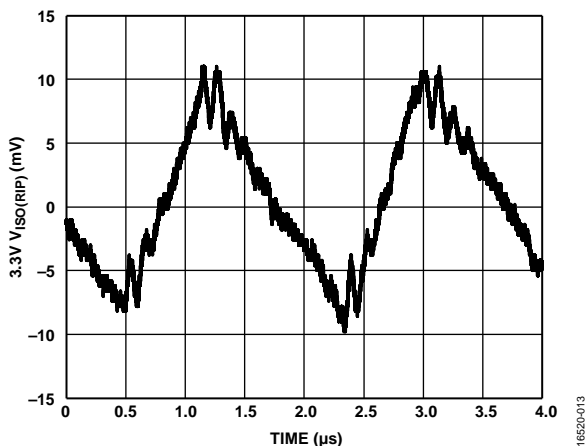


Figure 15. V_{ISO} Ripple, 5 V Input to 3.3 V Output at 90% Load, Bandwidth = 20 MHz

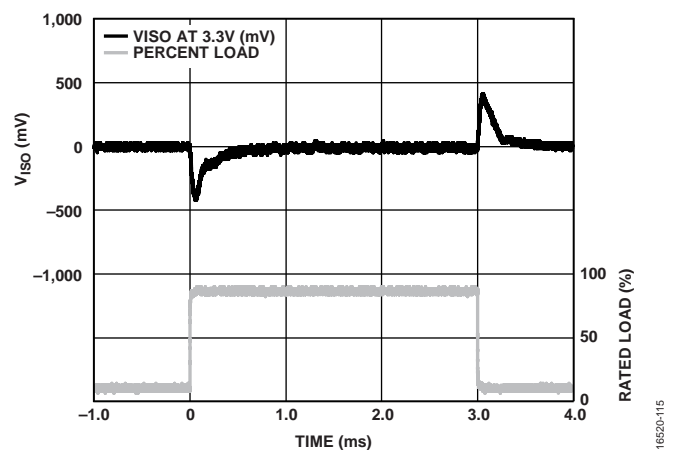


Figure 18. V_{ISO} Transient Load Response 5 V Input to 3.3 V Output, 10% to 90% Load Step

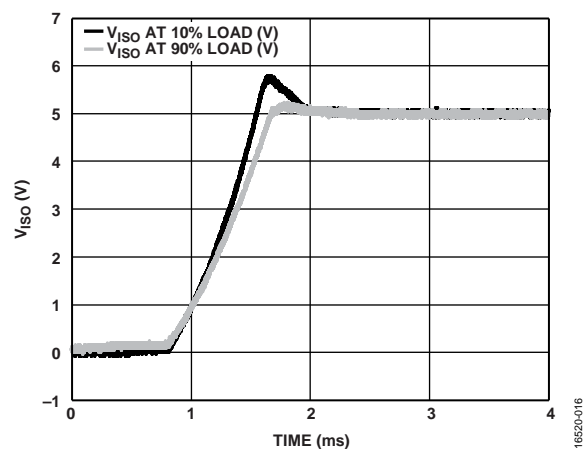


Figure 19. 5 V Input to 5 V Output V_{ISO} Start-Up Transient at 10% and 90% Load

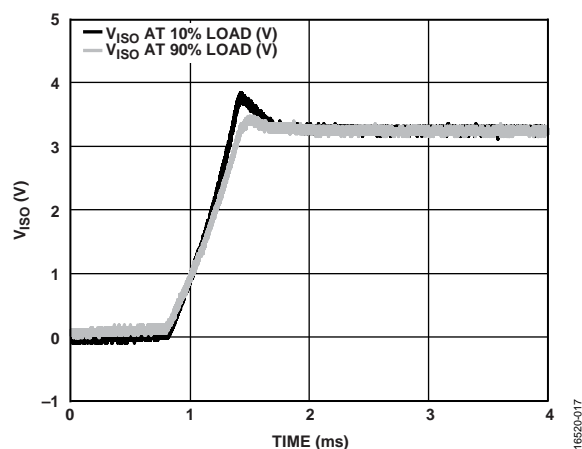


Figure 20. 5 V Input to 3.3 V Output V_{ISO} Start-Up Transient at 10% and 90% Load

THEORY OF OPERATION

The ADuM5020/ADuM5028 dc-to-dc work on principles that are common to most standard power supplies. The converters have a split controller architecture with isolated PWM feedback. VDDP power is supplied to an oscillating circuit that switches current into a chip scale air core transformer. Power transferred to the secondary side is rectified and regulated to 3.3 V or 5.0 V, depending on the setting of the V_{SEL} pin. The secondary (V_{ISO}) side controller regulates the output by creating a PWM control signal that is sent to the primary (V_{DDP}) side by a dedicated

*i*Coupler data channel. The PWM modulates the oscillator circuit to control the power being sent to the secondary side. Feedback allows significantly higher power and efficiency.

The ADuM5020/ADuM5028 implement undervoltage lockout (UVLO) with hysteresis on the primary and secondary side input and output pins as well as the V_{DDP} power input. The UVLO feature ensures that the converters do not go into oscillation due to noisy input power or slow power-on ramp rates.

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM5020 and ADuM5028 *isoPower* integrated dc-to-dc converters require power supply bypassing at the input and output supply pins (see Figure 25 and Figure 26). Low effective series resistance (ESR) 0.1 μF bypass capacitors are required between the V_{DDP} pin and GND_1 pin, as close to the chip pads as possible. Low ESR 0.1 μF or 0.22 μF capacitors are required between the V_{ISO} pin and GND_{ISO} pin, as close to the chip pads as possible (see the C_{ISO} note in Figure 23 and Figure 24 for more information). The *isoPower* inputs require multiple passive components to bypass the power effectively, as well as set the output voltage and bypass the core voltage regulator (see Figure 21 through Figure 26).

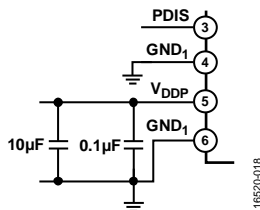


Figure 21. ADuM5020 V_{DDP} Bias and Bypass Components

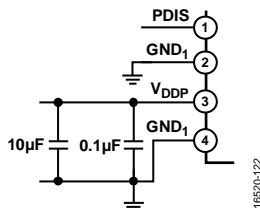
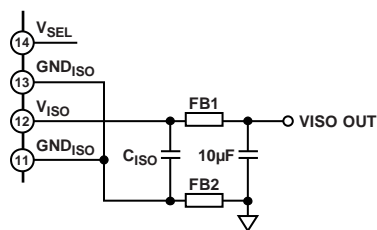
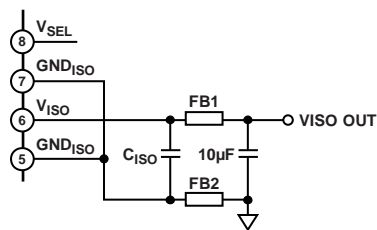


Figure 22. ADuM5028 V_{DDP} Bias and Bypass Components



$C_{ISO} = 0.1\mu\text{F}$ FOR $V_{DDP} = 5\text{V}$ AND $V_{ISO} = 5\text{V}$,
 $C_{ISO} = 0.22\mu\text{F}$ FOR $V_{DDP} = 5\text{V}$ AND $V_{ISO} = 3.3\text{V}$

Figure 23. ADuM5020 V_{ISO} Bias and Bypass Components



$C_{ISO} = 0.1\mu\text{F}$ FOR $V_{DDP} = 5\text{V}$ AND $V_{ISO} = 5\text{V}$,
 $C_{ISO} = 0.22\mu\text{F}$ FOR $V_{DDP} = 5\text{V}$ AND $V_{ISO} = 3.3\text{V}$

Figure 24. ADuM5028 V_{ISO} Bias and Bypass Components

The power supply section of the ADuM5020 and ADuM5028 uses a 180 MHz oscillator frequency to efficiently pass power through its chip scale transformers. Bypass capacitors are required

for several operating frequencies. Noise suppression requires a low inductance, high frequency capacitor, whereas ripple suppression and proper regulation require a large value capacitor. These capacitors are most conveniently connected between the V_{DDP} pin and GND_1 pin, and between the V_{ISO} pin and GND_{ISO} pin. To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required. The recommended capacitor values are 0.1 μF and 10 μF for V_{DDP} and V_{ISO} . The smaller capacitor must have a low ESR. For example, use of a ceramic capacitor is advised. The total lead length between the ends of the 0.1 μF low ESR capacitors, and the power supply pins must not exceed 2 mm.

To reduce the level of electromagnetic radiation, the impedance to high frequency currents between the V_{ISO} and GND_{ISO} pins and the PCB trace connections can be increased. Using this method of electromagnetic interference (EMI) suppression controls the radiating signal at its source by placing surface-mount ferrite beads in series with the V_{ISO} and GND_{ISO} pins, as shown in Figure 25 and Figure 26. The impedance of the ferrite bead is chosen to be about 1.8 k Ω between the 100 MHz and 1 GHz frequency range to reduce the emissions at the 180 MHz primary switching frequency and the 360 MHz secondary side rectifying frequency and harmonics. See Table 18 for examples of appropriate surface-mount ferrite beads.

Table 18. Surface-Mount Ferrite Beads Example

Manufacturer	Part No.
Taiyo Yuden	BKH1005LM182-T
Murata Electronics	BLM15HD182SN1

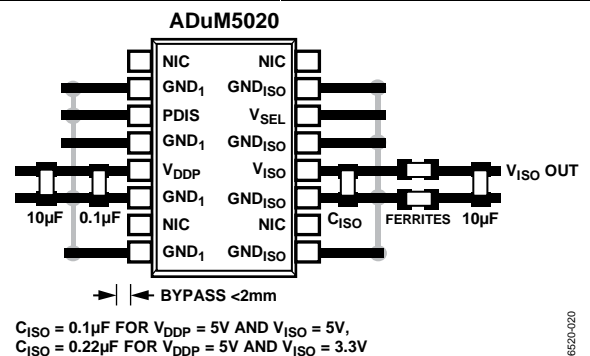


Figure 25. Recommended ADuM5020 PCB Layout

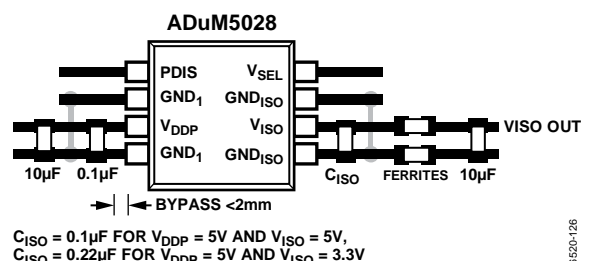


Figure 26. Recommended ADuM5028 PCB Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling

that does occur equally affects all pins on a given component side. Failure to ensure these steps can cause voltage differentials between pins, exceeding the absolute maximum ratings specified in Table 13, thereby leading to latch-up or permanent damage.

THERMAL ANALYSIS

The ADuM5020 and ADuM5028 each consist of three internal die attached to a split lead frame. For thermal analysis, the die is treated as a thermal unit, with the highest junction temperature reflected in the θ_{JA} values, shown in Table 8 and Table 9. The value of θ_{JA} is based on measurements taken with the devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air. Under normal operating conditions, the ADuM5020 and ADuM5028 can operate at full load, but at temperatures greater than 85°C, derating the output current may be needed, as shown in Figure 3 and Figure 4.

EMI CONSIDERATIONS

The ADuM5020/ADuM5028 dc-to-dc converters must, of necessity, operate at a high frequency to allow efficient power transfer through the small transformers. This high frequency operation creates high frequency currents that can propagate in circuit board ground and power planes, requiring proper power supply bypassing at the input and output supply pins (see Figure 25 and Figure 26). Using proper layout, bypassing techniques, and surface-mount ferrite beads in series with the V_{ISO} and GND_{ISO} pins, the dc-to-dc converters are designed to provide regulated, isolated power that is below CISPR22 Class B limits at full load on a 2-layer PCB with ferrites.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation, as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group

ratings are more resistant to surface tracking and, therefore, can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. The material group and creepage for the ADuM5020 and ADuM5028 are presented in Table 6 and Table 7.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by its thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling show that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be grouped into broad categories, such as dc stress, which causes very little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on a 60 Hz sinusoidal waveform because this stress reflects isolation from line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the barrier as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as shown in Equation 2. For insulation wear out with the polyimide materials used in these products, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\ RMS}^2 + V_{DC}^2} \quad (1)$$

or

$$V_{AC\ RMS} = \sqrt{V_{RMS}^2 - V_{DC}^2} \quad (2)$$

where:

V_{RMS} is the total rms working voltage.

$V_{AC\ RMS}$ is the time varying portion of the working voltage.

V_{DC} is the dc offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 V ac rms and a 400 V dc bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance, and lifetime of a device, see Figure 27 and the following equations.

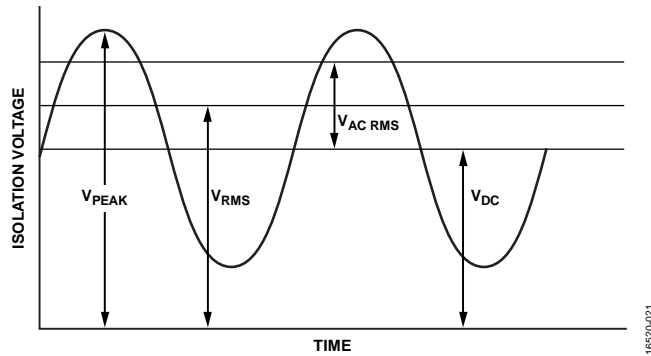


Figure 27. Critical Voltage Example

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{V_{AC RMS}^2 + V_{DC}^2}$$

$$V_{RMS} = \sqrt{240^2 + 400^2}$$

$$V_{RMS} = 466 \text{ V}$$

This V_{RMS} value is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the ac rms voltage, use Equation 2.

$$V_{AC RMS} = \sqrt{V_{RMS}^2 - V_{DC}^2}$$

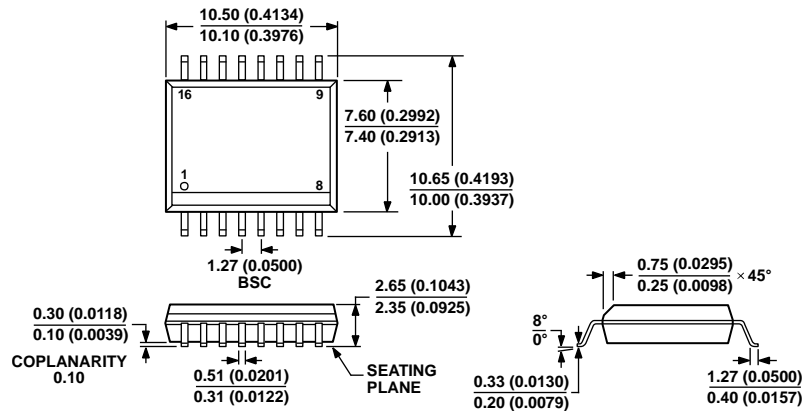
$$V_{AC RMS} = \sqrt{466^2 - 400^2}$$

$$V_{AC RMS} = 240 \text{ V rms}$$

In this case, the ac rms voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The value is compared to the limits for working voltage in Table 14 for the expected lifetime, which is less than a 60 Hz sine wave, and it is well within the limit for a 50-year service life.

Note that the dc working voltage limit is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 28. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimensions shown in millimeters and (inches)

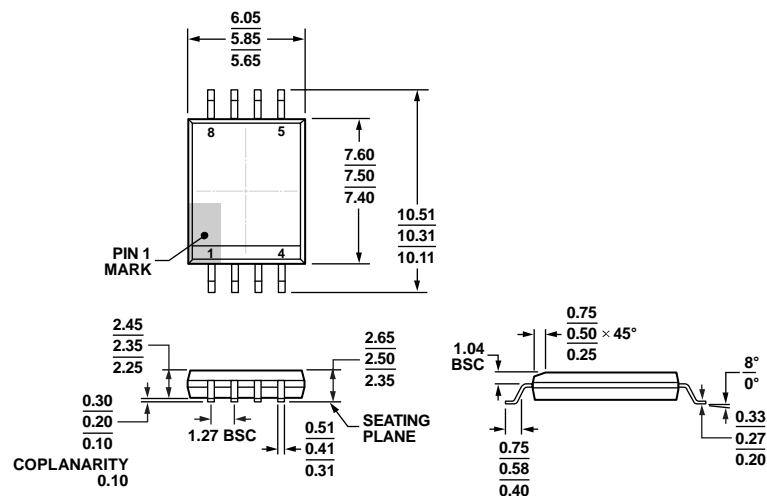


Figure 29. 8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]
Wide Body
(RI-8-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model ^{1,2,3}	Typical V _{DDP} Voltage (V)	Temperature Range	Package Description	Package Option
ADuM5020-5BRWZ	5.0	−40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM5020-5BRWZ-RL	5.0	−40°C to +125°C	16-Lead SOIC_W	RW-16
ADuM5028-5BRIZ	5.0	−40°C to +125°C	8-Lead SOIC_IC	RI-8-1
ADuM5028-5BRIZ-RL	5.0	−40°C to +125°C	8-Lead SOIC_IC	RI-8-1
EVAL-ADuM5020EBZ			ADuM5020 Evaluation Board	
EVAL-ADuM5028EBZ			ADuM5028 Evaluation Board	

¹ Z = RoHS Compliant Part.

² The EVAL-ADuM5020EBZ is packaged with the ADuM5020-5BRWZ installed.

³ The EVAL-ADuM5028EBZ is packaged with the ADuM5028-5BRIZ installed.