10-Bit 75 MSPS A/D Converter

AD9060

FEATURES

Monolithic 10-Bit/75 MSPS Converter
ECL Outputs
Bipolar (±1.75 V) Analog Input
57 dB SNR @ 2.3 MHz Input
Low (45 pF) Input Capacitance

APPLICATIONS

Digital Oscilloscopes
Medical Imaging
Professional Video
Radar Warning/Guidance Systems
Infrared Systems

GENERAL DESCRIPTION

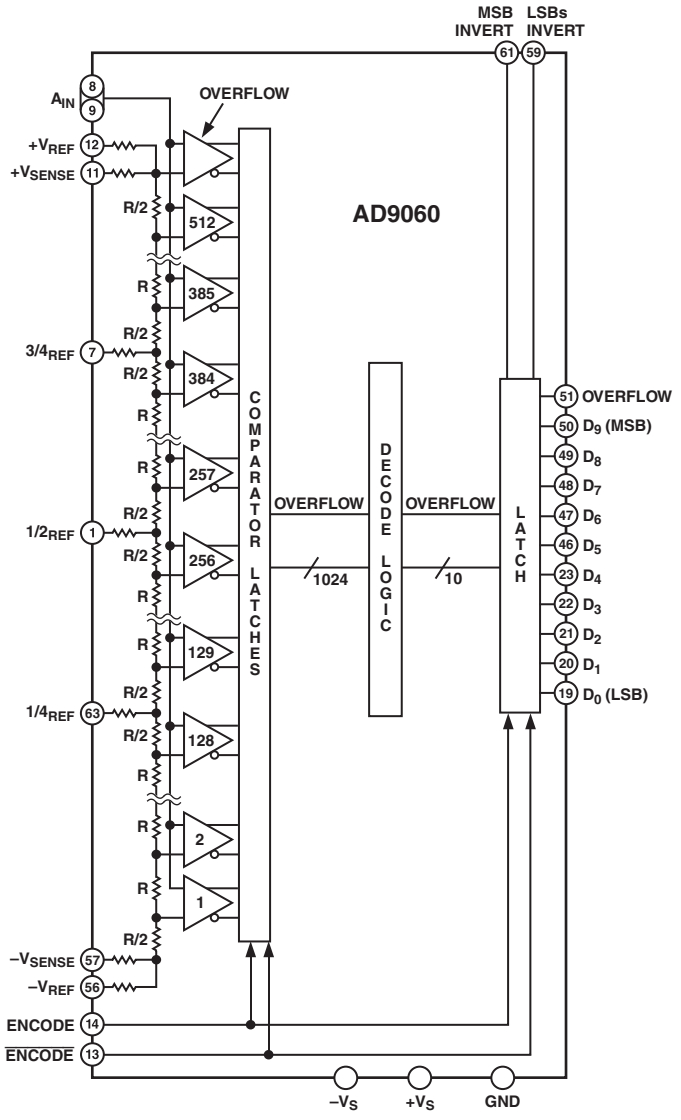
The AD9060 A/D converter is a 10-bit monolithic converter capable of word rates of 75 MSPS and above. Innovative architecture using 512 input comparators instead of the traditional 1024 required by other flash converters reduces input capacitance and improves linearity.

Inputs and outputs are ECL compatible, which makes the AD9060 the recommended choice for systems with conversion rates >30 MSPS to minimize system noise. An overflow bit is provided to indicate analog input signals greater than $+V_{SENSE}$.

Voltage sense lines are provided to ensure accurate driving of the $\pm V_{REF}$ voltages applied to the units. Quarter point taps on the resistor ladder help optimize the integral linearity of the unit.

The AD9060 is available in a 68-lead ceramic leaded (gull wing) chip carrier package specifically designed for low thermal impedances. Two performance grades for temperatures of both 0°C to +70°C and –55°C to +125°C ranges are offered to allow the user to select the linearity best suited for each application. Dynamic performance is fully characterized and production tested at 25°C.

FUNCTIONAL BLOCK DIAGRAM



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AD9060–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V; $-V_S$ = –5.2 V; $\pm V_{SENSE}$ = ±1.75 V; ENCODE = 60 MSPS, unless otherwise noted.)[1]

Parameter	Temp	Test Level	AD9060JZ Min	AD9060JZ Typ	AD9060JZ Max	AD9060KZ Min	AD9060KZ Typ	AD9060KZ Max	Unit
RESOLUTION			10			10			Bits
DC ACCURACY[1]									
Differential Nonlinearity	25°C	I		1.0	1.25		0.75	1.0	LSB
	Full	VI			1.5			1.25	LSB
Integral Nonlinearity	25°C	I		1.25	2.0		1.0	1.5	LSB
	Full	VI			2.5			2.0	LSB
No Missing Codes	Full	VI					Guaranteed		
ANALOG INPUT									
Input Bias Current[2]	25°C	I		0.4	1.0		0.4	1.0	mA
	Full	VI			2.0			2.0	mA
Input Resistance	25°C	I	2.0	7.0		2.0	7.0		kΩ
Input Capacitance[2]	25°C	V		45			45		pF
Analog Bandwidth	25°C	V		175			175		MHz
REFERENCE INPUT									
Reference Ladder Resistance	25°C	I	22	37	56	22	37	56	Ω
	Full	VI	14		66	14		66	Ω
Ladder Tempco	Full	V		0.1			0.1		Ω/°C
Reference Ladder Offset									
Top of Ladder	25°C	I		45	90		45	90	mV
	Full	VI			90			90	mV
Bottom of Ladder	25°C	I		45	90		45	90	mV
	Full	VI			90			90	mV
Offset Drift Coefficient	Full	V		50			50		µV/°C
SWITCHING PERFORMANCE									
Conversion Rate	25°C	I	75			75			MSPS
Aperture Delay (t_A)	25°C	V		1			1		ns
Aperture Uncertainty (Jitter)	25°C	V		5			5		ps, rms
Output Delay (t_{OD})[3]	25°C	I	2	4	9	2	4	9	ns
Output Rise Time	25°C	I		1	3		1	3	ns
Output Fall Time	25°C	I		1	3		1	3	ns
Output Time Slew[3]	25°C	I		1.5	3		1.5	3	ns
DYNAMIC PERFORMANCE									
Transient Response	25°C	V		10			10		ns
Overvoltage Recovery Time	25°C	V		10			10		ns
Effective Number of Bits (ENOB)									
f_{IN} = 2.3 MHz	25°C	I	8.7	9.1		8.7	9.1		Bits
f_{IN} = 10.3 MHz	25°C	IV	8.0	8.6		8.0	8.6		Bits
f_{IN} = 29.3 MHz	25°C	IV	7.0	7.4		7.0	7.4		Bits
Signal-to-Noise Ratio[4]									
f_{IN} = 2.3 MHz	25°C	I	54	56		54	56		dB
f_{IN} = 10.3 MHz	25°C	I	51	54		51	54		dB
f_{IN} = 29.3 MHz	25°C	I	44	47		44	47		dB

Parameter	Temp	Test Level	AD9060JZ Min	AD9060JZ Typ	AD9060JZ Max	AD9060KZ Min	AD9060KZ Typ	AD9060KZ Max	Unit
DYNAMIC PERFORMANCE (continued)									
Signal-to-Noise Ratio[4] (Without Harmonics)									
f_{IN} = 2.3 MHz	25°C	I	54	56		54	58		dB
f_{IN} = 10.3 MHz	25°C	I	51	55		51	55		dB
f_{IN} = 29.3 MHz	25°C	I	46	48		46	48		dB
Harmonic Distortion									
f_{IN} = 2.3 MHz	25°C	I	61	65		61	65		dBc
f_{IN} = 10.3 MHz	25°C	I	55	58		55	58		dBc
f_{IN} = 29.3 MHz	25°C	I	47	50		47	50		dBc
Two-Tone Intermodulation Distortion Rejection[5]	25°C	V		70			70		dBc
Differential Phase	25°C	V		0.5			0.5		Degrees
Differential Gain	25°C	V		1			1		%
ENCODE INPUT									
Logic 1 Voltage	Full	VI	–1.1			–1.1			V
Logic 0 Voltage	Full	VI			–1.5			–1.5	V
Logic 1 Current	Full	VI		150	300		150	300	µA
Logic 0 Current	Full	VI		150	300		150	300	µA
Input Capacitance	25°C	V		5			5		pF
Pulsewidth (High)	25°C	I	6			6			ns
Pulsewidth (Low)	25°C	I	6			6			ns
DIGITAL OUTPUTS									
Logic 1 Voltage	Full	VI	–1.1			–1.1			V
Logic 0 Voltage	Full	VI			–1.5			–1.5	V
POWER SUPPLY									
$+V_S$ Supply Current	25°C	VI		420	500		420	500	mA
	Full	VI			500			500	mA
$–V_S$ Supply Current	25°C	VI		150	180		150	180	mA
	Full	VI			190			190	mA
Power Dissipation	25°C	VI		2.8	3.3		2.8	3.3	W
	Full	VI			3.5			3.5	W
Power Supply Rejection Ratio (PSRR)[6]	Full	VI		6	10		6	10	mV/V

NOTES

[1] $3/4_{REF}$, $1/2_{REF}$, and $1/4_{REF}$ reference ladder taps are driven from dc sources at +0.875 V, 0 V, and –0.875 V, respectively. Outputs terminated through 100 Ω to –2.0 V; C_L < 4 pF. Accuracy of the overflow comparator is not tested and not included in linearity specifications.

[2] Measured with $A_{IN} = +V_{SENSE}$

[3] Output delay measured as worst-case time from 50% point of the rising edge of ENCODE to 50% point of the slowest rising or falling edge of D_0–D_9. Output skew measured as worst-case difference in output delay among D_0–D_9.

[4] RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.

[5] Intermodulation measured with analog input frequencies of 2.3 MHz and 3.0 MHz at 7 dB below full scale.

[6] Measured as the ratio of the worst-case change in transition voltage of a single comparator for a 5% change in $+V_S$ or $–V_S$.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$	+6 V
$-V_S$	–6 V
A_{IN}	–2 V to +2 V
$+V_{REF}$, $-V_{REF}$, $3/4_{REF}$, $1/2_{REF}$, $1/4_{REF}$	–2 V to +2 V
$+V_{REF}$ to $-V_{REF}$	4.0 V
ENCODE, $\overline{\text{ENCODE}}$	0 V to $-V_S$
$3/4_{REF}$, $1/2_{REF}$, $1/4_{REF}$ Current	±10 mA
Digital Output Current	20 mA
Operating Temperature	
AD9060JZ/AD9060KZ	0°C to 70°C
Storage Temperature	–65°C to +150°C
Maximum Junction Temperature[2]	150°C
Lead Soldering Temp (10 sec)	300°C

NOTES

[1] Absolute maximum ratings are limiting values to be applied individually and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

[2] Typical thermal impedances (part soldered onto board): 68-lead ceramic chip carrier: θ_{JC} = 1°C/W; θ_{JA} = 17°C/W (no air flow); θ_{JA} = 15°C/W (air flow = 500 LFM).

EXPLANATION OF TEST LEVELS

Test Level

I. 100% production tested.

II. 100% production tested at 25°C and sample tested at specified temperatures.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

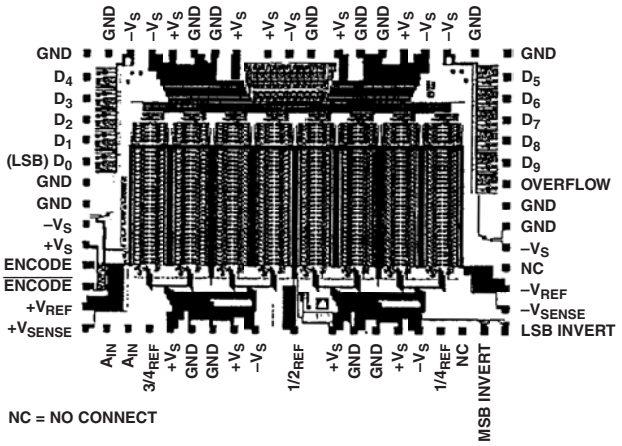
V. Parameter is a typical value only.

VI. All devices are 100% production tested at 25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

MECHANICAL INFORMATION (DIE LAYOUT)

Die Dimensions	206 mils × 140 mils × 15 (±2) mils
Pad Dimensions	4 mils × 4 mils
Metallization	Gold
Backing	None
Substrate Potential	$-V_S$
Passivation	Nitride

DIE LAYOUT



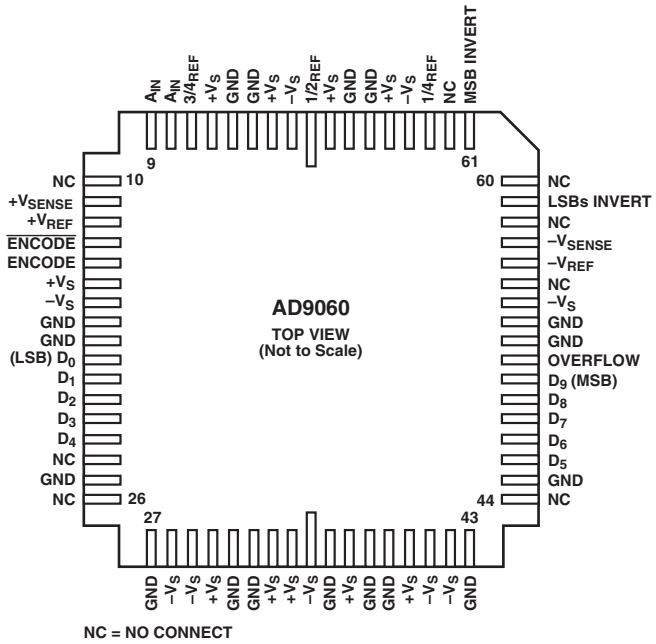
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD9060JZ	0°C to 70°C	Leaded Chip Carrier	Z-68D
AD9060KZ	0°C to 70°C	Leaded Chip Carrier	Z-68D
AD9060/PCB	0°C to 70°C	Evaluation Board	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9060 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	$1/2_{REF}$	Midpoint of Internal Reference Ladder.
2, 16, 28, 29, 35, 41, 42, 54, 64	$-V_S$	Negative Supply Voltage; Nominally –5.2 V ± 5%.
3, 6, 15, 30, 33, 34, 37, 40, 65, 68	$+V_S$	Positive Supply Voltage; Nominally +5 V ± 5%.
4, 5, 17, 18, 25, 27, 31, 32, 36, 38, 39, 43, 45, 52, 53, 66, 67	GND	All ground pins should be connected together and to low impedance ground plane.
7	$3/4_{REF}$	Three-Quarter Point of Internal Reference Ladder.
8, 9	A_{IN}	Analog Input; Nominally between ±1.75 V.
11	$+V_{SENSE}$	Voltage Sense Line to Most Positive Point on Internal Resistor Ladder. Normally 1.75 V.
12	$+V_{REF}$	Voltage Force Connection for Top of Internal Reference Ladder. Normally driven to provide 1.75 V at $+V_{SENSE}$.
13	$\overline{ENCODE}$	Differential ECL Convert Signal, Starts Digitizing Process.
14	ENCODE	ECL Compatible Convert Command, Used to Begin Digitizing Process.
19–23, 46–50	D_0–D_9	ECL Compatible Digital Output Data.
51	OVERFLOW	ECL Compatible Output Indicating $A_{IN} > +V_{SENSE}$.
56	$-V_{REF}$	Voltage Force Connection for Bottom of Internal Reference Ladder. Normally driven to provide –1.75 V at $-V_{SENSE}$.
57	$-V_{SENSE}$	Voltage Sense Line to Most Negative Point on Internal Resistor Ladder. Normally –1.75 V.
59	LSBs INVERT	Normally Grounded. When connected to $+V_S$, lower order bits (D_0–D_8) are inverted. Not ECL compatible.
61	MSB INVERT	Normally Grounded. When connected to $+V_S$, most significant bit (MSB; D_9) is inverted. Not ECL compatible.
63	$1/4_{REF}$	One-Quarter Point of Internal Reference Ladder.

THEORY OF OPERATION

Refer to the Functional Block Diagram. As shown, the AD9060 uses a modified "flash," or parallel, A/D architecture. The analog input range is determined by an external voltage reference ($+V_{REF}$ and $-V_{REF}$), nominally ±1.75 V. An internal resistor ladder divides this reference into 512 steps, each representing two quantization levels. Taps along the resistor ladder ($1/4_{REF}$, $1/2_{REF}$, and $3/4_{REF}$) are provided to optimize linearity. Rated performance is achieved by driving these points at 1/4, 1/2, and 3/4, respectively, of the voltage reference range.

The A/D conversion for the nine most significant bits (MSB) is performed by 512 comparators. The value of the least significant bit (LSB) is determined by a unique interpolation scheme between adjacent comparators. The decoding logic processes the comparator outputs and provides a 10-bit code to the output stage of the converter.

Flash architecture has an advantage over other A/D architectures because conversion occurs in one step. This means the performance of the converter is limited primarily by the speed and matching of the individual comparators. In the AD9060, an innovative interpolation scheme takes advantage of the flash architecture but minimizes the input capacitance, power, and device count usually associated with that method of conversion.

These advantages occur because of using only half the normal number of input comparator cells to accomplish the conversion. In addition, a proprietary decoding scheme minimizes error codes. Input control pins allow the user to select from among binary, inverted binary, twos complement, and inverted twos complement coding (see Table I, the AD9060 Truth Table).

APPLICATIONS

Many of the specifications used to describe A/D converters have evolved from system performance requirements in these applications. Different systems emphasize particular specifications, depending on how the part is used. The following applications highlight some of the specifications and features that make the AD9060 attractive in these systems.

Wideband Receivers

Radar and communication receivers (baseband and direct IF digitization), ultrasound medical imaging, signal intelligence, and spectral analysis all place stringent ac performance requirements on analog-to-digital converters (ADCs). Frequency domain characterization of the AD9060 provides signal-to-noise ratio (SNR) and harmonic distortion data to simplify selection of the ADC.

Receiver sensitivity is limited by the *Signal-to-Noise Ratio (SNR)* of the system. The SNR for an ADC is measured in the frequency domain and calculated with a Fast Fourier Transform (FFT). The SNR equals the ratio of the fundamental component of the signal (rms amplitude) to the rms value of the noise. The noise is the sum of all other spectral components, including harmonic distortion but excluding dc.

Good receiver design minimizes the level of spurious signals in the system. Spurious signals developed in the ADC are the result of imperfections in the device transfer function (nonlinearities, delay mismatch, varying input impedance, and so on). In the ADC, these spurious signals appear as *Harmonic Distortion.* Harmonic Distortion is also measured with an FFT and is specified as the ratio of the fundamental component of the signal (rms amplitude) to the rms value of the worst-case harmonic (usually the second or third).

Two-Tone Intermodulation Distortion (IMD) is a frequently cited specification in receiver design. In narrow-band receivers, third-order IMD products result in spurious signals in the pass band of the receiver. Like mixers and amplifiers, the ADC is characterized with two, equal amplitude, pure input frequencies. The IMD equals the ratio of the power of either of the two input signals to the power of the strongest third order IMD signal. Unlike mixers and amplifiers, the IMD does not always behave as it does in linear devices (reduced input levels do not result in predictable reductions in IMD).

Performance graphs provide typical harmonic and SNR data for the AD9060 for increasing analog input frequencies. In choosing an A/D converter, always look at the dynamic range for the analog input frequency of interest. The AD9060 specifications provide guaranteed minimum limits at three analog test frequencies.

Aperture Delay is the delay between the rising edge of the ENCODE command and the instant at which the analog input is sampled. Many systems require simultaneous sampling of more than one analog input signal with multiple ADCs. In these situations timing is critical, and the absolute value of the aperture delay is not as critical as the matching between devices.

Aperture Uncertainty, or jitter, is the sample-to-sample variation in aperture delay. This is especially important when sampling high slew rate signals in wide bandwidth systems. Aperture uncertainty is one of the factors that degrades dynamic performance as the analog input frequency is increased.

Digitizing Oscilloscopes

Oscilloscopes provide amplitude information about an observed waveform with respect to time. Digitizing oscilloscopes must accurately sample this signal without distorting the information to be displayed.

One figure of merit for the ADC in these applications is *Effective Number of Bits* (*ENOB*). *ENOB* is calculated with a sine wave curve fit and equals

$$ENOB = N - \log_2 \left[Error\left(measured\right) / Error\left(ideal\right) \right]$$

N is the resolution (number of bits) of the ADC. The measured error is the actual rms error calculated from the converter outputs with a pure sine wave input.

The *Analog Bandwidth* of the converter is the analog input frequency at which the spectral power of the fundamental signal is reduced 3 dB from its low frequency value. The analog bandwidth is a good indicator of a converter's slewing capabilities.

The *Maximum Conversion Rate* is defined as the encode rate at which the SNR for the lowest analog signal test frequency tested drops by no more than 3 dB below the guaranteed limit.

Imaging

Visible and infrared imaging systems each require similar characteristics from ADCs. The signal input (from a CCD camera or multiplexer) is a time division multiplexed signal consisting of a series of pulses whose amplitude varies in direct proportion to the intensity of the radiation detected at the sensor. These varying levels are then digitized by applying ENCODE commands at the correct times, as shown in Figure 1.

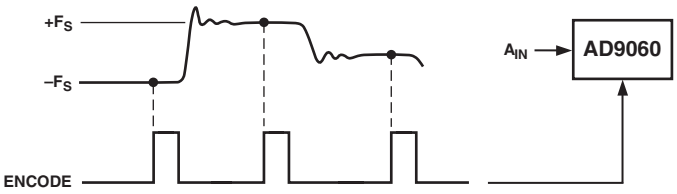


Figure 1. Imaging Application Using AD9060

The actual resolution of the converter is limited by the thermal and quantization noise of the ADC. The low frequency test for SNR or ENOB is a good measure of the noise of the AD9060. At this frequency, the static errors in the ADC determine the useful dynamic range of the ADC.

Although the signal being sampled does not have a significant slew rate, this does not imply that dynamic performance is not important. The *Transient Response and Overvoltage Recovery Time* specifications ensure that the ADC can track full-scale changes in the analog input sufficiently fast to capture a valid sample.

Transient Response is the time required for the AD9060 to achieve full accuracy when a step function is applied. *Overvoltage Recovery Time* is the time required for the AD9060 to recover to full accuracy after an analog input signal 150% of full scale is reduced to the full-scale range of the converter.

Professional Video

Digital Signal Processing (DSP) is now common in television production. Modern studios rely on digitized video to create state-of-the-art special effects. Video instrumentation also requires high resolution ADCs for studio quality measurement and frame storage.

The AD9060 provides sufficient resolution for these demanding applications. Conversion speed, dynamic performance, and analog bandwidth are suitable for digitizing both composite and RGB video sources.

USING THE AD9060

Voltage References

The AD9060 requires the user to provide two voltage references: $+V_{REF}$ and $-V_{REF}$. These two voltages are applied across an internal resistor ladder (nominally 37 Ω) and set the analog input voltage range of the converter. The voltage references should be driven from a stable, low impedance source. In addition to these two references, three evenly spaced taps on the resistor ladder ($1/4_{REF}$, $1/2_{REF}$, and $3/4_{REF}$) are available. Providing a reference to these quarter points on the resistor ladder will improve the integral linearity of the converter and improve ac performance (ac and dc specifications are tested while driving the quarter points at the indicated levels). The figure below is not intended to show the transfer characteristic of the ADC but illustrates how the linearity of the device is affected by the reference voltages applied to the ladder.

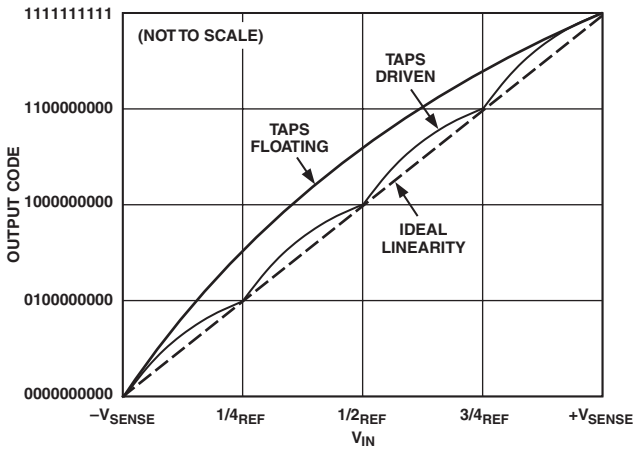


Figure 2. Effect of Reference Taps on Linearity

Resistance between the reference connections and the taps of the first and last comparators causes offset errors. These errors, called "top and bottom of the ladder offsets," can be nulled by using the voltage sense lines, $+V_{SENSE}$ and $-V_{SENSE}$, to adjust the reference voltages. Current through the sense lines should be limited to less than 100 μA. Excessive current drawn through the voltage sense lines will affect the accuracy of the sense line voltage.

Figure 4 shows a reference circuit that nulls out the offset errors using two op amps and provides appropriate voltage references to the quarter-point taps. Feedback from the sense lines causes the op amps to compensate for the offset errors. The two transistors limit the amount of current drawn directly from the op amps; resistors at the base connections stabilize their operation. The 10 kΩ resistors (R1–R4) between the voltage sense lines form an external resistor ladder; the quarter point voltages are taken off this external ladder and buffered by an op amp. The actual values of resistors R1–R4 are not critical, but they should match well and be large enough (≥10 kΩ) to limit the amount of current drawn from the voltage sense lines.

The select resistors (R_S) shown in the schematic (each pair can be a potentiometer) are chosen to adjust the quarter-point voltage references but are not necessary if R1–R4 match within 0.05%.

An alternative approach for defining the quarter-point references of the resistor ladder is to evaluate the integral linearity error of an individual device and adjust the voltage at the quarter-points to minimize this error. This may improve the low frequency ac performance of the converter.

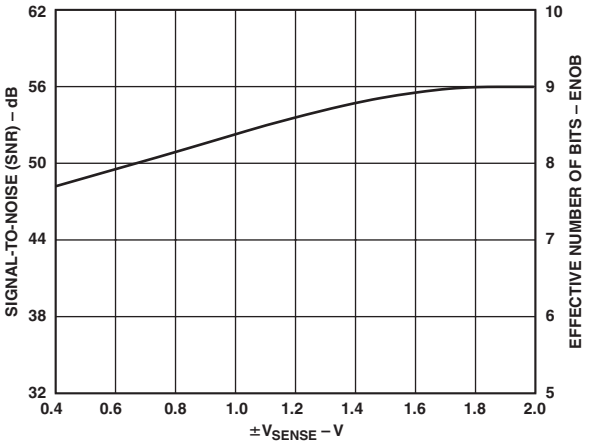


Figure 3. SNR and ENOB vs. Reference Voltage

Performance of the AD9060 has been optimized with an analog input voltage of ±1.75 V (as measured at $\pm V_{SENSE}$). If the analog input range is reduced below these values, relatively larger differential nonlinearity errors may result because of comparator mismatches. As shown in Figure 3, performance of the converter is a function of $\pm V_{SENSE}$.

Applying a voltage greater than 4 V across the internal resistor ladder will cause current densities to exceed rated values and may cause permanent damage to the AD9060. The design of the reference circuit should limit the voltage available to the references.

Analog Input Signal

The signal applied to A_{IN} drives the inputs of 512 parallel comparator cells (see Figure 5). This connection has a typical input resistance of 7 kΩ and input capacitance of 45 pF. The input capacitance is nearly constant over the analog input voltage range as shown in Figure 12, which illustrates that characteristic.

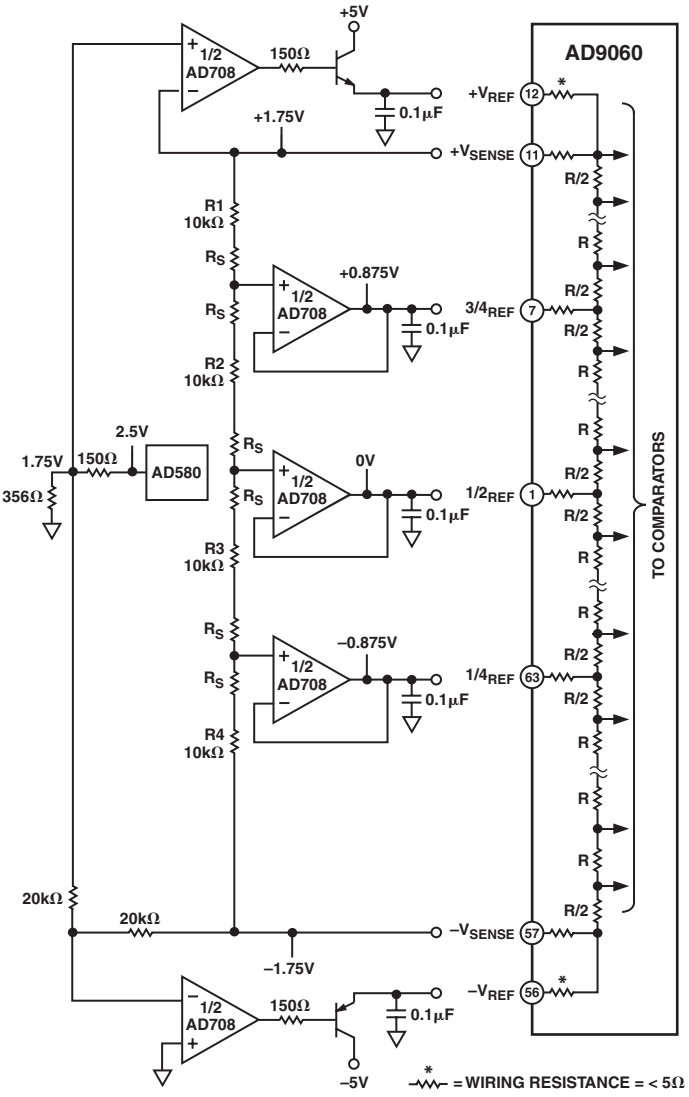


Figure 4. Reference Circuit

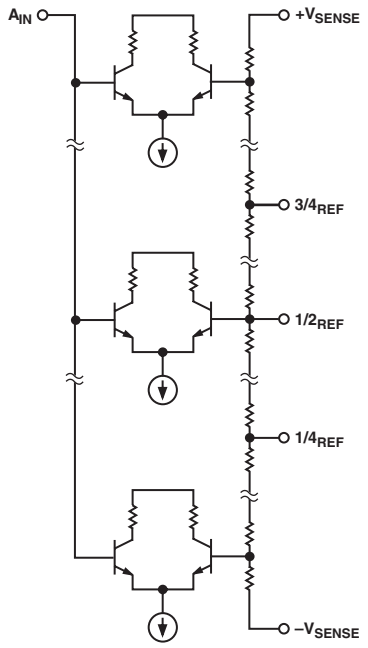


Figure 5. Equivalent Analog Input

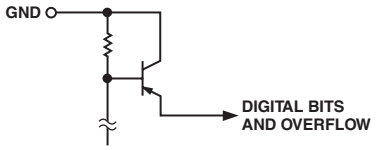


Figure 6. Equivalent Digital Outputs

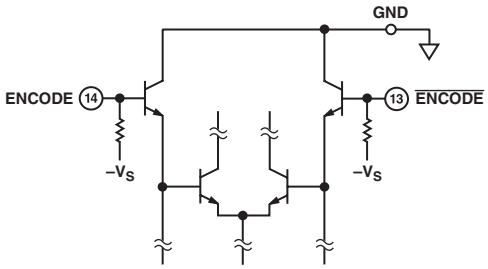


Figure 7. ENCODE and $\overline{\text{ENCODE}}$ Equivalent Circuits

Timing

In the AD9060, the rising edge of the ENCODE signal triggers the A/D conversion by latching the comparators (see Figure 8). These ENCODE and $\overline{\text{ENCODE}}$ signals are ECL compatible and should be driven differentially. Jitter on the ENCODE signal will raise the noise floor of the converter. Differential signals, with fast clean edges, will reduce the jitter in the signal and allow optimum ac performance. In applications with a fixed, high frequency encode rate, converter performance is also improved (jitter reduced) by using a crystal oscillator as the system clock.

The AD9060 units are designed to operate with a 50% duty cycle encode signal; adjustment of the duty cycle may improve the dynamic performance of individual devices. Since the ENCODE and $\overline{\text{ENCODE}}$ signals are differential, the logic levels are not critical. Users should remember, however, that reduced logic levels will reduce the slew rate of the edges and effectively increase the jitter of the signal. ECL terminations for the ENCODE and $\overline{\text{ENCODE}}$ signals should be as close as possible to the AD9060 package to avoid reflections.

In systems where only single-ended signals are available, the use of a high speed comparator (such as the AD96685) is recommended to convert to differential signals. An alternative is to connect 1.3 V (ECL midpoint) to $\overline{\text{ENCODE}}$ and drive the ENCODE connection single ended. In such applications, clean, fast edges are necessary to minimize jitter in the signal.

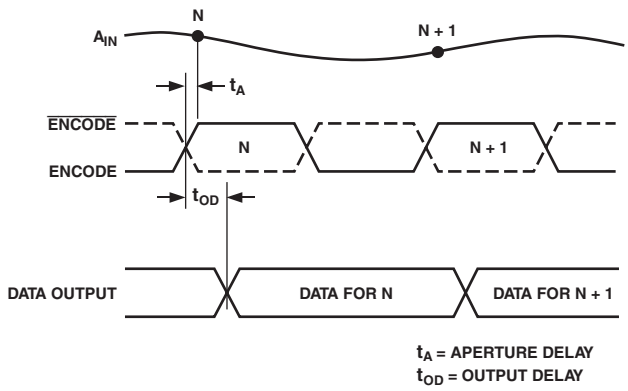


Figure 8. Timing Diagram

Output data of the AD9060 (D_0–D_9 and OVERFLOW) are also ECL compatible and should be terminated through 100 Ω to –2 V (or an equivalent load).

Data Format

The format of the output data (D_0–D_9) is controlled by the MSB INVERT and LSBs INVERT pins. These inputs are dc control inputs and should be connected to GND or $+V_S$. Table I gives information on how to choose from among binary, inverted binary, twos complement, and inverted twos complement coding.

The OVERFLOW output is an indication that the analog input signal has exceeded the voltage at $+V_{SENSE}$. The accuracy of the overflow transition voltage and output delay are not tested or included in the data sheet limits. Performance of the overflow indicator is dependent on the circuit layout and the slew rate of the encode signal. The operation of this function does not affect the other data bits (D_0–D_9). It is not recommended for applications requiring a critical measure of analog input voltage.

Layout and Power Supplies

Proper layout of high speed circuits is always critical but is particularly important when both analog and digital signals are involved.

Analog signal paths should be kept as short as possible and be properly terminated to avoid reflections. The analog input voltage and the voltage references should be kept away from digital signal paths; this reduces the amount of digital switching noise that is capacitively coupled into the analog section of the circuit.

Digital signal paths should also be kept short, and run lengths should be matched to avoid propagation delay mismatch. Terminations for ECL signals should be as close as possible to the receiving gate.

In high speed circuits, layout of the ground circuit is a critical factor. A single, low impedance ground plane on the component side of the board will reduce noise on the circuit ground. Power supplies should be capacitively coupled to the ground plane to reduce noise in the circuit. Multilayer boards allow designers to lay out signal traces without interrupting the ground plane and provide low impedance power planes.

It is especially important to maintain the continuity of the ground plane under and around the AD9060. In systems with dedicated digital and analog grounds, all grounds of the AD9060 should be connected to the analog ground plane.

The power supplies ($+V_S$ and $–V_S$) of the AD9060 should be isolated from the supplies used for external devices; this further reduces the amount of noise coupled into the A/D converter. Sockets limit the dynamic performance and should be used only for prototypes or evaluation—PCK Elastomerics Part No. CCS6855 is recommended for the LCC package.

An evaluation board is available to aid designers and provide a suggested layout.

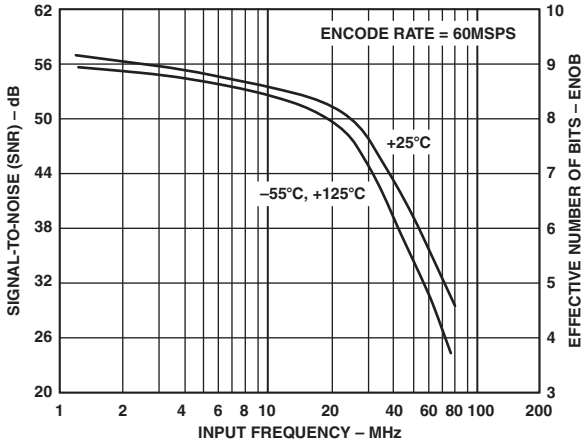


Figure 9. SNR and ENOB vs. Input Frequency

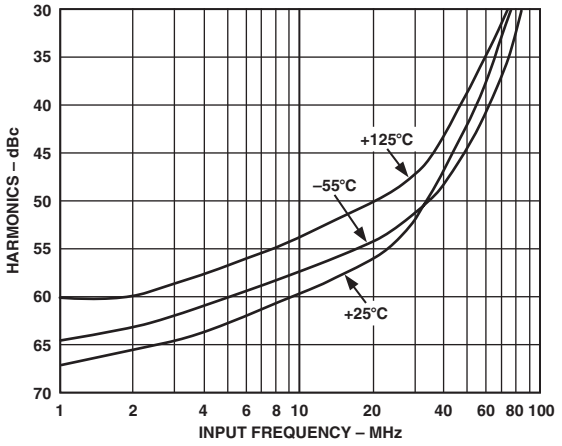


Figure 11. Harmonics vs. Input Frequency

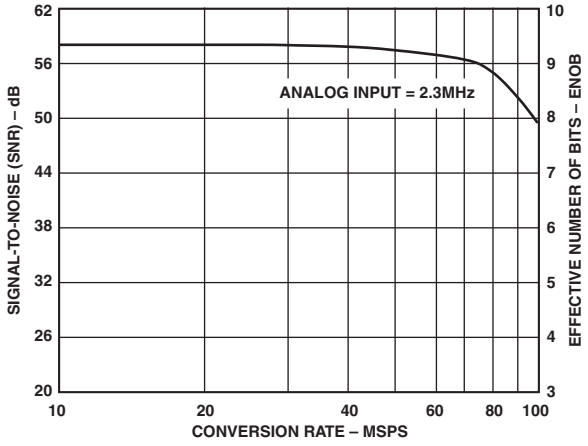


Figure 10. SNR and ENOB vs. Conversion Rate

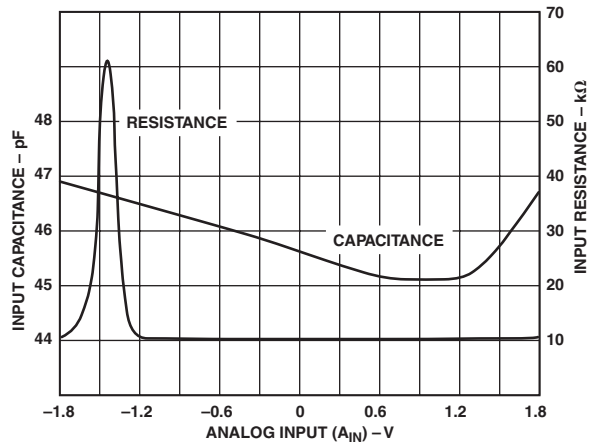


Figure 12. Input Capacitance/Resistance vs. Input Voltage

Table I. Truth Table

Step	Range 0 = –1.75 V FS = +1.75 V	Offset Binary		Twos Complement	
		True MSB INV = 0 LSBs INV = 0	Inverted MSB INV = 1 LSBs INV = 1	True MSB INV = 1 LSBs INV = 0	Inverted MSB INV = 0 LSBs INV = 1
1024	> +1.7500	(1)1111111111	(1)0000000000	(1)0111111111	(1)1000000000
1023	+1.7466	1111111111	0000000000	0111111111	1000000000
1022	+1.7432	1111111110	0000000001	0111111110	1000000001
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
512	+0.0034	1000000000	0111111111	0000000000	1111111111
511	0.000	0111111111	1000000000	1111111111	0000000000
510	–0.0034	0111111110	1000000001	1111111110	0000000001
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
02	–1.7432	0000000010	1111111101	1000000010	0111111101
01	–1.7466	0000000001	1111111110	1000000001	0111111110
00	< –1.7466	0000000000	1111111111	1000000000	0111111111

The overflow bit is always 0 except where noted in parentheses ( ). MSB INVERT and LSBs INVERT are considered dc controls.

AD9060/PCB EVALUATION BOARD

The AD9060/PCB Evaluation Board is available from the factory and is shown here in block diagram form. The board includes a reference circuit that allows the user to adjust both references and the quarter-point voltages. The AD9617 is included as the drive amplifier, and the user can configure the gain from –1 to –15.

On-board reconstruction of the digital data is provided through the AD9712, a 12-bit monolithic DAC. The analog and reconstructed waveforms can be summed on the board to allow the user to observe the linearity of the AD9060 and the effects of the quarter-point voltages. The digital data and an adjustable data ready signal are available via a 37-pin edge connector.

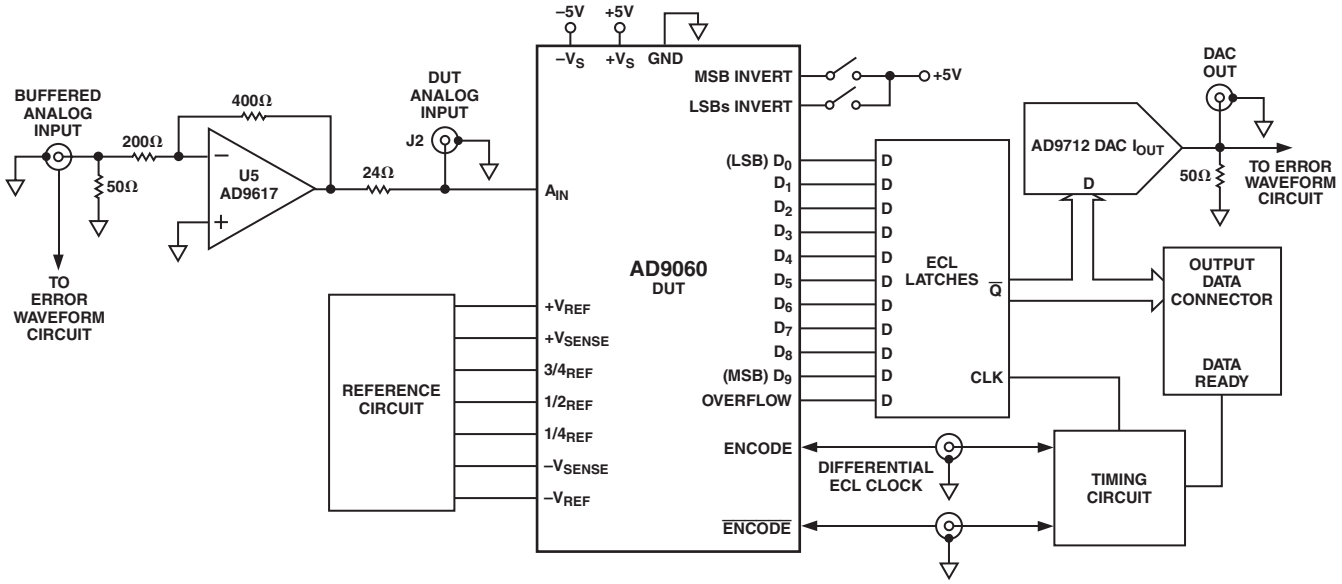
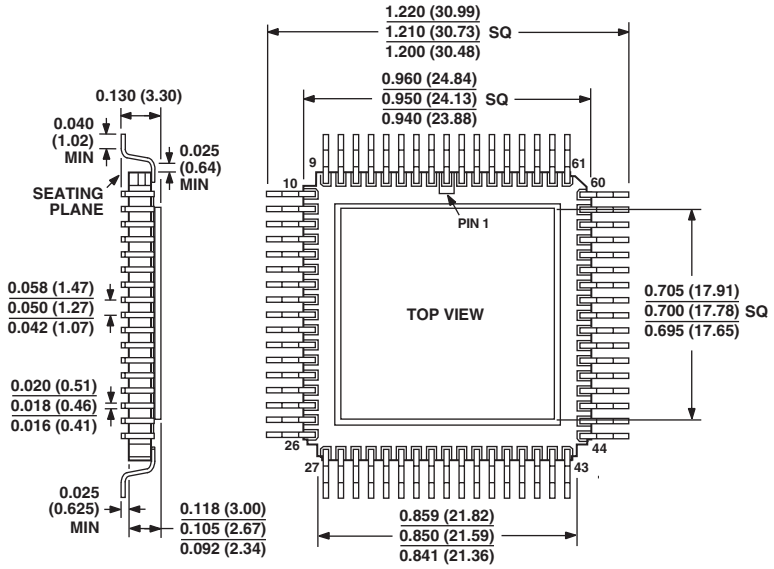


Figure 13. PCB Evaluation Board Block Diagram

OUTLINE DIMENSIONS
68-Lead Ceramic Leaded Chip Carrier [CLCC]
(Z-68D)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

C00564–0–4/03(B)

Revision History

Location	Page
4/03—Data Sheet changed from REV. A to REV. B.	
Removed AD9060JE/KE/SZ/SE/TZ/TE	Universal
Removed MIL-STD-833 Compliance Information	Universal
Renumbered Figures	Universal
Edits to ABSOLUTE MAXIMUM RATINGS	4
Updated OUTLINE DIMENSIONS	12