

M16C/6N Group (M16C/6NK, M16C/6NM)

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

REJ03B0058-0100Z
Rev.1.00
Jul 20, 2004

1. Overview

The M16C/6N Group (M16C/6NK, M16C/6NM) of single-chip microcomputers are built using the high-performance silicon gate CMOS process using an M16C/60 Series CPU core and are packaged in 100-pin and 128-pin plastic molded LQFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed. Being equipped with two CAN (Controller Area Network) modules in M16C/6N Group (M16C/6NK, M16C/6NM), the microcomputer is suited to car audio and industrial control systems. The CAN modules comply with the 2.0B specification. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA and communication equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Car audio and industrial control systems, other

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

1.2 Performance Outline

Tables 1.1 and 1.2 list a performance outline of M16C/6N Group (M16C/6NK, M16C/6NM).

Table 1.1 Performance outline of M16C/6N Group (100-pin version: M16C/6NK)

Item			Performance
CPU	Number of Basic Instructions		91 instructions
	Minimum Instruction Execution Time		41.7ns (f(BCLK) = 24MHz, 1/1 prescaler, without software wait)
	Operation Mode		Single-chip mode
	Address Space		1 Mbyte
	Memory Capacity		See Table 1.3 Product List
Peripheral Function	Port		Input/Output: 87 pins, Input: 1 pin
	Multifunction Timer		Timer A: 16 bits × 5 channels Timer B: 16 bits × 6 channels Three-phase motor control circuit
	Serial I/O		3 channels Clock synchronous, UART, I ² C-bus ⁽¹⁾ , IEBus ⁽²⁾ 2 channels Clock synchronous
	A/D Converter		10-bit A/D converter: 1 circuit, 26 channels
	D/A Converter		8 bits × 2 channels
	DMAC		2 channels
	CRC Calculation Circuit		CRC-CCITT
	CAN Module		2 channels with 2.0B specification
	Watchdog Timer		15 bits × 1 channel (with prescaler)
	Interrupt		internal: 32 sources, external: 9 sources Software: 4 sources, Priority level: 7 levels
	Clock Generating Circuit		4 circuits • Main clock oscillation circuit (*) • Sub clock oscillation circuit (*) • On-chip oscillator • PLL frequency synthesizer (*) Equipped with a built-in feedback resistor
	Oscillation Stop Detection Function		Main clock oscillation stop and re-oscillation detection function
Electrical Characteristics	Supply Voltage		VCC = 3.0 to 5.5V (f(BCLK) = 24MHz, 1/1 prescaler, without software wait)
	Power Consumption	Mask ROM	21mA (f(BCLK) = 24MHz, PLL operation, no division)
		Flash Memory	23mA (f(BCLK) = 24MHz, PLL operation, no division)
		Mask ROM	3μA (f(BCLK) = 32kHz, Wait mode, Oscillation capacity Low)
		Flash Memory	0.8μA (Stop mode, Topr = 25°C)
Flash Memory Version	Program/Erase Supply Voltage		3.3 ± 0.3V or 5.0 ± 0.5V
	Program and Erase Endurance		100 times
I/O Characteristics	I/O Withstand Voltage		5.0V
	Output Current		5mA
Operating Ambient Temperature			-40 to 85°C
Device Configuration			CMOS high performance silicon gate
Package			100-pin plastic mold LQFP

NOTES:

1: I²C-bus is a registered trademark of Koninklijke Philips Electronics N.V.

2: IEBus is a registered trademark of NEC Electronics Corporation.

Table 1.2 Performance outline of M16C/6N Group (128-pin version: M16C/6NM)

Item		Performance
CPU	Number of Basic Instructions	91 instructions
	Minimum Instruction Execution Time	41.7ns (f(BCLK) = 24MHz, 1/1 prescaler, without software wait)
	Operation Mode	Single-chip mode
	Address Space	1 Mbyte
	Memory Capacity	See Table 1.3 Product List
Peripheral Function	Port	Input/Output: 113 pins, Input: 1 pin
	Multifunction Timer	Timer A: 16 bits × 5 channels Timer B: 16 bits × 6 channels Three-phase motor control circuit
	Serial I/O	3 channels Clock synchronous, UART, I ² C-bus ⁽¹⁾ , IEBus ⁽²⁾ 4 channels Clock synchronous
	A/D Converter	10-bit A/D converter: 1 circuit, 26 channels
	D/A Converter	8 bits × 2 channels
	DMAC	2 channels
	CRC Calculation Circuit	CRC-CCITT
	CAN Module	2 channels with 2.0B specification
	Watchdog Timer	15 bits × 1 channel (with prescaler)
	Interrupt	internal: 34 sources, external: 12 sources Software: 4 sources, Priority level: 7 levels
	Clock Generating Circuit	4 circuits • Main clock oscillation circuit (*) • Sub clock oscillation circuit (*) • On-chip oscillator • PLL frequency synthesizer (*) Equipped with a built-in feedback resistor
	Oscillation Stop Detection Function	Main clock oscillation stop and re-oscillation detection function
Electrical Characteristics	Supply Voltage	VCC = 3.0 to 5.5V (f(BCLK) = 24MHz, 1/1 prescaler, without software wait)
	Power Consumption	Mask ROM 21mA (f(BCLK) = 24MHz, PLL operation, no division)
		Flash Memory 23mA (f(BCLK) = 24MHz, PLL operation, no division)
		Mask ROM 3μA (f(BCLK) = 32kHz, Wait mode, Oscillation capacity Low)
		Flash Memory 0.8μA (Stop mode, Topr = 25°C)
Flash Memory Version	Program/Erase Supply Voltage	3.3 ± 0.3V or 5.0 ± 0.5V
	Program and Erase Endurance	100 times
I/O Characteristics	I/O Withstand Voltage	5.0V
	Output Current	5mA
Operating Ambient Temperature		-40 to 85°C
Device Configuration		CMOS high performance silicon gate
Package		128-pin plastic mold LQFP

NOTES:

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1.3 Block Diagram

Figure 1.1 shows a block diagram of M16C/6N Group (M16C/6NK, M16C/6NM).

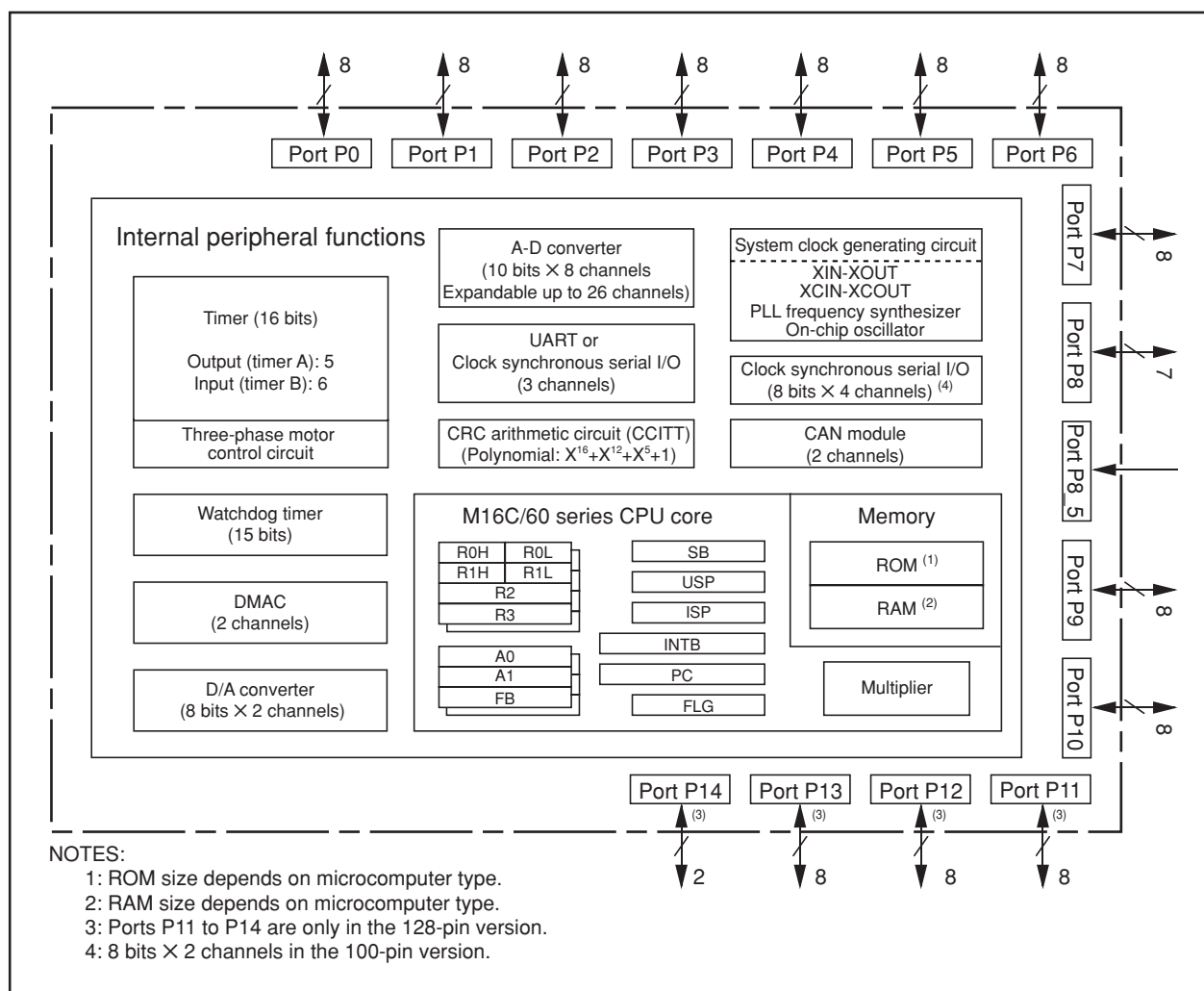


Figure 1.1 Block Diagram

1.4 Product List

Table 1.3 lists the M16C/6N Group (M16C/6NK, M16C/6NM) products and Figure 1.2 shows the type numbers, memory sizes and packages.

Table 1.3 Product List

As of Jul. 2004

Type No.	ROM capacity	RAM capacity	Package type	Remarks
M306NKFHGP (D)	384 K	31 Kbytes	100P6Q-A	Flash memory version
M306NMFHGP (D)	+ 4 Kbytes		128P6Q-A	
M306NKFJGP (D)	512 K	31 Kbytes	100P6Q-A	
M306NMFJGP (D)	+ 4 Kbytes		128P6Q-A	
M306NKME-XXXGP (D)	192 Kbytes	16 Kbytes	100P6Q-A	Mask ROM version
M306NMME-XXXGP (D)			128P6Q-A	
M306NKM-XXXGP (D)	256 Kbytes	20 Kbytes	100P6Q-A	
M306NMM-XXXGP (D)			128P6Q-A	

(D): Under development

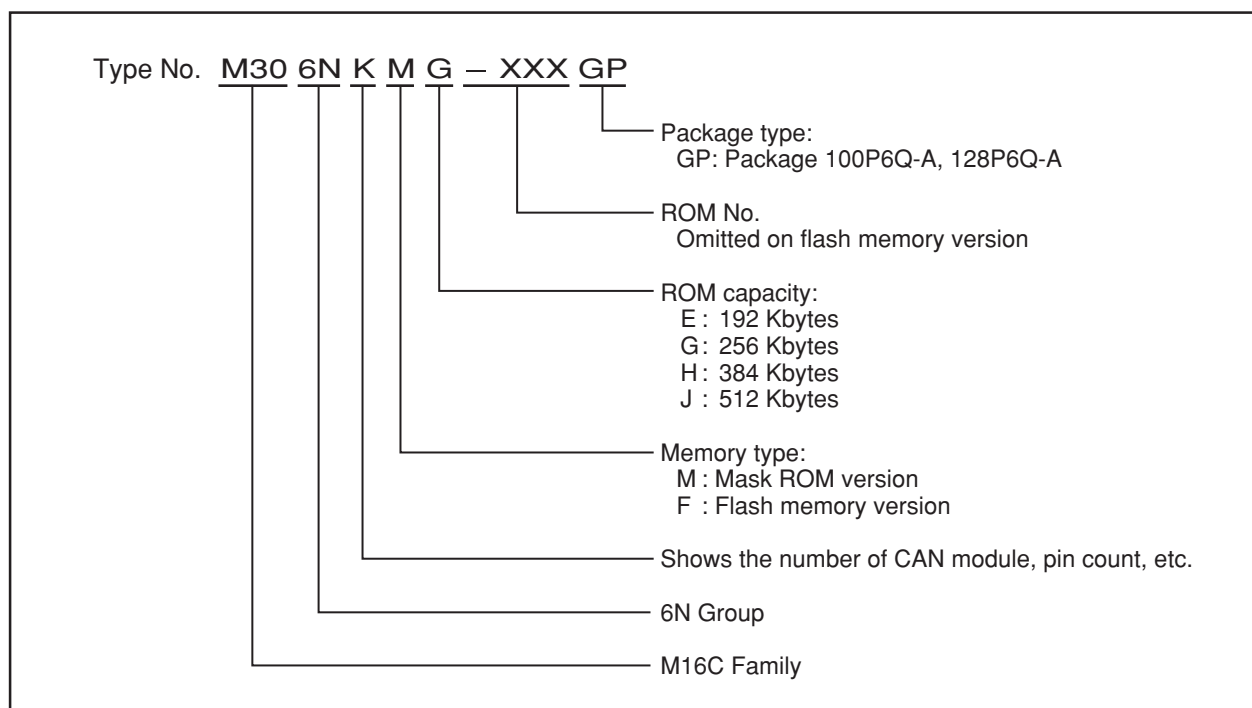


Figure 1.2 Type No., Memory Size, and Package

1.5 Pin Configuration

Figures 1.3 and 1.4 show the pin configuration (top view).

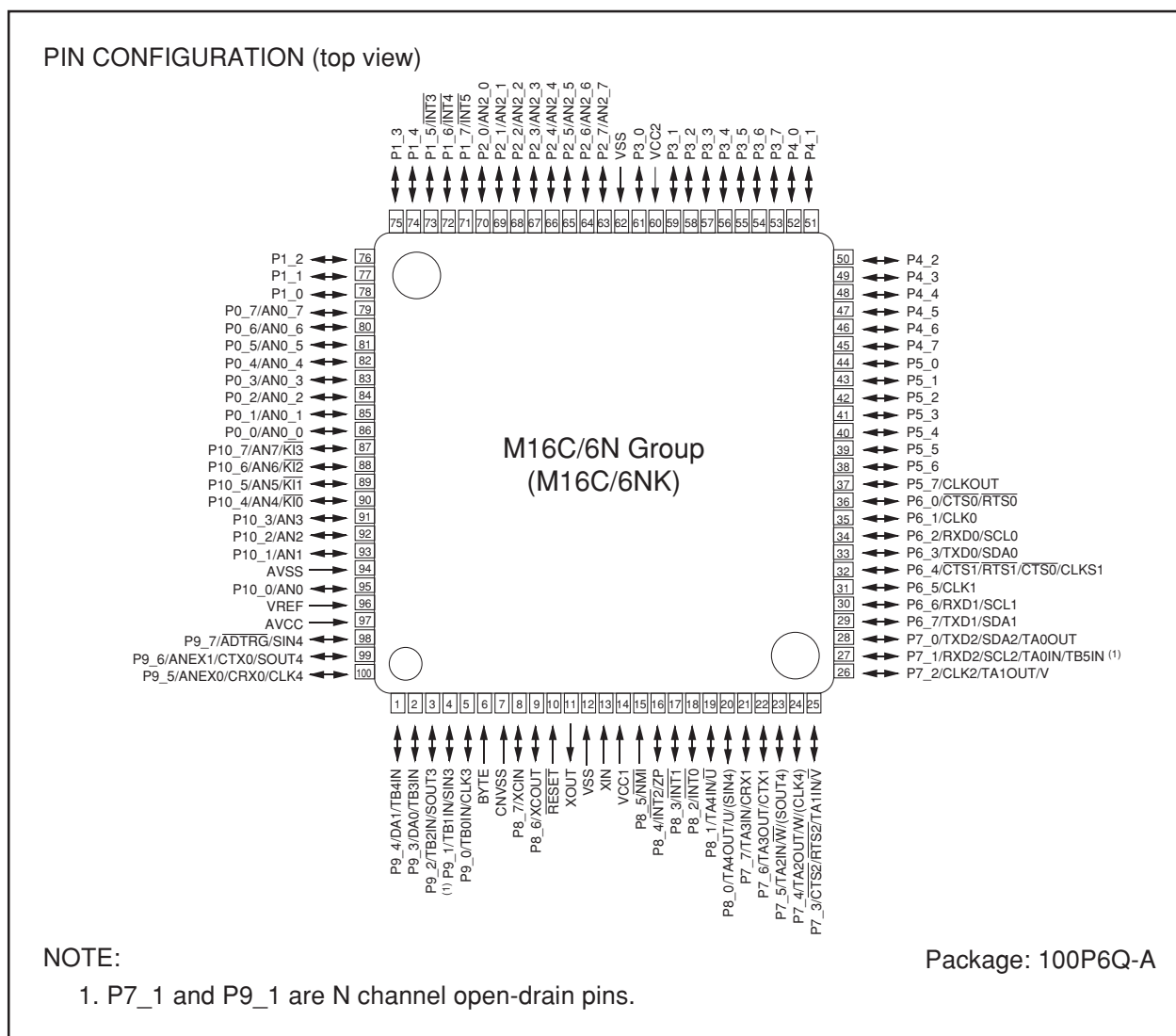


Figure 1.3 Pin Configuration (Top View)



1.6 Pin Description

Tables 1.4 and 1.5 list the pin descriptions.

Table 1.4 Pin Description (100-pin and 128-pin Versions) (1)

Signal Name	Pin Name	I/O Type	Description
Power supply input	VCC1, VCC2, VSS	I	Apply 3.0 to 5.5V to the VCC1 and VCC2 pins and 0V to the VSS pin. The VCC apply condition is that VCC2 = VCC1 ⁽¹⁾ .
Analog power supply input	AVCC, AVSS	I	Applies the power supply for the A/D converter. Connect the AVCC pin to VCC1. Connect the AVSS pin to VSS.
Reset input	RESET	I	The microcomputer is in a reset state when applying "L" to the this pin.
CNVSS	CNVSS	I	Connect this pin to VSS.
External data bus width select input	BYTE	I	Connect this pin to VSS.
Main clock input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT ⁽²⁾ . To use the external clock, input the clock from XIN and leave XOUT open.
Main clock output	XOUT	O	
Sub clock input	XCIN	I	I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOU ⁽²⁾ . To use the external clock, input the clock from XCIN and leave XCOU open.
Sub clock output	XCOU	O	
Clock output	CLKOUT	O	The clock of the same cycle as fC, f8, or f32 is output.
INT interrupt input	INT0 to INT8 ⁽³⁾	I	Input pins for the INT interrupt.
NMI interrupt input	NMI	I	Input pin for the NMI interrupt. Pin states can be read by the P8_5 bit in the P8 register.
Key input interrupt input	KI0 to KI3	I	Input pins for the key input interrupt.
Timer A	TA0OUT to TA4OUT	I/O	These are timer A0 to timer A4 I/O pins.
	TA0IN to TA4IN	I	These are timer A0 to timer A4 input pins.
	ZP	I	Input pin for the Z-phase.
Timer B	TB0IN to TB5IN	I	These are timer B0 to timer B5 input pins.
Three-phase motor control output	U, $\bar{U}$, V, $\bar{V}$, W, $\bar{W}$	O	These are Three-phase motor control output pins.
Serial I/O	CTS0 to CTS2	I	These are send control input pins.
	RTS0 to RTS2	O	These are receive control output pins.
	CLK0 to CLK6 ⁽³⁾	I/O	These are transfer clock I/O pins.
	RXD0 to RXD2	I	These are serial date input pins.
	SIN3 to SIN6 ⁽³⁾	I	These are serial date input pins.
	TXD0 to TXD2	O	These are serial date output pins.
	SOUT3 to SOUT6 ⁽³⁾	O	These are serial date output pins.
	CLKS1	O	This is output pin for transfer clock output from multiple pins function.
I ² C mode	SDA0 to SDA2	I/O	These are serial date output pins.
	SCL0 to SCL2	I/O	These are transfer clock I/O pins. (except SCL2 for the N-channel open drain output.)

I: Input O: Output I/O: Input/Output

NOTES:

1. In this manual, hereafter, VCC refers to VCC1 unless otherwise noted.
2. Ask the oscillator maker the oscillation characteristic.
3. INT6 to INT8, CLK5, CLK6, SIN5, SIN6, SOUT5, SOUT6 are only in the 128-pin version.

Table 1.5 Pin Description (100-pin and 128-pin Versions) (2)

Signal Name	Pin Name	I/O Type	Description
Reference voltage input	VREF	I	Applies the reference voltage for the A/D converter and D/A converter.
A/D converter	AN0 to AN7 AN0_0 to AN0_7 AN2_0 to AN2_7	I	Analog input pins for the A/D converter.
	ADTRG	I	This is an A/D trigger input pin.
	ANEX0	I/O	This is the extended analog input pin for the A/D converter, and is the output in external op-amp connection mode.
	ANEX1	I	This is the extended analog input pin for the A/D converter.
D/A converter	DA0, DA1	O	These are the output pins for the D/A converter.
CAN module	CRX0, CRX1	I	These are the input pins for the CAN module.
	CTX0, CTX1	O	These are the output pins for the CAN module.
I/O port	P0_0 to P0_7 P1_0 to P1_7 P2_0 to P2_7 P3_0 to P3_7 P4_0 to P4_7 P5_0 to P5_7 P6_0 to P6_7 P7_0 to P7_7 P8_0 to P8_4 P8_6, P8_7 P9_0 to P9_7 P10_0 to P10_7 P11_0 to P11_7 ⁽¹⁾ P12_0 to P12_7 ⁽¹⁾ P13_0 to P13_7 ⁽¹⁾ P14_0, P14_1 ⁽¹⁾	I/O	8-bit I/O ports in CMOS, having a direction register to select an input or output. Each pin is set as an input port or output port. An input port can be set for a pull-up or for no pull-up in 4-bit unit by program. (except P7_1 and P9_1 for the N-channel open drain output.)
Input port	P8_5	I	Input pin for the $\overline{\text{NMI}}$ interrupt. Pin states can be read by the P8_5 bit in the P8 register.

I: Input O: Output I/O: Input/Output

NOTE:

1. Ports P11 to P14 are only in the 128-pin version.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

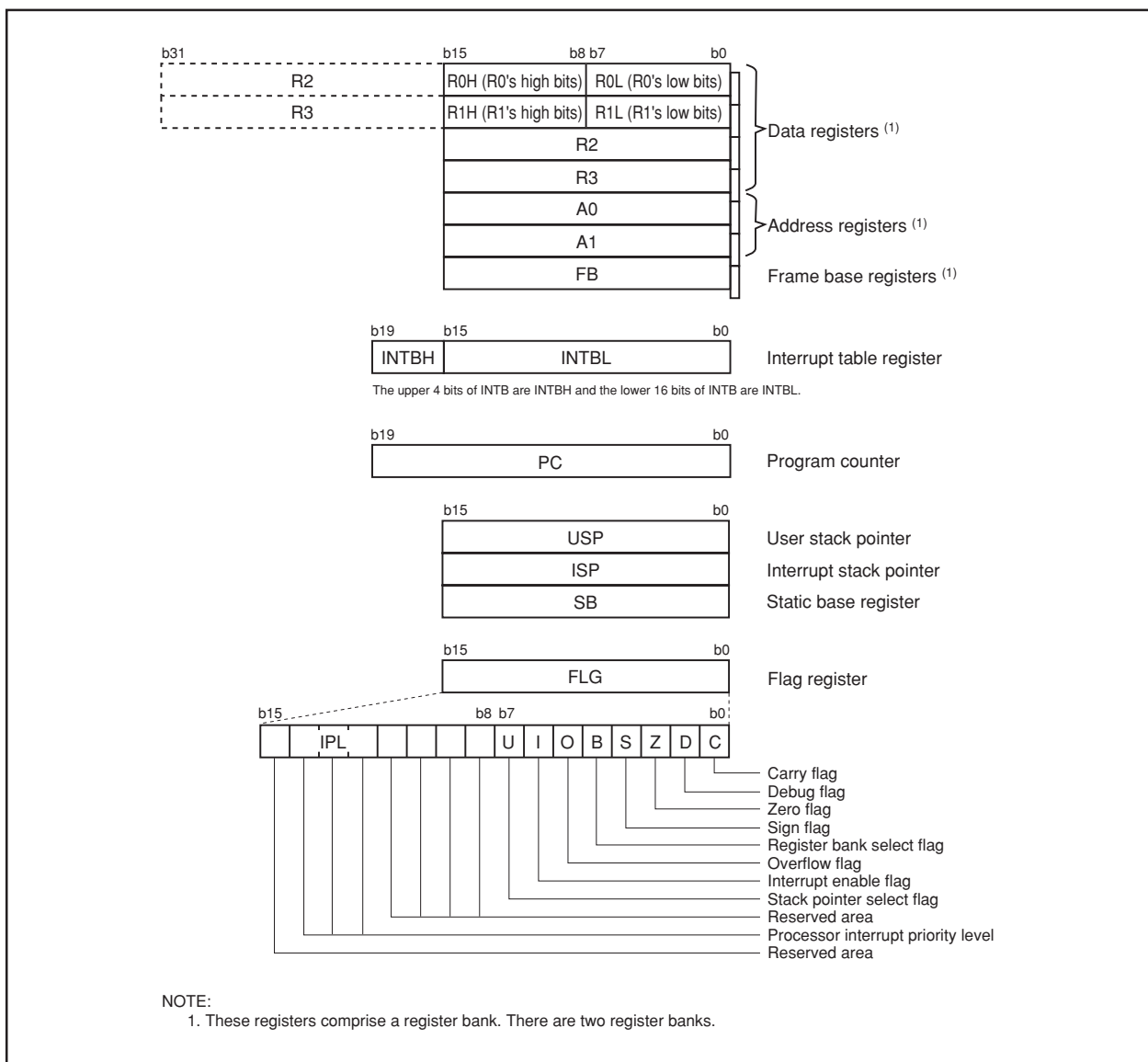


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The A0 register consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0.

In some instructions, A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

This flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is set to "0" when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is set to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt request is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 shows a memory map of the M16C/6N Group (M16C/6NK, M16C/6NM). The address space extends the 1 Mbyte from address 00000h to FFFFFh.

The internal ROM is allocated in a lower address direction beginning with address FFFFFh. For example, a 512-Kbyte internal ROM is allocated to the addresses from 80000h to FFFFFh.

As for the flash memory version, 4-Kbyte space (block A) exists in 0F000h to 0FFFFh. 4-Kbyte space is mainly for storing data. In addition to storing data, 4-Kbyte space also can store programs.

The fixed interrupt vector table is allocated to the addresses from FFFDCh to FFFFFh. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400h. For example, a 31-Kbyte internal RAM is allocated to the addresses from 00400h to 07FFFh. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated. The SFR is allocated to the addresses from 00000h to 003FFh. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.

The special page vector table is allocated to the addresses from FFE00h to FFFDBh. This vector is used by the JMPS or JSRS instruction. For details, refer to the **M16C/60 and M16C/20 Series Software Manual**.

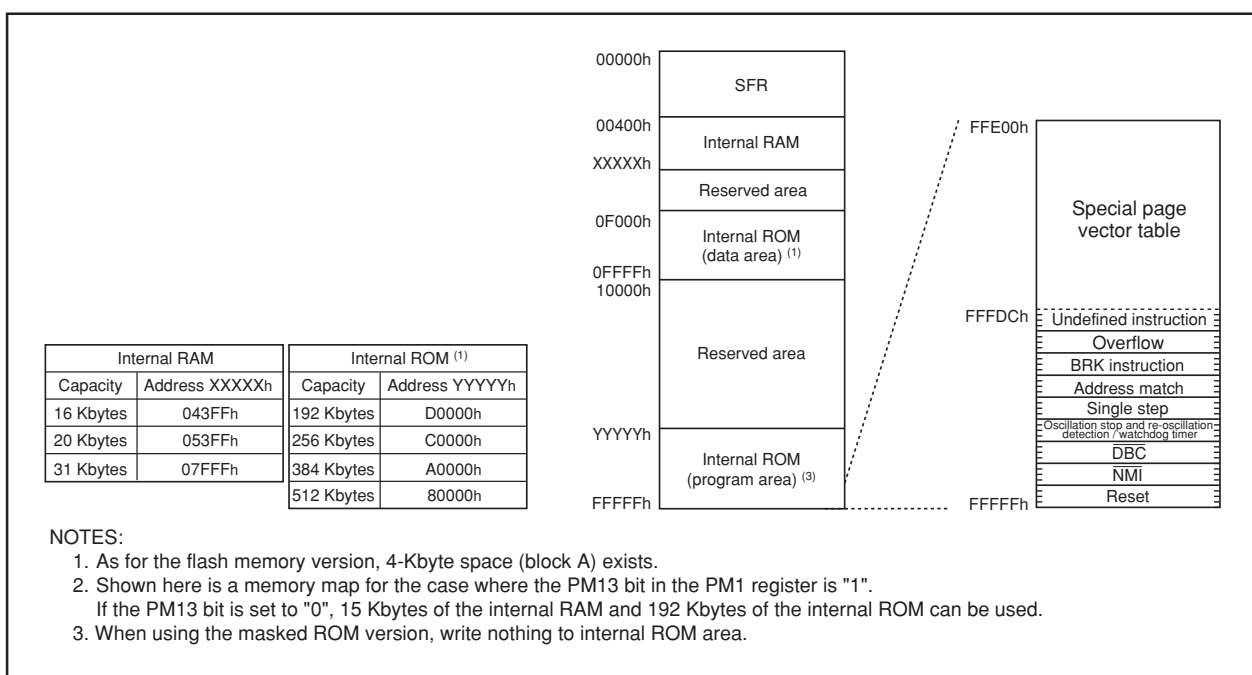


Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR (Special Function Register) is the control register of peripheral functions.

Tables 4.1 to 4.16 list the SFR information.

Table 4.1 SFR Information (1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor mode register 0	PM0	00h
0005h	Processor mode register 1	PM1	00001000b
0006h	System clock control register 0	CM0	01001000b
0007h	System clock control register 1	CM1	00100000b
0008h			
0009h	Address match interrupt enable register	AIER	XXXXXX00b
000Ah	Protect register	PRCR	XX000000b
000Bh			
000Ch	Oscillation stop detection register ⁽¹⁾	CM2	0X00X000b
000Dh			
000Eh	Watchdog timer start register	WDTS	XXh
000Fh	Watchdog timer control register	WDC	00XXXXXXb
0010h	Address match interrupt register 0	RMAD0	00h
0011h			00h
0012h			X0h
0013h			
0014h	Address match interrupt register 1	RMAD1	00h
0015h			00h
0016h			X0h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	PLL control register 0	PLC0	0001X010b
001Dh			
001Eh	Processor mode register 2	PM2	XXX00000b
001Fh			
0020h	DMA0 source pointer	SAR0	XXh
0021h			XXh
0022h			XXh
0023h			
0024h	DMA0 destination pointer	DAR0	XXh
0025h			XXh
0026h			XXh
0027h			
0028h	DMA0 transfer counter	TCR0	XXh
0029h			XXh
002Ah			
002Bh			
002Ch	DMA0 control register	DM0CON	00000X00b
002Dh			
002Eh			
002Fh			
0030h	DMA1 source pointer	SAR1	XXh
0031h			XXh
0032h			XXh
0033h			
0034h	DMA1 destination pointer	DAR1	XXh
0035h			XXh
0036h			XXh
0037h			
0038h	DMA1 transfer counter	TCR1	XXh
0039h			XXh
003Ah			
003Bh			
003Ch	DMA1 control register	DM1CON	00000X00b
003Dh			
003Eh			
003Fh			

X: Undefined

NOTES:

1. The CM20, CM21, and CM27 bits in the CM2 register do not change at oscillation stop detection reset.
2. The blank areas are reserved and cannot be accessed by users.

Table 4.2 SFR Information (2)

Address	Register	Symbol	After reset
0040h			
0041h	CAN0/1 wake up interrupt control register	C01WKIC	XXXXX000b
0042h	CAN0 successful reception interrupt control register	C0RECIC	XXXXX000b
0043h	CAN0 successful transmission interrupt control register	C0TRMIC	XXXXX000b
0044h	INT3 interrupt control register	INT3IC	XX00X000b
0045h	Timer B5 interrupt control register	TB5IC	XXXXX000b
	SI/O5 interrupt control register ⁽¹⁾	S5IC	
0046h	Timer B4 interrupt control register	TB4IC	XXXXX000b
	UART1 bus collision detection interrupt control register	U1BCNIC	
0047h	Timer B3 interrupt control register	TB3IC	XXXXX000b
	UART0 bus collision detection interrupt control register	U0BCNIC	
0048h	CAN1 successful reception interrupt control register	C1RECIC	XX00X000b
	SI/O4 interrupt control register	S4IC	
	INT5 interrupt control register	INT5IC	
0049h	CAN1 successful transmission interrupt control register	C1TRMIC	XX00X000b
	SI/O3 interrupt control register	S3IC	
	INT4 interrupt control register	INT4IC	
004Ah	UART2 bus collision detection interrupt control register	U2BCNIC	XXXXX000b
004Bh	DMA0 interrupt control register	DM0IC	XXXXX000b
004Ch	DMA1 interrupt control register	DM1IC	XXXXX000b
004Dh	CAN0/1 error interrupt control register	C01ERRIC	XXXXX000b
004Eh	A/D conversion interrupt control register	ADIC	XXXXX000b
	Key input interrupt control register	KUPIC	
004Fh	UART2 transmit interrupt control register	S2TIC	XXXXX000b
0050h	UART2 receive interrupt control register	S2RIC	XXXXX000b
0051h	UART0 transmit interrupt control register	S0TIC	XXXXX000b
0052h	UART0 receive interrupt control register	S0RIC	XXXXX000b
0053h	UART1 transmit interrupt control register	S1TIC	XXXXX000b
0054h	UART1 receive interrupt control register	S1RIC	XXXXX000b
0055h	Timer A0 interrupt control register	TA0IC	XXXXX000b
0056h	Timer A1 interrupt control register	TA1IC	XXXXX000b
	Timer A2 interrupt control register	TA2IC	
0057h	INT7 interrupt control register ⁽¹⁾	INT7IC	XX00X000b
	Timer A3 interrupt control register	TA3IC	
0058h	INT6 interrupt control register ⁽¹⁾	INT6IC	XX00X000b
	Timer A4 interrupt control register	TA4IC	
0059h	Timer B0 interrupt control register	TB0IC	XXXXX000b
	SI/O6 interrupt control register ⁽¹⁾	S6IC	
005Bh	Timer B1 interrupt control register	TB1IC	XX00X000b
	INT8 interrupt control register ⁽¹⁾	INT8IC	
005Ch	Timer B2 interrupt control register	TB2IC	XXXXX000b
005Dh	INT0 interrupt control register	INT0IC	XX00X000b
005Eh	INT1 interrupt control register	INT1IC	XX00X000b
005Fh	INT2 interrupt control register	INT2IC	XX00X000b
0060h	CAN0 message box 0: Identifier / DLC		XXh
0061h			XXh
0062h			XXh
0063h			XXh
0064h			XXh
0065h	CAN0 message box 0: Data field		XXh
0066h			XXh
0067h			XXh
0068h			XXh
0069h			XXh
006Ah	CAN0 message box 0: Time stamp		XXh
006Bh			XXh
006Ch			XXh
006Dh			XXh
006Eh			XXh
0070h	CAN0 message box 1: Identifier / DLC		XXh
0071h			XXh
0072h			XXh
0073h			XXh
0074h			XXh
0075h	CAN0 message box 1: Data field		XXh
0076h			XXh
0077h			XXh
0078h			XXh
0079h			XXh
007Ah	CAN0 message box 1: Time stamp		XXh
007Bh			XXh
007Ch			XXh
007Dh			XXh
007Eh			XXh
007Fh			XXh

X: Undefined

NOTES:

1. These registers exist only in the 128-pin version.
2. The blank area is reserved and cannot be accessed by users.

Table 4.3 SFR Information (3)

Address	Register	Symbol	After reset
0080h	CAN0 message box 2: Identifier / DLC		XXh
0081h			XXh
0082h			XXh
0083h			XXh
0084h			XXh
0085h			XXh
0086h			XXh
0087h			XXh
0088h			XXh
0089h			XXh
008Ah	CAN0 message box 2: Data field		XXh
008Bh			XXh
008Ch			XXh
008Dh			XXh
008Eh			XXh
008Fh	CAN0 message box 2: Time stamp		XXh
0090h			XXh
0091h			XXh
0092h			XXh
0093h			XXh
0094h			XXh
0095h			XXh
0096h			XXh
0097h			XXh
0098h			XXh
0099h			XXh
009Ah	CAN0 message box 3: Data field		XXh
009Bh			XXh
009Ch			XXh
009Dh			XXh
009Eh			XXh
009Fh	CAN0 message box 3: Time stamp		XXh
00A0h			XXh
00A1h			XXh
00A2h			XXh
00A3h			XXh
00A4h			XXh
00A5h			XXh
00A6h			XXh
00A7h			XXh
00A8h			XXh
00A9h			XXh
00AAh	CAN0 message box 4: Data field		XXh
00ABh			XXh
00ACh			XXh
00ADh			XXh
00AEh			XXh
00AFh	CAN0 message box 4: Time stamp		XXh
00B0h			XXh
00B1h			XXh
00B2h			XXh
00B3h			XXh
00B4h			XXh
00B5h			XXh
00B6h			XXh
00B7h			XXh
00B8h			XXh
00B9h			XXh
00BAh	CAN0 message box 5: Data field		XXh
00BBh			XXh
00BCh			XXh
00BDh			XXh
00BEh			XXh
00BFh	CAN0 message box 5: Time stamp		XXh

X: Undefined

Table 4.4 SFR Information (4)

Address	Register	Symbol	After reset
00C0h	CAN0 message box 6: Identifier / DLC		XXh
00C1h			XXh
00C2h			XXh
00C3h			XXh
00C4h			XXh
00C5h			XXh
00C6h	CAN0 message box 6: Data field		XXh
00C7h			XXh
00C8h			XXh
00C9h			XXh
00CAh			XXh
00CBh			XXh
00CCh			XXh
00CDh			XXh
00CEh	CAN0 message box 6: Time stamp		XXh
00CFh			XXh
00D0h	CAN0 message box 7: Identifier / DLC		XXh
00D1h			XXh
00D2h			XXh
00D3h			XXh
00D4h			XXh
00D5h			XXh
00D6h	CAN0 message box 7: Data field		XXh
00D7h			XXh
00D8h			XXh
00D9h			XXh
00DAh			XXh
00DBh			XXh
00DCh			XXh
00DDh			XXh
00DEh	CAN0 message box 7: Time stamp		XXh
00DFh			XXh
00E0h	CAN0 message box 8: Identifier / DLC		XXh
00E1h			XXh
00E2h			XXh
00E3h			XXh
00E4h			XXh
00E5h			XXh
00E6h	CAN0 message box 8: Data field		XXh
00E7h			XXh
00E8h			XXh
00E9h			XXh
00EAh			XXh
00EBh			XXh
00ECh			XXh
00EDh			XXh
00EEh	CAN0 message box 8: Time stamp		XXh
00EFh			XXh
00F0h	CAN0 message box 9: Identifier / DLC		XXh
00F1h			XXh
00F2h			XXh
00F3h			XXh
00F4h			XXh
00F5h			XXh
00F6h	CAN0 message box 9: Data field		XXh
00F7h			XXh
00F8h			XXh
00F9h			XXh
00FAh			XXh
00FBh			XXh
00FCh			XXh
00FDh			XXh
00FEh	CAN0 message box 9: Time stamp		XXh
00FFh			XXh

X: Undefined

Table 4.5 SFR Information (5)

Address	Register	Symbol	After reset
0100h	CAN0 message box 10: Identifier / DLC		XXh
0101h			XXh
0102h			XXh
0103h			XXh
0104h			XXh
0105h			XXh
0106h			XXh
0107h			XXh
0108h			XXh
0109h			XXh
010Ah	CAN0 message box 10: Data field		XXh
010Bh			XXh
010Ch			XXh
010Dh			XXh
010Eh			XXh
010Fh	CAN0 message box 10: Time stamp		XXh
0110h			XXh
0111h			XXh
0112h			XXh
0113h			XXh
0114h			XXh
0115h			XXh
0116h			XXh
0117h			XXh
0118h			XXh
0119h			XXh
011Ah	CAN0 message box 11: Data field		XXh
011Bh			XXh
011Ch			XXh
011Dh			XXh
011Eh			XXh
011Fh	CAN0 message box 11: Time stamp		XXh
0120h			XXh
0121h			XXh
0122h			XXh
0123h			XXh
0124h			XXh
0125h			XXh
0126h			XXh
0127h			XXh
0128h			XXh
0129h			XXh
012Ah	CAN0 message box 12: Data field		XXh
012Bh			XXh
012Ch			XXh
012Dh			XXh
012Eh			XXh
012Fh	CAN0 message box 12: Time stamp		XXh
0130h			XXh
0131h			XXh
0132h			XXh
0133h			XXh
0134h			XXh
0135h			XXh
0136h			XXh
0137h			XXh
0138h			XXh
0139h			XXh
013Ah	CAN0 message box 13: Data field		XXh
013Bh			XXh
013Ch			XXh
013Dh			XXh
013Eh			XXh
013Fh	CAN0 message box 13: Time stamp		XXh

X: Undefined

Table 4.6 SFR Information (6)

Address	Register	Symbol	After reset
0140h	CAN0 message box 14: Identifier /DLC		XXh
0141h			XXh
0142h			XXh
0143h			XXh
0144h			XXh
0145h	CAN0 message box 14: Data field		XXh
0146h			XXh
0147h			XXh
0148h			XXh
0149h			XXh
014Ah			XXh
014Bh			XXh
014Ch	CAN0 message box 14: Time stamp		XXh
014Dh			XXh
014Eh	CAN0 message box 15: Identifier /DLC		XXh
014Fh			XXh
0150h			XXh
0151h			XXh
0152h			XXh
0153h	CAN0 message box 15: Data field		XXh
0154h			XXh
0155h			XXh
0156h			XXh
0157h			XXh
0158h			XXh
0159h			XXh
015Ah	CAN0 message box 15: Time stamp		XXh
015Bh			XXh
015Ch	CAN0 global mask register	C0GMR	XXh
015Dh			XXh
015Eh			XXh
015Fh			XXh
0160h			XXh
0161h	CAN0 local mask A register	C0LMAR	XXh
0162h			XXh
0163h			XXh
0164h			XXh
0165h			XXh
0166h			XXh
0167h			XXh
0168h	CAN0 local mask B register	C0LMBR	XXh
0169h			XXh
016Ah			XXh
016Bh			XXh
016Ch			XXh
016Dh			XXh
016Eh			XXh
016Fh			XXh
0170h			XXh
0171h			XXh
0172h			XXh
0173h			XXh
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined

NOTE:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7)

Address	Register	Symbol	After reset
0180h			
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h			
01B3h			
01B4h			
01B5h	Flash memory control register 1 ⁽¹⁾	FMR1	0X00XX0Xb
01B6h			
01B7h	Flash memory control register 0 ⁽¹⁾	FMR0	00000001b
01B8h			00h
01B9h	Address match interrupt register 2	RMAD2	00h
01BAh			X0h
01BBh	Address match interrupt enable register 2	AIER2	XXXXXX00b
01BCh			00h
01BDh	Address match interrupt register 3	RMAD3	00h
01BEh			X0h
01BFh			

X: Undefined

NOTES:

1. These registers are included in the flash memory version.
2. The blank areas are reserved and cannot be accessed by users.

Table 4.8 SFR Information (8)

Address	Register	Symbol	After reset
01C0h	Timer B3, 4, 5 count start flag	TBSR	000XXXXXb
01C1h			
01C2h	Timer A1-1 register	TA11	XXh
01C3h			XXh
01C4h	Timer A2-1 register	TA21	XXh
01C5h			XXh
01C6h	Timer A4-1 register	TA41	XXh
01C7h			XXh
01C8h	Three-phase PWM control register 0	INVC0	00h
01C9h	Three-phase PWM control register 1	INVC1	00h
01CAh	Three-phase output buffer register 0	IDB0	00h
01CBh	Three-phase output buffer register 1	IDB1	00h
01CCh	Dead time timer	DTT	XXh
01CDh	Timer B2 interrupt occurrence frequency set counter	ICTB2	XXh
01CEh			
01CFh	Interrupt cause select register 2	IFSR2	X0000000b
01D0h	Timer B3 register	TB3	XXh
01D1h			XXh
01D2h	Timer B4 register	TB4	XXh
01D3h			XXh
01D4h	Timer B5 register	TB5	XXh
01D5h			XXh
01D6h	SI/O6 transmit/receive register ⁽¹⁾	S6TRR	XXh
01D7h			
01D8h	SI/O6 control register ⁽¹⁾	S6C	01000000b
01D9h	SI/O6 bit rate generator ⁽¹⁾	S6BRG	XXh
01DAh	SI/O3, 4, 5, 6 transmit/receive register ⁽²⁾	S3456TRR	XXXX0000b
01DBh	Timer B3 mode register	TB3MR	00XX0000b
01DCh	Timer B4 mode register	TB4MR	00XX0000b
01DDh	Timer B5 mode register	TB5MR	00XX0000b
01DEh	Interrupt cause select register 0	IFSR0	00h
01DFh	Interrupt cause select register 1	IFSR1	00h
01E0h	SI/O3 transmit/receive register	S3TRR	XXh
01E1h			
01E2h	SI/O3 control register	S3C	01000000b
01E3h	SI/O3 bit rate generator	S3BRG	XXh
01E4h	SI/O4 transmit/receive register	S4TRR	XXh
01E5h			
01E6h	SI/O4 control register	S4C	01000000b
01E7h	SI/O4 bit rate generator	S4BRG	XXh
01E8h	SI/O5 transmit/receive register ⁽¹⁾	S5TRR	XXh
01E9h			
01EAh	SI/O5 control register ⁽¹⁾	S5C	01000000b
01EBh	SI/O5 bit rate generator ⁽¹⁾	S5BRG	XXh
01ECh	UART0 special mode register 4	U0SMR4	00h
01EDh	UART0 special mode register 3	U0SMR3	000X0X0Xb
01EEh	UART0 special mode register 2	U0SMR2	X0000000b
01EFh	UART0 special mode register	U0SMR	X0000000b
01F0h	UART1 special mode register 4	U1SMR4	00h
01F1h	UART1 special mode register 3	U1SMR3	000X0X0Xb
01F2h	UART1 special mode register 2	U1SMR2	X0000000b
01F3h	UART1 special mode register	U1SMR	X0000000b
01F4h	UART2 special mode register 4	U2SMR4	00h
01F5h	UART2 special mode register 3	U2SMR3	000X0X0Xb
01F6h	UART2 special mode register 2	U2SMR2	X0000000b
01F7h	UART2 special mode register	U2SMR	X0000000b
01F8h	UART2 transmit/receive mode register	U2MR	00h
01F9h	UART2 bit rate generator	U2BRG	XXh
01FAh	UART2 transmit buffer register	U2TB	XXh
01FBh			XXh
01FCh	UART2 transmit/receive mode register 0	U2C0	00001000b
01FDh	UART2 transmit/receive mode register 1	U2C1	00000010b
01FEh	UART2 receive buffer register	U2RB	XXh
01FFh			XXh

X: Undefined

NOTES:

1. These registers exist only in the 128-pin version.
2. The S5TRF and S6TRF bits in the S3456TRR register are used in the 128-pin version.
3. The blank areas are reserved and cannot be accessed by users.

Table 4.9 SFR Information (9)

Address	Register	Symbol	After reset
0200h	CAN0 message control register 0	C0MCTL0	00h
0201h	CAN0 message control register 1	C0MCTL1	00h
0202h	CAN0 message control register 2	C0MCTL2	00h
0203h	CAN0 message control register 3	C0MCTL3	00h
0204h	CAN0 message control register 4	C0MCTL4	00h
0205h	CAN0 message control register 5	C0MCTL5	00h
0206h	CAN0 message control register 6	C0MCTL6	00h
0207h	CAN0 message control register 7	C0MCTL7	00h
0208h	CAN0 message control register 8	C0MCTL8	00h
0209h	CAN0 message control register 9	C0MCTL9	00h
020Ah	CAN0 message control register 10	C0MCTL10	00h
020Bh	CAN0 message control register 11	C0MCTL11	00h
020Ch	CAN0 message control register 12	C0MCTL12	00h
020Dh	CAN0 message control register 13	C0MCTL13	00h
020Eh	CAN0 message control register 14	C0MCTL14	00h
020Fh	CAN0 message control register 15	C0MCTL15	00h
0210h	CAN0 control register	C0CTLR	X0000001b
0211h			XX0X0000b
0212h	CAN0 status register	C0STR	00h
0213h			X0000001b
0214h	CAN0 slot status register	C0SSTR	00h
0215h			00h
0216h	CAN0 interrupt control register	C0ICR	00h
0217h			00h
0218h	CAN0 extended register	C0IDR	00h
0219h			00h
021Ah	CAN0 configuration register	C0CONR	XXh
021Bh			XXh
021Ch	CAN0 receive error count register	C0RECR	00h
021Dh	CAN0 transmit error count register	C0TECR	00h
021Eh	CAN0 time stamp register	C0TSR	00h
021Fh			00h
0220h	CAN1 message control register 0	C1MCTL0	00h
0221h	CAN1 message control register 1	C1MCTL1	00h
0222h	CAN1 message control register 2	C1MCTL2	00h
0223h	CAN1 message control register 3	C1MCTL3	00h
0224h	CAN1 message control register 4	C1MCTL4	00h
0225h	CAN1 message control register 5	C1MCTL5	00h
0226h	CAN1 message control register 6	C1MCTL6	00h
0227h	CAN1 message control register 7	C1MCTL7	00h
0228h	CAN1 message control register 8	C1MCTL8	00h
0229h	CAN1 message control register 9	C1MCTL9	00h
022Ah	CAN1 message control register 10	C1MCTL10	00h
022Bh	CAN1 message control register 11	C1MCTL11	00h
022Ch	CAN1 message control register 12	C1MCTL12	00h
022Dh	CAN1 message control register 13	C1MCTL13	00h
022Eh	CAN1 message control register 14	C1MCTL14	00h
022Fh	CAN1 message control register 15	C1MCTL15	00h
0230h	CAN1 control register	C1CTLR	X0000001b
0231h			XX0X0000b
0232h	CAN1 status register	C1STR	00h
0233h			X0000001b
0234h	CAN1 slot status register	C1SSTR	00h
0235h			00h
0236h	CAN1 interrupt control register	C1ICR	00h
0237h			00h
0238h	CAN1 extended register	C1IDR	00h
0239h			00h
023Ah	CAN1 configuration register	C1CONR	XXh
023Bh			XXh
023Ch	CAN1 receive error count register	C1RECR	00h
023Dh	CAN1 transmit error count register	C1TECR	00h
023Eh	CAN1 time stamp register	C1TSR	00h
023Fh			00h

X: Undefined

Table 4.10 SFR Information (10)

Address	Register	Symbol	After reset
0240h			
0241h			
0242h	CAN0 acceptance filter support register	C0AFS	XXh
0243h			XXh
0244h	CAN1 acceptance filter support register	C1AFS	XXh
0245h			XXh
0246h			
0247h			
0248h			
0249h			
024Ah			
024Bh			
024Ch			
024Dh			
024Eh			
024Fh			
0250h			
0251h			
0252h			
0253h			
0254h			
0255h			
0256h			
0257h			
0258h			
0259h			
025Ah			
025Bh			
025Ch			
025Dh			
025Eh	Peripheral clock select register	PCLKR	00h
025Fh	CAN0/1 clock select register	CCLKR	00h
0260h	CAN1 message box 0: Identifier / DLC		XXh
0261h			XXh
0262h			XXh
0263h			XXh
0264h			XXh
0265h	CAN1 message box 0: Data field		XXh
0266h			XXh
0267h			XXh
0268h			XXh
0269h			XXh
026Ah			XXh
026Bh			XXh
026Ch	CAN1 message box 0:Time stamp		XXh
026Dh			XXh
026Eh	CAN1 message box 1: Identifier / DLC		XXh
026Fh			XXh
0270h			XXh
0271h			XXh
0272h			XXh
0273h	CAN1 message box 1: Data field		XXh
0274h			XXh
0275h			XXh
0276h			XXh
0277h			XXh
0278h			XXh
0279h			XXh
027Ah	CAN1 message box 1:Time stamp		XXh
027Bh			XXh
027Ch			XXh
027Dh			
027Eh			
027Fh			

X: Undefined

NOTE:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.11 SFR Information (11)

Address	Register	Symbol	After reset
0280h	CAN1 message box 2: Identifier / DLC		XXh
0281h			XXh
0282h			XXh
0283h			XXh
0284h			XXh
0285h			XXh
0286h	CAN1 message box 2: Data field		XXh
0287h			XXh
0288h			XXh
0289h			XXh
028Ah			XXh
028Bh			XXh
028Ch			XXh
028Dh			XXh
028Eh	CAN1 message box 2: Time stamp		XXh
028Fh			XXh
0290h	CAN1 message box 3: Identifier / DLC		XXh
0291h			XXh
0292h			XXh
0293h			XXh
0294h			XXh
0295h			XXh
0296h	CAN1 message box 3: Data field		XXh
0297h			XXh
0298h			XXh
0299h			XXh
029Ah			XXh
029Bh			XXh
029Ch			XXh
029Dh			XXh
029Eh	CAN1 message box 3: Time stamp		XXh
029Fh			XXh
02A0h	CAN1 message box 4: Identifier / DLC		XXh
02A1h			XXh
02A2h			XXh
02A3h			XXh
02A4h			XXh
02A5h			XXh
02A6h	CAN1 message box 4: Data field		XXh
02A7h			XXh
02A8h			XXh
02A9h			XXh
02AAh			XXh
02ABh			XXh
02ACh			XXh
02ADh			XXh
02AEh	CAN1 message box 4: Time stamp		XXh
02AFh			XXh
02B0h	CAN1 message box 5: Identifier / DLC		XXh
02B1h			XXh
02B2h			XXh
02B3h			XXh
02B4h			XXh
02B5h			XXh
02B6h	CAN1 message box 5: Data field		XXh
02B7h			XXh
02B8h			XXh
02B9h			XXh
02BAh			XXh
02BBh			XXh
02BCh			XXh
02BDh			XXh
02BEh	CAN1 message box 5: Time stamp		XXh
02BFh			XXh

X: Undefined

Table 4.12 SFR Information (12)

Address	Register	Symbol	After reset
02C0h	CAN1 message box 6: Identifier / DLC		XXh
02C1h			XXh
02C2h			XXh
02C3h			XXh
02C4h			XXh
02C5h			XXh
02C6h			XXh
02C7h			XXh
02C8h			XXh
02C9h			XXh
02CAh	CAN1 message box 6: Data field		XXh
02CBh			XXh
02CCh			XXh
02CDh			XXh
02CEh			XXh
02CFh	CAN1 message box 6: Time stamp		XXh
02D0h			XXh
02D1h			XXh
02D2h			XXh
02D3h			XXh
02D4h			XXh
02D5h			XXh
02D6h			XXh
02D7h			XXh
02D8h			XXh
02D9h			XXh
02DAh	CAN1 message box 7: Data field		XXh
02DBh			XXh
02DCh			XXh
02DDh			XXh
02DEh			XXh
02DFh	CAN1 message box 7: Time stamp		XXh
02E0h			XXh
02E1h			XXh
02E2h			XXh
02E3h			XXh
02E4h			XXh
02E5h			XXh
02E6h			XXh
02E7h			XXh
02E8h			XXh
02E9h			XXh
02EAh	CAN1 message box 8: Data field		XXh
02EBh			XXh
02ECh			XXh
02EDh			XXh
02EEh			XXh
02EFh	CAN1 message box 8: Time stamp		XXh
02F0h			XXh
02F1h			XXh
02F2h			XXh
02F3h			XXh
02F4h			XXh
02F5h			XXh
02F6h			XXh
02F7h			XXh
02F8h			XXh
02F9h			XXh
02FAh	CAN1 message box 9: Data field		XXh
02FBh			XXh
02FCh			XXh
02FDh			XXh
02FEh			XXh
02FFh	CAN1 message box 9: Time stamp		XXh

X: Undefined

Table 4.13 SFR Information (13)

Address	Register	Symbol	After reset
0300h	CAN1 message box 10: Identifier / DLC		XXh
0301h			XXh
0302h			XXh
0303h			XXh
0304h			XXh
0305h	CAN1 message box 10: Data field		XXh
0306h			XXh
0307h			XXh
0308h			XXh
0309h			XXh
030Ah	CAN1 message box 10: Time stamp		XXh
030Bh			XXh
030Ch			XXh
030Dh			XXh
030Eh			XXh
030Fh	CAN1 message box 11: Identifier / DLC		XXh
0310h			XXh
0311h			XXh
0312h			XXh
0313h			XXh
0314h	CAN1 message box 11: Data field		XXh
0315h			XXh
0316h			XXh
0317h			XXh
0318h			XXh
0319h	CAN1 message box 11: Time stamp		XXh
031Ah			XXh
031Bh			XXh
031Ch			XXh
031Dh			XXh
031Eh	CAN1 message box 12: Identifier / DLC		XXh
031Fh			XXh
0320h			XXh
0321h			XXh
0322h			XXh
0323h	CAN1 message box 12: Data field		XXh
0324h			XXh
0325h			XXh
0326h			XXh
0327h			XXh
0328h	CAN1 message box 12: Time stamp		XXh
0329h			XXh
032Ah			XXh
032Bh			XXh
032Ch			XXh
032Dh	CAN1 message box 13: Identifier / DLC		XXh
032Eh			XXh
032Fh			XXh
0330h			XXh
0331h			XXh
0332h	CAN1 message box 13: Data field		XXh
0333h			XXh
0334h			XXh
0335h			XXh
0336h			XXh
0337h	CAN1 message box 13: Time stamp		XXh
0338h			XXh
0339h			XXh
033Ah			XXh
033Bh			XXh
033Ch	CAN1 message box 13: Time stamp		XXh
033Dh			XXh
033Eh			XXh
033Fh			XXh

X: Undefined

Table 4.14 SFR Information (14)

Address	Register	Symbol	After reset
0340h	CAN1 message box 14: Identifier / DLC		XXh
0341h			XXh
0342h			XXh
0343h			XXh
0344h			XXh
0345h			XXh
0346h	CAN1 message box 14: Data field		XXh
0347h			XXh
0348h			XXh
0349h			XXh
034Ah			XXh
034Bh			XXh
034Ch			XXh
034Dh			XXh
034Eh	CAN1 message box 14: Time stamp		XXh
034Fh			XXh
0350h	CAN1 message box 15: Identifier / DLC		XXh
0351h			XXh
0352h			XXh
0353h			XXh
0354h			XXh
0355h			XXh
0356h	CAN1 message box 15: Data field		XXh
0357h			XXh
0358h			XXh
0359h			XXh
035Ah			XXh
035Bh			XXh
035Ch			XXh
035Dh			XXh
035Eh	CAN1 message box 15: Time stamp		XXh
035Fh			XXh
0360h	CAN1 global mask register	C1GMR	XXh
0361h			XXh
0362h			XXh
0363h			XXh
0364h			XXh
0365h			XXh
0366h	CAN1 local mask A register	C1LMAR	XXh
0367h			XXh
0368h			XXh
0369h			XXh
036Ah			XXh
036Bh			XXh
036Ch	CAN1 local mask B register	C1LMBR	XXh
036Dh			XXh
036Eh			XXh
036Fh			XXh
0370h			XXh
0371h			XXh
0372h			
0373h			
0374h			
0375h			
0376h			
0377h			
0378h			
0379h			
037Ah			
037Bh			
037Ch			
037Dh			
037Eh			
037Fh			

X: Undefined

NOTE:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.15 SFR Information (15)

Address	Register	Symbol	After reset
0380h	Count start flag	TABSR	00h
0381h	Clock prescaler reset flag	CPSRF	0XXXXXXb
0382h	One-shot start flag	ONSF	00h
0383h	Trigger select register	TRGSR	00h
0384h	Up-down flag	UDF	00h ⁽¹⁾
0385h			
0386h	Timer A0 register	TA0	XXh
0387h			XXh
0388h	Timer A1 register	TA1	XXh
0389h			XXh
038Ah	Timer A2 register	TA2	XXh
038Bh			XXh
038Ch	Timer A3 register	TA3	XXh
038Dh			XXh
038Eh	Timer A4 register	TA4	XXh
038Fh			XXh
0390h	Timer B0 register	TB0	XXh
0391h			XXh
0392h	Timer B1 register	TB1	XXh
0393h			XXh
0394h	Timer B2 register	TB2	XXh
0395h			XXh
0396h	Timer A0 mode register	TA0MR	00h
0397h	Timer A1 mode register	TA1MR	00h
0398h	Timer A2 mode register	TA2MR	00h
0399h	Timer A3 mode register	TA3MR	00h
039Ah	Timer A4 mode register	TA4MR	00h
039Bh	Timer B0 mode register	TB0MR	00XX0000b
039Ch	Timer B1 mode register	TB1MR	00XX0000b
039Dh	Timer B2 mode register	TB2MR	00XX0000b
039Eh	Timer B2 special mode register	TB2SC	XXXXXX00b
039Fh			
03A0h	UART0 transmit/receive mode register	U0MR	00h
03A1h	UART0 bit rate generator	U0BRG	XXh
03A2h	UART0 transmit buffer register	U0TB	XXh
03A3h			XXh
03A4h	UART0 transmit/receive control register 0	U0C0	00001000b
03A5h	UART0 transmit/receive control register 1	U0C1	00XX0010b
03A6h	UART0 receive buffer register	U0RB	XXh
03A7h			XXh
03A8h	UART1 transmit/receive mode register	U1MR	00h
03A9h	UART1 bit rate generator	U1BRG	XXh
03AAh	UART1 transmit buffer register	U1TB	XXh
03ABh			XXh
03ACh	UART1 transmit/receive control register 0	U1C0	00001000b
03ADh	UART1 transmit/receive control register 1	U1C1	00XX0010b
03AEh	UART1 receive buffer register	U1RB	XXh
03AFh			XXh
03B0h	UART transmit/receive control register 2	UCON	X0000000b
03B1h			
03B2h			
03B3h			
03B4h			
03B5h			
03B6h			
03B7h			
03B8h	DMA0 request cause select register	DM0SL	00h
03B9h			
03BAh	DMA1 request cause select register	DM1SL	00h
03BBh			
03BCCh	CRC data register	CRCD	XXh
03BDh			XXh
03BEh	CRC input register	CRCIN	XXh
03BFh			

X: Undefined

NOTES:

1. The TA2P to TA4P bits in the UDF register are set to "0" after reset. However, the contents in these bits are indeterminate when read.
2. The blank areas are reserved and cannot be accessed by users.

Table 4.16 SFR Information (16)

Address	Register	Symbol	After reset
03C0h	A/D register 0	AD0	XXh
03C1h			XXh
03C2h			XXh
03C3h	A/D register 1	AD1	XXh
03C4h			XXh
03C5h	A/D register 2	AD2	XXh
03C6h			XXh
03C7h	A/D register 3	AD3	XXh
03C8h			XXh
03C9h			XXh
03CAh	A/D register 4	AD4	XXh
03CBh			XXh
03CCh	A/D register 5	AD5	XXh
03CDh			XXh
03CEh	A/D register 6	AD6	XXh
03CFh			XXh
03D0h			XXh
03D1h	A/D register 7	AD7	XXh
03D2h			XXh
03D3h			XXh
03D4h	A/D control register 2	ADCON2	00h
03D5h	A/D control register 0	ADCON0	00000XXXb
03D6h			00h
03D7h			00h
03D8h	D/A register 0	DA0	00h
03D9h	D/A register 1	DA1	00h
03DAh			00h
03DBh			00h
03DCh	D/A control register	DACON	00h
03DDh	Port P14 control register ⁽¹⁾	PC14	XX00XXXXb
03DEh			00h
03DFh			00h
03E0h	Pull-up control register 3 ⁽¹⁾	PUR3	00h
03E1h	Port P0 register	P0	XXh
03E2h	Port P1 register	P1	XXh
03E3h	Port P0 direction register	PD0	00h
03E4h	Port P1 direction register	PD1	00h
03E5h	Port P2 register	P2	XXh
03E6h	Port P3 register	P3	XXh
03E7h	Port P2 direction register	PD2	00h
03E8h	Port P3 direction register	PD3	00h
03E9h	Port P4 register	P4	XXh
03EAh	Port P5 register	P5	XXh
03EBh	Port P4 direction register	PD4	00h
03ECh	Port P5 direction register	PD5	00h
03EDh	Port P6 register	P6	XXh
03EEh	Port P7 register	P7	XXh
03EFh	Port P6 direction register	PD6	00h
03F0h	Port P7 direction register	PD7	00h
03F1h	Port P8 register	P8	XXh
03F2h	Port P9 register	P9	XXh
03F3h	Port P8 direction register	PD8	00X00000b
03F4h	Port P9 direction register	PD9	00h
03F5h	Port P10 register	P10	XXh
03F6h	Port P11 register ⁽¹⁾	P11	XXh
03F7h	Port P10 direction register	PD10	00h
03F8h	Port P11 direction register ⁽¹⁾	PD11	00h
03F9h	Port P12 register ⁽¹⁾	P12	XXh
03FAh	Port P13 register ⁽¹⁾	P13	XXh
03FBh	Port P12 direction register ⁽¹⁾	PD12	00h
03FCh	Port P13 direction register ⁽¹⁾	PD13	00h
03FDh	Pull-up control register 0	PUR0	00h
03FEh	Pull-up control register 1	PUR1	00h
03FFh	Pull-up control register 2	PUR2	00h
03FFh	Port control register	PCR	00h

X: Undefined

NOTES:

1. These registers exist only in the 128-pin version.
2. The blank areas are reserved and cannot be accessed by users.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated value	Unit
V _{CC}	Supply Voltage (VCC1 = VCC2)		VCC = AVCC	−0.3 to 6.5	V
AV _{CC}	Analog Supply Voltage		VCC = AVCC	−0.3 to 6.5	V
V _I	Input Voltage	RESET, CNVSS, BYTE, P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, VREF, XIN		−0.3 to VCC+0.3	V
		P7_1, P9_1		−0.3 to 6.5	V
V _O	Output Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XOUT		−0.3 to VCC+0.3	V
		P7_1, P9_1		−0.3 to 6.5	V
P _d	Power Dissipation		T _{opr} = 25°C	700	mW
T _{opr}	Operating Ambient Temperature	When the Microcomputer is Operating		−40 to 85	°C
		Flash Program Erase		0 to 60	
T _{stg}	Storage Temperature			−65 to 150	°C

NOTE:

1. Ports P11 to P14 are only in the 128-pin version.

Table 5.2 Recommended Operating Conditions (1) ⁽¹⁾

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply Voltage (V _{CC1} = V _{CC2})		3.0	5.0	5.5	V
AV _{CC}	Analog Supply Voltage			V _{CC}		V
V _{SS}	Supply Voltage			0		V
AV _{SS}	Analog Supply Voltage			0		V
V _{IH}	HIGH Input Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	0.8V _{CC}		V _{CC}	V
		P7_1, P9_1	0.8V _{CC}		6.5	V
V _{IL}	LOW Input Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	0		0.2V _{CC}	V
I _{OH(peak)}	HIGH Peak Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			−10.0	V
I _{OH(avg)}	HIGH Average Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0, P7_2 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			−5.0	mA
I _{OL(peak)}	LOW Peak Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			10.0	mA
I _{OL(avg)}	LOW Average Output Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1			5.0	mA

NOTES:

1. Referenced to V_{CC} = 3.0 to 5.5V at T_{opr} = −40 to 85°C unless otherwise specified.
2. The mean output current is the mean value within 100 ms.
3. The total I_{OL(peak)} for ports P0, P1, P2, P8_6, P8_7, P9, P10, P11, P14_0 and P14_1 must be 80mA max.
The total I_{OL(peak)} for ports P3, P4, P5, P6, P7, P8_0 to P8_4, P12 and P13 must be 80mA max.
The total I_{OH(peak)} for ports P0, P1, and P2 must be −40mA max.
The total I_{OH(peak)} for ports P3, P4, P5, P12 and P13 must be −40mA max.
The total I_{OH(peak)} for ports P6, P7 and P8_0 to P8_4 must be −40mA max.
The total I_{OH(peak)} for ports P8_6, P8_7, P9, P10, P11, P14_0 and P14_1 must be −40mA max.
4. P11 to P14 are only in the 128-pin version.

Table 5.3 Recommended Operating Conditions (2) ⁽¹⁾

Symbol	Parameter				Standard			Unit
					Min.	Typ.	Max.	
f(XIN)	Main Clock Input Oscillation Frequency ^{(2) (3) (4)}	No Wait	Mask ROM Version	VCC = 3.0 to 5.5V	0		16	MHz
f(XCIN)	Sub Clock Oscillation Frequency					32.768	50	kHz
f(Ring)	On-chip Oscillation Frequency					1		MHz
f(PLL)	PLL Clock Oscillation Frequency				16		24	MHz
f(BCLK)	CPU Operation Clock			VCC = 3.0 to 5.5V	0		24	MHz
t _{su} (PLL)	PLL Frequency Synthesizer Stabilization Wait Time						20	ms
f _(ripple)	Power Supply Ripple Allowable Frequency						10	kHz
V _{P-P} (ripple)	Power Supply Ripple Allowable Amplitude Voltage			VCC = 5V			0.5	V
				VCC = 3V			0.3	
V _{CC} (ΔV/ΔT)	Power Supply Ripple Rising/Falling Gradient			VCC = 5V			0.3	V/ms
				VCC = 3V			0.3	

NOTES:

1. Referenced to VCC = 3.0 to 5.5V at Topr = -40 to 85°C unless otherwise specified.
2. Relationship between main clock oscillation frequency and supply voltage is shown right.
3. Execute program/erase of flash memory by VCC = 3.0 ± 0.3 V or VCC = 5.0 ± 0.5 V.
4. When using 16MHz and over, use PLL clock. PLL clock oscillation frequency which can be used is 16MHz, 20MHz or 24MHz.

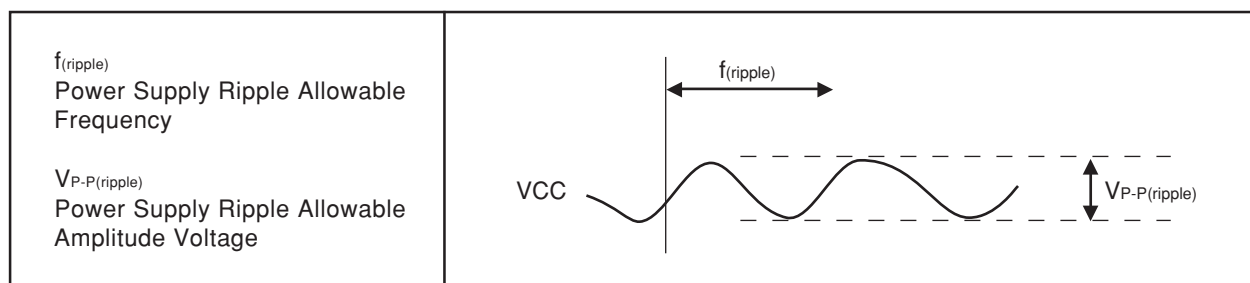
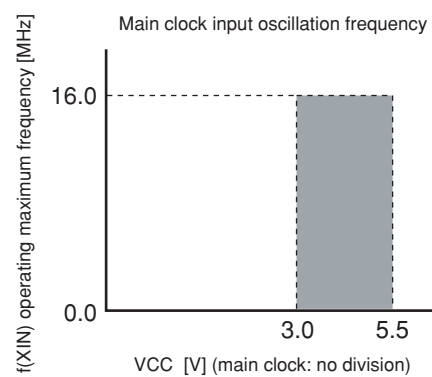
**Figure 5.1 Timing of Voltage Fluctuation**

Table 5.4 Electrical Characteristics (1) ⁽¹⁾

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	HIGH Output Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	I _{OH} = -5mA	V _{CC} -2.0		V _{CC}	V
V _{OH}	HIGH Output Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	I _{OH} = -200μA	V _{CC} -0.3		V _{CC}	V
V _{OH}	HIGH Output Voltage	XOUT	HIGHPOWER	I _{OH} = -1mA	3.0	V _{CC}	V
			LOWPOWER	I _{OH} = -0.5mA	3.0	V _{CC}	
	HIGH Output Voltage	XCOUT	HIGHPOWER	With no load applied	2.5		V
			LOWPOWER	With no load applied	1.6		
V _{OL}	LOW Output Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	I _{OL} = 5mA			2.0	V
V _{OL}	LOW Output Voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	I _{OL} = -200μA			0.45	V
V _{OL}	LOW Output Voltage	XOUT	HIGHPOWER	I _{OL} = 1mA		2.0	V
			LOWPOWER	I _{OL} = 0.5mA		2.0	
	LOW Output Voltage	XCOUT	HIGHPOWER	With no load applied	0		V
			LOWPOWER	With no load applied	0		
V _{T+} -V _{T-}	Hysteresis	TA0IN to TA4IN, TB0IN to TB5IN, INT0 to INT8, NMI, ADTRG, CTS0 to CTS2, SCL0 to SCL2, SDA0 to SDA2, CLK0 to CLK6, TA0OUT to TA4OUT, K10 to K13, RXD0 to RXD2, SIN3 to SIN6		0.2		1.0	V
V _{T+} -V _{T-}	Hysteresis	RESET		0.2		2.5	V
V _{T+} -V _{T-}	Hysteresis	XIN		0.2		0.8	V
I _{IH}	HIGH Input Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_3, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	V _I = 5V			5.0	μA
I _{IL}	LOW Input Current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_3, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1, XIN, RESET, CNVSS, BYTE	V _I = 0V			-5.0	μA
R _{PULLUP}	Pull-up Resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_0 to P4_7, P5_0 to P5_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_4, P8_6, P8_7, P9_0, P9_2 to P9_7, P10_0 to P10_7, P11_0 to P11_7, P12_0 to P12_7, P13_0 to P13_7, P14_0, P14_1	V _I = 0V	30	50	170	kΩ
R _{IXIN}	Feedback Resistance	XIN			1.5		MΩ
R _{IXCIN}	Feedback Resistance	XCIN			15		MΩ
V _{RAM}	RAM Retention Voltage		At stop mode	2.0			V

NOTES:

1. Referenced to VCC = 3.0 to 5.5V, VSS = 0V at T_{opr} = -40 to 85°C, f(BCLK) = 24MHz unless otherwise specified.
2. P11 to P14, INT6 to INT8, CLK5, CLK6, SIN5 and SIN6 are only in the 128-pin version.

Table 5.5 Electrical Characteristics (2) ⁽¹⁾

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
I _{cc}	Power Supply Current (VCC = 3.0 to 5.5V)	Output pins are open and other pins are VSS.	Mask ROM	f(BCLK) = 24MHz, PLL operation, No division		21	37	mA
				On-chip oscillation, No division		1		mA
			Flash Memory	f(BCLK) = 24MHz, PLL operation, No division		23	39	mA
				On-chip oscillation, No division		1.8		mA
			Flash Memory Program	f(BCLK) = 10MHz, VCC = 5V		15		mA
			Flash Memory Erase	f(BCLK) = 10MHz, VCC = 5V		25		mA
			Mask ROM	f(XCIN) = 32kHz, Low power dissipation mode, ROM ⁽²⁾		25		μA
			Flash Memory	f(BCLK) = 32kHz, Low power dissipation mode, RAM ⁽²⁾		25		μA
				f(BCLK) = 32kHz, Low power dissipation mode, Flash memory ⁽²⁾		420		μA
			Mask ROM Flash Memory	On-chip oscillation, Wait mode		50		μA
				f(BCLK) = 32kHz, Wait mode (3), Oscillation capacity High		8.5		μA
				f(BCLK) = 32kHz, Wait mode (3), Oscillation capacity Low		3.0		μA
				Stop mode, T _{opr} = 25°C		0.8	3.0	μA

NOTES:

1. Referenced to VCC = 3.0 to 5.5V, VSS = 0V at T_{opr} = -40 to 85°C, f(BCLK) = 24MHz unless otherwise specified.
2. This indicates the memory in which the program to be executed exists.
3. With one timer operated using fC32.

Table 5.6 A/D Conversion Characteristics ⁽¹⁾

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		VREF = VCC				10	Bit
INL	Integral Non-Linearity Error	10 bits	VREF = VCC	ANEX0, ANEX1 input, AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input			±3	LSB
				External op-amp connection mode			±7	LSB
			VREF = 5V	ANEX0, ANEX1 input, AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input			±5	LSB
				External op-amp connection mode			±7	LSB
		8 bits	VREF = AVCC = VCC = 3.3V				±2	LSB
—	Absolute Accuracy	10 bits	VREF = VCC	ANEX0, ANEX1 input, AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input			±3	LSB
				External op-amp connection mode			±7	LSB
			VREF = 5V	ANEX0, ANEX1 input, AN0 to AN7 input, AN0_0 to AN0_7 input, AN2_0 to AN2_7 input			±5	LSB
				External op-amp connection mode			±7	LSB
		8 bits	VREF = AVCC = VCC = 3.3V				±2	LSB
—	Tolerance Level Impedance					3		kΩ
DNL	Differential Non-Linearity Error						±1	LSB
—	Offset Error						±3	LSB
—	Gain Error						±3	LSB
R _{LADDER}	Ladder Resistance		VREF = VCC		10		40	kΩ
t _{CONV}	10-bit Conversion Time, Sample & Hold function Available		VREF = VCC = 5V, ϕAD = 10MHz		3.3			μs
	8-bit Conversion time, Sample & Hold function Available		VREF = VCC = 5V, ϕAD = 10MHz		2.8			μs
t _{SAMP}	Sampling Time				0.3			μs
V _{REF}	Reference Voltage				2.0		V _{CC}	V
V _{IA}	Analog Input Voltage				0		V _{REF}	V

NOTES:

1. Referenced to VCC = AVCC = VREF = 3.3 to 5.5V, VSS = AVSS = 0V, -40 to 85°C unless otherwise specified.
2. φAD frequency must be 10MHz or less.
3. A case without sample & hold function turn φAD frequency into 250kHz or more in addition to a limit of NOTE 2.
A case with sample & hold function turn φAD frequency into 1MHz or more in addition to a limit of NOTE 2.

Table 5.7 D/A conversion Characteristics ⁽¹⁾

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute Accuracy				1.0	%
t _{su}	Setup Time				3	μs
R _O	Output Resistance		4	10	20	kΩ
I _{VREF}	Reference Power Supply Input Current	(NOTE 2)			1.5	mA

NOTES:

1. Referenced to VCC = AVCC = VREF = 3.3 to 5.5V, VSS = AVSS = 0V, -40 to 85°C unless otherwise specified.
2. This applies when using one D/A converter, with the DAi register (i = 0, 1) for the unused D/A converter set to "00h".
The ladder resistance of the A/D converter is not included. Also, the current I_{VREF} always flows even though VREF may have been set to be unconnected by the ADCON1 register.

Table 5.8 Flash Memory Version Electrical Characteristics ⁽¹⁾

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
-	Word Program Time		30	200	μs
-	Block Erase Time		1	4	s
-	Erase All Unlocked Blocks Time		1 × n ⁽²⁾	4 × n ⁽²⁾	s
-	Lock Bit Program Time		30	200	μs
t _{ps}	Flash Memory Circuit Stabilization Wait Time			15	μs

NOTES:

1. Referenced to VCC = 4.5 to 5.5V, 3.0 to 3.6V, Topr = 0 to 60°C unless otherwise specified.

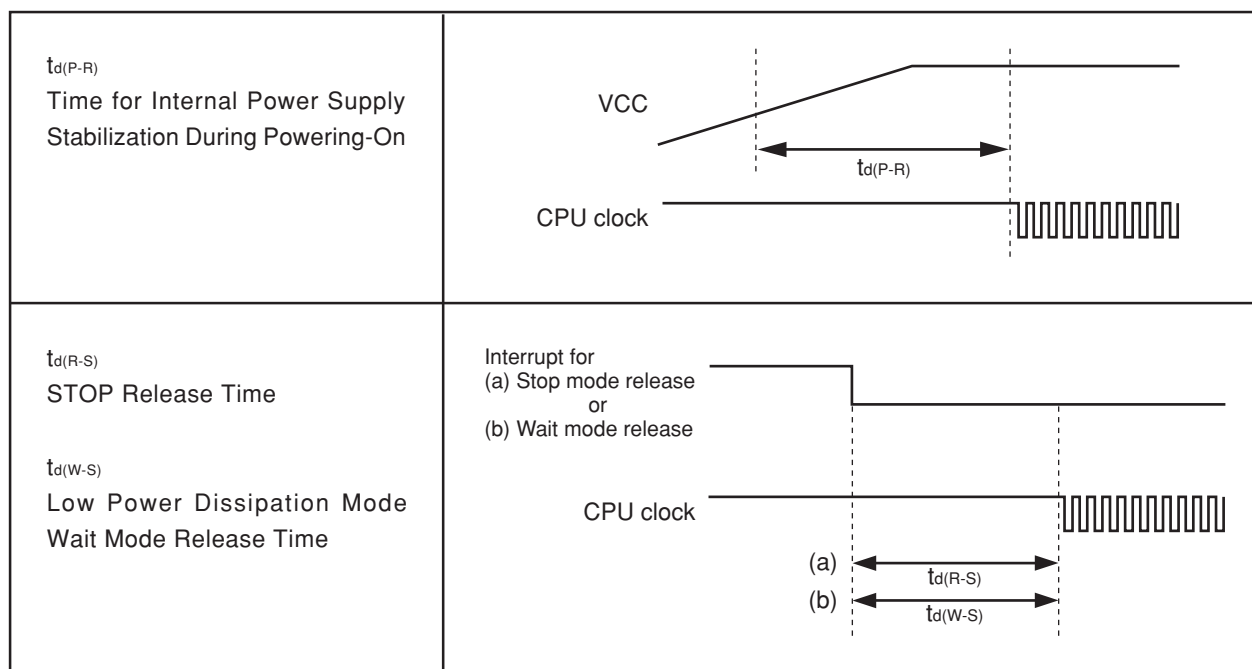
2. n denotes the number of blocks to erase.

Table 5.9 Flash Memory Version Program/Erase Voltage and Read Operation Voltage Characteristics (at Topr = 0 to 60°C)

Flash program, erase voltage	Flash read operation voltage
VCC = 3.0 ± 0.3V or 5.0 ± 0.5V	VCC = 3.0 to 5.5V

Table 5.10 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
t _{d(P-R)}	Time for Internal Power Supply Stabilization During Powering-On	VCC = 3.0 to 5.5V			2	ms
t _{d(R-S)}	STOP Release Time				150	μs
t _{d(W-S)}	Low Power Dissipation Mode Wait Mode Release Time				150	μs

**Figure 5.2 Power Supply Circuit Timing Diagram**

Timing Requirements**(Referenced to VCC = 5V, VSS = 0V, at Topr = -40 to 85°C unless otherwise specified)****Table 5.11 External Clock Input (XIN Input)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _c	External Clock Input Cycle Time	62.5		ns
t _{w(H)}	External Clock Input HIGH Pulse Width	25		ns
t _{w(L)}	External Clock Input LOW Pulse Width	25		ns
t _r	External Clock Rise Time		15	ns
t _f	External Clock Fall Time		15	ns

Table 5.12 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _{c(TA)}	TAiN Input Cycle Time	100		ns
t _{w(TAH)}	TAiN Input HIGH Pulse Width	40		ns
t _{w(TAL)}	TAiN Input LOW Pulse Width	40		ns

Table 5.13 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _{c(TA)}	TAiN Input Cycle Time	400		ns
t _{w(TAH)}	TAiN Input HIGH Pulse Width	200		ns
t _{w(TAL)}	TAiN Input LOW Pulse Width	200		ns

Table 5.14 Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _{c(TA)}	TAiN Input Cycle Time	200		ns
t _{w(TAH)}	TAiN Input HIGH Pulse Width	100		ns
t _{w(TAL)}	TAiN Input LOW Pulse Width	100		ns

Table 5.15 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _{w(TAH)}	TAiN Input HIGH Pulse Width	100		ns
t _{w(TAL)}	TAiN Input LOW Pulse Width	100		ns

Table 5.16 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _{c(UP)}	TAiOUT Input Cycle Time	2000		ns
t _{w(UPH)}	TAiOUT Input HIGH Pulse Width	1000		ns
t _{w(UPL)}	TAiOUT Input LOW Pulse Width	1000		ns
t _{su(UP-TIN)}	TAiOUT Input Setup Time	400		ns
t _{h(TIN-UP)}	TAiOUT Input Hold Time	400		ns

Table 5.17 Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t _{c(TA)}	TAiN Input Cycle Time	800		ns
t _{su(TAIN-TAOUT)}	TAiOUT Input Setup Time	200		ns
t _{su(TAOUT-TAIN)}	TAiN Input Setup Time	200		ns

Timing Requirements**(Referenced to VCC = 5V, VSS = 0V, at Topr = –40 to 85°C unless otherwise specified)****Table 5.18 Timer B Input (Counter Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width (counted on both edges)	80		ns

Table 5.19 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.20 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input HIGH Pulse Width	200		ns
$t_{w(TBL)}$	TBiIN Input LOW Pulse Width	200		ns

Table 5.21 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	ADTRG Input Cycle Time (trigger able minimum)	1000		ns
$t_{w(ADL)}$	ADTRG Input LOW Pulse Width	125		ns

Table 5.22 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input HIGH Pulse Width	100		ns
$t_{w(CKL)}$	CLKi Input LOW Pulse Width	100		ns
$t_{d(C-Q)}$	TXDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TXDi Hold Time	0		ns
$t_{su(D-C)}$	RXDi Input Setup Time	70		ns
$t_{h(C-D)}$	RXDi Input Hold Time	90		ns

Table 5.23 External Interrupt INTi Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	INTi Input HIGH Pulse Width	250		ns
$t_{w(INL)}$	INTi Input LOW Pulse Width	250		ns

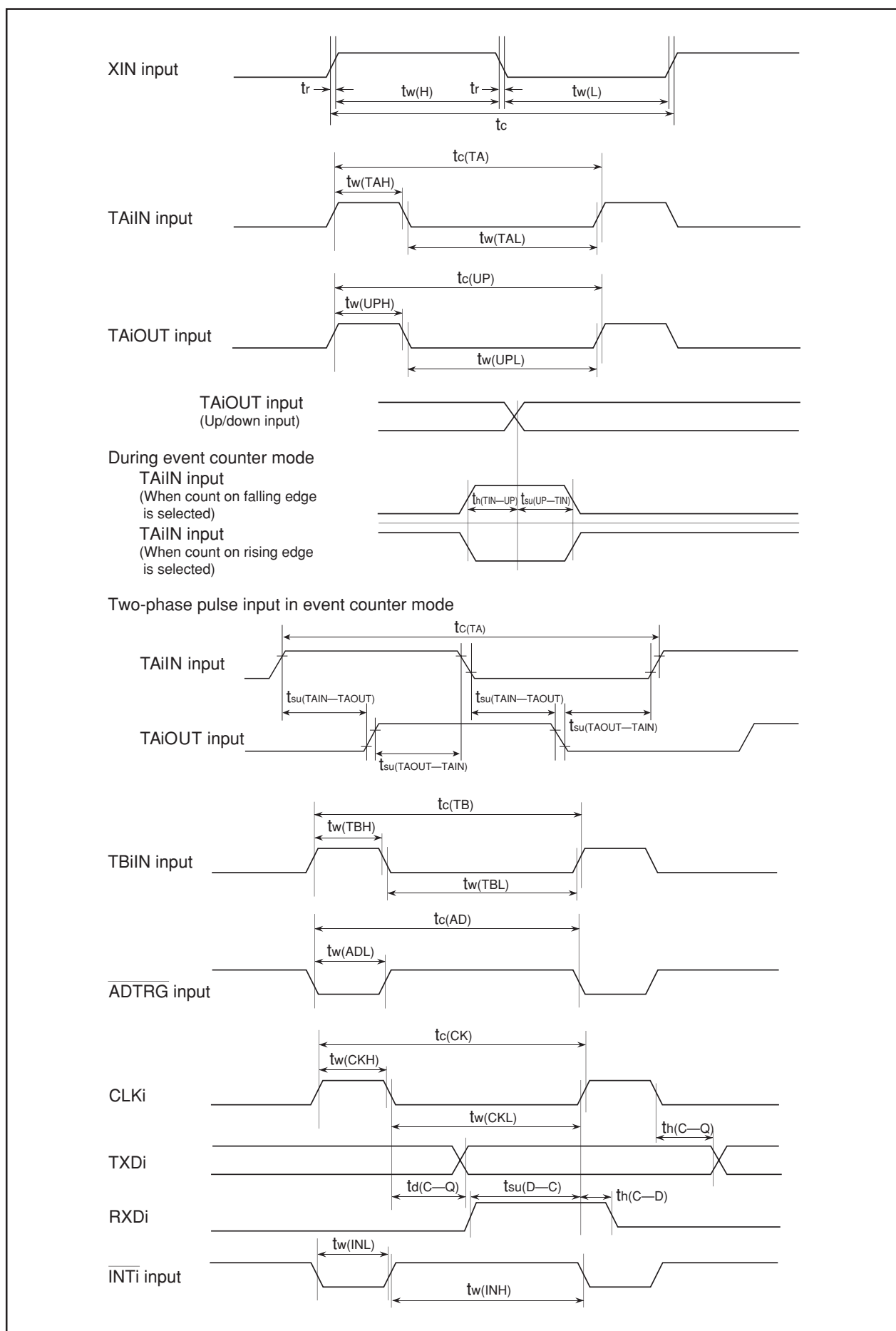


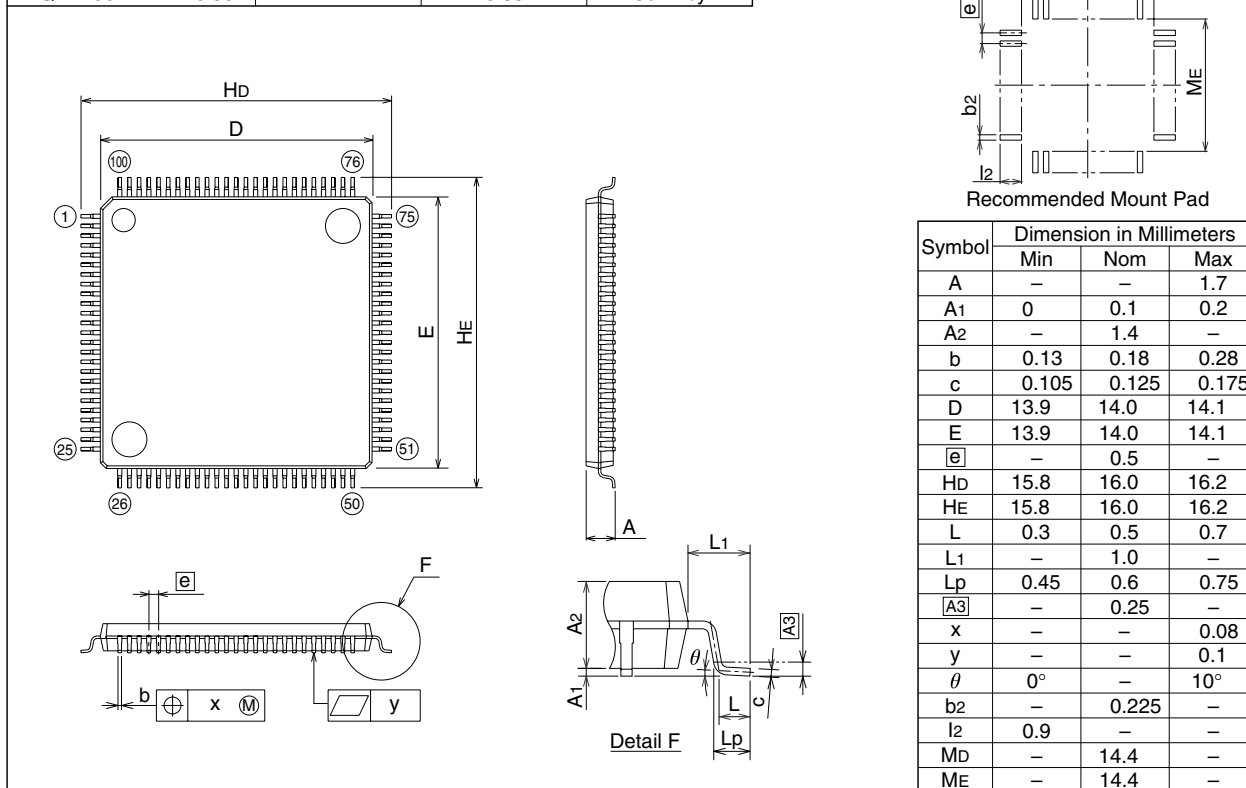
Figure 5.3 Timing Diagram

Package Dimensions

100P6Q-A Recommended

Plastic 100pin 14×14mm body LQFP

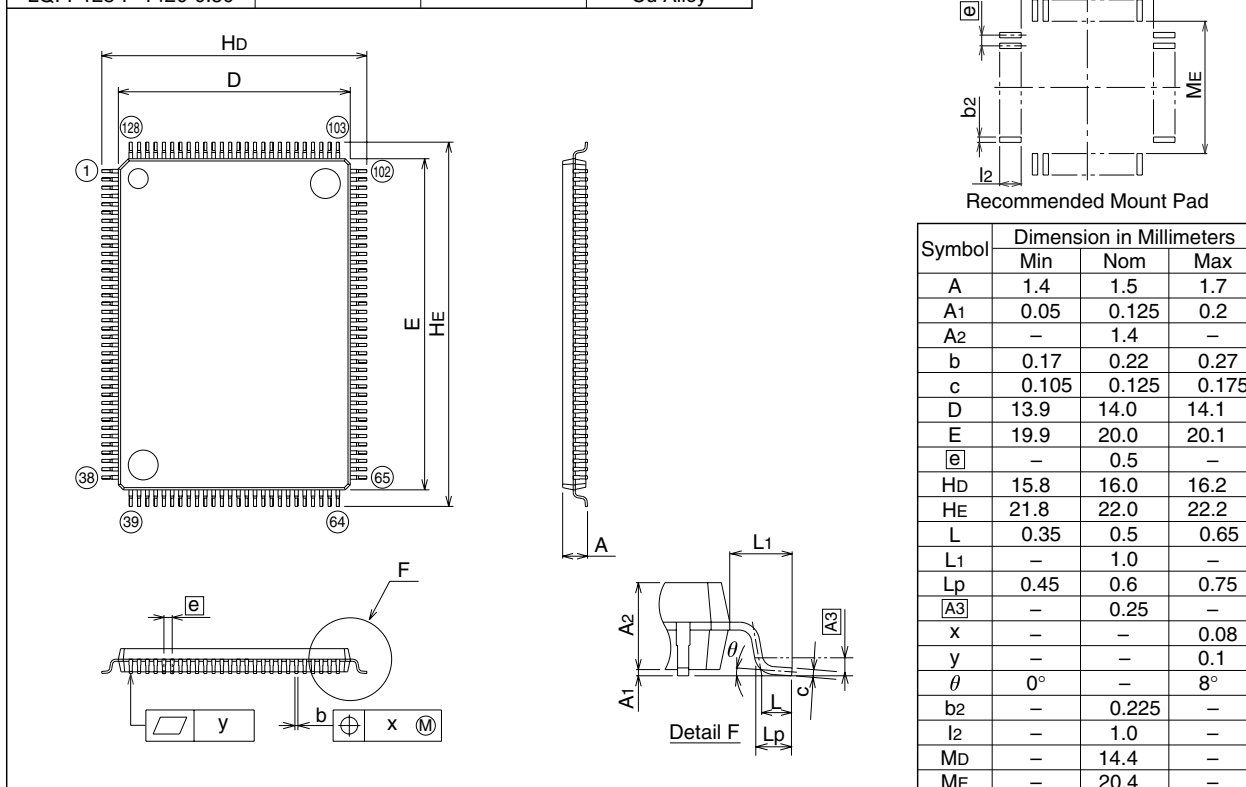
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	—	0.63	Cu Alloy



128P6Q-A Recommended

Plastic 128pin 14×20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP128-P-1420-0.50	—	—	Cu Alloy



REVISION HISTORY

M16C/6N Group (M16C/6NK, M16C/6NM) Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Jul. 20, 2004	–	First edition issued

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