File Number **2269**

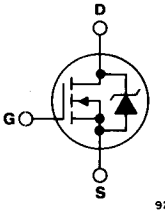
RFD16N05L, RFD16N05LSM

N-Channel Logic Level Enhancement-Mode Power Field-Effect Transistors (MegaFETs)

16 A, 50 V
$r_{ds(on)}$ = 0.047 Ω

Features:
- *Design optimized for 5 volt gate drive*
- *Can be driven directly from Q-MOS, N-MOS, TTL Circuits*
- *Compatible with automotive drive requirements*
- *SOA is power-dissipation limited*
- *Nanosecond switching speeds*
- *Linear transfer characteristics*
- *High input impedance*
- *Majority carrier device*

TERMINAL DIAGRAM



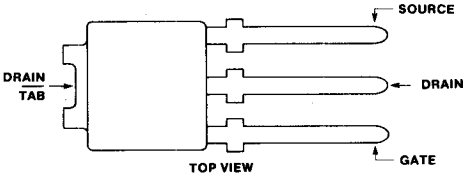
92CS-42658

N-CHANNEL ENHANCEMENT MODE

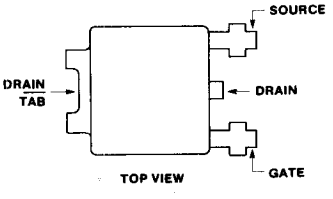
The RFD16N05L and RFD16N05LSM n-channel logic level power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor-relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3-5 volt range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

The RFD16N05L is supplied in the JEDEC TO-251 plastic package and the RFD16N05LSM in the JEDEC TO-252 plastic package.

TERMINAL DESIGNATION



TO-251AA



TO-252AA

92CS-43478

MAXIMUM RATINGS, *Absolute-Maximum Values (T_c = 25°C):*

DRAIN-SOURCE VOLTAGE, V_{DSS} ..... 50 V
DRAIN-GATE VOLTAGE, V_{DGR} (R_{GE} = 1MΩ) ..... 50 V
GATE-SOURCE VOLTAGE, V_{GS} ..... ±10 V
DRAIN CURRENT:
- •I_D, RMS Continuous ..... 16 A
- I_{DM}, Pulsed ..... 45 A

SINGLE PULSE AVALANCHE ENERGY RATING, E_{AS}† ..... 200 mj
AVALANCHE CURRENT, I_{AS} ..... 16 A
POWER DISSIPATION P_T:
- At T_C = 25°C ..... 60 W
- Derated above T_C = 25°C ..... 0.48 W/°C

OPERATING AND STORAGE TEMPERATURE, T_j, T_{stg} ..... −55 to +150°C

•ID Current Limited by package.
†V_{DD} = 10 V, starting T_j = 25°C, L = 1.25 mHy, I_{peak} = 16 A. See Figs. 13 and 14.

RFD16N05L, RFD16N05LSM

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C) = 25° C unless otherwise specified:*

CHARACTERISTIC		TEST CONDITIONS		LIMITS MIN.	LIMITS MAX.	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25 mA, V_{GS} = 0 V		50	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS} = V_{DS}, I_D = 0.25 mA		1	2	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V T_C = 150° C		—	1 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V		—	100	nA
Static Drain-Source On Resistance	$r_{DS}(on)$	I_D = 16 A, V_{GS} = 5 V I_D = 16 A, V_{GS} = 4 V		—	0.047 0.056	Ω
Turn-On Time	t(on)	V_{DD} = 25 V, I_D = 8 A I_{g1} = I_{g2} = 0.8 A V_{GS} (clamp) + 5 V, − 0.6 V R_L = 3.125 Ω		—	60	ns
Turn-On Delay Time	$t_d(on)$			—	15 (typ.)	
Rise Time	t_r			—	30 (typ.)	
Turn-Off Delay Time	$t_d(off)$			—	42 (typ.)	
Fall Time	t_f			—	14 (typ.)	
Turn-Off Time	t(off)			—	100	
Total Gate Charge	$Q_g(total)$	V_{GS} = 0-10 V	V_{DD} = 40 V	—	80	nC
Gate Charge at 5 V	$Q_g(5)$	V_{GS} = 0-5 V	I_D = 16 A	—	45	
Threshold Gate Charge	$Q_g(th)$	V_{GS} = 0-1 V	R_L = 2.5 Ω	—	3	
Plateau Voltage	V(plateau)	I_D = 16 A, V_{DS} = 15 V		—	4	V
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 25 V, I_D = 8 A, R_L = 3.125 Ω L = 0.2 μH, I_{g1} = I_{g2} = 0.8 A V_{GS} (clamp) + 5 V, −0.6 V		—	19	μJ
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$			—	2.083	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$			—	100	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS:

CHARACTERISTIC		TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 16 A	—	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 16 A, dI_F/d_t = 100 A/μs	—	125	ns

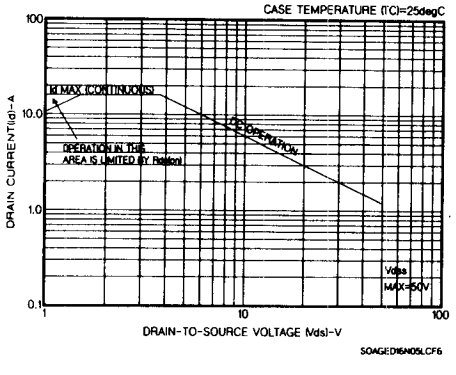


Fig. 1 - Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

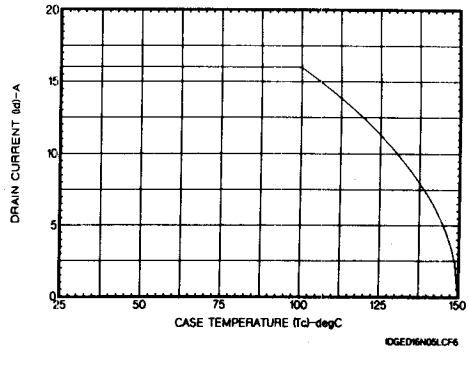


Fig. 2 - Maximum continuous drain current vs. temperature.

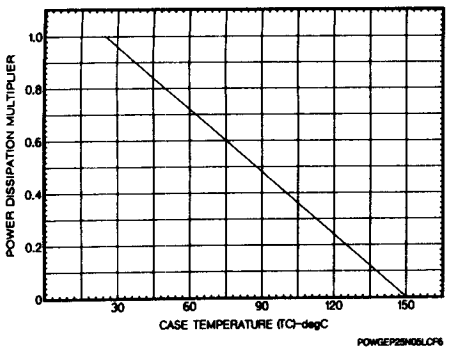


Fig. 3 - Normalized power dissipation vs. temperature derating curve.

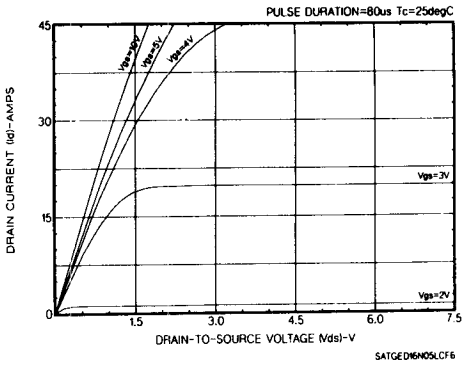


Fig. 4 - Typical saturation characteristics.

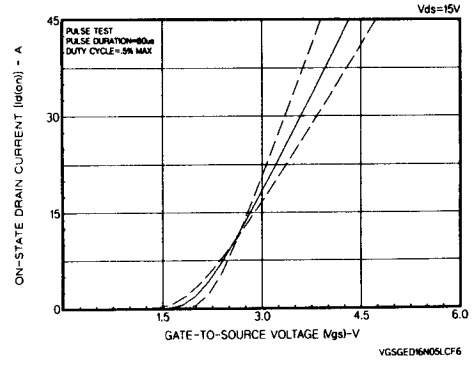


Fig. 5 - Typical transfer characteristics.

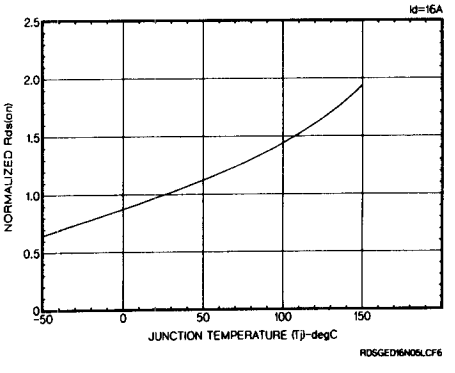


Fig. 6 - Normalized $r_{ds}(on)$ vs. junction temperature.

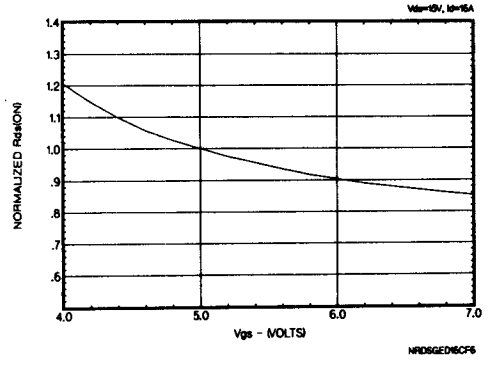


Fig. 7 - Normalized $r_{ds}(on)$ vs. V_{gs}.

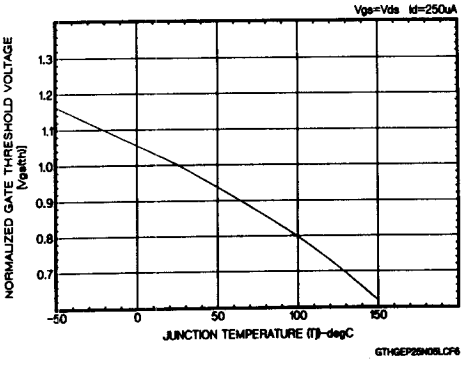


Fig. 8 - Typical normalized gate threshold voltage.

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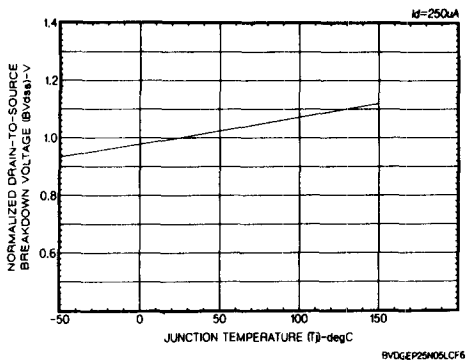

Fig. 9 - Drain source breakdown voltage vs. temperature.

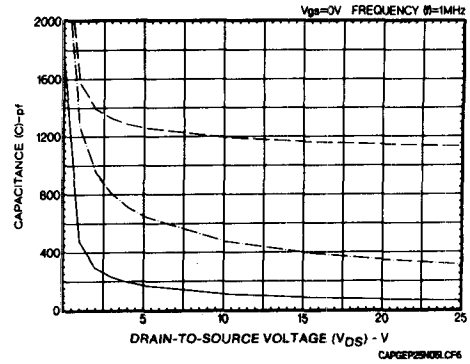

Fig. 10 - Typical capacitance vs. voltage.

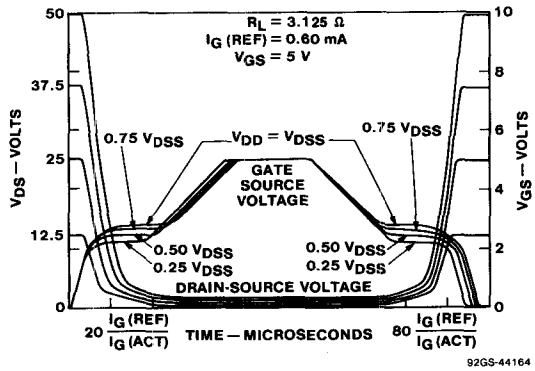

Fig. 11 - Normalized switching waveforms for constant gate-current.
(Refer to RCA application notes AN-7254 and AN-7260.)

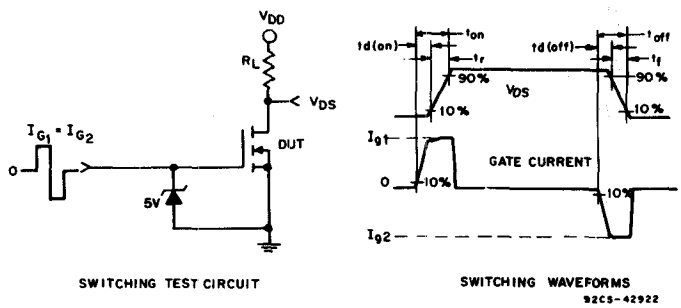

Fig. 12 - Resistive switching.