

CMOS 8-Bit Microcontroller

TMP88CP77F, TMP88CS77F, TMP88CU77F

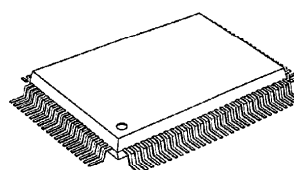
The TMP88CP77/S77/U77 are the high speed and high performance 8-bit single chip microcomputers. These MCU contain VFT (Vacuum Fluorescent Tube) driver, serial interface, 8-bit AD converter and multi-function timer/counter on a chip.

PART No.	ROM	RAM	PACKAGE	OTP MCU
TMP88CP77F	48K × 8 bit + 256 × 8 bit	1K × 8-bit	P-QFP100-1420-0.65A	TMP88PU77F
TMP88CS77F	64K × 8 bit + 256 × 8 bit	2K × 8-bit		
TMP88CU77F	96K × 8 bit + 256 × 8 bit	3K × 8-bit		

Features

- ◆ 8-bit single-chip microcomputer TLCS-870/X series microcomputer
- ◆ interrupt sources: 20 (6 external, 14 internal)
- ◆ I/O ports: 88 pins
- ◆ Three 16-bit Timer/Counters
 - TC1: Timer, Event counter, Pulse width measurement, External trigger timer, Window modes
 - TC2: Timer, Event counter, Window modes
 - ETC1: Timer, Event counter, Window mode
 - Minimum resolution: 500 μ s at 8 MHz
 - Two capture inputs (edge-selectable)
 - Two compare outputs
 - (High/Low/Toggle/Steady output modes)
- ◆ 8-bit Timer/Counter
 - TC4: Timer, Event counter, PWM output, Programmable divider output modes
- ◆ Time Base Timer (Interrupt frequency: 1 Hz to 16384 Hz)
- ◆ Divider output function (frequency: 1 kHz to 8 kHz)

P-QFP100-1420-0.65A



TMP88CP77F
TMP88CS77F
TMP88CU77F
TMP88PU77F

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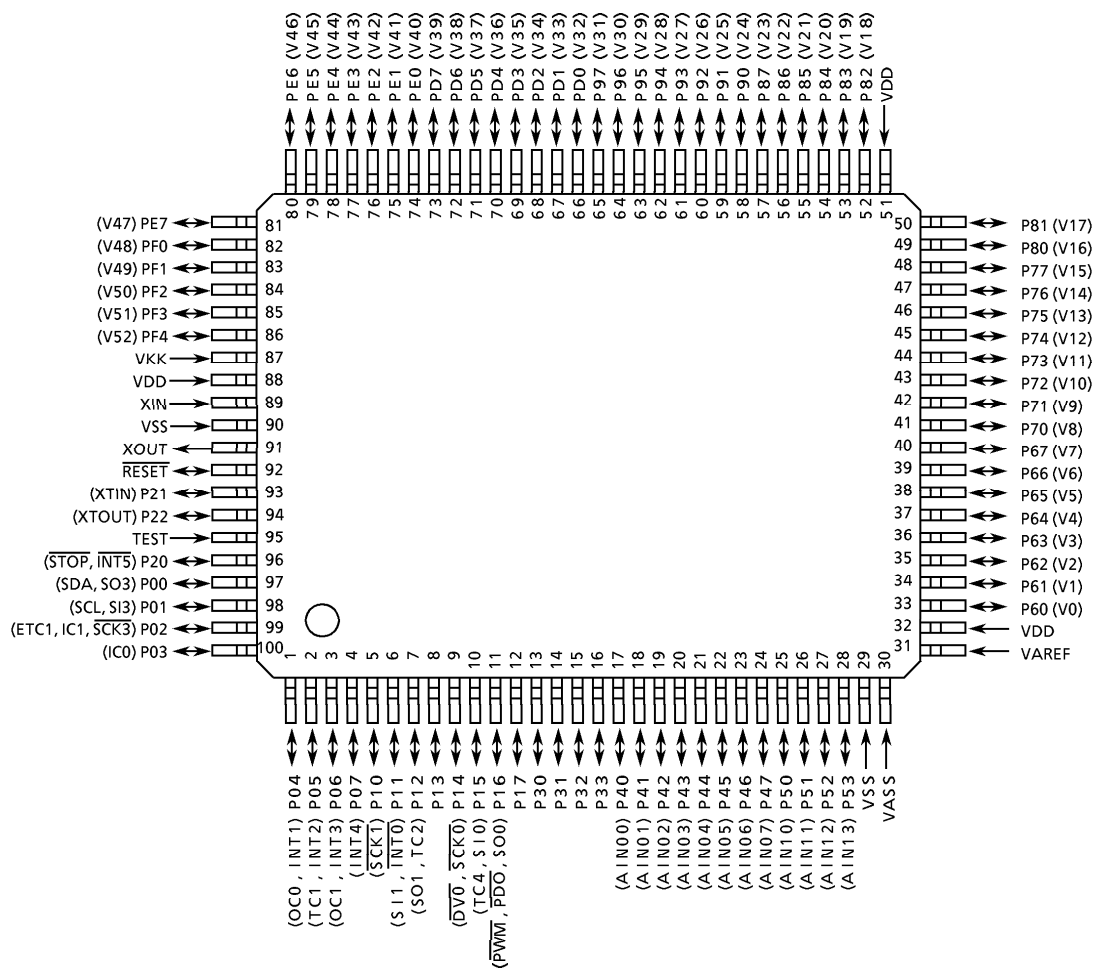


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- ◆ Watchdog Timer
 - Interrupt source/reset output (programmable)
- ◆ Two 8-bit Serial Interfaces
 - With 8 bytes and 32 bytes transmits/receive data buffer
 - Internal/external serial clock, and 4/8-bit mode
- ◆ Serial bus Interface
 - I²C-bus, 8-bit SIO modes
- ◆ 8-bit successive approximate type AD converter with sample and hold
 - 12 analog inputs
 - Conversion time: 23 μ s at 8 MHz
- ◆ Vacuum Fluorescent Tube Driver (automatic display)
 - Programmable grid scan
 - High breakdown voltage ports (max.40 V $\times$ 53 bits)
- ◆ Dual clock operation
 - Single/Dual-clock mode
- ◆ Five Power saving operating modes
 - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.
 - SLOW mode: Low power consumption operation using low-frequency clock (32.768 kHz)
 - IDLE1 mode: CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts.
 - IDLE2 mode: CPU stops, and Peripherals operate using high-and low-frequency clock. Release by interrupt.
 - SLEEP mode: CPU stops, and Peripherals operate using low-frequency clock. Release by interrupts.
- ◆ Wide operating voltage: 4.5 to 5.5 V at 12.5 MHz / 32.768 kHz, 2.7 to 5.5 V at 32.768 kHz
- ◆ Emulation Pod: BM87CP77FOA

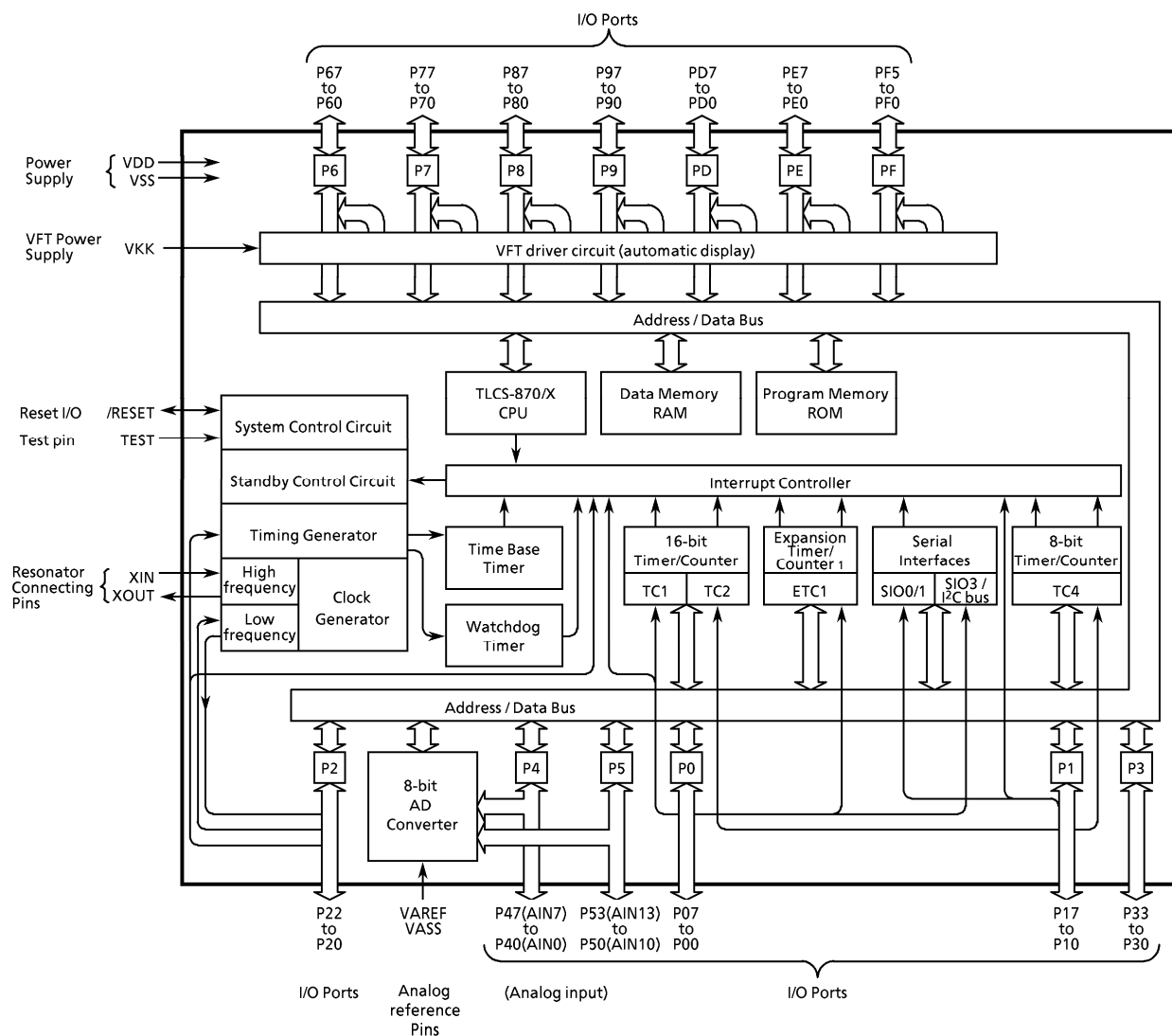
Pin Assignments (Top View)

P-QFP100-1420-0.65A



Note: All VDDs should be connected externally for keeping the same voltage level.

Block Diagram



Pin Function

Pin Name	I/O	Function	
P07 (INT4)	I/O (input)	8-bit input/output port with latch. When used as input port, multi function timer/counter, external interrupt input, serial bus interface, the latch must be set to "1".	External interrupt input 4
P06 (INT3, OC1)	I/O (I/O)		External interrupt input 3 or Expansion Timer/Counter compare output 1
P05 (TC1, INT2)	I/O (input)		Timer/Counter 1 input or External interrupt input 2
P04 (OC0, INT1)	I/O (I/O)		Expansion Timer/Counter compare output 0 or External interrupt input 1
P03 (IC0)	I/O (input)		Expansion Timer/Counter capture input 0
P02 (IC1, ETC1, $\overline{SCK3}$)	I/O (I/O)		Expansion Timer/Counter capture input 1 or Expansion Timer/Counter 1 input or SIO3 serial clock input/output
P01 (SCL, SI3)	I/O (I/O)		I ² C bus serial clock input/output or SIO3 serial data input
P00 (SDA, SO3)	I/O (I/O)		I ² C bus serial data input/output or SIO3 serial data output
P17	I/O	8-bit programmable input/output ports (tri-state). Each bit of this port can be individually configured as an input or an output under software control. When used as serial data input, external interrupt input, timer/counter input, the input mode is configured.	8-bit PWM output or 8-bit programmable divider output or SIO0 serial data output
P16 (PWM, $\overline{PDO}$, SO0)	I/O (output)		Timer/Counter 4 input or SIO0 serial data input
P15 (TC4, SIO)	I/O (input)		Divider output or SIO0 serial clock input/output
P14 ($\overline{DVO}$, $\overline{SCK0}$)	I/O (I/O)		SIO1 serial data output or Timer/Counter 2 input
P13	I/O		SIO1 serial data input or External interrupt 0 input
P12 (SO1, TC2)	I/O (I/O)		SIO1 serial clock input/output
P11 (SI1, $\overline{INT0}$)	I/O (input)		
P10 ($\overline{SCK1}$)	I/O (I/O)		
P22 (XTOUT)	I/O (I/O)	3-bit input/output port with latch. When used as input port, external interrupt input, STOP mode release signal input, the input mode is configured.	Resonator connection pins (32.768 kHz). For inputting external clock, XTIN is used and XOUT is opened.
P21 (XTIN)	I/O (input)		External interrupt input 5 or STOP mode release signal input
P20 ($\overline{INT5}$, STOP)	I/O (input)		
P33 to P30	I/O	4-bit programmable input/output ports (tri-state). Each bit of this port can be individually configured as an input or an output under software control.	
P47 (AIN07) to P40 (AIN00)	I/O (input)	8-bit programmable input/output ports (tri-state). Each bit of this port can be individually configured as an input or an output under software control. When used as analog input, the input mode is configured.	AD converter analog inputs
P53 (AIN13) to P50 (AIN10)	I/O (input)	4-bit programmable input/output ports (tri-state). Each bit of this port can be individually configured as an input or an output under software control. When used as analog input, the input mode is configured.	AD converter analog inputs

Pin Name	I/O	Function	
P67 (V7) to P60 (V0)	I/O (output)	VFT driver output	Six 8-bit high breakdown voltage output ports with the latch. When used as a VFT driver output, the latch must be cleared to "0".
P77 (V15) to P70 (V8)	I/O (output)		
P87 (V23) to P80 (V16)	I/O (output)		
P97 (V31) to P90 (V24)	I/O (output)		
PD7 (V39) to PD0 (V31)	I/O (output)		
PE7 (V47) to PE0 (V40)	I/O (output)		
PF4 (V52) to PF0 (V48)	I/O (output)		6-bit high breakdown voltage output ports with the latch. When used as a VFT driver output, the latch must be cleared to "0".
XIN, XOUT	Input, output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.	
RESET	I/O	Reset signal input or watchdog timer output/address-trap-reset output/system-clock-reset output.	
TEST	Input	Test pin for out-going test. Be tied to low.	
VDD, VSS (Note)	Power Supply	+ 5 V, 0 V (GND)	
VKK		VFT driver power supply	
VAREF, VASS		Analog reference voltage inputs (High, Low)	

Note: All VDDs should be connected externally for keeping the same voltage level.

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

TLCS-870/X Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). Figure 1-1 shows the memory address maps of the 88CP77/S77/U77. It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers.

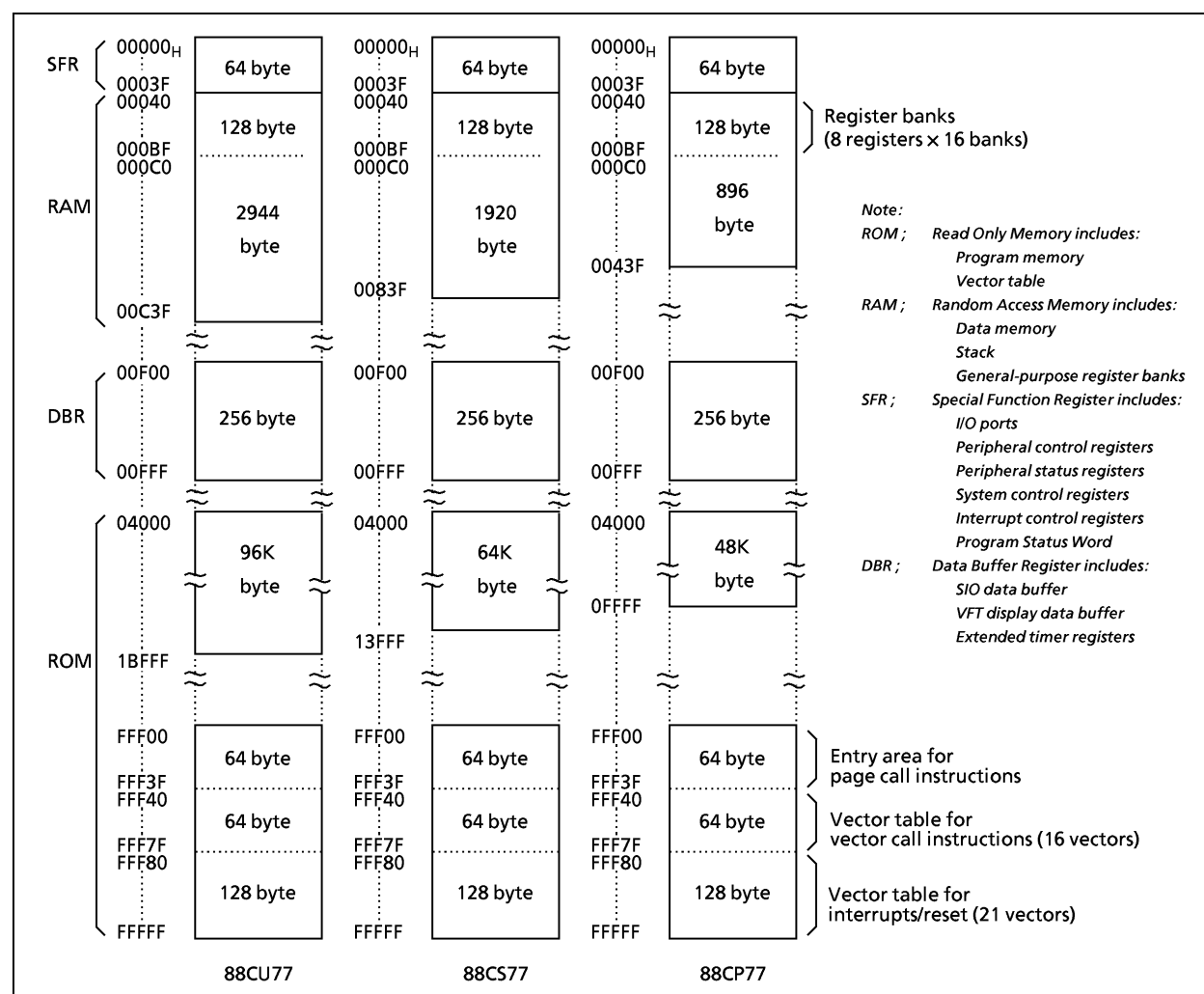


Figure 1-1. Memory Address Maps

Electrical Characteristics

Absolute Maximum Ratings		(V _{SS} = 0 V)		
PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage (* Note4)	V _{DD}		– 0.3 to 6.5	V
Input Voltage	V _{IN1}	P1, P2, P3, P4, P5, XOUT, RESET	– 0.3 to V _{DD} + 0.3	V
	V _{IN2}	P0 port (* Note 3)	– 0.3 to 5.5 V	
Output Voltage	V _{OUT1}	P1, P2, P3, P4, P5, XOUT, RESET	– 0.3 to V _{DD} + 0.3	V
	V _{OUT2}	P0 port (* Note 3)	– 0.3 to 5.5 V	
	V _{OUT3}	Source open drain ports	V _{DD} – 40 to V _{DD} + 0.3	
Output Current (Per 1 pin)	I _{OUT1}	P0, P1, P2, P3, P4, P5 ports	3.2	mA
	I _{OUT2}	P6, P7, P8, 81 Ports	– 25	
	I _{OUT3}	P82 to P87, P9, PD, PE, PF ports	– 12	
Output Current (Total)	Σ I _{OUT1}	P1, P3, P4, P5 ports	– 40	mA
	Σ I _{OUT2}	P0, P1, P2, P3, P4, P5 ports	60	
	Σ I _{OUT3}	P6, P7, P8, P9, PD, PE, PF ports	– 120	
Power Dissipation [Topr = 25°C]	PD Note		1200	mW
Soldering Temperature (time)	T _{sld}		260 (10 s)	°C
Storage Temperature	T _{stg}		– 55 to + 125	°C
Operating Temperature	Topr		– 30 to + 70	°C

Note 1: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Note 2: Power Dissipation (PD) ; For PD, it is necessary to decrease -14.3 mW/°C.

Note 3: The P0 port of TMP88CU77 is different from TMP88PU77/CS77/CP77 and has guard diodes built-in VDD side. Therefore, absolute maximum rating of input voltage is “– 0.3 to VDD + 0.3” volts.

Note 4: All VDDs should be connected externally for keeping the same voltage level.

Recommended Operating Conditions			(V _{SS} = 0 V, Topr = – 30 to 70°C)				
PARAMETER	SYMBOL	PINS	CONDITIONS		Min	Max	UNIT
Supply Voltage	V _{DD}		f _c = 12.5 MHz	NORMAL 1, 2 modes	4.5	5.5	V
				IDLE1, 2 modes			
			f _s = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode	2.0		
Input High Voltage	V _{IH1}	Except hysteresis input	V _{DD} ≥ 4.5 V		V _{DD} × 0.70	V _{DD}	V
	V _{IH2}	Hysteresis input			V _{DD} × 0.75		
	V _{IH3}		V _{DD} < 4.5 V	V _{DD} × 0.90			
Input Low Voltage	V _{IL1}	Except hysteresis input	V _{DD} ≥ 4.5 V		0	V _{DD} × 0.30	V
	V _{IL2}	Hysteresis input				V _{DD} × 0.25	
	V _{IL3}		V _{DD} < 4.5 V	V _{DD} × 0.10			
Clock Frequency	f _c	XIN, XOUT	V _{DD} = 4.5 V to 5.5 V		1.0	12.5	MHz
	f _s	XTIN, XTOUT	V _{DD} = 2.7 V to 5.5 V		30.0	34.0	kHz

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

How to calculate power consumption.

With the TMP88CP77/S77/U77, a pull-down resistor ($R_k = 80 \text{ k}\Omega$ typ.) can be built into a VFT driver using mask option (port by port). The share of VFT driver loss (VFT driver output loss + pull-down resistor (R_k) loss) in power consumption P_{max} is high. When using a fluorescent display tube with a large number of segments, the maximum power consumption P_d must not be exceeded.

power consumption $P_{\text{max}} = \text{operating power consumption} + \text{normal output port loss} + \text{VFT driver loss}$

Where,

operating power consumption: $V_{DD} \times I_{DD}$

normal power consumption: $\sum I_{\text{out}2} \times 0.4$

VFT driver loss: VFT driver output loss + pull-down resistor (R_k) loss

Example:

When $T_a = 10$ to 50°C and a fluorescent display tube with segment output = 3 mA, digit output = 15 mA, $V_{xx} = -25 \text{ V}$ is used.

Operating conditions: $V_{DD} = 5 \text{ V} \pm 10\%$, $f_c = 8 \text{ MHz}$, VFT dimmer time (DIM) = $(14/16) \times t_{\text{seg}}$

Power consumption $P_{\text{max}} = (1) + (2) + (3)$

Where, segments pin = X grid pin = Y, Y = 2

(1) Operating power consumption: $V_{DD} \times I_{DD} = 5.5 \text{ V} \times 22 \text{ mA} = 121 \text{ mW}$

(2) Normal output port loss: $\sum I_{\text{out}2} \times 0.4 \text{ V} = 60 \text{ mA} \times 0.4 \text{ V} = 24 \text{ mW}$

(3) VFT driver loss: segment pin = $3 \text{ mA} \times 2 \text{ V} \times \text{number of segments } X = 6 \text{ mW} \times X$
 digit pin = $15 \text{ mA} \times 2 \text{ V} \times 14/16 (\text{DIM}) \times \text{number of grids } Y$
 = 52.5 mW

$R_k \text{ loss} = (5.5 + 25 \text{ V})^2 / 50 \text{ k}\Omega \times (\text{number of segments } X + \text{number of digits } Y) =$
 $18.605 \text{ mW} \times (X + 2)$

Therefore, $P_{\text{max}} = 121 \text{ mW} + 24 \text{ mW} + 6 \text{ mW} \times X + 52.5 \text{ mW} + 18.605 \text{ mW} \times (X + 2) = 234.71 + 24.605X$

Maximum power consumption P_d when $T_a = 50^\circ\text{C}$ is determined by the following equation:

$P_D = 1200 \text{ mW} - (14.3 \times 25) = 842.5 \text{ mW}$

The number of segments X which can be lit is:

$P_D > P_{\text{max}}$

$842.5 \text{ mW} > 234.71 \text{ mW} + 24.605 X$

$24.7 > X$

Thus, a fluorescent display tube with less than 24 segments can be used. If a fluorescent display tube with 24 segments or more is used, either a pull-down resistor must be attached externally, or the number of segments to be lit must be kept to less than 24 by software.

D.C. Characteristics

(V_{SS} = 0 V, T_{opr} = – 30 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min	Typ.	Max	UNIT
Hysteresis Voltage	V _{HS}	Hysteresis input		–	0.9	–	V
Input Current	I _{IN1}	TEST	V _{DD} = 5.5 V V _{IN} = 5.5 V / 0 V	–	–	± 2	μA
	I _{IN2}	Open drain ports, Tri-state ports					
	I _{IN3}	RESET, STOP					
	I _{IN4}	PD, PE, PF ports (Note3)		–	–	80	
Input Resistance	R _{IN2}	RESET		100	220	450	kΩ
Pull-down Resistance	R _K	Source open drain ports	V _{DD} = 5.5 V, V _{KK} = – 30 V	50	80	110	
Output Leakage Current	I _{LO1}	Sink open drain ports	V _{DD} = 5.5 V, V _{OUT} = 5.5 V	–	–	2	μA
	I _{LO2}	Source open drain ports	V _{DD} = 5.5 V, V _{OUT} = – 32 V	–	–	– 2	
	I _{LO3}	Tri-state ports	V _{DD} = 5.5 V, V _{OUT} = 5.5 V / 0 V	–	–	2	
Output High Voltage	V _{OH2}	Tri-state ports	V _{DD} = 4.5 V, I _{OH} = – 0.7 mA	4.1	–	–	V
	V _{OH3}	P82 to P87, P9, PD, PE, PF ports	V _{DD} = 4.5 V, I _{OH} = – 8 mA	2.4	–	–	
Output Low Voltage	V _{OL}	Except XOUT	V _{DD} = 4.5 V, I _{OL} = 1.6 mA	–	–	0.4	V
Output High current	I _{OH1}	P6, P7, P80, P81 ports	V _{DD} = 4.5 V, V _{OH} = 2.4 V	–	– 30	–	mA
	I _{OH2}	P82 to P87, P9, PD, PE, PF ports		–	– 15	–	
Supply Current in NORMAL 1, 2 modes	I _{DD}		V _{DD} = 5.5 V V _{IN} = 5.3 V / 0.2 V f _c = 12.5 MHz f _s = 32.768 kHz	–	15	22	mA
Supply Current in IDLE 1, 2 modes				–	6	12	
Supply Current in SLOW mode			V _{DD} = 3.0 V V _{IN} = 2.8 V / 0.2 V f _s = 32.768 kHz	–	30	60	μA
Supply Current in SLEEP mode				–	15	30	
Supply Current in STOP mode				V _{DD} = 5.5 V V _{IN} = 5.3 V / 0.2 V	–	0.5	

Note 1: Typical values show those at T_{opr} = 25°C, V_{DD} = 5 V.

Note 2: Input Current I_{IN1}, I_{IN3}; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3: Input Current I_{IN4}; The current when the pull-down register (R_K) is not connected by the mask option.

AD Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, T_{opr} = – 30 to 70°C)

PARAMETER	SYMBOL	CONDITIONS	Min	Typ.	Max	UNIT
Analog Reference Voltage	V _{AREF}		4.5	–	V _{DD}	V
	V _{ASS}					
Analog Input Voltage	V _{AIN}		V _{ASS}	–	V _{AREF}	V
Analog Supply Current	I _{REF}	V _{AREF} = 5.5 V, V _{ASS} = 0.0 V	–	0.5	1.0	mA
Nonlinearity Error		V _{DD} = 5.0 V, V _{SS} = 0.0 V	–	–	± 1	LSB
Zero Point Error		V _{AREF} = 5.000 V	–	–	± 1	
Full Scale Error		V _{ASS} = 0.000 V	–	–	± 1	
Total Error			–	–	± 2	

Note: Total errors includes all errors, except quantization error.

A.C. Characteristics

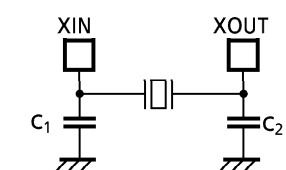
(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

PARAMETER	SYMBOL	CONDITIONS	Min	Typ.	Max	UNIT
Machine Cycle Time	tcy	In NORMAL1, 2 modes	0.32	–	10	μs
		In IDLE 1, 2 modes				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t _{WCH}	For external clock operation (XIN input), fc = 12.5 MHz	32	–	–	ns
Low Level Clock Pulse Width	t _{WCL}					
High Level Clock Pulse Width	t _{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	15.2	–	–	μs
Low Level Clock Pulse Width	t _{WSL}					

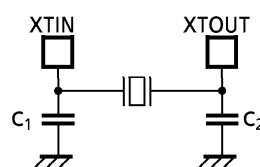
Recommended Oscillating Conditions

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

PARAMETER	Oscillator	Oscillation Frequency	Recommended Oscillator	Recommended Constant	
				C ₁	C ₂
High-frequency Oscillation	Ceramic Resonator	12.5 MHz	Murata CSA12.5MTZ	30 pF	30 pF
		8 MHz	Murata CSA8.00MTZ	30 pF	30 pF
	Crystal Oscillator	12.5 MHz	NDK AT-51	10 pF	10 pF
Low-frequency Oscillation	Crystal Oscillator	32.768 kHz	NDK MX-38T	15 pF	15 pF



(1) High-frequency Oscillation



(2) Low-frequency Oscillation

Note: An electrical shield by metal shield plate on the surface of IC package should be recommendable in order to prevent the device from the high electric fieldstress applied from CRT (Cathode Ray Tube) for continuous reliable operation.

Typical Characteristics

(Ta = 25°C)

