



100MHZ 3-DIMM CLOCK FOR VIA MVP4

1.0 GENERAL DESCRIPTION

The W83194R-67A is a Clock Synthesizer which provides all clocks required for high-speed RISC or CISC microprocessor such as Intel Pentium , AMD and Cyrix. W83194R-67A provides sixteen CPU/PCI frequencies which are externally selectable with smooth transitions. W83194R-67AA also provides 13 SDRAM clocks controlled by the none-delay buffer_in pin.

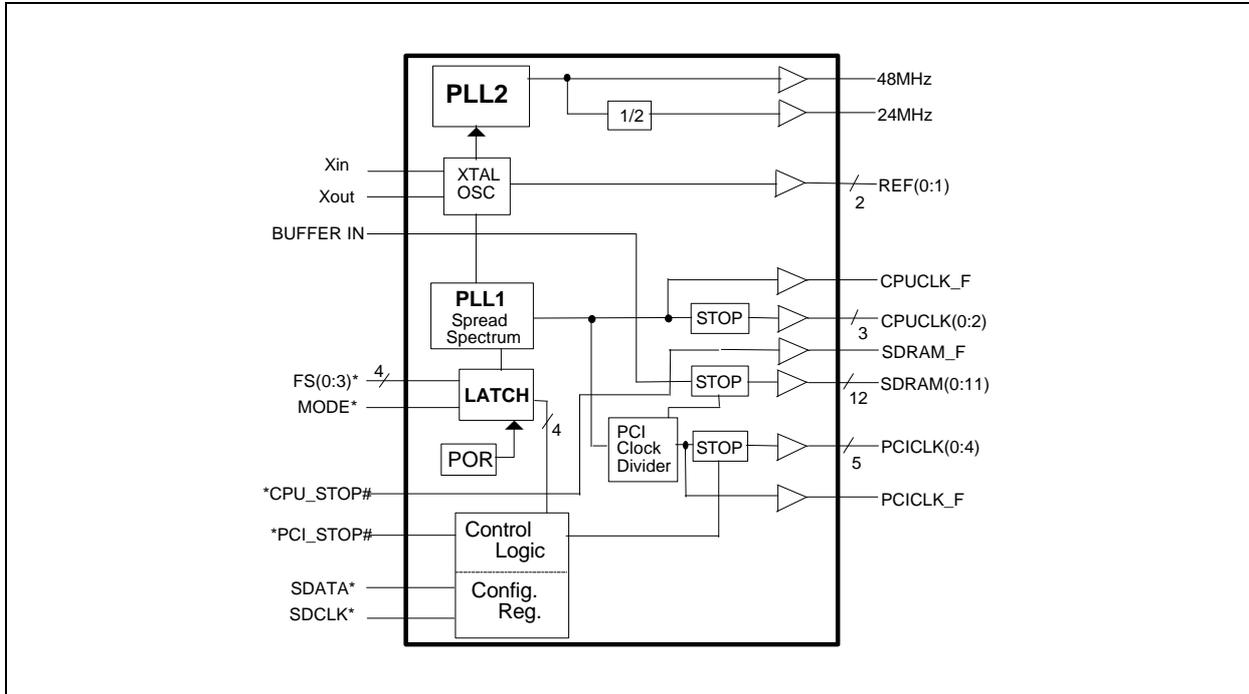
The W83194R-67A accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. Spread spectrum built in at $\pm 0.5\%$ or $\pm 0.25\%$ to reduce EMI. Programmable stopping individual clock outputs and frequency selection through I²C interface. The device meets the Pentium power-up stabilization, which requires CPU and PCI clocks be stable within 2 ms after power-up.

High drive six PCI and thirteen SDRAM CLOCK outputs typically provide greater than 1 V/ns slew rate into 30 pF loads. Two CPU CLOCK outputs typically provide better than 1 V/ns slew rate into 20 pF loads as maintaining 50% duty cycle. The fixed frequency outputs as REF, 24MHz, and 48 MHz provide better than 0.5V/ns slew rate.

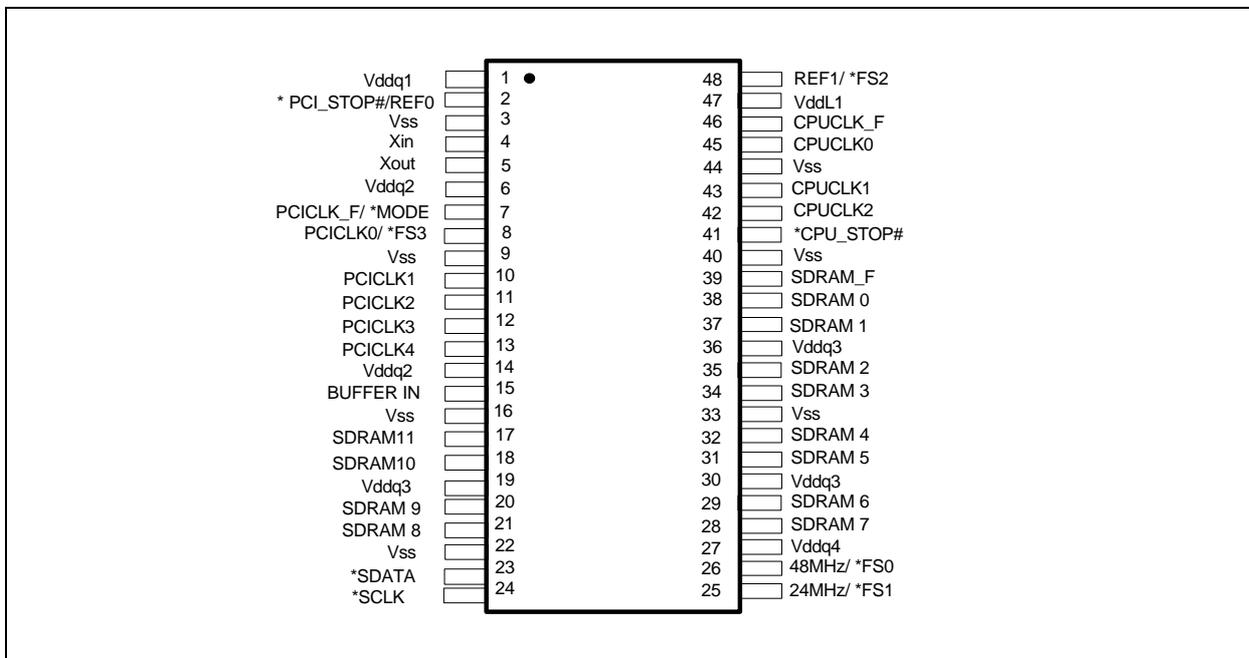
2.0 PRODUCT FEATURES

- Supports Pentium™ , AMD, Cyrix CPU with I²C.
- 4 CPU clocks (one free-running CPU clock)
- 13 SDRAM clocks for 3 DIMs
- 6 PCI synchronous clocks
- Optional single or mixed supply:
(Vddq1=Vddq2 = Vddq3 = Vddq4 = VddL1 =VddL2= 3.3V) or (Vddq1= Vddq2 = Vddq3=Vddq4 = 3.3V, VddL1 = VddL2 = 2.5V)
- < 250ps skew among CPU and SDRAM clocks
- < 4ns propagation delay SDRAM from buffer input
- Skew from CPU(earlier) to PCI clock -1 to 4ns, center 2.6ns.
- Smooth frequency switch with selections from 60 MHz to 124 MHz CPU
- I²C 2-Wire serial interface and I²C read back
- $\pm 0.25\%$ or $\pm 0.5\%$ spread spectrum function to reduce EMI
- Programmable registers to enable/stop each output and select modes (mode as Tri-state or Normal)
- 2ms power up clock stable time
- MODE pin for power Management
- One 48 MHz for USB & one 24 MHz for super I/O
- 48-pin SSOP package

3.0 BLOCK DIAGRAM



4.0 PIN CONFIGURATION





PRELIMINARY

5.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

- Active Low

* - Internal 250kΩ pull-up

5.1 Crystal I/O

| SYMBOL | PIN | I/O | FUNCTION |
|--------|-----|-----|--|
| Xin | 4 | IN | Crystal input with internal loading capacitors and feedback resistors. |
| Xout | 5 | OUT | Crystal output at 14.318MHz nominally. |

5.2 CPU, SDRAM, PCI, IOAPIC Clock Outputs

| SYMBOL | PIN | I/O | FUNCTION |
|--------------------|-------------------------------------|-----|--|
| CPUCLK_F | 46 | OUT | Free running CPU clock. Not affected by CPU_STOP# |
| CPUCLK[0:2] | 45,43,42 | OUT | Low skew (< 250ps) clock outputs for host frequencies such as CPU, Chipset and Cache. Powered by VddL2. Low if CPU_STOP# is low. |
| *CPU_STOP# | 41 | IN | This asynchronous input halts CPUCLK[0:2] and SDRAM(0:11) at logic level when driven low. |
| SDRAM_F | 39 | OUT | Free running SDRAM clock. Not affected by CPU_STOP# |
| SDRAM [0:11] | 17,18,20,21,28,29,31,32,34,35,37,38 | OUT | SDRAM clock outputs. Fanout buffer outputs from BUFFER IN pin.(Controlled by chipset) |
| PCICLK_F/ *MODE | 7 | I/O | Free running PCI clock during normal operation. Latched Input. Mode=1, Pin 2 is REF0; Mode=0, Pin2 is PCI_STOP# |
| PCICLK0/*FS3 | 8 | I/O | Low skew (< 250ps) PCI clock outputs. Latched input for FS3 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. |
| PCICLK [1:4] | 10,11,12,13 | OUT | Low skew (< 250ps) PCI clock outputs. Synchronous to CPU clocks with 1/-4ns skew(CPU early). |
| BUFFER IN | 15 | IN | Inputs to fanout for SDRAM outputs. |



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5.3 I²C Control Interface

| SYMBOL | PIN | I/O | FUNCTION |
|--------|-----|-----|---|
| *SDATA | 23 | I/O | Serial data of I ² C 2-wire control interface with internal pull-up resistor. |
| *SDCLK | 24 | IN | Serial clock of I ² C 2-wire control interface with internal pull-up resistor. |

5.4 Fixed Frequency Outputs

| SYMBOL | PIN | I/O | FUNCTION |
|-------------------|-----|-----|---|
| REF0 / *PCI_STOP# | 2 | I/O | 14.318MHz reference clock. This REF output is the stronger buffer for ISA bus loads. Halt PCICLK(0:4) clocks at logic 0 level, when input low (In mobile mode. MODE=0) |
| REF1 / *FS2 | 48 | I/O | 14.318MHz reference clock. Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. |
| 24MHz / *FS1 | 25 | I/O | 24MHz output clock. Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. |
| 48MHz / *FS0 | 26 | I/O | 48MHz output for USB during normal operation. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. |

5.5 Power Pins

| SYMBOL | PIN | FUNCTION |
|--------|--------------------|---|
| Vddq1 | 1 | Power supply for Ref [0:1] , Xin and Xout crystal. |
| VddL1 | 47 | Power supply for CPU clock outputs, either 2.5V or 3.3V. |
| Vddq2 | 6, 14 | Power supply for PCICLK_F, PCICLK[1:4], 3.3V. |
| Vddq3 | 19, 30, 36 | Power supply for SDRAM_F,SDRAM[0:11], and PLL core, nominal 3.3V. |
| Vddq4 | 27 | Power for 24 & 48MHz output buffers and PLL core. |
| Vss | 3,9,16,22,33,40,44 | Circuit Ground. |



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6.0 FREQUENCY SELECTION

| FS3 | FS2 | FS1 | FS0 | CPU,SDRAM(MHz) | PCI(MHz) | REF,IOAPIC (MHz) |
|-----|-----|-----|-----|----------------|--------------|------------------|
| 1 | 1 | 1 | 1 | 60 | 30(CPU/2) | 14.318 |
| 1 | 1 | 1 | 0 | 66.8 | 33.4(CPU/2) | 14.318 |
| 1 | 1 | 0 | 1 | 70 | 35(CPU/2) | 14.318 |
| 1 | 1 | 0 | 0 | 90 | 30(CPU/3) | 14.318 |
| 1 | 0 | 1 | 1 | 80 | 26.67(CPU/3) | 14.318 |
| 1 | 0 | 1 | 0 | 83.3 | 27.77(CPU/3) | 14.318 |
| 1 | 0 | 0 | 1 | 95.25 | 31.75(CPU/3) | 14.318 |
| 1 | 0 | 0 | 0 | 100.2 | 33.3(CPU/3) | 14.318 |
| 0 | 1 | 1 | 1 | 75 | 37.5(CPU/2) | 14.318 |
| 0 | 1 | 1 | 0 | 80 | 40(CPU/2) | 14.318 |
| 0 | 1 | 0 | 1 | 83.3 | 41.65(CPU/2) | 14.318 |
| 0 | 1 | 0 | 0 | 105 | 35(CPU/3) | 14.318 |
| 0 | 0 | 1 | 1 | 110 | 36.67(CPU/3) | 14.318 |
| 0 | 0 | 1 | 0 | 115 | 38.33(CPU/3) | 14.318 |
| 0 | 0 | 0 | 1 | 120 | 40(CPU/3) | 14.318 |
| 0 | 0 | 0 | 0 | 124 | 41.33(CPU/3) | 14.318 |

7.0 MODE PIN -POWER MANAGEMENT INPUT CONTROL

| MODE, Pin7 (Latched Input) | PIN 2 |
|----------------------------|-------------------|
| 0 | PCI_STOP# (Input) |
| 1 | REF0 (Output) |



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8.0 FUNTION DESCRIPTION

8.1 POWER MANAGEMENT FUNCTIONS

All clocks can be individually enabled or disabled via the 2-wire control interface. On power up, external circuitry should allow 3 ms for the VCO's to stabilize prior to enabling clock outputs to assure correct pulse widths. When MODE=0, pins 15 and 46 are inputs (PCI_STOP#), (CPU_STOP#), when MODE=1, these functions are not available. A particular clock could be enabled as both the 2-wire serial control interface and one of these pins indicate that it should be enable.

The W83194R-67A may be disabled in the low state according to the following table in order to reduce power consumption. All clocks are stopped in the low state, but maintain a valid high period on transitions from running to stop. The CPU and PCI clocks transform between running and stop by waiting for one positive edge on PCICLK_F followed by negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

| CPU_STOP# | PCI_STOP# | CPUCLK 0:2, SDRAM 0:11 | PCI | SDRAM_F, CPU_F,PCI_F | OTHER CLKs |
|-----------|-----------|---------------------------|---------|-------------------------|------------|
| 0 | 0 | LOW | LOW | RUNNING | RUNNING |
| 0 | 1 | LOW | RUNNING | RUNNING | RUNNING |
| 1 | 0 | RUNNING | LOW | RUNNING | RUNNING |
| 1 | 1 | RUNNING | RUNNING | RUNNING | RUNNING |

8.2 2-WIRE I²C CONTROL INTERFACE

The clock generator is a slave I²C component which can be read back the data stored in the latches for verification. All proceeding bytes must be sent to change one of the control bytes. The 2-wire control interface allows each clock output individually enabled or disabled. On power up, the W83194R-67A initializes with default register settings, and then it is optional to use the 2-wire control interface.

The SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high during normal data transfer. There are only two exceptions. One is a high-to-low transition on SDATA while SDCLK is high used to indicate the beginning of a data transfer cycle. The other is a low-to-high transition on SDATA while SDCLK is high used to indicate the end of a data transfer cycle. Data is always sent as complete 8-bit bytes followed by an acknowledge generated.

Byte writing starts with a start condition followed by 7-bit slave address and a write command bit [1101 0010], command code checking [0000 0000], and byte count checking. After successful reception of each byte, an acknowledge (low) on the SDATA wire will be generated by the clock chip. Controller can start to write to internal I²C registers after the string of data. The sequence order is as follows:

Publication Release Date: Feb. 1999

Revision 0.30



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Bytes sequence order for I²C controller :

| | | | | | | |
|----------------------------|-----|---------------------------|-----|-------------------------|-----|-------------------------|
| Clock Address A(6:0) & R/W | Ack | 8 bits dummy Command code | Ack | 8 bits dummy Byte count | Ack | Byte0,1,2... until Stop |
|----------------------------|-----|---------------------------|-----|-------------------------|-----|-------------------------|

Set R/W to 1 when read back the data sequence is as follows :

| | | | | | | |
|----------------------------|-----|--------|-----|--------|-----|---------------------------|
| Clock Address A(6:0) & R/W | Ack | Byte 0 | Ack | Byte 1 | Ack | Byte2, 3, 4... until Stop |
|----------------------------|-----|--------|-----|--------|-----|---------------------------|

8.3 SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the default state at true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2,) will be valid and acknowledged.

8.3.1 Register 0: CPU Frequency Select Register (default = 0)

| Bit | @PowerUp | Pin | Description |
|-----|----------|-----|---|
| 7 | 0 | - | 0 = ¡0.25% Center type Spread Spectrum Modulation 1 = ¡0.5% Center type Spread Spectrum Modulation |
| 6 | 0 | - | SSEL2 (for frequency table selection by software via I ² C) |
| 5 | 0 | - | SSEL1 (for frequency table selection by software via I ² C) |
| 4 | 0 | - | SSEL0 (for frequency table selection by software via I ² C) |
| 3 | 0 | - | 0 = Selection by hardware 1 = Selection by software I ² C - Bit 2, 6:4 |
| 2 | 0 | - | SSEL3 (for frequency table selection by software via I ² C) |
| 1 | 0 | - | 0 = Normal 1 = Spread Spectrum enabled |
| 0 | 0 | - | 0 = Running 1 = Tristate all outputs |



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Frequency table by I2C

| SSEL3 | SSEL2 | SSEL1 | SSEL0 | CPU,SDRAM(MHz) | PCI(MHz) | REF,IOAPIC (MHz) |
|-------|-------|-------|-------|----------------|--------------|------------------|
| 1 | 1 | 1 | 1 | 60 | 30(CPU/2) | 14.318 |
| 1 | 1 | 1 | 0 | 66.8 | 33.4(CPU/2) | 14.318 |
| 1 | 1 | 0 | 1 | 70 | 35(CPU/2) | 14.318 |
| 1 | 1 | 0 | 0 | 90 | 30(CPU/3) | 14.318 |
| 1 | 0 | 1 | 1 | 80 | 26.67(CPU/3) | 14.318 |
| 1 | 0 | 1 | 0 | 83.3 | 27.77(CPU/3) | 14.318 |
| 1 | 0 | 0 | 1 | 95.25 | 31.75(CPU/3) | 14.318 |
| 1 | 0 | 0 | 0 | 100.2 | 33.3(CPU/3) | 14.318 |
| 0 | 1 | 1 | 1 | 75 | 37.5(CPU/2) | 14.318 |
| 0 | 1 | 1 | 0 | 80 | 40(CPU/2) | 14.318 |
| 0 | 1 | 0 | 1 | 83.3 | 41.65(CPU/2) | 14.318 |
| 0 | 1 | 0 | 0 | 105 | 35(CPU/3) | 14.318 |
| 0 | 0 | 1 | 1 | 110 | 36.67(CPU/3) | 14.318 |
| 0 | 0 | 1 | 0 | 115 | 38.33(CPU/3) | 14.318 |
| 0 | 0 | 0 | 1 | 120 | 40(CPU/3) | 14.318 |
| 0 | 0 | 0 | 0 | 124 | 41.33(CPU/3) | 14.318 |

8.3.2 Register 1 : CPU Clock Register (1 = Active, 0 = Inactive)

| Bit | @PowerUp | Pin | Description |
|-----|----------|-----|------------------------------|
| 7 | x | - | Latched FS2# |
| 6 | 1 | - | Reserved |
| 5 | 1 | - | Reserved |
| 4 | 1 | - | Reserved |
| 3 | 1 | 42 | CPUCLK2 (Active / Inactive) |
| 2 | 1 | 43 | CPUCLK1 (Active / Inactive) |
| 1 | 1 | 45 | CPUCLK0 (Active / Inactive) |
| 0 | 1 | 46 | CPUCLK_F (Active / Inactive) |

8.3.3 Register 2: PCI Clock Register (1 = Active, 0 = Inactive)

| Bit | @PowerUp | Pin | Description |
|-----|----------|-----|------------------------------|
| 7 | 1 | - | Reserved |
| 6 | 1 | 7 | PCICLK_F (Active / Inactive) |
| 5 | 1 | - | Reserved |
| 4 | 1 | 13 | PCICLK4 (Active / Inactive) |
| 3 | 1 | 12 | PCICLK3 (Active / Inactive) |
| 2 | 1 | 11 | PCICLK2 (Active / Inactive) |
| 1 | 1 | 10 | PCICLK1 (Active / Inactive) |
| 0 | 1 | 8 | PCICLK0 (Active / Inactive) |

8.3.4 Register 3: SDRAM Clock Register (1 = Active, 0 = Inactive)

| Bit | @PowerUp | Pin | Description |
|-----|----------|-------------|---------------------------------|
| 7 | 1 | - | Reserved |
| 6 | x | - | Latched FS0# |
| 5 | 1 | 26 | 48MHz (Active / Inactive) |
| 4 | 1 | 25 | 24MHz (Active / Inactive) |
| 3 | 1 | 39 | SDRAM_F(Active / Inactive) |
| 2 | 1 | 21,20,18,17 | SDRAM(8:11) (Active / Inactive) |
| 1 | 1 | 32,31,29,28 | SDRAM(4:7) (Active / Inactive) |
| 0 | 1 | 38,37,35,34 | SDRAM(0:3) (Active / Inactive) |

8.3.5 Register 4: Reserved Register (1 = Active, 0 = Inactive)

| Bit | @PowerUp | Pin | Description |
|-----|----------|-----|--------------|
| 7 | 1 | - | Reserved |
| 6 | 1 | - | Reserved |
| 5 | 1 | - | Reserved |
| 4 | 1 | - | Reserved |
| 3 | x | - | Latched FS1# |
| 2 | 1 | - | Reserved |
| 1 | x | - | Latched FS3# |
| 0 | 1 | - | Reserved |

8.3.6 Register 5: Peripheral Control (1 = Active, 0 = Inactive)

| Bit | @PowerUp | Pin | Description |
|-----|----------|-----|--------------------------|
| 7 | 1 | - | Reserved |
| 6 | 1 | - | Reserved |
| 5 | 1 | - | Reserved |
| 4 | 1 | - | Reserved |
| 3 | 1 | - | Reserved |
| 2 | 1 | - | Reserved |
| 1 | 1 | 48 | REF1 (Active / Inactive) |
| 0 | 1 | 2 | REF0 (Active / Inactive) |

8.3.7 Register 6: Winbond Chip ID Register (Read Only)

| Bit | @PowerUp | Pin | Description |
|-----|----------|-----|-----------------|
| 7 | 0 | - | Winbond Chip ID |
| 6 | 1 | - | Winbond Chip ID |
| 5 | 0 | - | Winbond Chip ID |
| 4 | 1 | - | Winbond Chip ID |
| 3 | 0 | - | Winbond Chip ID |
| 2 | 0 | - | Winbond Chip ID |
| 1 | 1 | - | Winbond Chip ID |
| 0 | 0 | - | Winbond Chip ID |

NOTE:

1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects(FS#) will be inverted logic load of the input frequency select pin conditions.



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9.0 SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or Vdd).

| Symbol | Parameter | Rating |
|-----------------------------------|--|--------------------|
| V _{dd} , V _{IN} | Voltage on any pin with respect to GND | - 0.5 V to + 7.0 V |
| T _{STG} | Storage Temperature | - 65°C to + 150°C |
| T _B | Ambient Temperature | - 55°C to + 125°C |
| T _A | Operating Temperature | 0°C to + 70°C |

9.2 AC CHARACTERISTICS

| V _{ddq1} =V _{ddq2} = V _{ddq3} = V _{ddq4} =3.3V , V _{ddL1} =V _{ddL2} = 2.5V , T _A = 0° C to +70° C | | | | | | |
|--|--------------------------------------|-----|-----|--------|-------|--|
| Parameter | Symbol | Min | Typ | Max | Units | Test Conditions |
| Output Duty Cycle | | 45 | 50 | 55 | % | Measured at 1.5V |
| CPU/SDRAM to PCI Offset | t _{OFF} | 1 | | 4 | ns | 15 pF Load Measured at 1.5V |
| Skew (CPU-CPU), (PCI-PCI), (SDRAM-SDRAM) | t _{SKEW} | | | 250 | ps | 15 pF Load Measured at 1.5V |
| CPU/SDRAM Cycle to Cycle Jitter | t _{CCJ} | | | ±0.250 | ps | |
| CPU/SDRAM Absolute Jitter | t _{JA} | | | 500 | ps | |
| Jitter Spectrum 20 dB Bandwidth from Center | BW _J | | | 500 | KHz | |
| Output Rise (0.4V ~ 2.0V) & Fall (2.0V ~0.4V) Time | t _{TLH} t _{THL} | 0.4 | | 1.6 | ns | 15 pF Load on CPU and PCI outputs |
| Overshoot/Undershoot Beyond Power Rails | V _{over} | | | 1.5 | V | 22 Ω at source of 8 inch PCB run to 15 pF load |
| Ring Back Exclusion | V _{RBE} | | | 2.1 | V | Ring Back must not enter this range. |

9.3 DC CHARACTERISTICS

| Vddq1=Vddq2 = Vddq3 = Vddq4 =3.3V, VddL1 =VddL2= 2.5V , $T_A = 0^\circ C$ to $+70^\circ C$ | | | | | | |
|--|-------------|-----|-----|-----|----------|--|
| Parameter | Symbol | Min | Typ | Max | Units | Test Conditions |
| Input Low Voltage | V_{IL} | | | 0.8 | V_{dc} | |
| Input High Voltage | V_{IH} | 2.0 | | | V_{dc} | |
| Input Low Current | I_{IL} | | | -66 | μA | |
| Input High Current | I_{IH} | | | 5 | μA | |
| Output Low Voltage $I_{OL} = 4$ mA | V_{OL} | | | 0.4 | V_{dc} | All outputs |
| Output High Voltage $I_{OH} = 4$ mA | V_{OH} | 2.4 | | | V_{dc} | All outputs using 3.3V power |
| Tri-State leakage Current | I_{OZ} | | | 10 | μA | |
| Dynamic Supply Current for Vdd + Vddq3 | I_{dd3} | | | | mA | CPU = 66.6 MHz PCI = 33.3 Mhz with load |
| Dynamic Supply Current for Vddq2 + Vddq2b | I_{dd2} | | | | mA | Same as above |
| CPU Stop Current for Vdd + Vddq3 | I_{CPUS3} | | | | mA | Same as above |
| CPU Stop Current for Vddq2 + Vddq2b | I_{CPUS2} | | | | mA | Same as above |
| PCI Stop Current for Vdd + Vddq3 | I_{PD3} | | | | mA | |

9.4 BUFFER CHARACTERISTICS

9.4.1 TYPE 1 BUFFER FOR CPU CLOCK

| Parameter | Symbol | Min | Typ | Max | Units | Test Conditions |
|---|---------------|-----|-----|-----|-------|-----------------|
| Pull-Up Current Min | $I_{OH(min)}$ | -27 | | | mA | Vout = 1.0 V |
| Pull-Up Current Max | $I_{OH(max)}$ | | | -27 | mA | Vout = 2.0V |
| Pull-Down Current Min | $I_{OL(min)}$ | | | | mA | Vout = 1.2 V |
| Pull-Down Current Max | $I_{OL(max)}$ | | | 27 | mA | Vout = 0.3 V |
| Rise/Fall Time Min Between 0.4 V and 2.0 V | $T_{RF(min)}$ | 0.4 | | | ns | 10pF Load |
| Rise/Fall Time Max Between 0.4 V and 2.0 V | $T_{RF(max)}$ | | | 1.6 | ns | 20pF Load |

9.4.2 TYPE 3 BUFFER FOR REF[0:1], 24MHZ, 48MHZ

| Parameter | Symbol | Min | Typ | Max | Units | Test Conditions |
|---|---------------|-----|-----|-----|-------|-----------------|
| Pull-Up Current Min | $I_{OH(min)}$ | -29 | | | mA | Vout = 1.0 V |
| Pull-Up Current Max | $I_{OH(max)}$ | | | -23 | mA | Vout = 3.135V |
| Pull-Down Current Min | $I_{OL(min)}$ | 29 | | | mA | Vout = 1.95 V |
| Pull-Down Current Max | $I_{OL(max)}$ | | | | mA | Vout = 0.4 V |
| Rise/Fall Time Min Between 0.8 V and 2.0 V | $T_{RF(min)}$ | 1.0 | | | ns | 10pF Load |
| Rise/Fall Time Max Between 0.8 V and 2.0 V | $T_{RF(max)}$ | | | 4.0 | ns | 20pF Load |

9.4.3 TYPE 4 BUFFER FOR SDRAM (F,0:11)

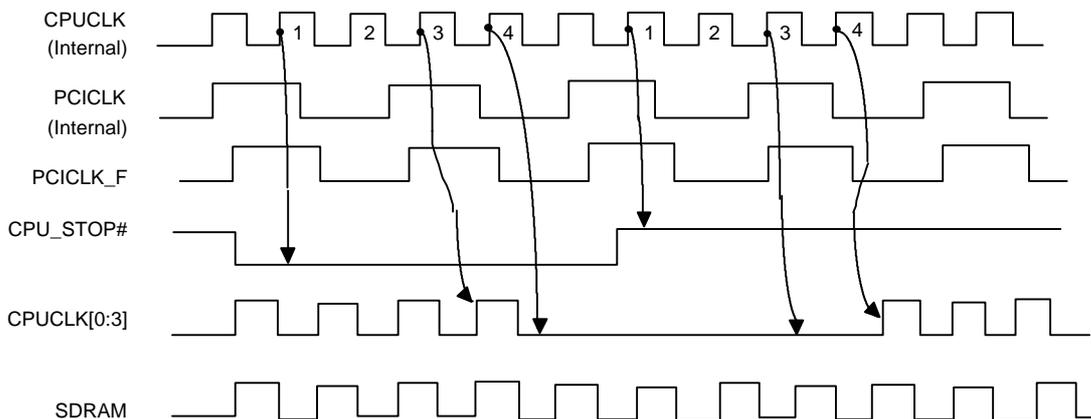
| Parameter | Symbol | Min | Typ | Max | Units | Test Conditions |
|---|---------------|-----|-----|-----|-------|-----------------|
| Pull-Up Current Min | $I_{OH(min)}$ | | | | mA | Vout = 1.65 V |
| Pull-Up Current Max | $I_{OH(max)}$ | | | -46 | mA | Vout = 3.135 V |
| Pull-Down Current Min | $I_{OL(min)}$ | | | | mA | Vout = 1.65 V |
| Pull-Down Current Max | $I_{OL(max)}$ | | | 53 | mA | Vout = 0.4 V |
| Rise/Fall Time Min Between 0.8 V and 2.0 V | $T_{RF(min)}$ | 0.5 | | | ns | 20pF Load |
| Rise/Fall Time Max Between 0.8 V and 2.0 V | $T_{RF(max)}$ | | | 1.3 | ns | 30pF Load |

9.4.4 TYPE 5 BUFFER FOR PCICLK(0:4,F)

| Parameter | Symbol | Min | Typ | Max | Units | Test Conditions |
|---|---------------|-----|-----|-----|-------|----------------------------|
| Pull-Up Current Min | $I_{OH(min)}$ | -33 | | | mA | $V_{out} = 1.0\text{ V}$ |
| Pull-Up Current Max | $I_{OH(max)}$ | | | -33 | mA | $V_{out} = 3.135\text{ V}$ |
| Pull-Down Current Min | $I_{OL(min)}$ | 30 | | | mA | $V_{out} = 1.95\text{ V}$ |
| Pull-Down Current Max | $I_{OL(max)}$ | | | 38 | mA | $V_{out} = 0.4\text{ V}$ |
| Rise/Fall Time Min Between 0.8 V and 2.0 V | $T_{RF(min)}$ | 0.5 | | | ns | 15pF Load |
| Rise/Fall Time Max Between 0.8 V and 2.0 V | $T_{RF(max)}$ | | | 2.0 | ns | 30pF Load |

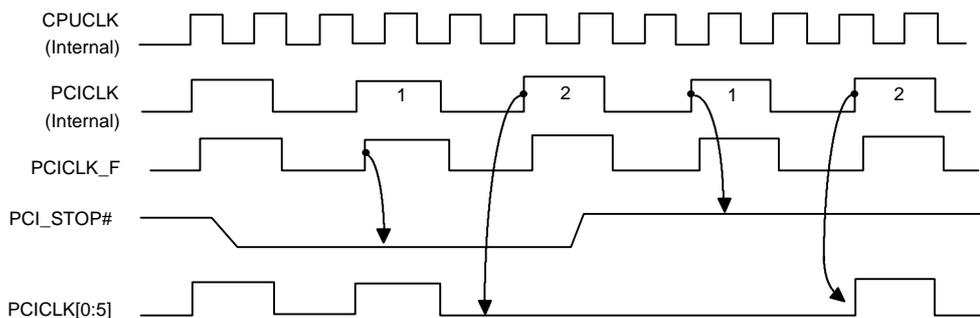
10.0 POWER MANAGEMENT TIMING

10.1 CPU_STOP# Timing Diagram



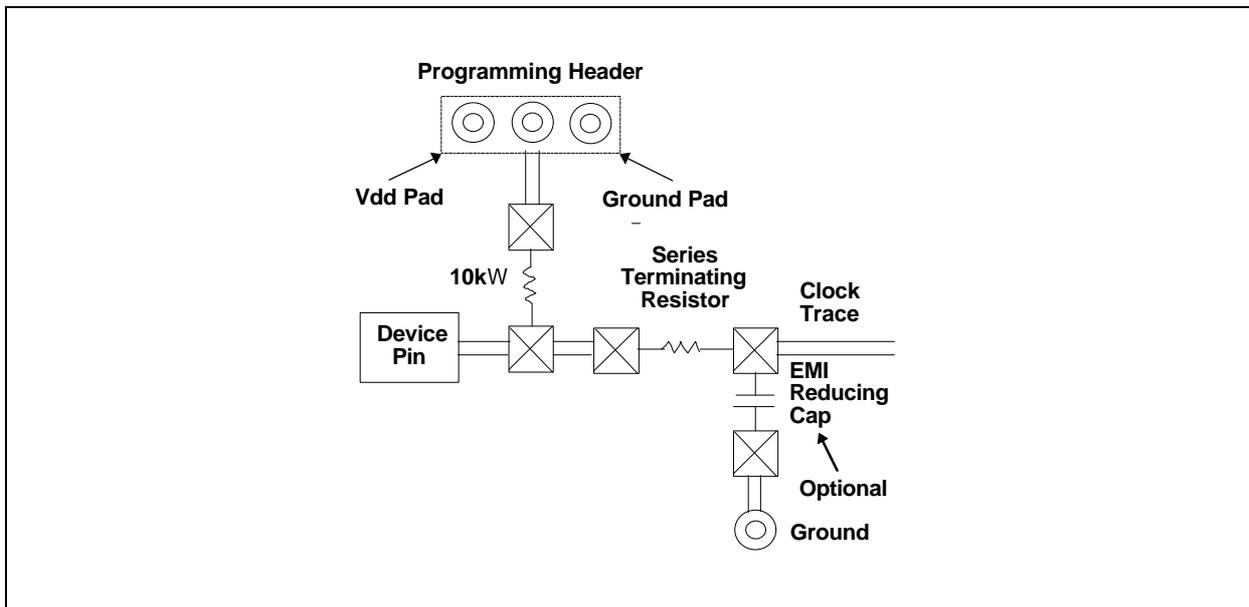
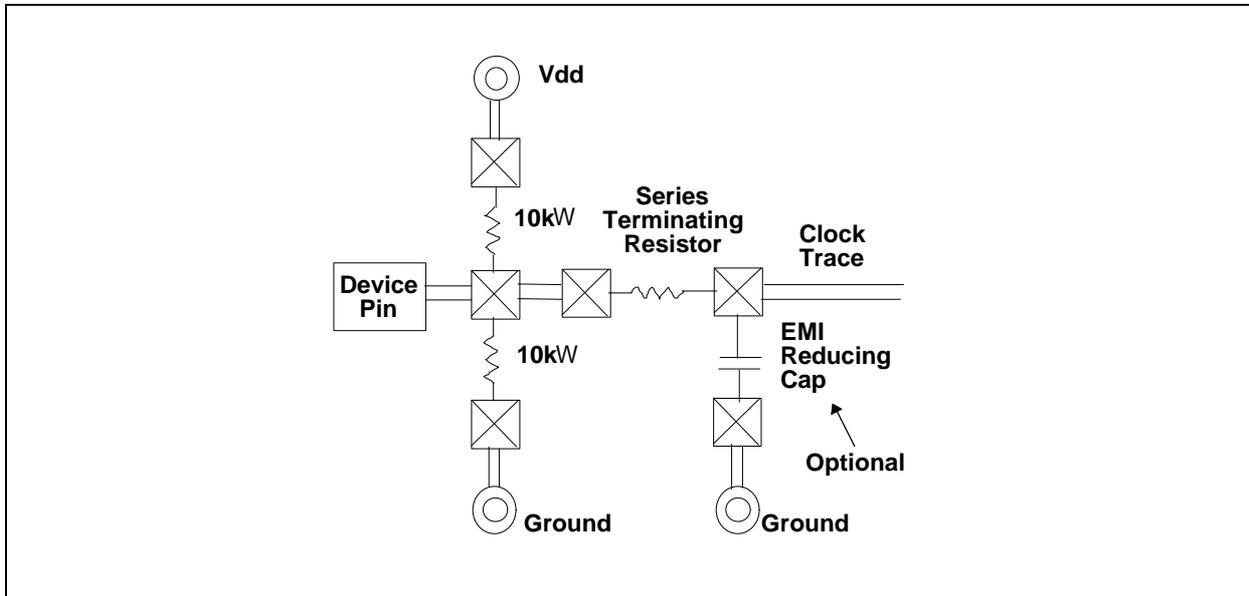
For synchronous Chipset, CPU_STOP# pin is an asynchronous “active low” input pin used to stop the CPU clocks for low power operation. This pin is asserted synchronously by the external control logic at the rising edge of free running PCI clock(PCICLK_F). All other clocks will continue to run while the CPU clocks are stopped. The CPU clocks will always be stopped in a low state and resume output with full pulse width. In this case, CPU “clocks on latency” is less than 4 CPU clocks and “clocks off latency” is less than 4 CPU clocks.

10.2 PCI_STOP# Timing Diagram



For synchronous Chipset, PCI_STOP# pin is an asynchronous “active low” input pin used to stop the PCICLK [0:4] for low power operation. This pin is asserted synchronously by the external control logic at the rising edge of free running PCI clock(PCICLK_F). All other clocks will continue to run while the PCI clocks are stopped. The PCI clocks will always be stopped in a low state and resume output with full pulse width. In this case, PCI “clocks on latency” is less than 2 PCI clocks and “clocks off latency” is less than 2 PCI clocks.

11.0 OPERATION OF DUAL FUCTION PINS



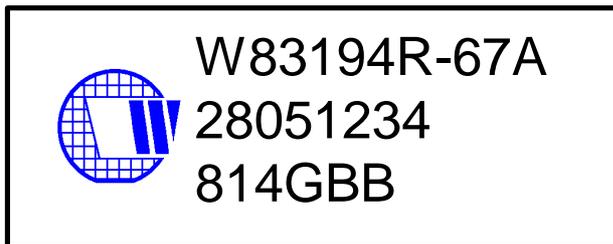


PRELIMINARY

12.0 ORDERING INFORMATION

| Part Number | Package Type | Production Flow |
|-------------|--------------|--------------------------|
| W83194R-67A | 48 PIN SSOP | Commercial, 0°C to +70°C |

13.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194R-67A

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

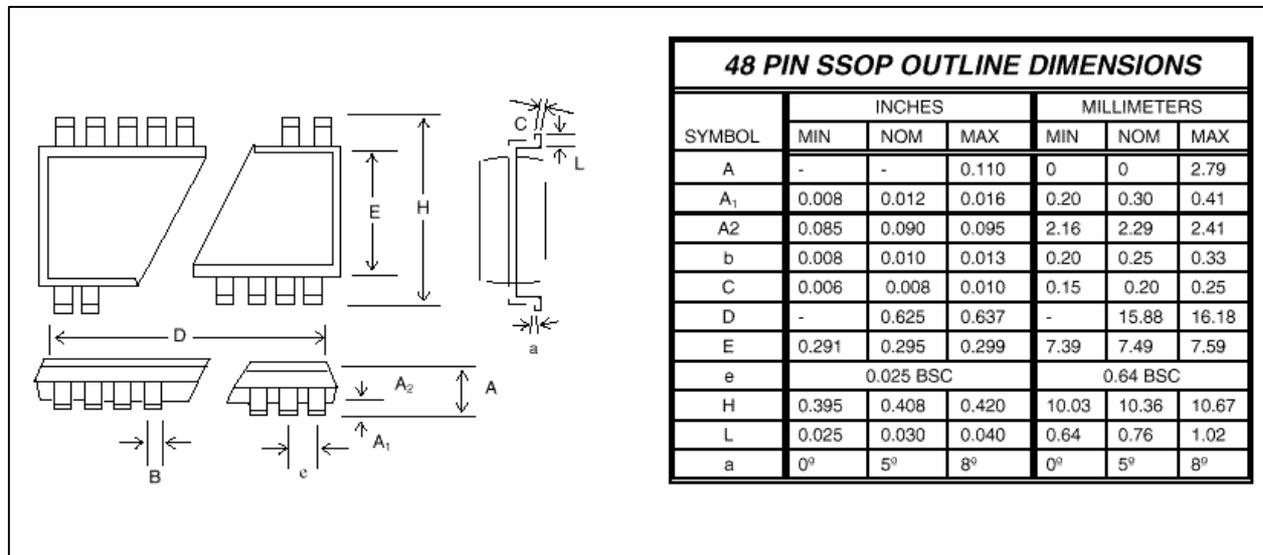
814: packages made in '98, week 14

G: assembly house ID; A means ASE, S means SPIL, G means GR

BB: IC revision

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14.0 PACKAGE DRAWING AND DIMENSIONS



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