3.3V 125-MHz 8-Output Zero Delay Buffer

Features

- **Output frequency range: 25 MHz to 125 MHz**
- **Input frequency range (÷4): 35 MHz to 125 MHz**
- **Input frequency range (÷8): 25 MHz to 62.5 MHz**
- **3.3V operation**
- **Eight Clock outputs: Drive up to 16 clock lines**
- **One feedback output**
- **LVPECL reference clock input**
- **150-ps max output-output skew**
- **Phase-locked loop (PLL) bypass mode**
- **Spread Aware™**
- **Output enable/disable**
- **Pin-compatible with MPC9653 and MPC953**
- **Industrial temperature range: –40°C to +85°C**
- **32-pin 1.0-mm TQFP package**

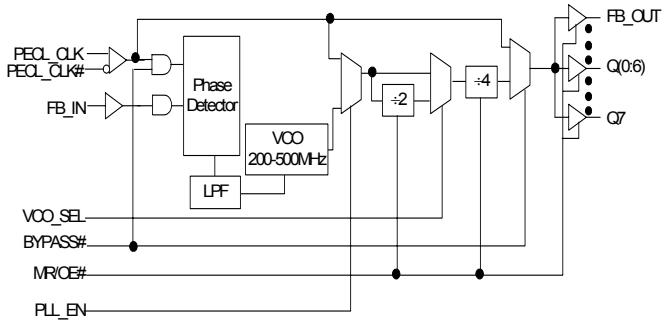
Description

The CY29653 is a low-voltage high-performance 125-MHz PLL-based zero delay buffer designed for high-speed clock distribution applications. The CY29653 features an LVPECL reference clock input and provides eight outputs plus one feedback output. VCO output divides by four or eight per VCO_SEL setting (see the *Function Table).* Each LVCMOS-compatible output can drive 50Ω series- or parallel-terminated transmission lines. For series-terminated transmission lines, each output can drive one or two traces giving the device an effective fanout of 1:16.

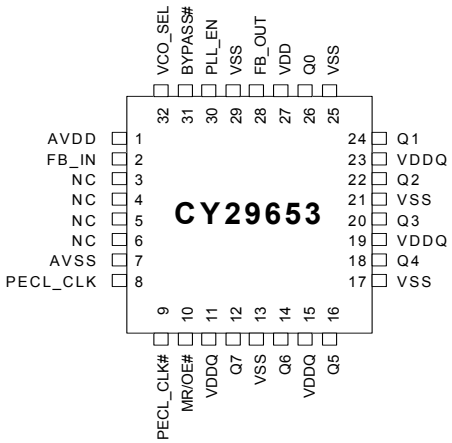
The PLL is ensured stable given that the VCO is configured to run between 140 MHz to 500 MHz. This allows a wide range of output frequencies from 25 MHz to 125 MHz. For normal operation, the external feedback input, FB_IN, is connected to the feedback output, FB_OUT. The internal VCO is running at multiples of the input reference clock set by the feedback divider (see the *Frequency Table).*

When PLL_EN is LOW, PLL is bypassed and the reference clock directly feeds the output dividers. This mode is fully static and the minimum input clock frequency specification does not apply. When BYPASS# is set LOW, PLL and output dividers are bypassed resulting in a 1:9 LVPECL to LVCMOS high performance fanout buffer. For normal PLL operation both PLL_EN and BYPASS# are set HIGH.

Block Diagram



Pin Configuration



Pin Description[1]

Pin	Name	I/O	Type	Description
8	PECL_CLK	I, PU	LVPECL	**LVPECL reference clock input**
9	PECL_CLK#	I, PU	LVPECL	**LVPECL reference clock input**. Pull-up to VDD/2.
12, 14, 16, 18, 20, 22, 24, 26	Q(7:0)	O	LVCMOS	**Clock output**
28	FB_OUT	O	LVCMOS	**Feedback clock output**. Connect to FB_IN for normal operation.
2	FB_IN	I, PU	LVCMOS	**Feedback clock input**. Connect to FB_OUT for normal operation. This input should be at the same voltage rail as input reference clock. See Frequency Table.
10	MR/OE#	I, PD	LVCMOS	**Output enable/disable input**. See Function Table.
30	PLL_EN	I, PU	LVCMOS	**PLL enable/disable input**. See Function Table.
31	BYPASS#	I, PU	LVCMOS	**PLL and output divider bypass select input**. See Function Table.
32	VCO_SEL	I, PU	LVCMOS	**VCO divider select input**. See Function Table.
11, 15, 19, 23	VDDQ	Supply	VDD	**3.3V Power supply for output clocks**[2]
1	AVDD	Supply	VDD	**3.3V Power supply for PLL**[2]
27	VDD	Supply	VDD	**3.3V Power supply for core and inputs**[2]
7	AVSS	Supply	Ground	**Analog Ground**
13, 17, 21, 25, 29	VSS	Supply	Ground	**Common Ground**
3, 4, 5, 6	NC			**No connection**

Frequency Table

Feedback Output Divider	VCO	Input Frequency Range
÷4	Input Clock * 4	35 MHz to 125 MHz
÷8	Input Clock * 8	25 MHz to 62.5 MHz

Function Table

Control	Default	0	1
VCO_SEL	1	VCO ÷ 1	VCO ÷ 2
PLL_EN	1	Bypass mode, PLL disabled. The input clock connects to the output dividers	PLL enabled. The VCO output connects to the output dividers
BYPASS#	1	Bypass mode with PLL and output dividers bypassed. The input clock connects to the outputs.	Selects the output dividers
MR/OE#	0	Outputs enabled	Outputs disabled (three-state), VCO running at its minimum frequency

Notes:
1. PU = Internal pull-up, PD = Internal pull-down.
2. A 0.1–μF bypass capacitor should be placed as close as possible to each positive power pin (<0.2”). If these bypass capacitors are not close to the pins their high-frequency filtering characteristics will be cancelled by the lead inductance of the traces.

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	DC Supply Voltage		–0.3	5.5	V
V_{DD}	DC Operating Voltage	Functional	3.135	3.465	V
V_{IN}	DC Input Voltage	Relative to V_{SS}	-0.3	V_{DD} + 0.3	V
V_{OUT}	DC Output Voltage	Relative to V_{SS}	–0.3	V_{DD} + 0.3	V
V_{TT}	Output termination Voltage			$V_{DD} \div 2$	V
LU	Latch Up Immunity	Functional	200		mA
R_{PS}	Power Supply Ripple	Ripple Frequency < 100 kHz		150	mVp-p
T_S	Temperature, Storage	Non-functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Functional	–	+85	°C
T_J	Temperature, Junction	Functional		150	°C
$Ø_{JC}$	Dissipation, Junction to Case	Functional		42	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	Functional		105	°C/W
ESD_H	ESD Protection (Human Body Model)		2000		V
FIT	Failure in Time	Manufacturing test	10		ppm

DC Parameters (V_{DD} = 3.3V ± 5%, T_A = operating temperature range)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Voltage, Low	LVCMOS	–	–	0.8	V
V_{IH}	Input Voltage, High	LVCMOS	2.0	–	V_{DD}+0.3	V
V_{PP}	Peak-Peak Input Voltage	LVPECL	250	–	1000	mV
V_{CMR}	Common Mode Range[4]	LVPECL	1.0	–	V_{DD} – 0.6	V
V_{OL}	Output Voltage, Low[5]	I_{OL} = 24 mA	–	–	0.55	V
		I_{OL} = 12 mA	–	–	0.30	
V_{OH}	Output Voltage, High[5]	I_{OH} = –24 mA	2.4	–		V
I_{IL}	Input Current, Low[6]	$V_{IL} = V_{SS}$	–	–	–100	µA
I_{IH}	Input Current, High[6]	$V_{IL} = V_{DD}$	–	–	100	µA
I_{DDA}	PLL Supply Current	AV_{DD} only	–	–	7	mA
I_{DDQ}	Quiescent Supply Current	All V_{DD} pins except AV_{DD}	–	–	4	mA
I_{DD}	Dynamic Supply Current	Outputs loaded @ 100 MHz	–	330	–	mA
C_{IN}	Input Pin Capacitance		–	4	–	pF
Z_{OUT}	Output Impedance		12	15	18	Ω

AC Parameters (V_{DD} = 3.3V ± 5%, T_A = operating temperature range) [3]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
f_{VCO}	VCO Frequency		140	–	500	MHz
f_{in}	Input Frequency	÷4 Feedback	35	–	125	MHz
		÷8 Feedback	25	–	62.5	
		Bypass mode (BYPASS# = 0)	0	–	200	
f_{refDC}	Input Duty Cycle		40	–	60	%
V_{PP}	Peak-Peak Input Voltage	LVPECL	500	–	1000	mV

Notes:

3. AC characteristics apply for parallel output termination of 50Ω to V_{TT}. Parameters are guaranteed by characterization and are not 100% tested.
4. V_{CMR} (DC) is the crossing point of the differential input signal. Normal operation is obtained when the crossing point is within the V_{CMR} range and the input swing is within the V_{PP} (DC) specification.
5. Driving one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, each output drives up to two 50 Ω series terminated transmission lines.
6. Inputs have pull-up or pull-down resistors that affect the input current.

AC Parameters (V_{DD} = 3.3V ± 5%, T_A = operating temperature range) (continued)[3]

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{CMR}	Common Mode Range[7]	LVPECL	1.2	–	VDD – 0.9	V
f_{MAX}	Maximum Output Frequency	÷4 Output	35	–	125	MHz
		÷8 Output	25	–	62.5	
DC	Output Duty Cycle		45	–	55	%
t_r , t_f	Output Rise/Fall times	0.55V to 2.4V	0.1	–	1.0	ns
$t_{(\phi)}$	Propagation Delay (static phase offset)	PCLK to FB_IN	–200	–	200	ps
t_{PD}	Propagation Delay (PLL and divider bypass)	PCLK to Q0 – Q7 BYPASS# = 0	3.6	4.8	6.0	ns
$t_{sk(O)}$	Output-to-Output Skew		–	–	150	ps
$t_{PLZ, HZ}$	Output Disable Time		–	–	6	ns
$t_{PZL, ZH}$	Output Enable Time		–	–	6	ns
BW	PLL Closed Loop Bandwidth (–3dB)	÷4 Feedback	–	1.8 – 2.1	–	MHz
		÷8 Feedback	–	1.4 – 1.6	–	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter		–	–	100	ps
$t_{JIT(PER)}$	Period Jitter		–	–	100	ps
$t_{JIT(\phi)}$	I/O Phase Jitter		–	–	150	ps
t_{LOCK}	Maximum PLL Lock Time		–	–	1	ms

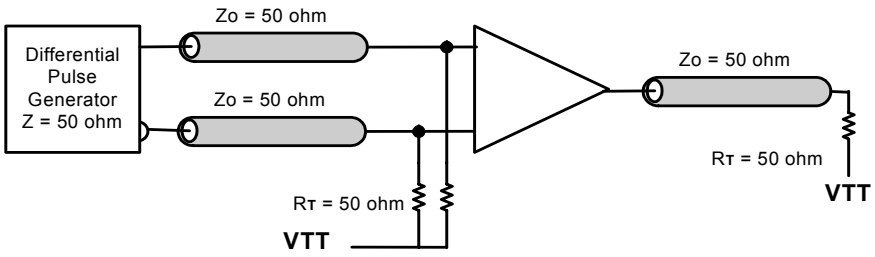


Figure 1. AC Test Reference

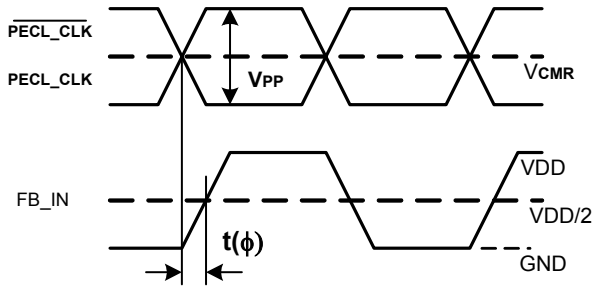


Figure 2. Propagation Delay t(ϕ), Static Phase Offset

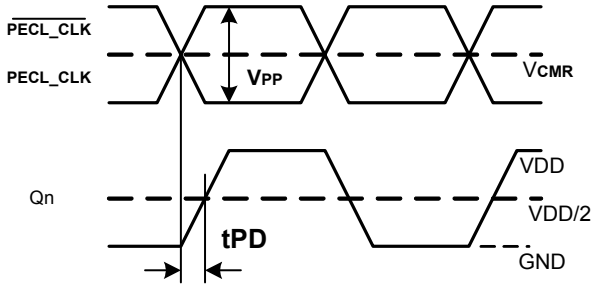


Figure 3. Propagation Delay t_{PD}, PLL Bypass

Note:
7. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset t(ϕ).

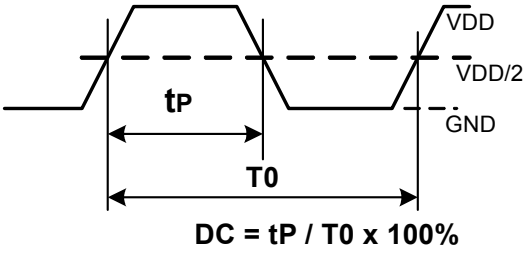


Figure 4. Output Duty Cycle (DC)

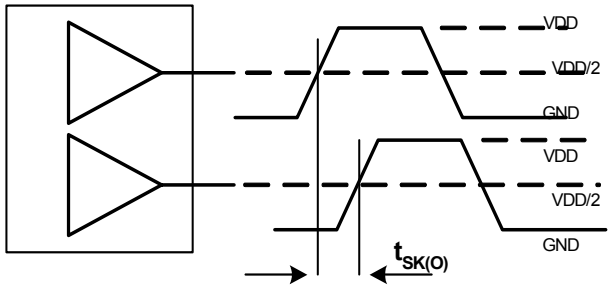


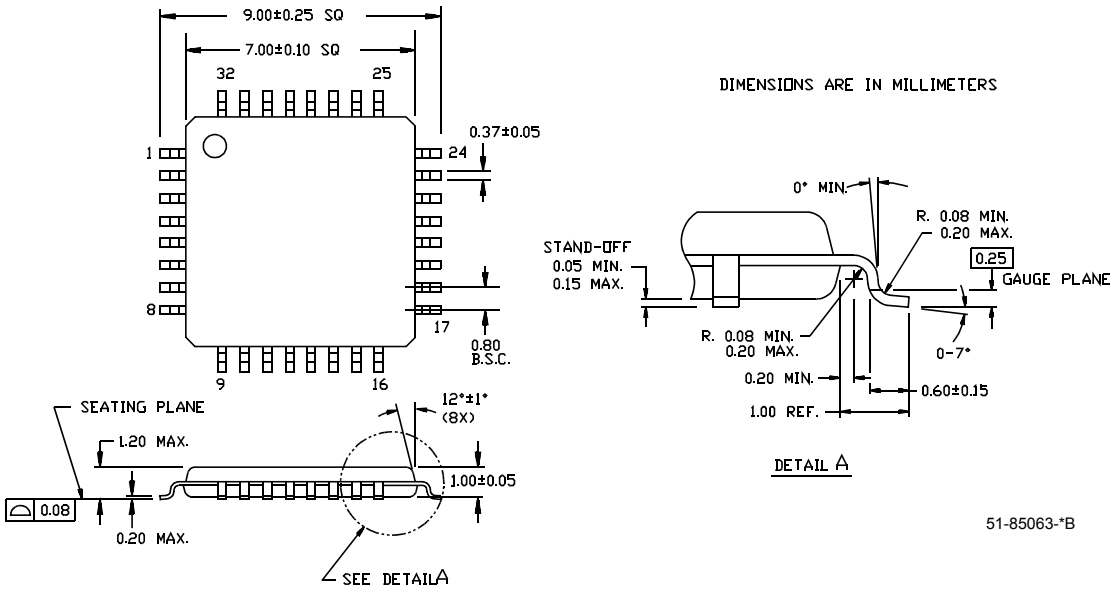
Figure 5. Output-to-Output Skew $t_{sk(O)}$

Ordering Information

Part Number	Package Type	Product Flow
CY29653AC	32-pin TQFP	Commercial, 0°C to +70°C
CY29653ACT	32-pin TQFP – Tape and Reel	Commercial, 0°C to 70°C
CY29653AI	32-pin TQFP	Industrial, –40°C to +85°C
CY29653AIT	32-pin TQFP – Tape and Reel	Industrial, –40°C to 85°C

Package Drawing and Dimension

32-lead Thin Plastic Quad Flatpack 7 x 7 x 1.0 mm A32



Document History Page

Document Title:CY29653 3.3V 125-MHz 8-Output Zero Delay Buffer Document Number: 38-07477				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	126715	05/15/03	RGL	New Data Sheet
*A	130841	11/07/03	RGL	Added Industrial Temp. Range
*B	209720	See ECN	RGL	Minor Change: To post in the CY external website