

SN5451, SN54LS51, SN54S51 SN7451, SN74LS51, SN74S51 AND-OR-INVERT GATES

SDLS113 – DECEMBER 1983 – REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

description

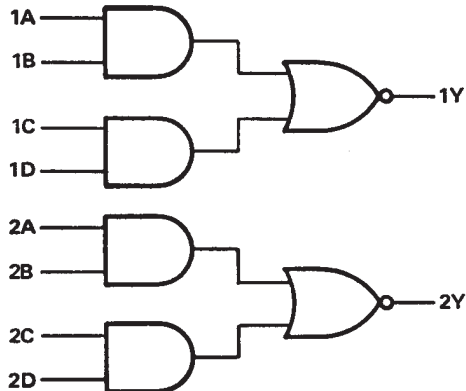
The '51 and 'S51 contain two independent 2-wide 2-input AND-OR-INVERT gates. They perform the Boolean function $Y = \overline{AB + CD}$.

The 'LS51 contains one 2-wide 3-input and one 2-wide 2-input AND-OR-INVERT gates. They perform the Boolean functions $1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$ and $2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$.

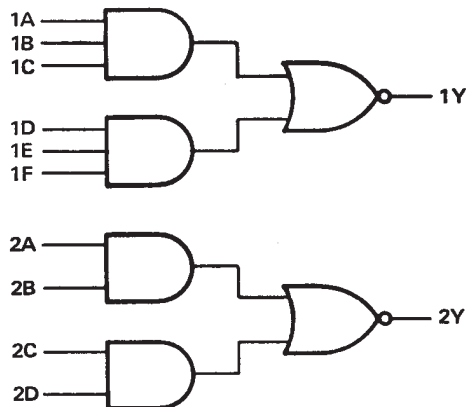
The SN5451, SN54LS51, and SN54S51 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7451, SN74LS51 and SN74S51 are characterized for operation from 0°C to 70°C .

logic diagrams

'51, 'S51

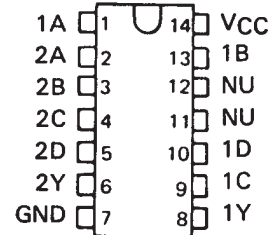


'LS51



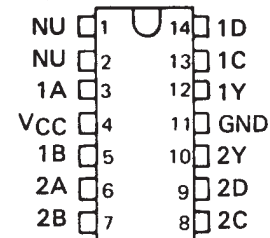
SN5451 . . . J PACKAGE
SN54S51 . . . J OR W PACKAGE
SN7451 . . . N PACKAGE
SN74S51 . . . D OR N PACKAGE

(TOP VIEW)



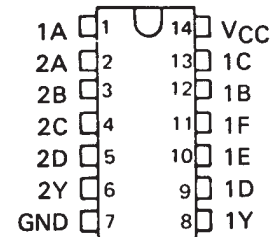
SN5451 . . . W PACKAGE

(TOP VIEW)



SN54LS51 . . . J OR W PACKAGE
SN74LS51 . . . D OR N PACKAGE

(TOP VIEW)



NC - No internal connection

NU - Make no external connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

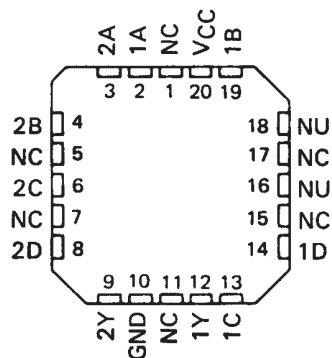
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1988, Texas Instruments Incorporated

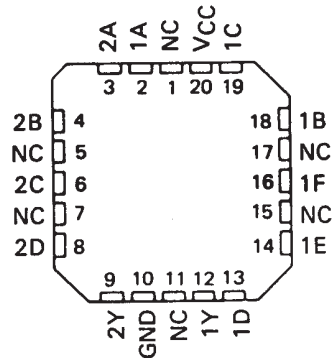
SN5451, SN54LS51, SN54S51 SN7451, SN74LS51, SN74S51 AND-OR-INVERT GATES

SDLS113 – DECEMBER 1983 – REVISED MARCH 1988

SN54S51 . . . FK PACKAGE
(TOP VIEW)

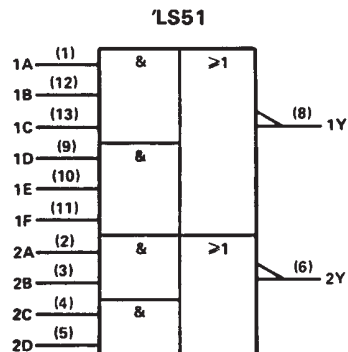
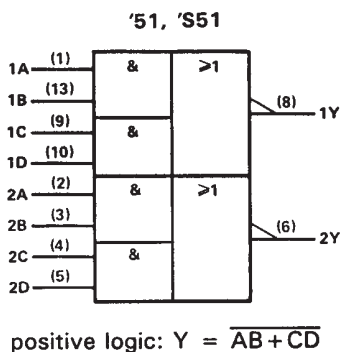


SN54LS51 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection
NU - Make no external connection

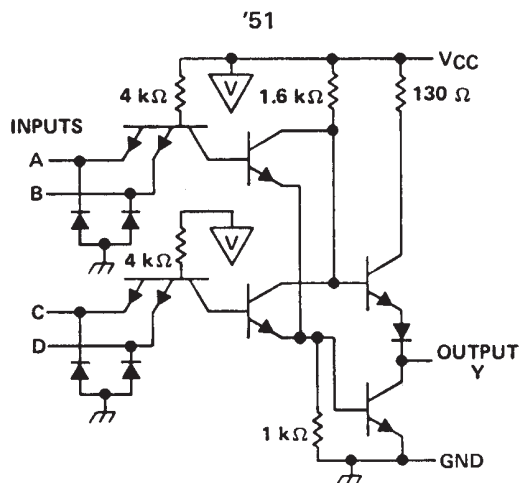
logic symbols†



positive logic:
 $1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$
 $2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$

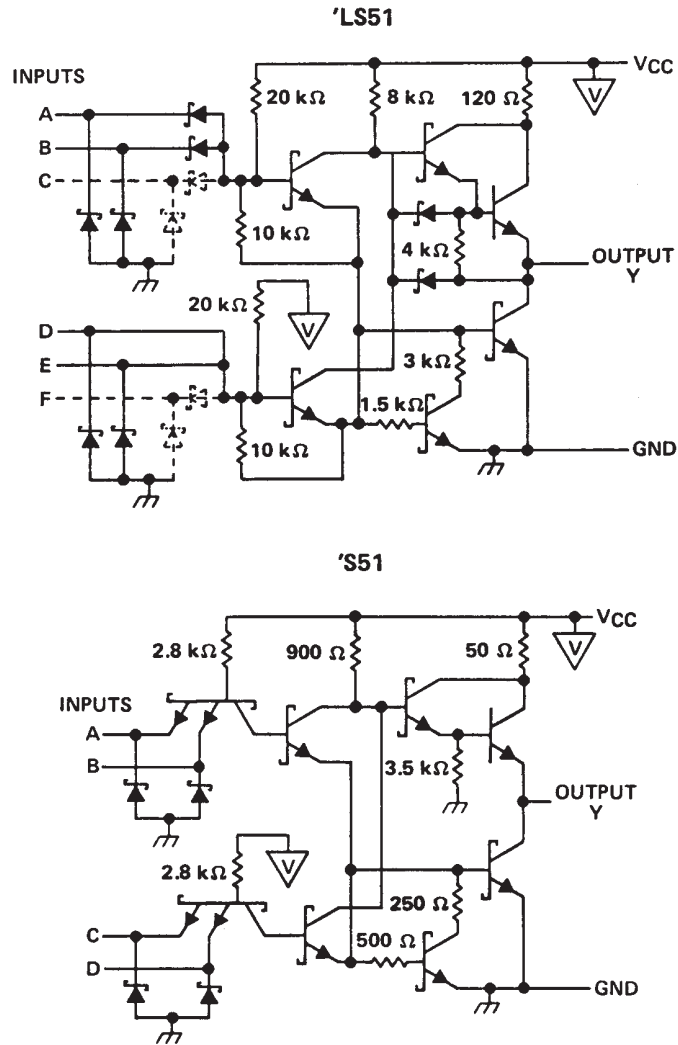
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

schematics



SN5451, SN54LS51, SN54S51
SN7451, SN74LS51, SN74S51
AND-OR-INVERT GATES

SDLS113 – DECEMBER 1983 – REVISED MARCH 1988



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1): '51, 'LS51, 'S51	7 V
Input voltage: '51, 'S51	5.5 V
'LS51	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

SN5451, SN54LS51, SN54S51 SN7451, SN74LS51, SN74S51 AND-OR-INVERT GATES

SDLS113 – DECEMBER 1983 – REVISED MARCH 1988

recommended operating conditions

	SN5451			SN7451			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH} High-level input voltage	2			2			V
V _{IL} Low-level input voltage			0.8			0.8	V
I _{OH} High-level output current			− 0.4			− 0.4	mA
I _{OL} Low-level output current			16			16	mA
T _A Operating free-air temperature	− 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN5451			SN7451			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = − 12 mA			− 1.5			− 1.5	V
V _{OH}	V _{CC} = MIN, V _{IL} = 0.8 V, I _{OH} = − 0.4 mA	2.4	3.4		2.4	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, I _{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I _I	V _{CC} = MAX, V _I = 5.5 V			1			1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.4 V			40			40	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4 V			− 1.6			− 1.6	mA
I _{OS} §	V _{CC} = MAX	− 20		− 55	− 18		− 55	mA
I _{CCH}	V _{CC} = MAX, V _I = 0 V		4	8		4	8	mA
I _{CCL}	V _{CC} = MAX, See Note 2		7.4	14		7.4	14	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Any	Y	R _L = 400 Ω, C _L = 15 pF		13	22	ns
t _{PHL}					8	15	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN5451, SN54LS51, SN54S51
SN7451, SN74LS51, SN74S51
AND-OR-INVERT GATES

SDLS113 – DECEMBER 1983 – REVISED MARCH 1988

recommended operating conditions

	SN54LS51			SN74LS51			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			– 0.4			– 0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS51			SN74LS51			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			– 1.5			– 1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4		V
	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$				0.35	0.5		
I_I	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			– 0.4			– 0.4	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	– 20		– 100	– 20		– 100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		0.8	1.6		0.8	1.6	mA
I_{CCL}	$V_{CC} = \text{MAX}, \text{ See Note 2}$		1.4	2.8		1.4	2.8	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 2 \text{ k}\Omega, C_L = 15 \text{ pF}$		12	20	ns
t_{PHL}					12.5	20	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



SN5451, SN54LS51, SN54S51 SN7451, SN74LS51, SN74S51 AND-OR-INVERT GATES

SDLS113 – DECEMBER 1983 – REVISED MARCH 1988

recommended operating conditions

	SN54S51			SN74S51			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			– 1			– 1	mA
I_{OL} Low-level output current			20			20	mA
T_A Operating free-air temperature	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S51			SN74S51			UNIT
		MIN	TYP ‡	MAX	MIN	TYP ‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			– 1.2			– 1.2	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50			50	µA
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			– 2			– 2	mA
$I_{OS} §$	$V_{CC} = \text{MAX}$	– 40		– 100	– 40		– 100	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		8.2	17.8		8.2	17.8	mA
I_{CCL}	$V_{CC} = \text{MAX}, \text{ See Note 2}$		13.6	22		13.6	22	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 280 \Omega, C_L = 15 \text{ pF}$		3.5	5.5	ns
t_{PHL}					3.5	5.5	ns
t_{PLH}			$R_L = 280 \Omega, C_L = 50 \text{ pF}$		5		ns
t_{PHL}					5.5		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.