LC²MOS
Precision Quad SPST Switches

ADG411/ADG412/ADG413

FEATURES

44 V supply maximum ratings
±15 V analog signal range
Low on resistance (< 35 Ω)
Ultralow power dissipation (35 µW)
Fast switching times
t_{ON} < 175 ns
t_{OFF} < 145 ns
TTL-/CMOS-compatible
Plug-in replacement for DG411/DG412/DG413

APPLICATIONS

Audio and video switching
Automatic test equipment
Precision data acquisition
Battery-powered systems
Sample-and-hold systems
Communication systems

GENERAL DESCRIPTION

The ADG411, ADG412, and ADG413 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process which provides low power dissipation yet gives high switching speed and low on resistance.

The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals. Fast switching speed coupled with high signal bandwidth also make the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

The ADG411, ADG412, and ADG413 contain four independent SPST switches. The ADG411 and ADG412 differ only in that the digital control logic is inverted. The ADG411 switches are turned on with a logic low on the appropriate control input, while a logic high is required for the ADG412. The ADG413 has two switches with digital control logic similar to that of the ADG411 while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when on, and each has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended signal range
   The ADG411, ADG412, and ADG413 are fabricated on an enhanced LC²MOS, giving an increased signal range which extends fully to the supply rails.
2. Ultralow power dissipation
3. Low R_{ON}
4. Break-before-make switching
   This prevents channel shorting when the switches are configured as a multiplexer.
5. Single-supply operation
   For applications where the analog signal is unipolar, the ADG411, ADG412, and ADG413 can be operated from a single-rail power supply. The parts are fully specified with a single 12 V power supply and remain functional with single supplies as low as 5 V.

FUNCTIONAL BLOCK DIAGRAMS

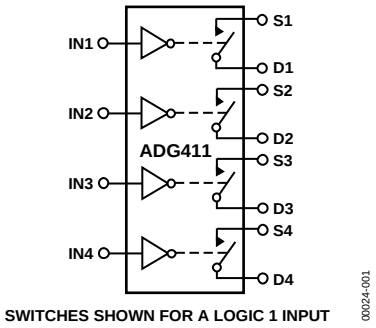

Figure 1. ADG411

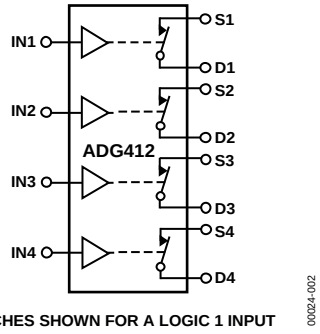

Figure 2. ADG412

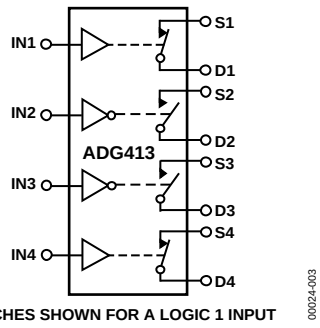

Figure 3. ADG413

Rev. C

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SPECIFICATIONS

DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, V_L = 5 V ± 10%, GND = 0 V, unless otherwise noted.[1]

Table 1.

	B Version		T Version			
Parameter	**+25°C**	**−40°C to +85°C**	**+25°C**	**−55°C to +125°C**	**Unit**	**Test Conditions/Comments**
ANALOG SWITCH						
Analog Signal Range		V_{DD} to V_{SS}		V_{DD} to V_{SS}	V	
R_{ON}	25		25		Ω typ	V_D = ±8.5 V, I_S = −10 mA;
	35	45	35	45	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source OFF Leakage I_S (OFF)	±0.1		±0.1		nA typ	V_D = +15.5 V/−15.5 V, V_S = −15.5 V/+15.5 V;
	±0.25	±0.25	±0.25	±20	nA max	Figure 15
Drain OFF Leakage I_D (OFF)	±0.1		±0.1		nA typ	V_D = +15.5 V/−15.5 V, V_S = −15.5 V/+15.5 V;
	±0.25	±5	±0.25	±20	nA max	Figure 15
Channel ON Leakage I_D, I_S (ON)	±0.1		±0.1		nA typ	V_D = V_S = +15.5 V/−15.5 V;
	±0.4	±10	±0.4	± 40	nA max	Figure 16
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}	0.005		0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5		±0.5	µA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	110		110		ns typ	R_L = 300 Ω, C_L = 35 pF;
		175		175	ns max	V_S = ±10 V; Figure 17
t_{OFF}	100		100		ns typ	R_L = 300 Ω, C_L = 35 pF;
		145		145	ns max	V_S = ±10 V; Figure 17
Break-Before-Make Time Delay, t_D (ADG413 Only)	25		25		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = 10 V; Figure 18
Charge Injection	5		5		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Figure 19
OFF Isolation	68		68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 20
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 21
C_S (OFF)	9		9		pF typ	f = 1 MHz
C_D (OFF)	9		9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		35		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V; Digital inputs = 0 V or 5 V
I_{DD}	0.0001		0.0001		µA typ	
	1	5	1	5	µA max	
I_{SS}	0.0001		0.0001		µA typ	
	1	5	1	5	µA max	
I_L	0.0001		0.0001		µA typ	
	1	5	1	5	µA max	

[1] Temperature ranges are as follows: B versions: −40°C to +85°C; T versions: −55°C to +125°C.
[2] Guaranteed by design; not subject to production test.

SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, V_L = 5 V ± 10%, GND = 0 V, unless otherwise noted.[1]

Table 2.

	B Version		T Version			
Parameter	**+25°C**	**−40°C to + 85°C**	**+25°C**	**−55°C to +125°C**	**Unit**	**Test Conditions/Comments**
ANALOG SIGNAL RANGE		0 V to V_{DD}		0 V to V_{DD}	V	
R_{ON}	40		40		Ω typ	0 < V_D = 8.5 V, I_S = −10 mA;
	80	100	80	100	Ω max	V_{DD} = 10.8 V
LEAKAGE CURRENTS						V_{DD} = 13.2 V
Source OFF Leakage I_S (OFF)	±0.1		±0.1		nA typ	V_D = 12.2 V/1 V, V_S = 1 V/12.2 V;
	±0.25	±5	±0.25	±20	nA max	Figure 15
Drain OFF Leakage I_D (OFF)	±0.1		±0.1		nA typ	V_D = 12.2 V/1 V, V_S = 1 V/12.2 V;
	±0.25	±5	±0.25	±20	nA max	Figure 15
Channel ON Leakage I_D, I_S (ON)	±0.1		±0.1		nA typ	V_D = V_S = 12.2 V/1 V;
	±0.4	±10	±0.4	±40	nA max	Figure 16
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}	0.005		0.005		µA typ	V_{IN} = V_{INL} or V_{INH}
		±0.5		±0.5	µA max	
DYNAMIC CHARACTERISTICS[2]						
t_{ON}	175		175		ns typ	R_L = 300 Ω, C_L = 35 pF;
		250		250	ns max	V_S = 8 V; Figure 17
t_{OFF}	95		95		ns typ	R_L = 300 Ω, C_L = 35 pF;
		125		125	ns max	V_S = 8 V; Figure 17
Break-Before-Make Time Delay, t_D (ADG413 Only)	25		25		ns typ	R_L = 300 Ω, C_L = 35 pF; V_{S1} = V_{S2} = +10 V; Figure 18
Charge Injection	25		25		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 10 nF; Figure 19
OFF Isolation	68		68		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 20
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 21
C_S (OFF)	9		9		pF typ	f = 1 MHz
C_D (OFF)	9		9		pF typ	f = 1 MHz
C_D, C_S (ON)	35		35		pF typ	f = 1 MHz
POWER REQUIREMENTS						V_{DD} = 13.2 V; Digital inputs = 0 V or 5 V
I_{DD}	0.0001		0.0001		µA typ	
	1	5	1	5	µA max	
I_L	0.0001		0.0001		µA typ	
	1	5	1	5	µA max	V_L = 5.25 V

[1] Temperature ranges are as follows: B versions:−40°C to +85°C; T versions: −55°C to +125°C.
[2] Guaranteed by design; not subject to production test.

Table 3. Truth Table (ADG411/ADG412)

ADG411 In	ADG412 In	Switch Condition
0	1	ON
1	0	OFF

Table 4. Truth Table (ADG413)

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameters	Ratings
V_{DD} to V_{SS}	44 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
V_L to GND	−0.3 V to V_{DD} + 0.3 V
Analog, Digital Inputs[1]	V_{SS} − 2 V to V_{DD} + 2 V or 30 mA, whichever occurs first
Continuous Current, S or D	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle max)	100 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Extended (T Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
CERDIP Package, Power Dissipation	900 mW
θ_{JA} Thermal Impedance	76°C/W
Lead Temperature, Soldering (10 s)	300°C
PDIP, Power Dissipation	470 mW
θ_{JA} Thermal Impedance	117°C/W
Lead Temperature, Soldering (10 s)	260°C
SOIC Package, Power Dissipation	600 mW
θ_{JA} Thermal Impedance	77°C/W
TSSOP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	115°C/W
θ_{JC} Thermal Impedance	35°C/W
Lead Temperature, Soldering	
Vapor Phase (60 s)	215°C
Infrared (15 s)	220°C

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

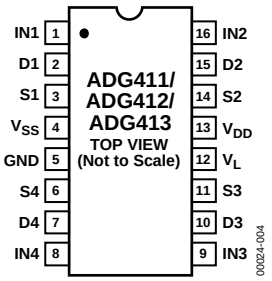


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 8, 9, 16	IN1–IN4	Logic Control Input.
2, 7, 10, 15	D1–D4	Drain Terminal. Can be an input or output.
3, 6, 11, 14	S1–S4	Source Terminal. Can be an input or output.
4	V_{SS}	Most Negative Power Supply Potential in Dual Supplies. In single supply applications, it may be connected to GND.
5	GND	Ground (0 V) Reference.
12	V_L	Logic Power Supply (5 V).
13	V_{DD}	Most Positive Power Supply Potential.

TYPICAL PERFORMANCE CHARACTERISTICS

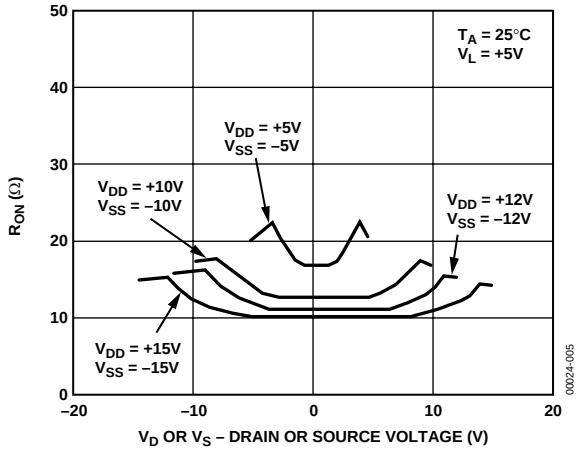


Figure 5. On Resistance as a Function of V_D (V_S) Dual Supplies

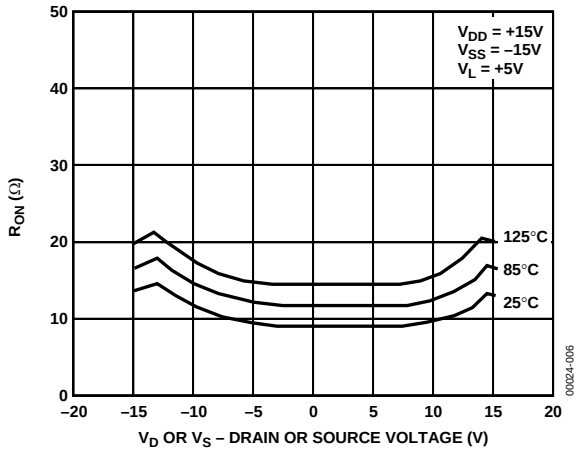


Figure 6. On Resistance as a Function of V_D (V_S) for Different Temperatures

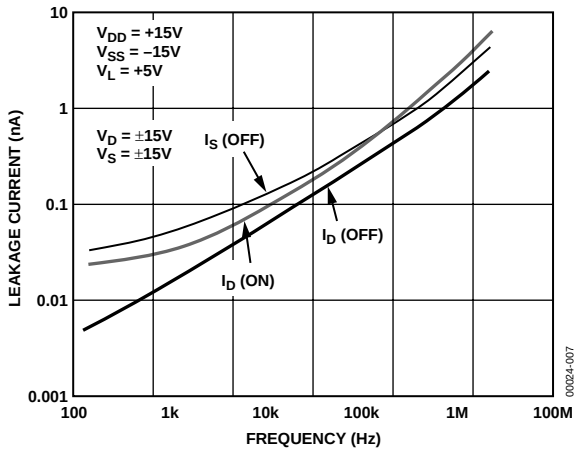


Figure 7. Leakage Currents as a Function of Temperature

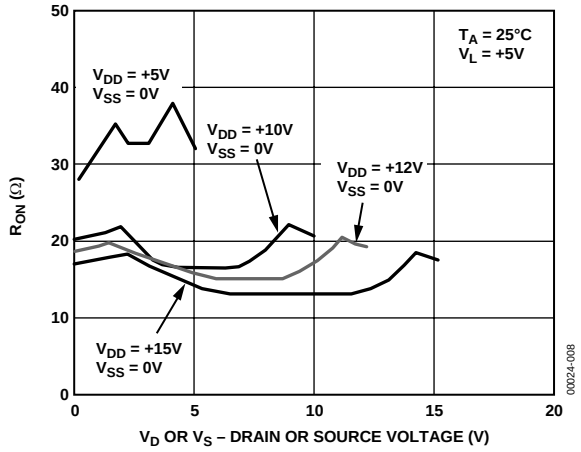


Figure 8. On Resistance as a Function of V_D (V_S) Single Supply

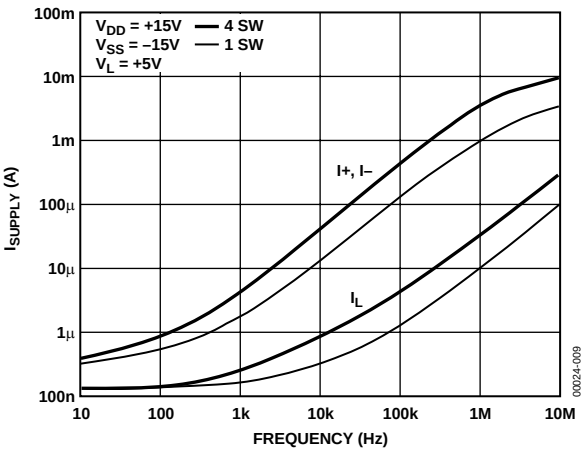


Figure 9. Supply Current vs. Input Switching Frequency

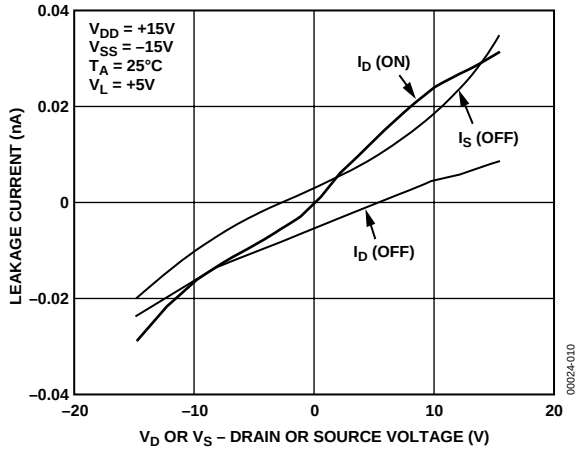


Figure 10. Leakage Currents as a Function of V_D (V_S)

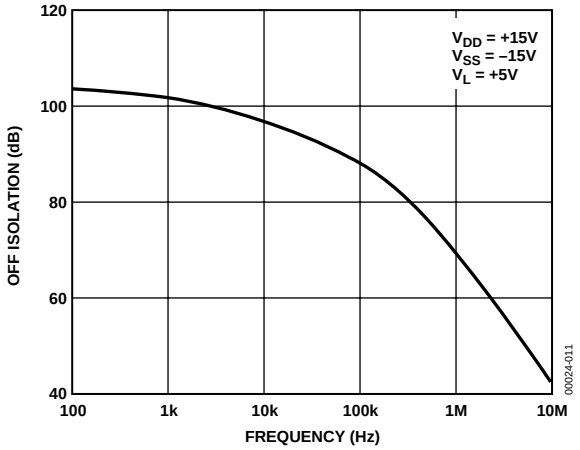


Figure 11. Off Isolation vs. Frequency

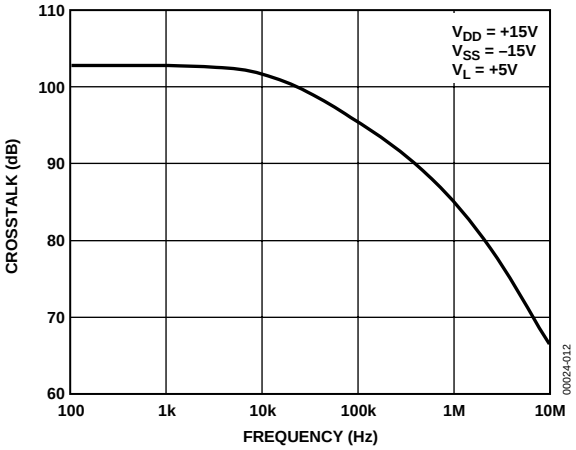


Figure 12. Crosstalk vs. Frequency

TERMINOLOGY

R_{ON}

Ohmic resistance between D and S.

I_S (OFF)

Source leakage current with the switch OFF.

I_D (OFF)

Drain leakage current with the switch OFF.

I_D, I_S (ON)

Channel leakage current with the switch ON.

V_D (V_S)

Analog voltage on terminals D, S.

C_S (OFF)

OFF switch source capacitance.

C_D (OFF)

OFF switch drain capacitance.

C_D, C_S (ON)

ON switch capacitance.

t_{ON}

Delay between applying the digital control input and the output switching on.

t_{OFF}

Delay between applying the digital control input and the output switching off.

t_D

OFF time or ON time measured between the 90% points of both switches, when switching from one address state to another.

Crosstalk

A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.

Off Isolation

A measure of unwanted signal coupling through an OFF switch.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

APPLICATIONS

Figure 13 illustrates a precise, fast, sample-and-hold circuit. An AD845 is used as the input buffer while the output operational amplifier is an AD711. During the track mode, SW1 is closed and the output V_{OUT} follows the input signal V_{IN}. In the hold mode, SW1 is opened and the signal is held by the hold capacitor C_H.

Due to switch and capacitor leakage, the voltage on the hold capacitor decreases with time. The ADG411/ADG412/ADG413 minimizes this droop due to its low leakage specifications. The droop rate is further minimized by the use of a polystyrene hold capacitor. The droop rate for the circuit shown is typically 30 μV/μs.

A second switch, SW2, which operates in parallel with SW1, is included in this circuit to reduce pedestal error. Since both switches are at the same potential, they have a differential effect on the op amp AD711, which minimizes charge injection effects. Pedestal error is also reduced by the compensation network R_C and C_C. This compensation network also reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the ±10 V input range. Both the acquisition and settling times are 850 ns.

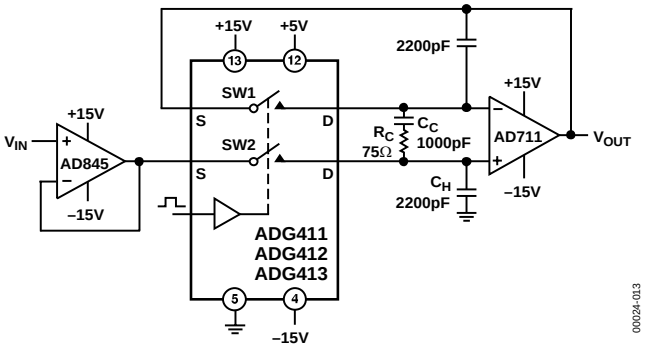


Figure 13. Fast, Accurate Sample-and-Hold

TEST CIRCUITS

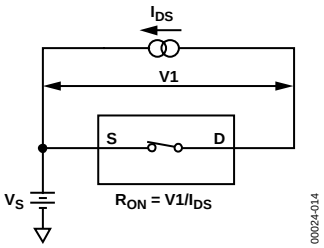


Figure 14. On Resistance

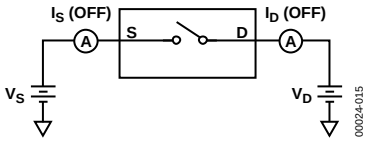


Figure 15. Off Leakage

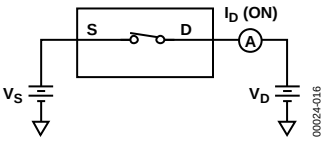


Figure 16. On Leakage

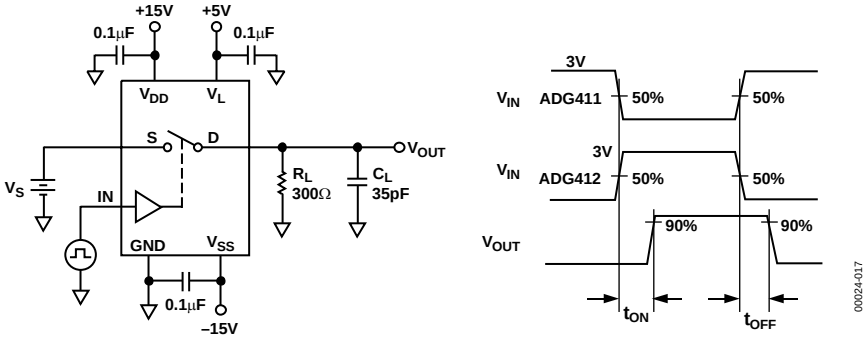


Figure 17. Switching Times

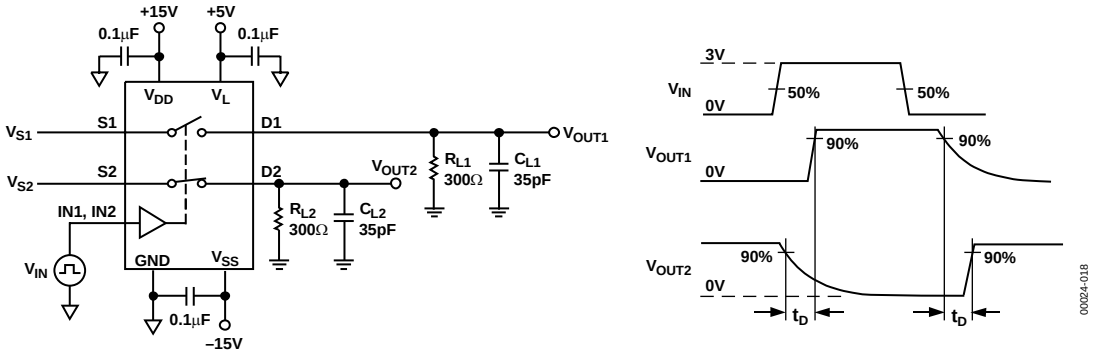


Figure 18. Break-Before-Make Time Delay

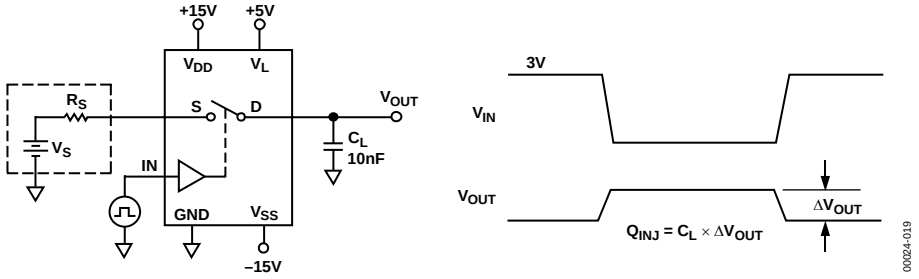


Figure 19. Charge Injection

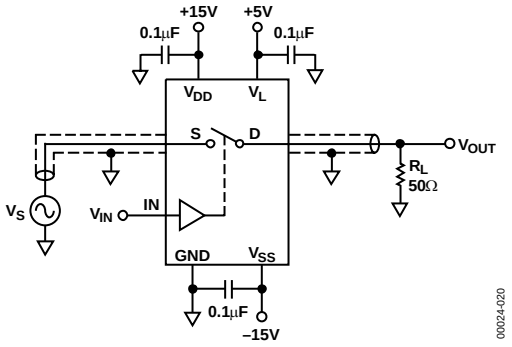


Figure 20. Off Isolation

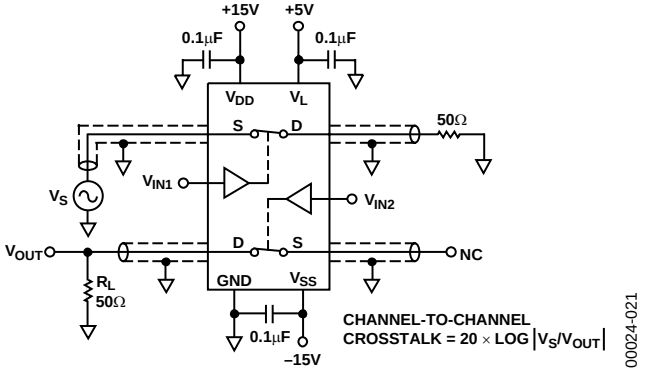
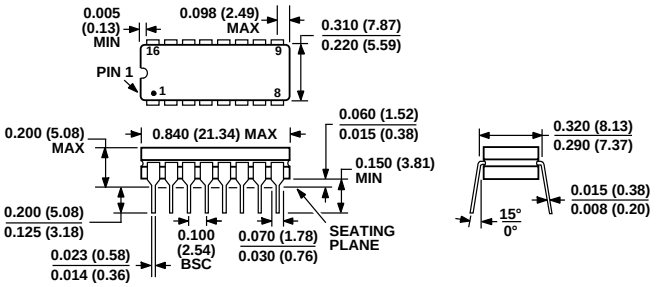


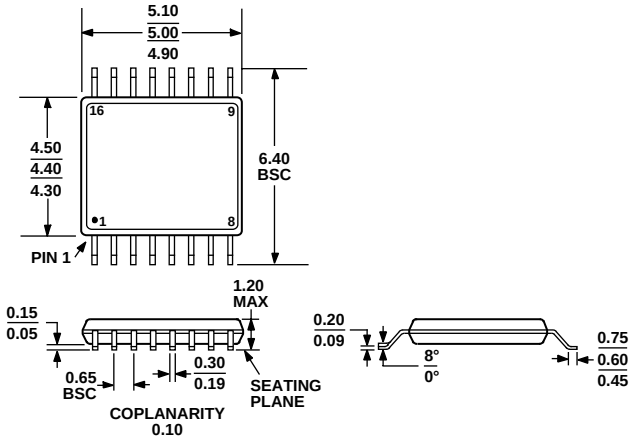
Figure 21. Channel-to-Channel Crosstalk

OUTLINE DIMENSIONS



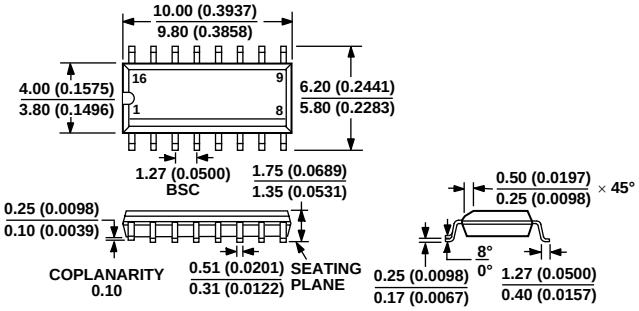
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 22. 16-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-16)
Dimensions shown in inches and (millimeters)



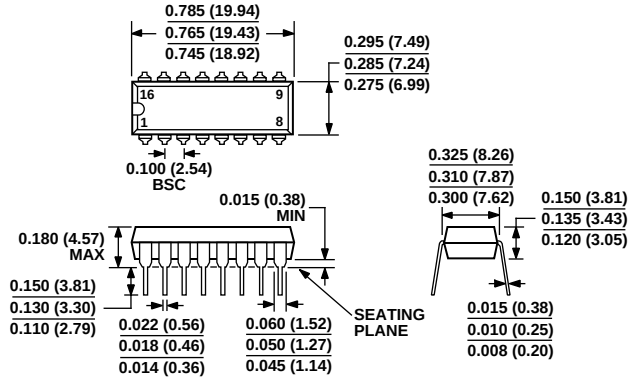
COMPLIANT TO JEDEC STANDARDS MO-153AB

Figure 24. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012AC
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 23. 16-Lead Standard Small Outline Package [SOIC]
Narrow Body
(R-16)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-095AC
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 25. 16-Lead Plastic Dual In-Line Package [PDIP]
(N-16)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG411BN	−40°C to +85°C	P-DIP	N-16
ADG411BR	−40°C to +85°C	SOIC	R-16A
ADG411BR-REEL	−40°C to +85°C	SOIC	R-16A
ADG411BR-REEL7	−40°C to +85°C	SOIC	R-16A
ADG411BRZ[1]	−40°C to +85°C	SOIC	R-16A
ADG411BRZ-REEL[1]	−40°C to +85°C	SOIC	R-16A
ADG411BRZ-REEL7[1]	−40°C to +85°C	SOIC	R-16A
ADG411BRU	−40°C to +85°C	TSSOP	RU-16
ADG411BRU-REEL	−40°C to +85°C	TSSOP	RU-16
ADG411BRU-REEL7	−40°C to +85°C	TSSOP	RU-16
ADG411BRUZ[1]	−40°C to +85°C	TSSOP	RU-16
ADG411BRUZ-REEL[1]	−40°C to +85°C	TSSOP	RU-16
ADG411BRUZ-REEL7[1]	−40°C to +85°C	TSSOP	RU-16
ADG411TQ	−55°C to +125°C	CERDIP	Q-16
ADG411BCHIPS		DIE	
ADG412BN	−40°C to +85°C	P-DIP	N-16
ADG412BR	−40°C to +85°C	SOIC	R-16A
ADG412BR-REEL	−40°C to +85°C	SOIC	R-16A
ADG412BR-REEL7	−40°C to +85°C	SOIC	R-16A
ADG412BRZ[1]	−40°C to +85°C	SOIC	R-16A
ADG412BRZ-REEL[1]	−40°C to +85°C	SOIC	R-16A
ADG412BRZ-REEL7[1]	−40°C to +85°C	SOIC	R-16A
ADG412BRU	−40°C to +85°C	TSSOP	RU-16
ADG412BRU-REEL	−40°C to +85°C	TSSOP	RU-16
ADG412BRU-REEL7	−40°C to +85°C	TSSOP	RU-16
ADG412BRUZ[1]	−40°C to +85°C	TSSOP	RU-16
ADG412BRUZ-REEL[1]	−40°C to +85°C	TSSOP	RU-16
ADG412BRUZ-REEL7[1]	−40°C to +85°C	TSSOP	RU-16
ADG412TQ	−55°C to +125°C	CERDIP	Q-16
ADG412TCHIPS		DIE	
ADG413BN	−40°C to +85°C	P-DIP	N-16
ADG413BR	−40°C to +85°C	SOIC	R-16A
ADG413BR-REEL	−40°C to +85°C	SOIC	R-16A
ADG413BRZ[1]	−40°C to +85°C	SOIC	R-16A
ADG413BRZ-REEL[1]	−40°C to +85°C	SOIC	R-16A
ADG413BRUZ[1]	−40°C to +85°C	TSSOP	RU-16
ADG413BRUZ-500RL7[1]	−40°C to +85°C	TSSOP	RU-16
ADG413BRUZ-REEL[1]	−40°C to +85°C	TSSOP	RU-16
ADG413BRUZ-REEL7[1]	−40°C to +85°C	TSSOP	RU-16

[1] Z = Pb-free part.

NOTES

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