IR3622AMPbF

HIGH FREQUENCY 2-PHASE, SINGLE OR DUAL OUTPUT SYNCHRONOUS STEP DOWN CONTROLLER WITH OUTPUT TRACKING AND SEQUENCING

Features

- Dual Synchronous Controller with 180º Out of Phase Operation
- Configurable to 2-Independent Outputs or Current Shared Single Output
- Output Voltage Tracking
- Power up / down Sequencing
- Current Sharing Using Inductor's DCR
- +/-1% Accurate Reference Voltage
- Programmable Switching Frequency up 600kHz
- Programmable Over Current Protection
- Hiccup Current Limit Using MOSFET $R_{ds(on)}$ sensing
- Latched Overvoltage Protection
- Dual Programmable Soft-Starts
- Programmable Enable Input
- Pre-Bias Start-up
- Dual Power Good Outputs
- On Board Regulator
- External Frequency Synchronization
- Thermal Protection
- 32-Lead MLPQ Package

Applications

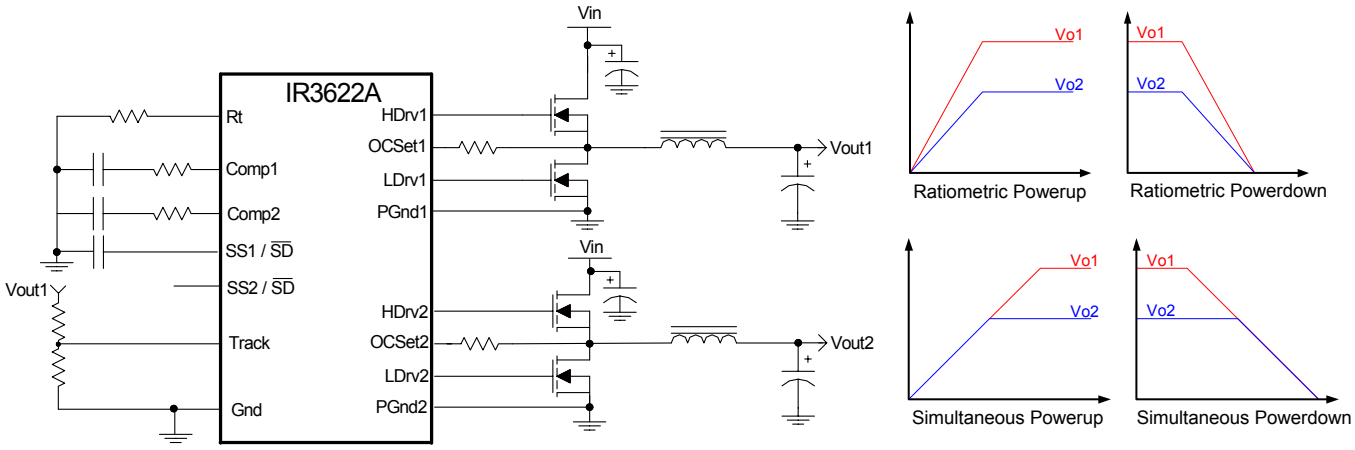
- Embedded Telecom Systems
- Distributed Point of Load Power Architectures
- Computing Peripheral Voltage Regulator
- Graphics Card
- General DC/DC Converters

Description

The IR3622A IC integrates a dual synchronous Buck controller, providing a high performance and flexible solution. The IR3622A can be configured as 2-independent outputs or as current shared single output. The current share configuration is ideal for high current applications.

The IR3622A enables output tracking and sequencing of multiple rails in either ratiometric or simultaneous fashion. The IR3622A features 180º out of phase operation which reduces the required input/output capacitance and results in lower number of capacitors. The switching frequency is programmable from 200kHz to 600kHz per phase using one external resistor. In addition, IR3622A also allows the switching frequency to be synchronized to an external clock signal.

Other key features offered by this device include two independent programmable soft starts, two independent power good outputs, precision enable input, and under voltage lockout function. The current limit is provided by sensing the lower MOSFET's on-resistance for optimum cost and performance. The output voltages are monitored through dedicated pins to protect against open circuit, and enhance faster response to an overvoltage event.



ORDERING INFORMATION

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER BAG	PARTS PER REEL	T&R ORIANTAION
M	IR3622AMPbF	32	100	-------	Fig A
M	IR3622AMTRPbF	32	--------	3000	

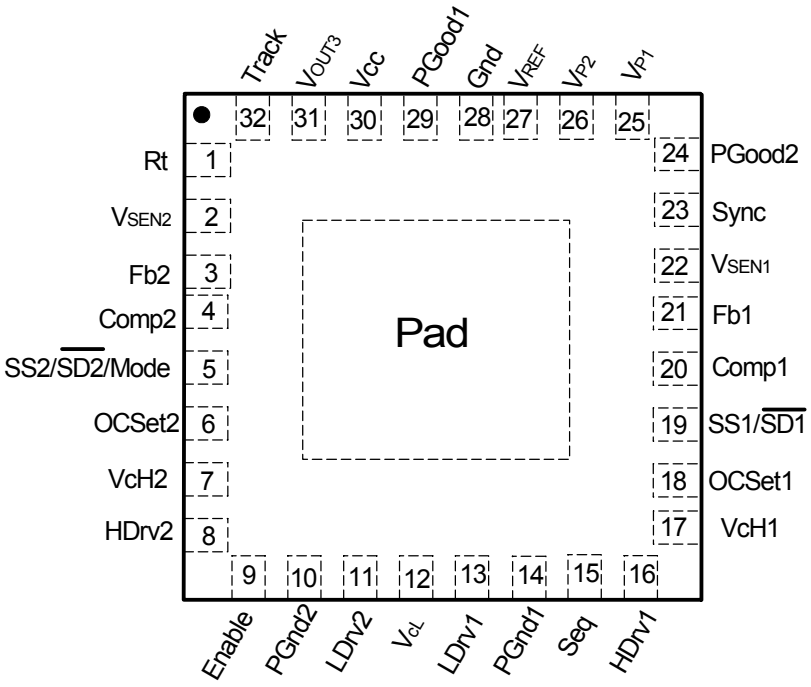
ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND)

- Vcc, VcL Supply Voltage ..... -0.5V to 16V
- VcH1,VcH2 ..... -0.5V to 30V
- PGood1, PGood2 ..... -0.5V to 16V
- HDrv1, HDrv2 ..... -0.5V to 30V (-2V for 100ns)
- LDrv1, LDrv2 ..... -0.5V to 16V (-2V for 100ns)
- Gnd to PGnd ..... +/- 0.3V
- Storage Temperature Range ..... -65°C To 150°C
- Operating Junction Temperature Range ..... -40°C To 125°C
- ESD Classification ..... JEDEC, JESD22-A114 (1KV)
- Moisture Sensitivity Level ..... JEDEC, Level 3 @ 260°C

Caution: *Stresses above those listed in "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only and function of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to "Absolute Maximum Rating" conditions for extended periods may affect device reliability.*

Package Information



Θ_{JA} = 36° C/W
Θ_{JC} = 1° C/W

**Exposed pad on underside is connected to a copper pad through vias for 4-layer PCB board design*

Recommended Operating Conditions

Symbol	Definition	Min	Max	Units
Vcc, VcL	Supply Voltage	4.5	14.5	V
VcH1, VcH2	Supply Voltage	Converter Voltage + 5V	28	V
Fs	Operating frequency	200	600	kHz
Tj*	Junction temperature	-40	125	°C

* The Operating Junction Temperature for 5V application is 0°C-125°C

Electrical Specifications

Unless otherwise specified, these specification apply over Vcc=VcL=VcH1=VcH2=12V, 0°C<Tj<105°C

Parameter	SYM	Test Condition	Min	TYP	MAX	Units
Output Voltage Accuracy						
FB1,2 Voltage	V_{FB}	Vp1=Vp2=Vref=0.8V		0.8		V
Accuracy		0°C <Tj< 125°C	-1		+1	%
		-40°C <Tj< 125°C; *Note2*	-1.5		+1.5	%
Supply Current						
V_{CC} Supply Current (Static)	I_{CC} (Static)	SS=0V, No Switching		13	18	mA
V_{CC} Supply Current (Dynamic)	I_{CC} (Dynamic)	Fs=300kHz, C_{LOAD}= 3.3nF		20	30	mA
V_{CL} Supply Current (Static)	I_{CL} (Static)	SS=0V, No Switching		8	10	mA
V_{CL} Supply Current (Dynamic)	I_{CL} (Dynamic)	Fs=300kHz, C_{LOAD}= 3.3nF		30	42	mA
$V_{CH1,2}$ Supply Current (Static)	I_{CH} (Static)	SS=0V, No Switching		9	11	mA
$V_{CH1,2}$ Supply Current (Dynamic)	I_{CH} (Dynamic	Fs=300kHz, C_{LOAD}= 3.3nF		30	42	mA
Under Voltage Lockout, Enable						
V_{CC}-Start Threshold	V_{CC}_UVLO(R)	Supply ramping up	3.9	4.1	4.3	V
V_{CC}-Stop Threshold	V_{CC}_UVLO(F)	Supply ramping down	3.7	3.8	4.1	V
V_{CC}-Hysteresis		Supply ramping up and down	0.15	0.25	0.3	V
Enable-Threshold	En_UVLO	Supply ramping up	1.14	1.24	1.34	V
Enable-Hysteresis		Supply ramping up and down	0.15	0.22	0.33	V
Oscillator						
Frequency Range	F_S		200		600	kHz
Accuracy		Fs=300kHz	-12		+12	%
Ramp Amplitude	Vramp	*Note1*		1.25		V
Min Duty Cycle	Dmin	Fb=1V			0	%
Min Pulse Width	Dmin(ctrl)	F_S=300kHz, *Note1*			150	ns
Max duty Cycle	Dmax	F_S=300kHz, Fb=0.6V	84			%
Sync Frequency Range	Sync(F)	20% above free running Freq			1200	kHz
Sync Pulse Duration	Sync(Pulse)		200	300		ns
Sync High Level Threshold	Sync(H)		2			V
Sync Low Level Threshold	Sync(L)				0.6	V

Electrical Specifications

Parameter	SYM	Test Condition	Min	TYP	MAX	Units
Error Amplifier 1, 2						
Fb Voltage Input Bias Current	IFB	SS=3V		-0.1	-0.5	µA
E/A Source/Sink Current	I(source/Sink)		120	200	280	µA
Transconductance	gm1,2		3000		4500	µmho
Input offset Voltage	Voffset	Fb to Vref	-4	0	+4	mV
VP Voltage Range	VP	*Note1*	0.4		Vcc-2	V
Internal Regulator						
Output Accuracy	Vout3		6.7	7.2	7.7	V
Dropout	Vdrop	Vcc(min)=9V, Isource=100mA			2	V
Current Limit	Ishort		110			mA
Soft Start/SD						
Soft Start Current	ISS	Source/Sink	18	23	28	µA
Shutdown Threshold	SD				0.25	V
Over Current Protection						
OCSET Current	I_{OCSET}		16	20	24	µA
Hiccup Duty Cycle	Hiccup(duty)	Ihiccup / Iocset, *Note1*		5		%
Over Voltage Protection						
OVP Trip Threshold	OVP(trip)		1.1Vref	1.15Vref	1.2Vref	V
OVP Fault Prop Delay	OVP(delay)	Output Forced to 1.25Vref			5	µS
Thermal Shutdown						
Thermal shutdown		*Note1*		140		°C
Thermal shutdown Hysteresis		*Note1*		20		°C
Power Good						
Vsen Lower Trip point	Vsen(trip)	Vsen Ramping Down	0.8Vref	0.9Vref	0.95Vref	V
PGood Output Low Voltage	PG(voltage)	I_{PGood}=2mA		0.1	0.5	V
Output Drivers						
LO, Drive Rise Time	Tr(Lo)	C_{LOAD}=3.3nF, Fs=300KHz, **2V to 9V**		25	50	ns
LO Drive Fall Time	Tf(Lo)	C_{LOAD} =3.3nF, Fs=300KHz, **9V to 2V**		25	50	ns
HI Drive Rise Time	Tr(Hi)	C_{LOAD} =3.3nF, Fs=300KHz, **2V to 9V**		25	50	ns
HI Drive Fall Time	Tf(Hi)	C_{LOAD} =3.3nF, Fs=300KHz, **9V to 2V**		25	50	ns
Dead Band Time	Tdead	See Figure1	20	60	100	ns
Seq Input						
Seq Threshold	Seq	On	2.0			V
		Off			0.3	
Tracking						
Track voltage range	TK	*Note1*	0		Vcc	V

Note1: Guaranteed by design but not test in production

Note2: Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production

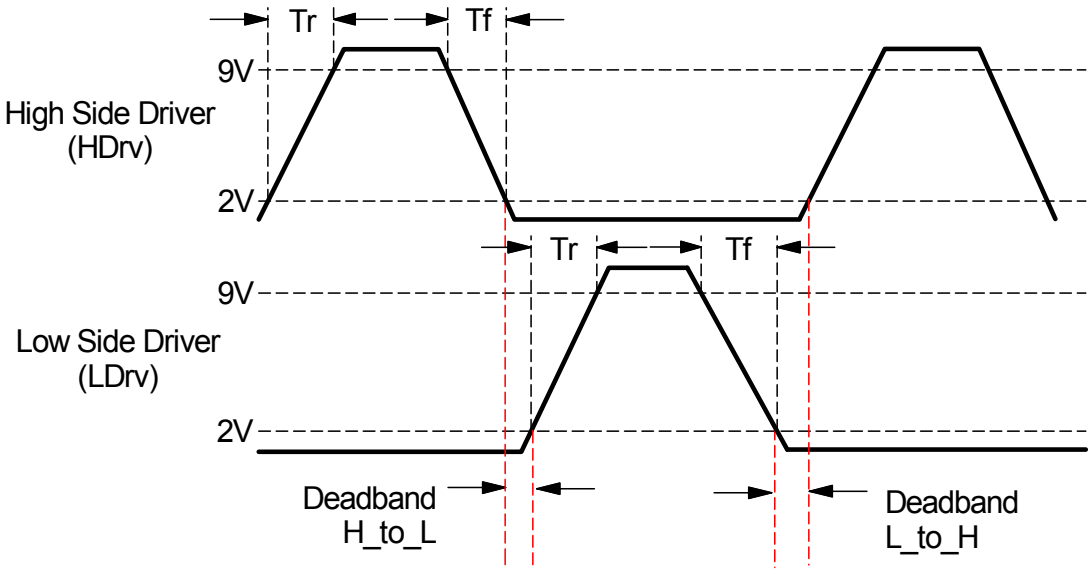


Fig. 1: Rise / Fall and deadband time for driver section

Pin#	Pin Name	Description
1	Rt	Connecting a resistor from this pin to ground sets the switching frequency (see figure 16 on page 17 for selecting resistor value)
2	V_{SEN2}	Sense pin for OVP2 and Power Good2, Channel 2
3	Fb2	Inverting input to the error amplifier2
4	Comp2	Compensation pin for the error amplifier2
5	SS2/SD2/Mode	Soft start for channel 2, can be used as SD pin. Float this pin for current share single output application
6	OCSet2	Current limit set point for channel2
7, 17	VcH2, VcH1	Supply voltage for the high side output drivers. These are connected to voltage that must be typically 6V higher than their bus voltages. A 0.1uF high frequency capacitor must be connected from these pins to PGND to provide peak drive current capability
8,16	HDrv2, HDrv1	Output drivers for the high side power MOSFETs
9	Enable	Enable pin, recycling this pin will reset OV, SS and Prebias latch
10, 14	PGnd2, PGnd1	These pins serve as the separate grounds for MOSFET drivers and should be connected to the system's ground plane
11, 13	LDrv2 , LDrv1	Output drivers for the synchronous power MOSFETs
12	VcL	Supply voltage for the low side output drivers
15	Seq	Enable pin for tracking and sequencing. If this pin is not used connect it to V_{out3}
18	OCSet1	Current limit set point for Channel 1
19	SS1/SD1	Soft start for Channel 1, can be used as SD pin
20	Comp1	Compensation pin for the error amplifier1
21	Fb1	Inverting input to the error amplifier1
22	V_{SEN1}	Sense pin for OVP1 and Power Good1, Channel 1
23	Sync	External synchronization pin
24	PGood2	Power Good pin output for channel 2, open collector. This pin needs to be externally pulled high
25	V_{P1}	Non inverting input of error amplifier1
26	V_{P2}	Non inverting input of error amplifier2
27	V_{REF}	Reference Voltage
28	Gnd	IC's Ground
29	PGood1	Power Good pin output for Channel 1, open collector. This pin needs to be externally pulled high
30	Vcc	Supply voltage for the internal blocks of the IC. A 0.1uF high frequency capacitor must be connected from this pin to Gnd.
31	V_{out3}	Output of the internal regulator. A 0.1uF high frequency capacitor must be connected from this pin to PGnd.
32	Track	Sets the type of power up / down sequencing (ratiometric or simultaneous). If this pin is not used connect it to V_{out3}

Block Diagram

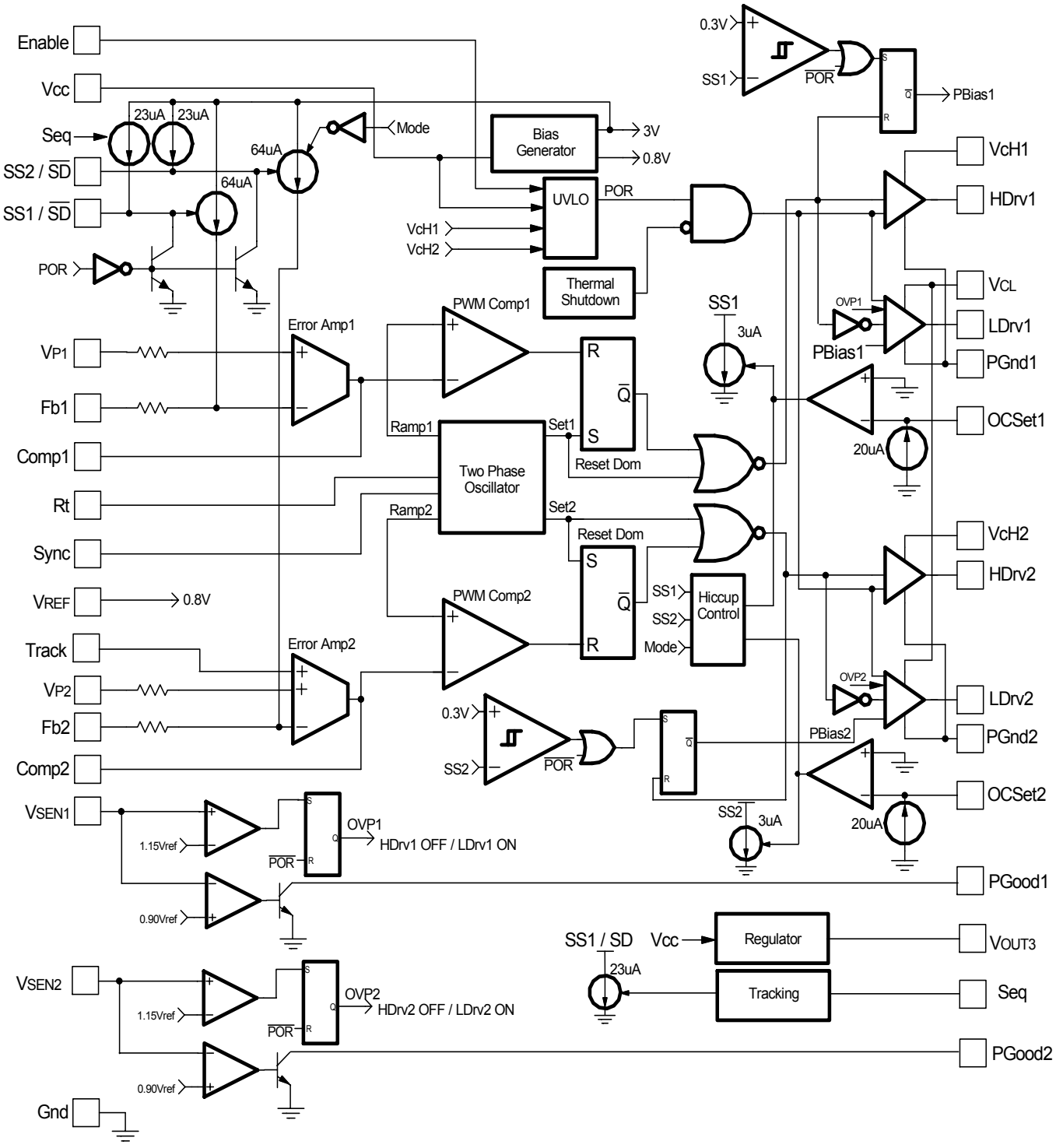
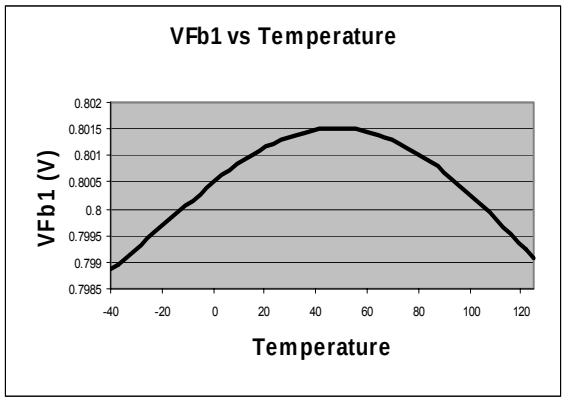
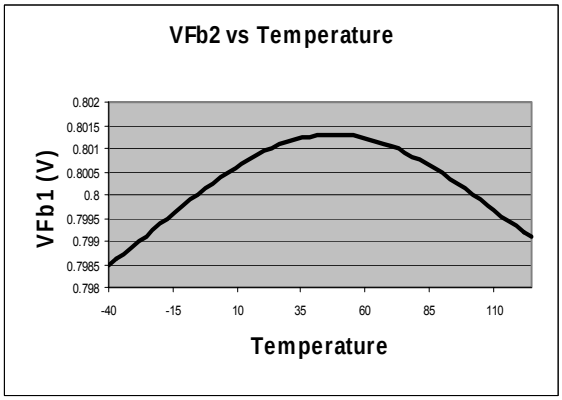
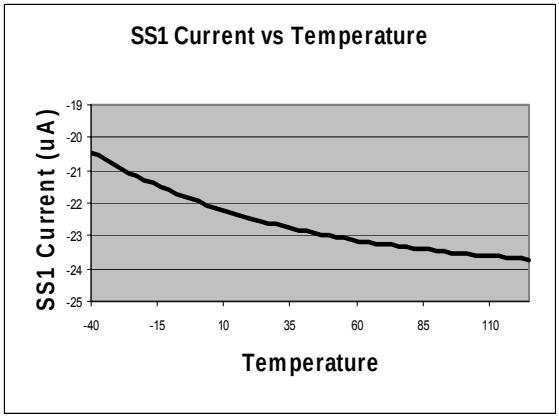


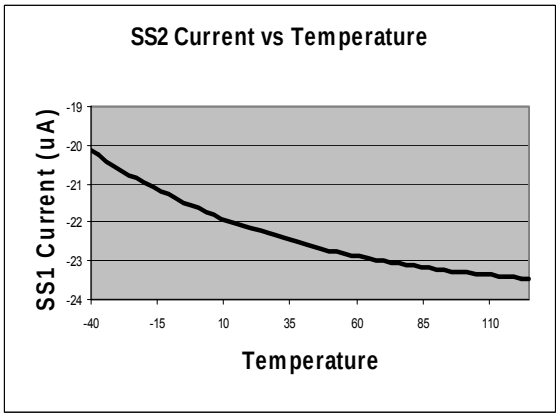
Fig. 2: Simplified block diagram of the IR3622A

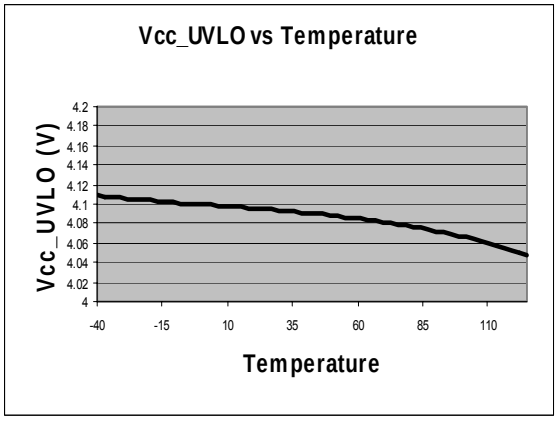
TYPICAL OPERATING CHARACTERISTICS (-40°C-125°C)

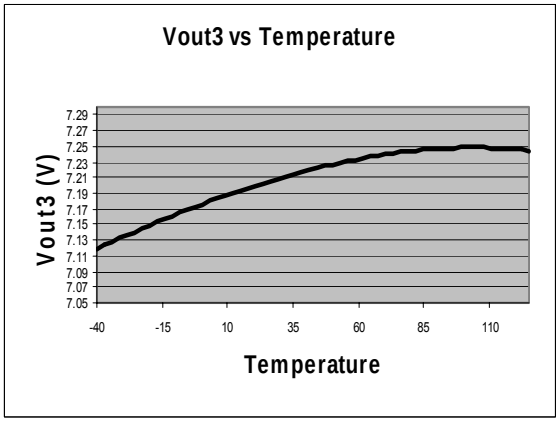




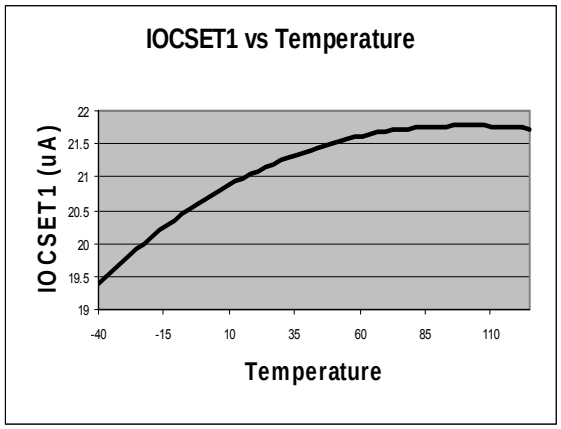


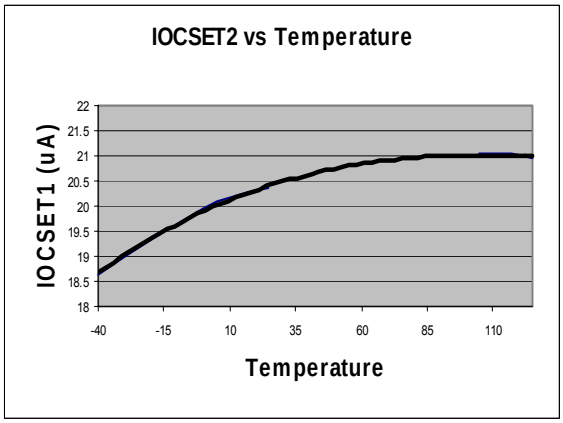


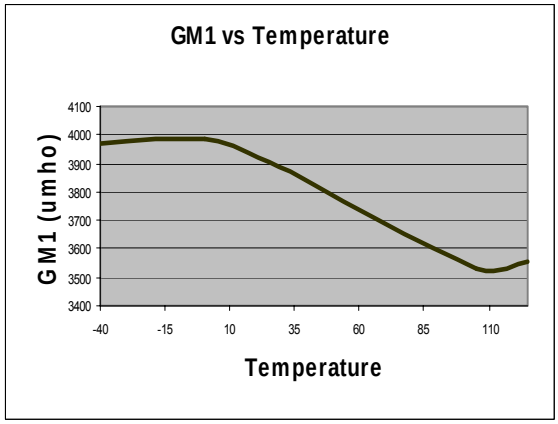


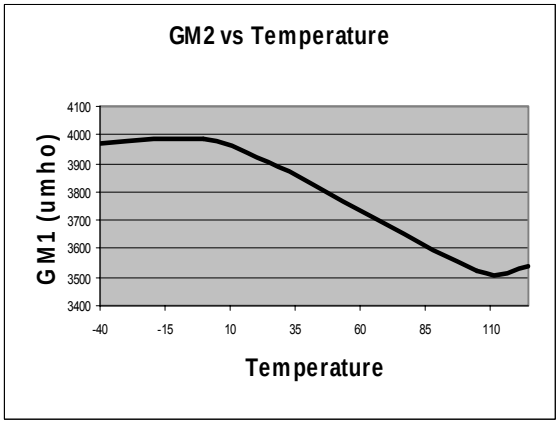


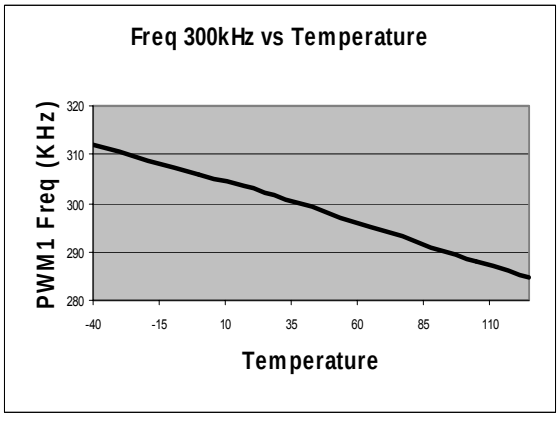
TYPICAL OPERATING CHARACTERISTICS (-40°C-125°C)

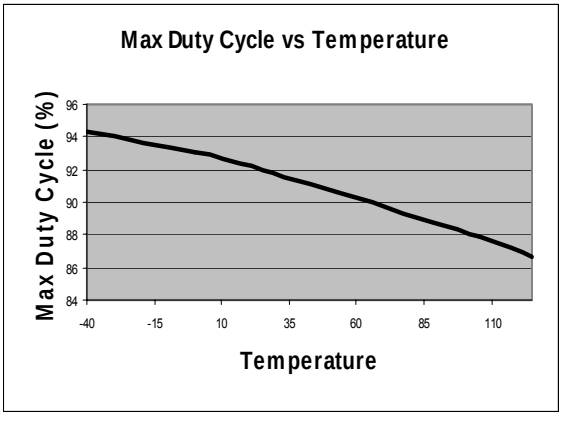












Circuit Description

THEORY OF OPEARTION

Introduction

The IR3622A is a versatile device for high performance buck converters. It consists of two synchronous buck controllers which can be operated either in two independent outputs mode or in current share single output mode for high current applications.

The timing of the IC is provided by an internal oscillator circuit which generates two-180°-out-of-phase clock that can be externally programmed up to 600kHz per phase.

Under-Voltage Lockout

The under-voltage lockout circuit monitors two signals (Vcc and Enable). This ensures the correct operation of the converter during power up and power down sequence. The driver outputs remain in the off state whenever one of these signals drop below set thresholds. Normal operation resumes once these signals rise above the set values. Figure 3 shows a typical start up sequence.

Enable

The enable features another level of flexibility for start up. The Enable has precise threshold which is internally monitored by under-voltage lockout circuit.

It's threshold can be externally programmed to desired level by using two external resistors, so the converter doesn't start up until the input voltage is sufficiently high (see figure 3).

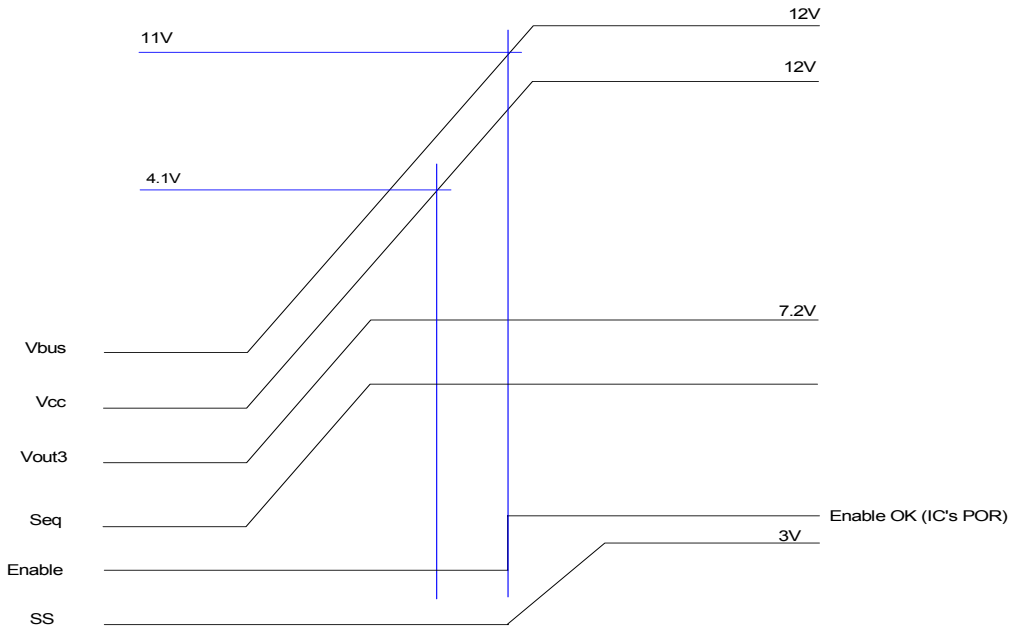


Fig. 3: Normal Start up, Enable threshold is externally set to 11V
Seq pin is pulled to Vout3 prior to start up

Internal Regulator

The IR3622A features an on-board 7.2V regulator with short circuit protection. The regulator is capable of sourcing current up to 100mA. This integrated regulator can be used to generate the necessary bias voltage for drivers, an example of how this can be used is shown in figure 23, page26.

Out-of-Phase Operation

The IR3622A drives its two output stages 180º out-of-phase. In current share mode single output, the two inductor ripple currents cancel each other and result in a reduction of the output current ripple and yield a smaller output capacitor for the same voltage ripple requirement. Figure 4 shows two channels inductor current and the resulting voltage ripple at the output.

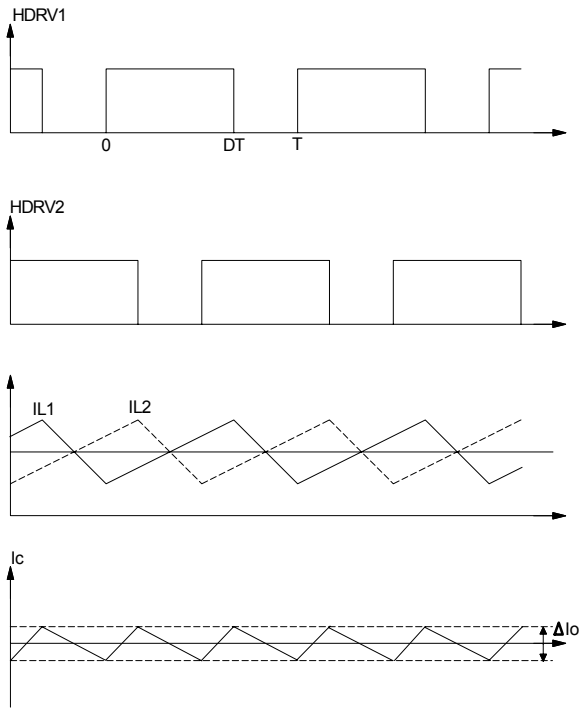


Fig. 4: Current ripple cancellation for output

In addition, the 180º out of phase contributes to input current cancellation. This results in much smaller input capacitor's RMS current and reduces the number of required input capacitors. Figure 5 shows the equivalent RMS current.

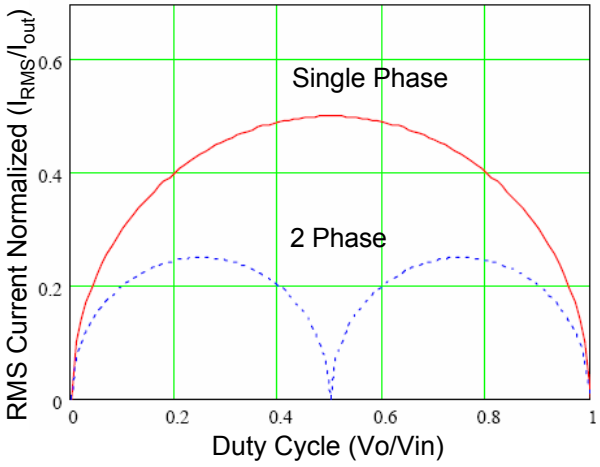


Fig. 5: Input RMS value vs. Duty Cycle

Mode Selection

The IR3622A can operate as a dual output independently regulated buck converter, or as a 2 phase single output buck converter (current share mode). The SS2 pin is used for mode selection. In current share mode this pin should be floating. In the dual output mode, a soft start capacitor must be connected from this pin to the ground to program the start time for the second output.

Independent Mode

In this mode the IR3622A provides control to two independent output power supplies with either common or different input voltages. The output voltage of each individual channel is set and controlled by the output of the error amplifier, which is the amplified error signal from the sensed output voltage and the reference voltage. The error amplifier output voltage is compared to the ramp signal thus generating fixed frequency pulses of variable duty-cycle, (PWM) which are applied to the internal MOSEFT drivers. Figure 24 shows a typical schematic for such application.

Current Share Mode

This feature allows to connect both outputs together to increase current handling capability of the converter to support a common load. In the current sharing mode, error amplifier 1 becomes the master which regulates the common output voltage and the error amplifier 2 performs the current sharing function, figure 6 shows the configuration of error amplifier 2.

In this mode, IR3622A makes sure the master channel starts first followed by slave channel to prevent any glitch during start up. This is done by clamping the output of slave's error amplifier until the master channel generates the first PWM signal.

At no load condition the slave channel may be kept off depending on the offset of the error amplifier.

Lossless Inductor Current Sensing

The IR3622A uses a lossless current sensing for current share purposes. The inductor current is sensed by connecting a series resistor and a capacitor network in parallel with the inductor and by measuring the voltage across the capacitor. The measured voltage is proportional to the inductor current. This is shown figure 6. The voltage across the inductor's DCR can be expressed by:

$$V_{RL1}(s) = (V_{in} - V_{out}) * \frac{R_{L1}}{R_{L1} + sL_1} \qquad ----(1)$$

$$V_{RL1}(s) = I_{L1} * R_{L1} \qquad ----(2)$$

The voltage across the C_1 can expressed by:

$$V_{C1}(s) = (V_{in} - V_{out}) * \frac{1/sC_1}{R_1 + 1/sC_1} \qquad ----(3)$$

Combining equations (1),(2) and (3) result in the following expression for V_{C1}:

$$V_{C1}(s) = I_{L1} * \frac{R_{L1} + sL_1}{1 + sR_1 * C_1} \qquad ----(4)$$

Usually the resistor R_1 and C_1 are chosen so that the time constant of R_1 and C_1 equals the time constant of the inductor which is the inductance L_1 over the inductor's DCR (R_{L1}). If the two time constants match, the voltage across C_1 is proportional to the current through L_1, and

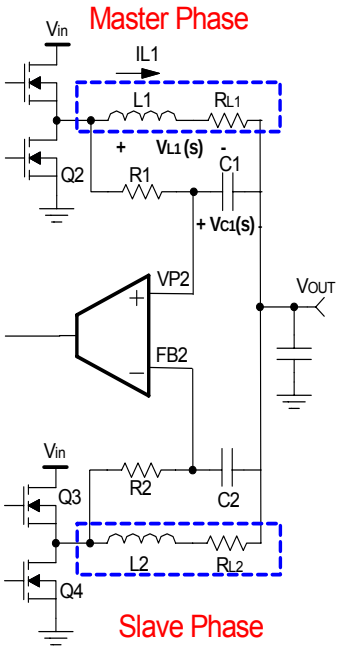


Fig. 6: Loss Less inductor current sensing and current sharing

the sense circuit can be treated as if only a sense resistor with the value R_{L1} was used.

$$If: R_1 * C_1 = \frac{L_1}{R_{L1}}$$

$$V_C(s) \approx I_{L1} * R_{L1}$$

The mismatch of the time constant does not affect the measurements of inductor DC current, but affects the AC component of the inductor current.

Soft-Start

The IR3622A has programmable soft-start to control the output voltage rise and limit the inrush current during start-up. It provides a separate soft-start function for each output. This will enable to sequence the outputs by controlling the rise time of each output through selection of different value soft-start capacitors.

To ensure correct start-up, the soft-start sequence initiates when the Vcc and Enable rise above their threshold and generate the Power On Reset (POR) signal. Soft-start function operates by sourcing an internal current to charge an external capacitor to about 3V. Initially, the soft-start function clamps the error amplifier's output of the PWM converter.

Soft-Start (cont.)

During power up, the converter output starts at zero and thus the voltage at Fb is about 0V. An internal voltage-controlled current source (64uA) injects current into the Fb pin and generates a voltage about 1.6V (64ux25K) across the negative input of error amplifier, see figure 7. This keeps the output of the error amplifier low.

The magnitude of this current is inversely proportional to the voltage at the soft-start pin. The 23uA current source starts to charge up the external capacitor. In the mean time, the soft-start voltage ramps up, the current flowing into Fb pin starts to decrease linearly and so does the voltage at the negative input of error amplifier.

When the soft-start voltage reaches about 1V, the voltage at the negative input of the error amplifier is approximately 0.8V.

As the soft-start capacitor voltage charges up, the current flowing into the Fb pin keeps decreasing.

The feedback voltage increases linearly as the injecting current goes down. The injecting current drops to zero when soft-start voltage is around 1.8V and the output voltage goes into steady state. Figure 8 shows the theoretical operational waveforms during soft-start.

The output start-up time is the time period when soft-start capacitor voltage increases from 1V to 1.8V. The start-up time will be dependent on the size of the external soft-start capacitor. The start-up time can be estimated by:

$$23\mu A * \frac{T_{start}}{C_{ss}} = 1.8V - 1V$$

For a given start up time, the soft-start capacitor (nF) can be estimated as:

$$C_{SS} \cong \frac{23(\mu A) * T_{start}(ms)}{0.8(V)} \qquad ----(5)$$

For normal start up the **Seq** pin should be pulled high (usually can be connected to Vout3).

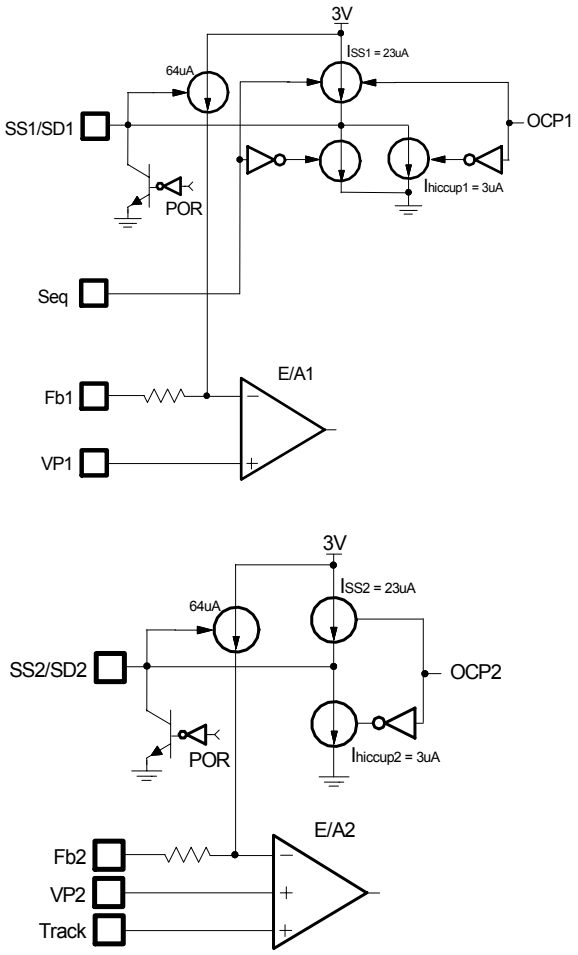


Fig. 7: Soft-Start circuit for IR3622A

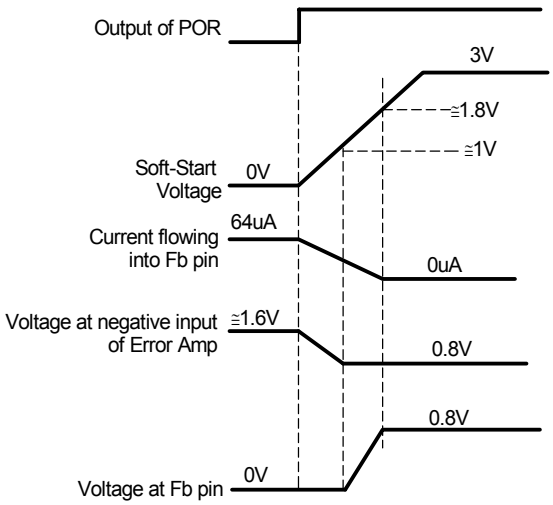


Fig. 8: Theoretical operation waveforms during soft-start

Output Voltage Tracking and Sequencing

The IR3622A can accommodate a full spectrum of user programmable tracking and sequencing options using Track, Seq, Enable and Power Good pins.

Through these pins both simple voltage tracking such as that required by the DDR memory application or more sophisticated sequencing such as ratiometric or simultaneous can be implemented.

The Seq pin controls the internal current sources to set the power up or down sequencing. Toggle this pin high for power up, and toggle this pin low for power down.

The Track pin is used to determine the second channel output for either ratiometric or simultaneous by using two external resistors. Figure 9 shows how these pins are configured for different sequencing mode.

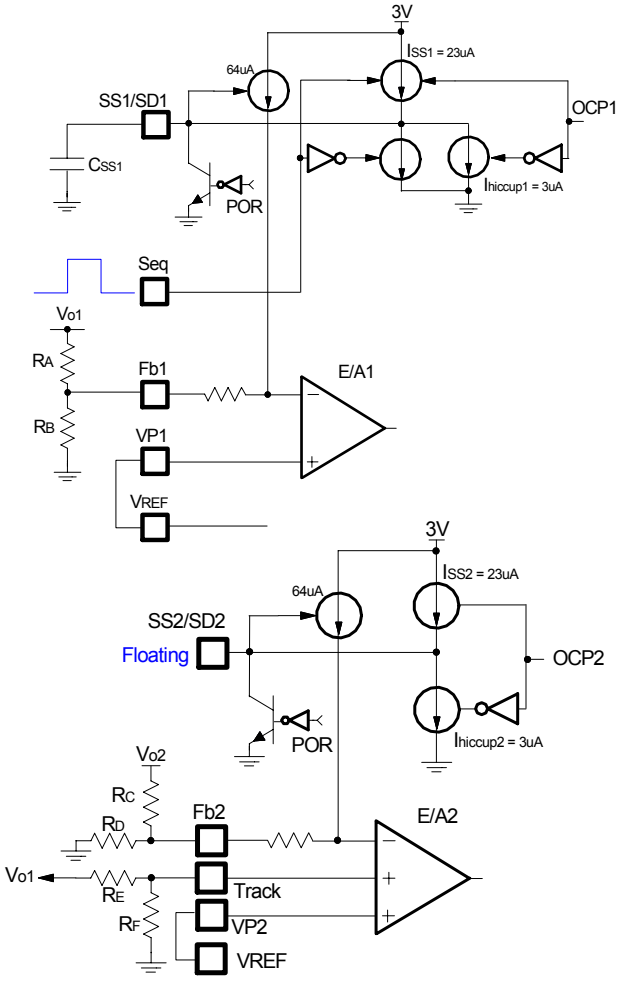


Fig. 9: Using Seq and Track pin for different sequencing

In general the R_A and R_B set the output voltage for the first output and R_C and R_D set the output voltage for the second output.

For simultaneous vs. ratiometric, RE and RF can be selected according to the table below:

Track Pin	
Simultaneously	$R_E=R_C$, $R_F=R_D$
Ratiometric	$R_E=R_A$, $R_F=R_B$

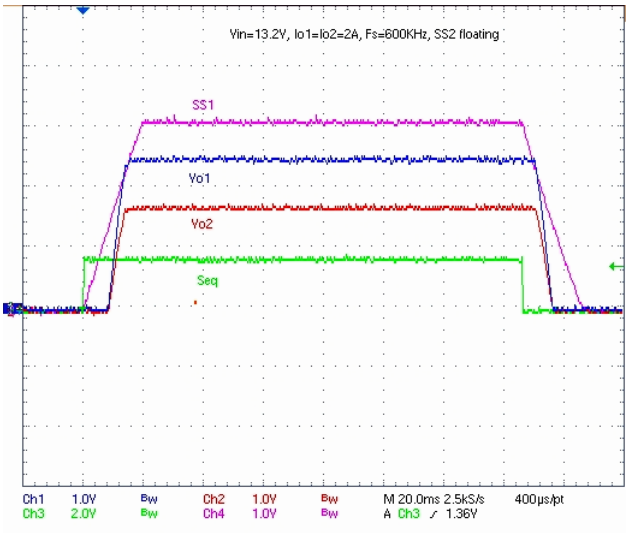


Fig. 10: Ratiometric Power Up / down

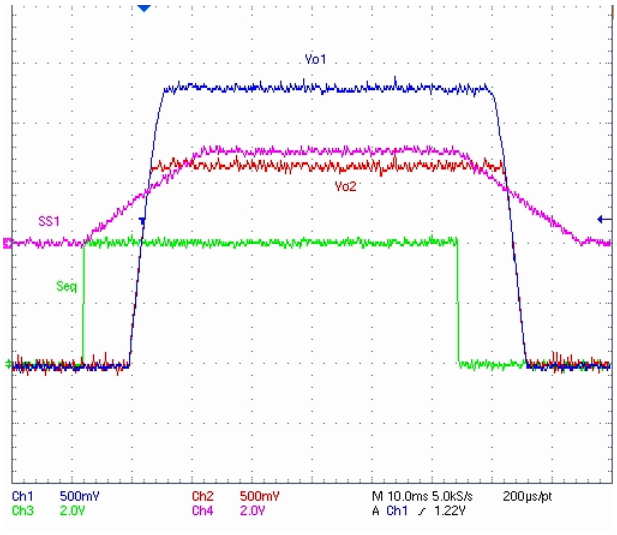


Fig. 11: Simultaneously Power up /down

Fault Protection

The IR3622A monitors the output voltage for over voltage protection and power good indication. It senses the $R_{ds(on)}$ of low side MOSFET for over current protection. It also protects the output for prebias conditions. Figure 12 shows the IC's operating waveforms under different fault conditions.

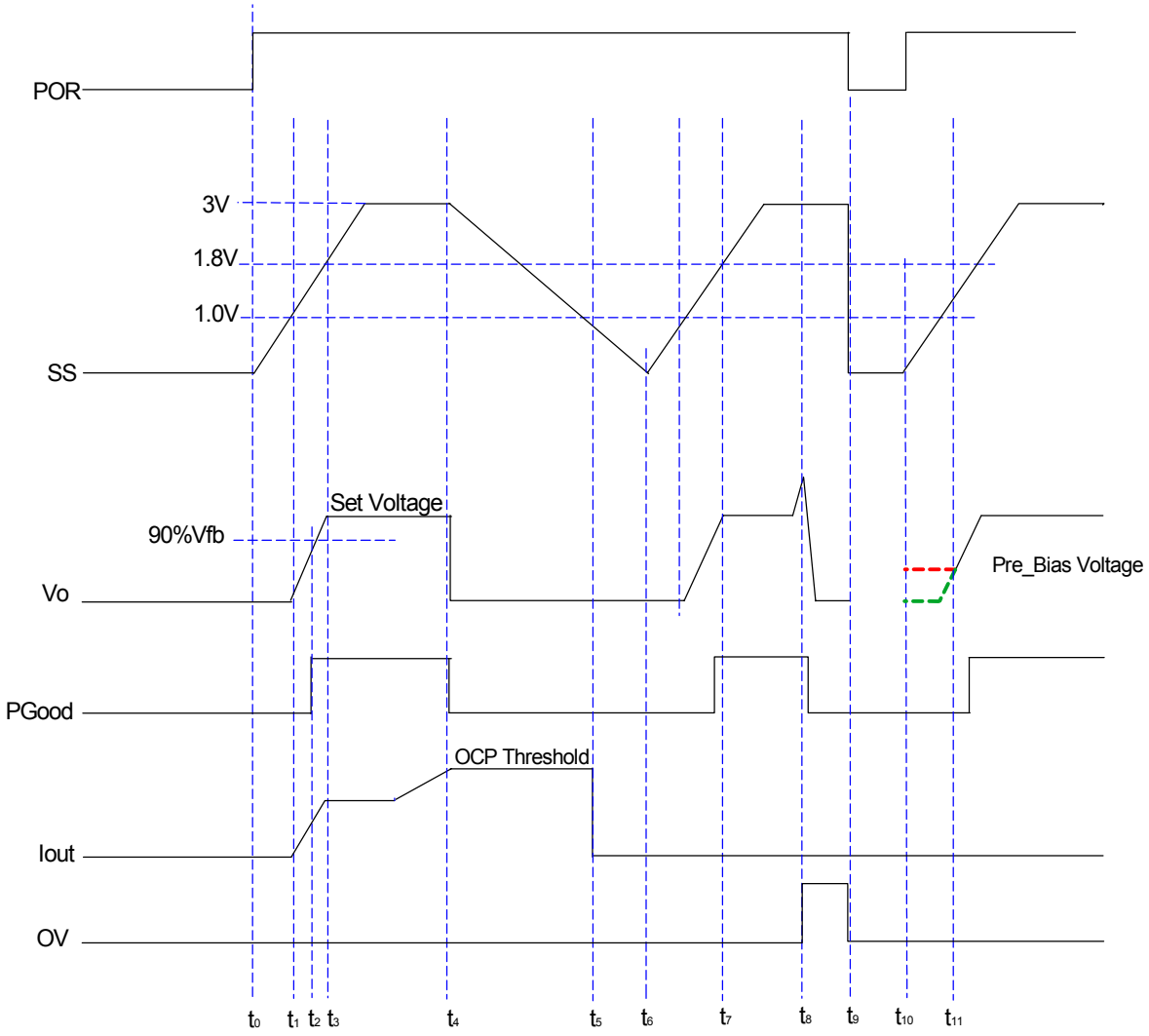


Fig. 12: Fault Conditions

$t_0 - t_1$: Vcc, VcH1,VcH2 and Enable signals passed their respective UVLO threshold. Soft start sequence starts.

$t_1 - t_2$: Power Good signal flags high.

$t_1 - t_3$: Output voltage ramps up and reaches the set voltage.

$t_4 - t_5$: OC event, SS ramps down. IC in Hiccup mode.

$t_5 - t_6$: OC is removed, recovery sequence, fresh SS.

$t_6 - t_7$: Output voltage reaches the set voltage.

t_8: OVP event. HDrv turns off and LDrv turns on. The IC latches off.

$t_9 - t_{10}$: Manually recycled the Vcc after latched OVP. PreBias start up.

$t_{10} - t_{11}$: New Soft Start sequence

Over-Current Protection

The over current protection is performed by sensing current through the $R_{ds(on)}$ of the low side MOSFET (Q2). This method enhances the converter's efficiency and reduce cost by eliminating a current sense resistor. As shown in figure 13, an external resistor (R_{SET}) is connected between the OCSet pin and the drain of Q2 which sets the current limit set point.

The internal current source develops a voltage across R_{SET}. When the Q2 is turned on, the inductor current flows through the Q2 and results in a voltage drop which is given by:

$$V_{OCSet} = (I_{OCSet} * R_{OCSet}) - (R_{ds(on)} * I_L) \quad ----(6)$$

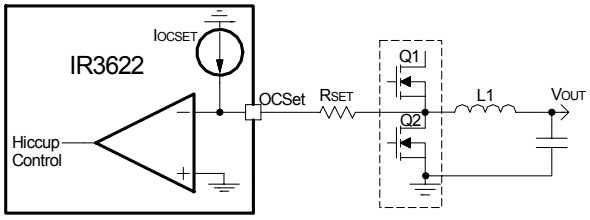


Fig. 13: Connection of over current sensing resistor

The critical inductor current can be calculated by setting:

$$V_{OCSet} = (I_{OCSet} * R_{OCSet}) - (R_{ds(on)} * I_L) = 0$$

$$I_{SET} = I_{L(critical)} = \frac{R_{OCSet} * I_{OCSet}}{R_{ds(on)}} \quad ----(7)$$

An over current is detected if the OCSet pin goes below ground. This trips the OCP comparator and cycles the soft start function in hiccup mode.

The hiccup is performed by charging and discharging the soft-start capacitor at a certain slope rate. As shown in figure 14 the 3uA current source is used to discharge the soft-start capacitor.

The OCP comparator resets after every soft start cycles, and the converter stays in this mode until the overload or short circuit is removed. The converter will automatically recover.

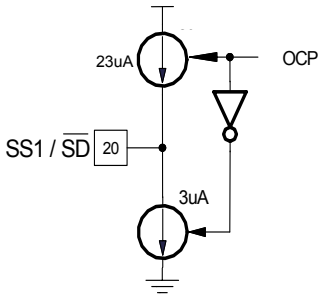


Fig. 14: 3uA current source for discharging soft-start capacitor during hiccup

The OCP circuit starts sampling current when the low gate drive is about 3V. The OCSet pin is internally clamped to approximately 1.4V during deadtime to prevent false trigging. Figure 15 shows the OCSet pin during one switching cycle. There is about 150ns delay to mask out the deadtime, since this node contains switching noise, this delay also functions as a filter.

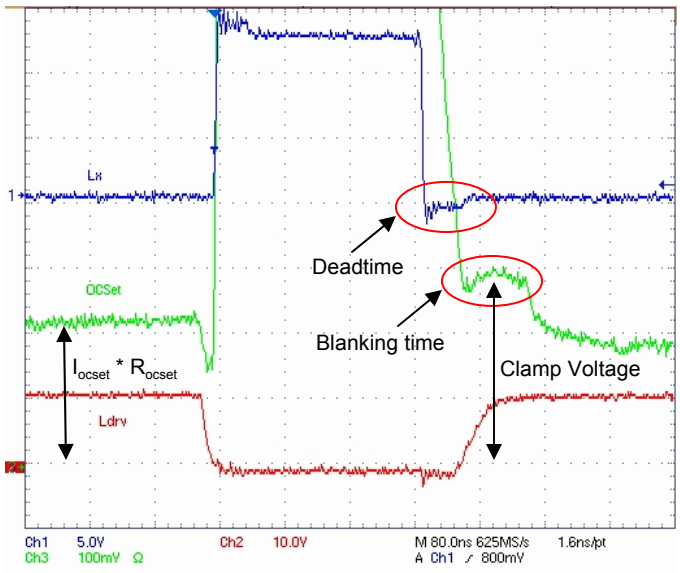


Fig. 15: OCset pin during normal condition
Ch1: Inductor point, Ch2:LDrv, Ch3:OCSet

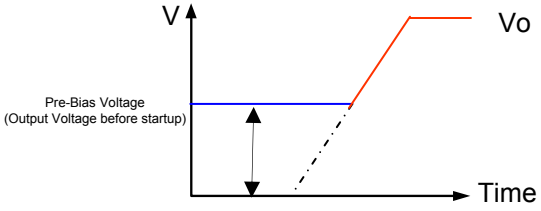
The value of R_{SET} should be checked in an actual circuit to ensure that the over current protection circuit activates as expected. The IR3622A current limit is designed primarily as short circuit protection, "no blow up" circuit, and doesn't operate as a precision current regulator.
When the SS2 is floating, an over current condition on either phase would result in hiccup current protection.

Pre-Bias

The IR3622A is able to start up into pre-charged output, which prevents oscillation and disturbances of the output voltage.

The output starts in asynchronous fashion and keeps the synchronous MOSFET off until the first gate signal for control MOSFET is generated. Figure below shows a typical Pre-Bias condition at start up.

Depending on system configuration, specific amount of output capacitance may be required to prevent discharging the output voltage.



Over Voltage Protection

Over-voltage is sensed through two dedicated sense pins V_{SEN1}, V_{SEN2}. A separate OVP circuit is provided for each channel.

The OVP threshold is user programmable and can be set by two external resistors. Upon over-voltage condition of either one of the outputs, the OVP forces a latched shutdown on the fault output. In this mode, the upper FET driver turns off and the lower FET drivers turn on, thus crowbaring the output. Reset is performed by recycling the Vcc or Enable.

Power Good

The IR3622A provides two separate open collector power good signals which report the status of the outputs. The outputs are sensed through the two dedicated V_{SEN1} and V_{SEN2} pins.

Once the IR3622A is enabled and the outputs reach the set value (90% of the Vout set point) the power good signals go open and stay open as long as the outputs stay within the set values. These pins need to be externally pulled high.

Shutdown using Soft Start pins

The outputs can be shutdown by pulling the soft-start pins below 0.3V. This can be easily done by using an external small signal transistor. During shutdown both MOSFET drivers will be turned off. Normal operation will resume by cycling soft start pin.

Operating Frequency Selection

The switching frequency is determined by connecting an external resistor (Rt) to ground. Figure 16 provides a graph of oscillator frequency versus Rt. The maximum recommended channel frequency is 600kHz.

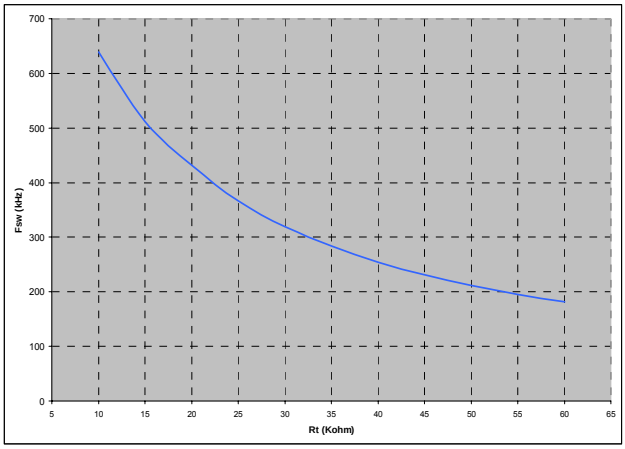


Fig. 16: Switching Frequency vs. External Resistor (R_t)

Frequency Synchronization

The IR3622A is capable of accepting an external digital synchronization signal. Synchronization will be enabled by the rising edge at an external clock. Per –channel switching frequency is set by external resistor (Rt). The free running frequency oscillator frequency is twice the per-channel frequency. During synchronization, Rt is selected such that the free running frequency is 20% below the synchronization frequency. Synchronization capability is provided for both single output current share mode and dual output configuration. The sync pin is noise immune, when unused it should be left floating.

Thermal Shutdown

Temperature sensing is provided inside IR3622A. The trip threshold is typically set to 140°C. When trip threshold is exceeded, thermal shutdown turns off both MOSFETs. Thermal shutdown is not latched and automatic restart is initiated when the sensed temperature drops to the normal range. There is a 20°C (typical) hysteresis in the shutdown threshold.

Application Information

Design Example:

The following is a design of typical single output current share application for IR3622A. The application circuit is shown on page 26.

$V_{in} = 12V, (\pm 10\%)$
$V_o = 1.8V$
$I_o = 40A$
$\Delta V_o \leq 30mV$
$F_s = 375kHz$

Output Voltage Programming

Output voltage is programmed by reference voltage and external voltage divider. As shown in figure 17 the Fb1 pin is the inverting input of the error amplifier, which is internally referenced to 0.8V. The divider is set to provide 0.8V at the Fb pin when the output is at its desired value. The output voltage is defined by the following equation:

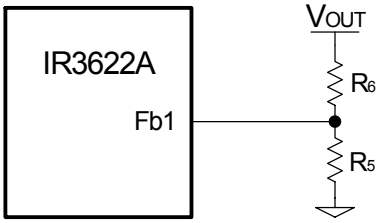


Fig. 17: Typical application of the IR3622A for programming the output voltage

$$V_o = V_{REF} * \left(1 + \frac{R_6}{R_5}\right) \quad ----(8)$$

Equation (8) can be rewritten as:

$$R_5 = R_6 * \left(\frac{V_{ref}}{V_o - V_{ref}}\right) \quad ----(9)$$

For the calculated values of R_5 and R_6 see feedback compensation section.

Soft-Start Programming

The soft-start timing can be programmed by selecting the soft-start capacitance value. The start-up time of the converter can be calculated using the following expression:

$$C_{SS}(nF) \cong 28.75(\mu A) * T_{start}(ms) \quad ----(10)$$

Where T_{start} is the desired start-up time (ms)
For a start-up time of 5ms, the soft-start capacitor will be 0.15uF. Choose a ceramic capacitor at 0.15uF.

Input Capacitor Selection

The 180º out of phase will reduce the RMS value of the ripple current seen by input capacitors. This reduces numbers of input capacitors. The input capacitors must be able to handle both the maximum ripple RMS current at the highest ambient temperature, as well as the maximum input voltage. The RMS value of current ripple for a duty cycle under 50% is expressed by:

$$I_{RMS} = \sqrt{\left(I_1^2 D_1(1-D_1) + I_2^2 D_2(1-D_2) - 2I_1 I_2 D_1 D_2\right)} \quad ----(11)$$

Where:
-I_{RMS} is the RMS value of the input capacitor current
-D_1 and D_2 are duty cycle for each channel
-I_1 and I_2 are the output current for each channel

For Io=40A and D=0.16 (1.8V/10.8V),
the I_{RMS}= 9.43A.

Ceramic capacitors are recommended due to their peak current capabilities. They also feature low ESR and ESL at higher frequency, which enhance circuit efficiency.
Use 10x22uF, 16V ceramic capacitor from TDK (C3225X5R1C226M).

For the single output application when the duty cycle is larger than 50% the following equation can be used to calculate the total RMS current for the input capacitor current:

$$I_{RMS} = I_o \sqrt{\left(2D(1-D) + (2-2D)\right)} \qquad D > 0.5$$

Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. Low inductor value results in large ripple current, smaller size, faster response to a load transient but poor efficiency and high output noise. Generally, the selection of inductor value can be reduced to desired maximum ripple current in the inductor (Δi) . The optimum point is usually found between 20% and 50% ripple of the output current.

For the buck converter, the inductor value for desired operating ripple current can be determined using the following relation:

$$V_{in} - V_o = L * \frac{\Delta i}{\Delta t};\quad \Delta t = D * \frac{1}{F_s}$$

$$L = (V_{in} - V_o) * \frac{V_o}{V_{in} * \Delta i * F_s} \qquad ----(12)$$

Where:

V_{in} = *Maximum input voltage*

V_o = *Output Voltage*

Δi = *Inductor ripple current*

F_s = *Switching frequency*

Δt = *Turn on time*

D = *Duty cycle*

For 2-phase single output application the inductor ripple current is chosen between 20-50% of maximum phase current

If $\Delta i \approx 50\%(I_o)$, then the output inductor will be:

L = 0.41uH

The Coilcraft MLC1260-401ML (L_1=0.4uH, 20A, R_{L1}=0.93mOhm) is a low profile inductor suitable for this application.
Use the following equation to calculate C_1 and R_1 for current sensing:
(refer to figure 6 on page 12)

$$R_1 * C_1 = \frac{L_1}{R_{L1}}$$

This results to C_1=1uF and R_1=0.432K

Output Capacitor Selection

The voltage ripple and transient requirements determine the output capacitors types and values. The criteria is normally based on the value of the Equivalent Series Resistance (ESR). However the actual capacitance value and the Equivalent Series Inductance (ESL) are other contributing factors. The overall output voltage ripple can be expressed as:

$$\Delta V_o = \Delta V_{o(ESR)} + \Delta V_{o(ESL)} + \Delta V_{o(C)}$$

where:

$$\Delta V_{o(ESR)} = \Delta I_L * ESR \qquad ----(13)$$

$$\Delta V_{o(ESL)} = \left(\frac{V_{in}}{L}\right) * ESL$$

$$\Delta V_{o(C)} = \frac{\Delta I_L}{8 * C_o * F_s}$$

ΔV_o = *Output voltage ripple*

ΔI_L = *Inductor ripple current*

Therefore it is recommended to select output capacitor with low enough ESR to meet output ripple and step load transient requirements.

The output ripple is highest at maximum input voltage since Δi increases with input voltage.

Special Polymer capacitors offers low ESR with large storage capacity per unit volume. These capacitors offer a cost effective output capacitor solution and are ideal choice when combined with a controller having high loop bandwidth.

The IR3622A can perform well with all types of capacitors.

Panasonic EEFSXOD221R (SP, 220F, 2V, 9mOhm) is selected for this design.

Equation (13) can be used to calculate the required ESR for the specific voltage ripple.

Four SP capacitors would meet the voltage ripple requirement.

Power MOSFET Selection

The IR3622A uses two N-Channel MOSFETs per channel. The selection criteria to meet power transfer requirements are based on maximum drain-source voltage (V_{DSS}), gate-source drive voltage (V_{gs}), maximum output current, On-resistance $R_{DS(on)}$, and thermal management.

The MOSFET must have a maximum operating voltage (V_{DSS}) exceeding the maximum input voltage (V_{in}).

The gate drive requirement is almost the same for both MOSFETs. Logic-level transistor can be used and caution should be taken with devices at very low gate threshold voltage (V_{gs}) to prevent undesired turn-on of the complementary MOSFET, which results a shoot-through current.

The total power dissipation for MOSFETs includes conduction and switching losses. For the Buck converter the average inductor current is equal to the DC load current. The conduction loss is defined as:

$$P_{cond} = (upperswitch) = I_{load}^2 * R_{ds(on)} * D * \vartheta$$

$$P_{cond} = (lowerswitch) = I_{load}^2 * R_{ds(on)} * (1-D) * \vartheta$$

$$\vartheta = R_{ds(on)}\ temperature\ \ dependency$$

The $R_{DS(on)}$ temperature dependency should be considered for the worst case operation. This is typically given in the MOSFET data sheet. Ensure that the conduction losses and switching losses do not exceed the package ratings or violate the overall thermal budget.

For this design, IRF6622 is selected for control FET and IRF6629 is selected for synchronous FET. These devices provide low on resistance in a compact Direct FET package.

The MOSFETs have the following data:

ControlFET(IRF6622):

$V_{ds} = 25V, Q_g = 18.7nC\ @10V_{gs}$

$R_{ds(on)} = 6.3m\Omega @ V_{gs} = 10V$

SyncFET(IRF6629):

$V_{ds} = 25V, Q_g = 51nC @ 10V_{gs}$

$R_{ds(on)} = 2.1m\Omega @ V_{gs} = 10V$

The conduction losses will be: P_{con}=1.1W/Phase

The switching loss is more difficult to calculate, even though the switching transition is well understood. The reason is the effect of the parasitic components and switching times during the switching procedures such as turn-on / turn-off delays and rise and fall times. The control MOSFET contributes to the majority of the switching losses in synchronous Buck converter. The synchronous MOSFET turns on under zero voltage conditions, therefore, the turn on losses for synchronous MOSFET can be neglected. With a linear approximation, the total switching loss can be expressed as:

$$P_{sw} = \frac{V_{ds(off)}}{2} * \frac{t_r + t_f}{T} * I_{load} \quad ---(13A)$$

Where:

$V_{ds(off)}$ = Drain to source voltage at the off time

t_r = Rise time

t_f = Fall time

T = Switching period

I_{load} = Load current

The switching time waveforms is shown in figure18.

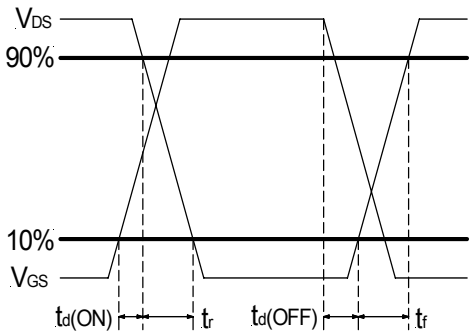


Fig. 18: switching time waveforms

From IRF6622 data sheet:

tr = 13ns

tf = 14ns

These values are taken under a certain condition test. For more details please refer to the IRF6622 data sheet.

By using equation (13A), we can calculate the switching losses. P_{sw}=2.8W

The reverse recovery loss is also another contributing factor in control FET switching losses. This is equivalent to extra current requires to remove the minority charges from synchronous FET. The reverse recovery loss can be expressed as:

$$P_{Qrr} = Q_{rr} * t_{rr} * F_s$$

Q_{rr} : ReverseRecoveryCharge

t_{rr} : ReverseRecoveryTime

F_s : SwitchingFrequency

Feedback Compensation

The IR3622A is a voltage mode controller; the control loop is a single voltage feedback path including error amplifier and error comparator. To achieve fast transient response and accurate output regulation, a compensation circuit is necessary. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency and adequate phase margin (greater than 45º).

The output LC filter introduces a double pole, –40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180º (see figure 19). The resonant frequency of the LC filter expressed as follows:

$$F_{LC} = \frac{1}{2*\pi\sqrt{L_o * C_o}} \quad ----(14)$$

Figure 19 shows gain and phase of the LC filter. Since we already have 180º phase shift just from the output filter, the system risks being unstable.

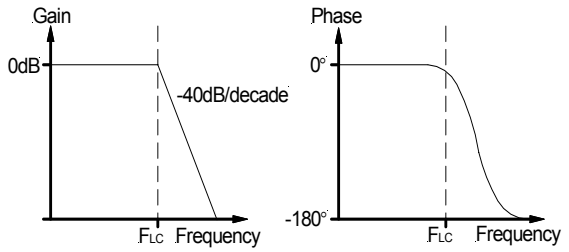


Fig. 19: Gain and Phase of LC filter

The IR3622A's error amplifier is a differential-input transconductance amplifier. The output is available for DC gain control and AC phase compensation.

The E/A can be compensated either in type II or type III compensation. When it is used in type II compensation the transconductance properties of the E/A become evident and can be used to cancel one of the output filter poles. This will be accomplished with a series RC circuit from Comp pin to ground as shown in figure 20.

This method requires that the output capacitor has enough ESR to satisfy stability requirements. In general the output capacitor's ESR generates a zero typically at 5kHz to 50kHz which is essential for an acceptable phase margin. The ESR zero of the output capacitor expressed as follows:

$$F_{ESR} = \frac{1}{2*\pi*ESR*C_o} \quad ----(15)$$

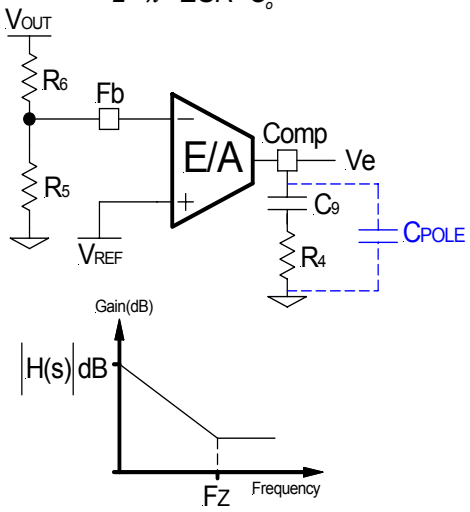


Fig. 20: TypeII compensation network and its asymptotic gain plot

The transfer function (Ve/Vo) is given by:

$$H(s) = \left(g_m * \frac{R_5}{R_5 + R_6}\right) * \frac{1 + sR_4C_9}{sC_9} \quad ----(16)$$

The (s) indicates that the transfer function varies as a function of frequency. This configuration introduces a gain and zero, expressed by:

$$[H(s)] = \left(g_m * \frac{R_5}{R_5 + R_6}\right) * R_4 \quad ----(17)$$

$$F_z = \frac{1}{2\pi * R_4 * C_9} \quad ----(18)$$

The gain is determined by the voltage divider and E/A's transconductance gain.
First select the desired zero-crossover frequency (Fo):

$$F_o > F_{ESR} \; and \; F_o \le (1/5 \sim 1/10) * F_s$$

Use the following equation to calculate R_4:

$$R_4 = \frac{V_{osc} * F_o * F_{ESR} * (R_5 + R_6)}{V_{in} * F_{LC}^2 * R_5 * g_m} \quad ----(19)$$

Where:
V_{in} = Maximum Input Voltage
V_{osc} = Oscillator Ramp Voltage
F_o = Crossover Frequency
F_{ESR} = Zero Frequency of the Output Capacitor
F_{LC} = Resonant Frequency of the Output Filter
g_m = Error Amplifier Transconductance

To cancel one of the LC filter poles, place the zero before the LC filter resonant frequency pole:

$$F_z = 75\%F_{LC}$$

$$F_z = 0.75 * \frac{1}{2\pi\sqrt{L_o * C_o}} \quad ----(20)$$

Using equations (18) and (20) to calculate C9.

$$C_9 = \frac{1}{2\pi * R_4 * F_z}$$

One more capacitor is sometimes added in parallel with C_9 and R_4. This introduces one more pole which is mainly used to suppress the switching noise.
The additional pole is given by:

$$F_P = \frac{1}{2\pi * R_4 * \frac{C_9 * C_{POLE}}{C_9 + C_{POLE}}}$$

The pole sets to one half of switching frequency which results in the capacitor C_{POLE}:

$$C_{POLE} = \frac{1}{\pi * R_4 * F_s - \frac{1}{C_9}} \cong \frac{1}{\pi * R_4 * F_s}$$

$$For\ F_P << \frac{F_s}{2}$$

For a general solution for unconditional stability for any type of output capacitors in a wide range of ESR values, we should implement local feedback with a compensation network (typeIII). The typically used compensation network for voltage-mode controller is shown in figure 21.

In such configuration, the transfer function is given by:

$$\frac{V_e}{V_o} = \frac{1 - g_m Z_f}{1 + g_m Z_{IN}}$$

The error amplifier gain is independent of the transconductance under the following condition:

$$g_m * Z_f >> 1 \ and \ \ g_m * Z_{in} >> 1 \quad ----(21)$$

By replacing Z_{in} and Z_f according to figure 15, the transformer function can be expressed as:

$$H(s) = \frac{1}{sR_6(C_{11} + C_{12})} * \frac{(1 + sR_7C_{11}) * [1 + sC_{10}(R_6 + R_8)]}{\left[1 + sR_7\left(\frac{C_{11} * C_{12}}{C_{11} + C_{12}}\right)\right] * (1 + sR_8C_{10})}$$

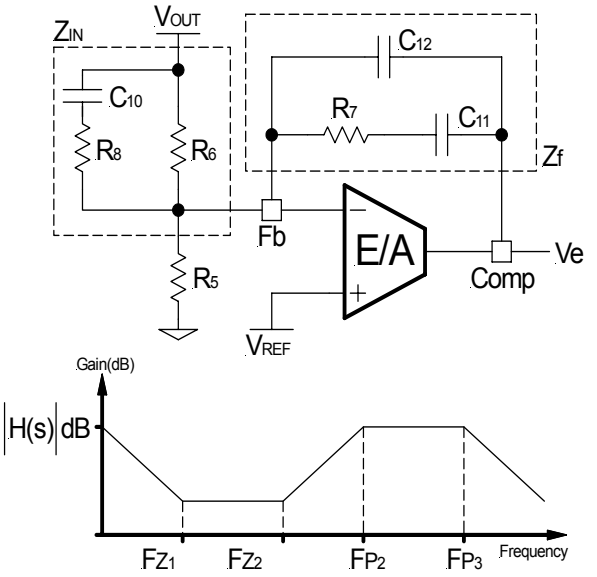


Fig. 21: Compensation network with local feedback and its asymptotic gain plot

As known, transconductance amplifier has high impedance (current source) output, which needs to be considered when loading the E/A output. If the source/sink output current capability is exceeded the amplifier will not be able to swing its output voltage over the necessary range.

The compensation network has three poles and two zeros and they are expressed as follows:

$$F_{P1} = 0$$

$$F_{P2} = \frac{1}{2\pi * R_8 * C_{10}}$$

$$F_{P3} = \frac{1}{2\pi * R_7\left(\frac{C_{11} * C_{12}}{C_{11} + C_{12}}\right)} \cong \frac{1}{2\pi * R_7 * C_{12}}$$

$$F_{z1} = \frac{1}{2\pi * R_7 * C_{11}}$$

$$F_{z2} = \frac{1}{2\pi * C_{10} * (R_6 + R_8)} \cong \frac{1}{2\pi * C_{10} * R_6}$$

Cross over frequency is expressed as:

$$F_o = R_7 * C_{10} * \frac{V_{in}}{V_{osc}} * \frac{1}{2\pi * L_o * C_o}$$

Based on the frequency of the zero generated by output capacitor and its ESR versus crossover frequency, the compensation type can be different. The table below shows the compensation types and location of crossover frequency.

Compensator type	F_{ESR} vs. F_o	Output capacitor
TypII(PI)	$F_{LC}<F_{ESR}<F_o<F_{s/2}$	Electrolytic , Tantalum
TypeIII(PID) **Method A**	$F_{LC}<F_o<F_{ESR}<F_{s/2}$	Tantalum, ceramic
TypeIII(PID) **Method B**	$F_{LC}<F_o<F_{s/2}<F_{ESR}$	Ceramic

Table1- The compensation type and location of F_{ESR} versus F_o

The details of these compensation types are discussed in application note AN-1043 which can be downloaded from IR Web-Site.

For this design we have:

V_{in}=13.2V
V_o=1.8V
V_{osc}=1.25V
V_{ref}=0.8V
g_m=3000umoh
L_o=0.4uH, DCR=0.930mOhm
C_o=4x220uF, ESR= 2.25mOhm
F_s=375kHz

These result in:

F_{LC}=12kHz

(Replace L to L/2 in formula#14 for current share configuration)

F_{ESR}=80.38kHz

$F_{s/2}$=185kHz

Select crossover frequency:

$F_o < F_{ESR}$ *and* $F_o \le (1/5 \sim 1/10) * F_s$

F_o=60kHz

Since: ***$F_{LC}<F_o<F_{ESR}<Fs/2$***, typeIII method A is selected to place the pole and zeros.

The following design rules will give a crossover frequency approximately one-sixth of the switching frequency. The higher the band width, the potentially faster the load transient response. The DC gain will be large enough to provide high DC-regulation accuracy (typically -5dB to -12dB). The phase margin should be greater than 45° for overall stability.

$$R_7 \ge \frac{2}{g_m}; R_7 \ge 0.67K\Omega; \quad Select: R_7 = 6.04K\Omega$$

Calculate C_{11}, C_{12} *and* C_{10} *:*

$$F_{Z1} = 0.75 * F_{LC}$$

$$C_{11} = \frac{1}{2\pi * F_{Z1} * R_7}; C_{11} = 2.90nF, \quad Select: \ C_{11} = 2.8nF$$

$$F_{P3} = F_s$$

$$C_{12} = \frac{1}{2\pi * F_{P3} * R_7}; C_{12} = 70pF, \quad Select: C_{12} = 56pF$$

$$C_{10} = \frac{2\pi * F_o * L_o * C_o * V_{osc}}{R_7 * V_{in}}; C_{10} = 1.03nF,$$

$$Select: C_{10} = 1.5nF$$

Calculate R_8, R_6 *and* R_5 *:*

$$R_8 = \frac{1}{2\pi * C_{10} * F_{P2}}; R_8 = 1.32K\Omega, \quad Select: R_8 = 1K\Omega$$

$$R_6 = \frac{1}{2\pi * C_{10} * F_{Z2}} - R_8; R_6 = 7.84K\Omega, \quad Select: R_6 = 7.87K\Omega$$

$$R_5 = \frac{V_{ref}}{V_o - V_{ref}} * R_6; R_5 = 6.30K\Omega, \quad Select: R_5 = 6.34K\Omega$$

Check:

$$R_8 \| R_6 \| R_5 \| > \frac{1}{gm} \qquad \frac{1}{gm} = 0.33K\Omega$$

$$0.78k\Omega > \frac{1}{gm} \quad OK!$$

If this condition is not met, then iteration may be required by selecting larger R_7.

Compensation for Current Loop (slave channel)

The slave error amplifier is differential transconductance amplifier, in 2-phase configuration the main goal for the slave channel feedback loop is to control the inductor current to match the master channel inductor current as well provides highest bandwidth and adequate phase margin for overall stability. The following analysis is valid for both using external current sense resistors and using DCR of the inductor.
The transfer function of power stage is expressed by:

$$G(s)=\frac{I_{L2}(s)}{V_e}=\frac{V_{in}}{sL_2*V_{osc}} \quad ----(22)$$

Where:
V_{in}=Input voltage
L_2=Output inductor
V_{osc}=Oscillator Peak Voltage

As shown the G(s) is a function of inductor current. The transfer function for compensation network is given by equation (23), when using a series RC circuit as shown in figure22.

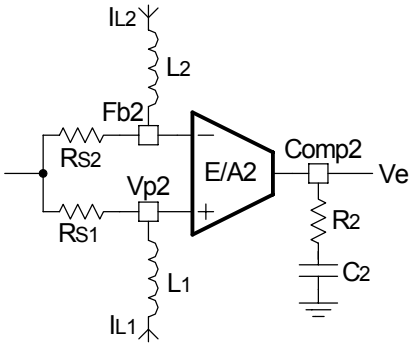


Fig. 22: The Compensation network for current loop

$$T(s)=\frac{V_e(s)}{R_{s2}}=\left(g_m*\frac{R_{s1}}{R_{s2}}\right)*\left(\frac{1+sC_2R_2}{sC_2}\right) \quad ----(23)$$

The loop gain function is:

$$H(s)=[G(s)*T(s)*R_{s2}]$$

$$H(s)=R_{s2}*\left(g_m*\frac{R_{s1}}{R_{s2}}\right)*\left(\frac{1+sR_2C_2}{sC_2}\right)*\left(\frac{V_{in}}{sL_2*V_{osc}}\right)$$

Select a zero frequency for current loop (F_{o2}) 1.2 times larger than zero cross frequency for voltage loop (F_{o1}).

$$F_{O2}\cong 1.25\%*F_{O1}$$

$$H(F_{O2})=g_m*R_{s1}*R_2*\frac{V_{in}}{2\pi*F_{O2}*L_2*V_{osc}}=1 \quad ----(24)$$

From (24), R2 can be expressed as:

$$R_2=\frac{1}{g_m*R_{s1}}*\frac{2\pi*F_{O2}*L_2*V_{osc}}{V_{in}} \quad ----(25)$$

V_{in}=13.2V
V_{osc}=1.25V
g_m=3000umoh
L_2=0.4uH
R_{s1}=DCR=0.930mOhm
F_{o2}=72kHz

This results to : R_2=6.14K
Select R_2=6.09K

The power stage of current loop has a dominant pole (Fp) at frequency expressed by:

$$F_P=\frac{R_{eq}}{2\pi*L_2}$$

$$R_{eq}=R_{ds(on1)}*D+R_{ds(on2)}*(1-D)+R_L$$

Where $R_{ds(on1)}$ is the on-resistance of control FET, $R_{ds(on2)}$ is the on-resistance of synchronous FET, R_L is the DCR of output inductance and D is the duty cycle

R_{eq}=3.7mOhm

Set the zero of compensator at 10 times the dominant pole frequency F_P, the compensator capacitor, C2 can be expressed as:

$$F_z=10*F_P$$

$$C_2=\frac{1}{2\pi*R_2*F_z}$$

C_2=1.8nF

All design should be tested for stability to verify the calculated values.

Programming the Current-Limit

The Current-Limit threshold can be set by connecting a resistor (R_{SET}) from drain of low side MOSFET to the OCSet pin. The resistor can be calculated by using equation (7).

The $R_{ds(on)}$ has a positive temperature coefficient and it should be considered for the worse case operation. This resistor must be placed close to the IC, place a small ceramic capacitor from this pin to ground for noise rejection purposes.

$$I_{SET} = I_{L(critical)} = \frac{R_{OCSet} * I_{OCSet}}{R_{ds(on)}} \quad ----(7)$$

$$R_{ds(on)} = 2.1m\Omega * 1.5 = 3.15m\Omega$$

$$I_{SET} \cong I_{o(LIM)} = 20A * 1.5 = 30A$$

(50% over nominal output current)

$$R_{OCSet} = R_3 = R_4 = 4K\Omega$$

Layout Consideration

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Start to place the power components, make all the connection in the top layer with wide, copper filled areas. The inductor, output capacitor should be close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place input capacitor close to control FETs, to reduce the ESR replace the single input capacitor with two parallel units. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC. In multilayer PCB use one layer as power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point. The exposed pad of IC should be connected to analog ground.

Typical Application

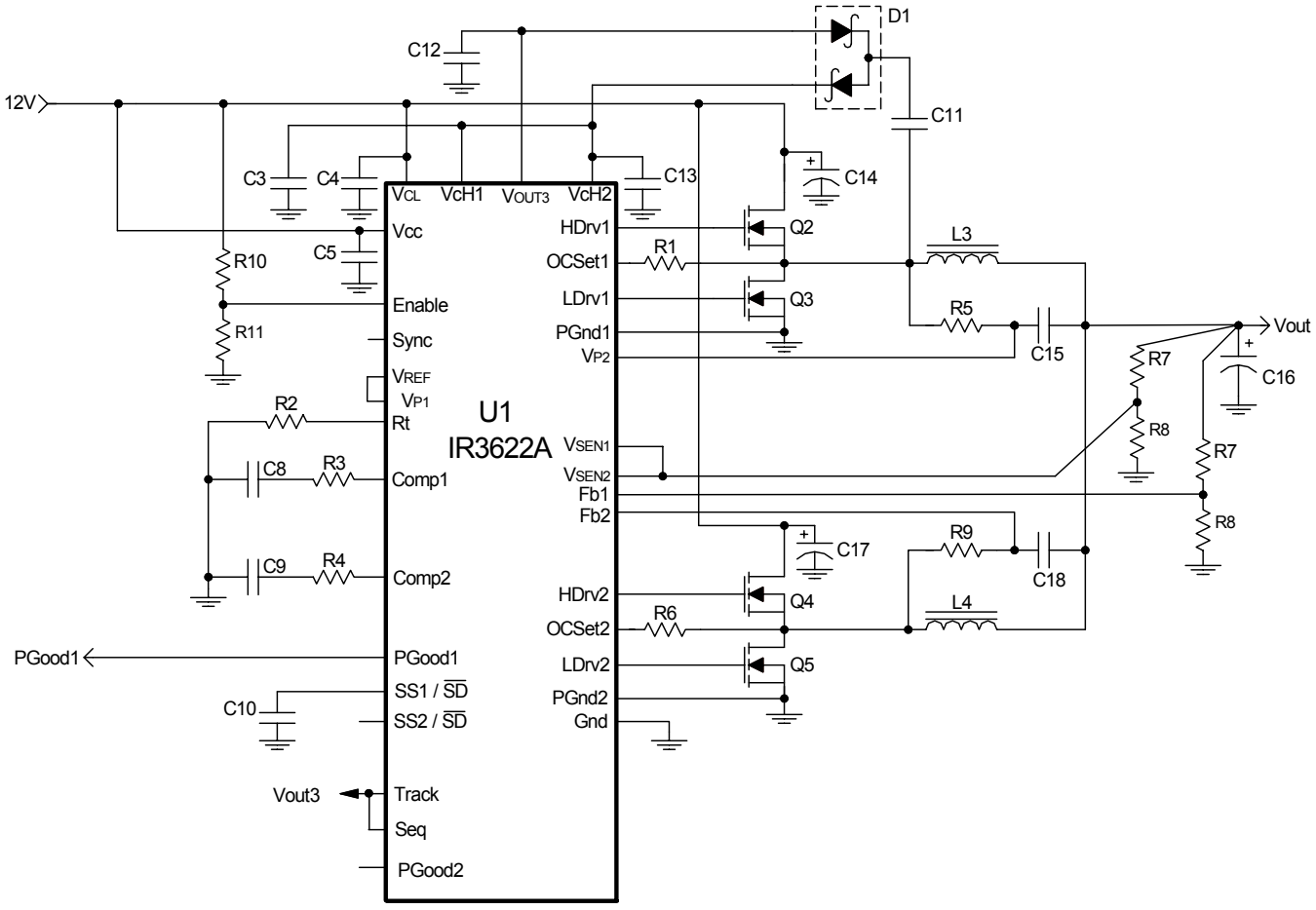


Fig. 23: Application circuit for 12V to 1.8V @ 40A

Note: To ensure correct start up Enable pin needs to be programmed (R10,R11) so the device turns on when the 12V rail is reached about 9-10V.

Typical Application

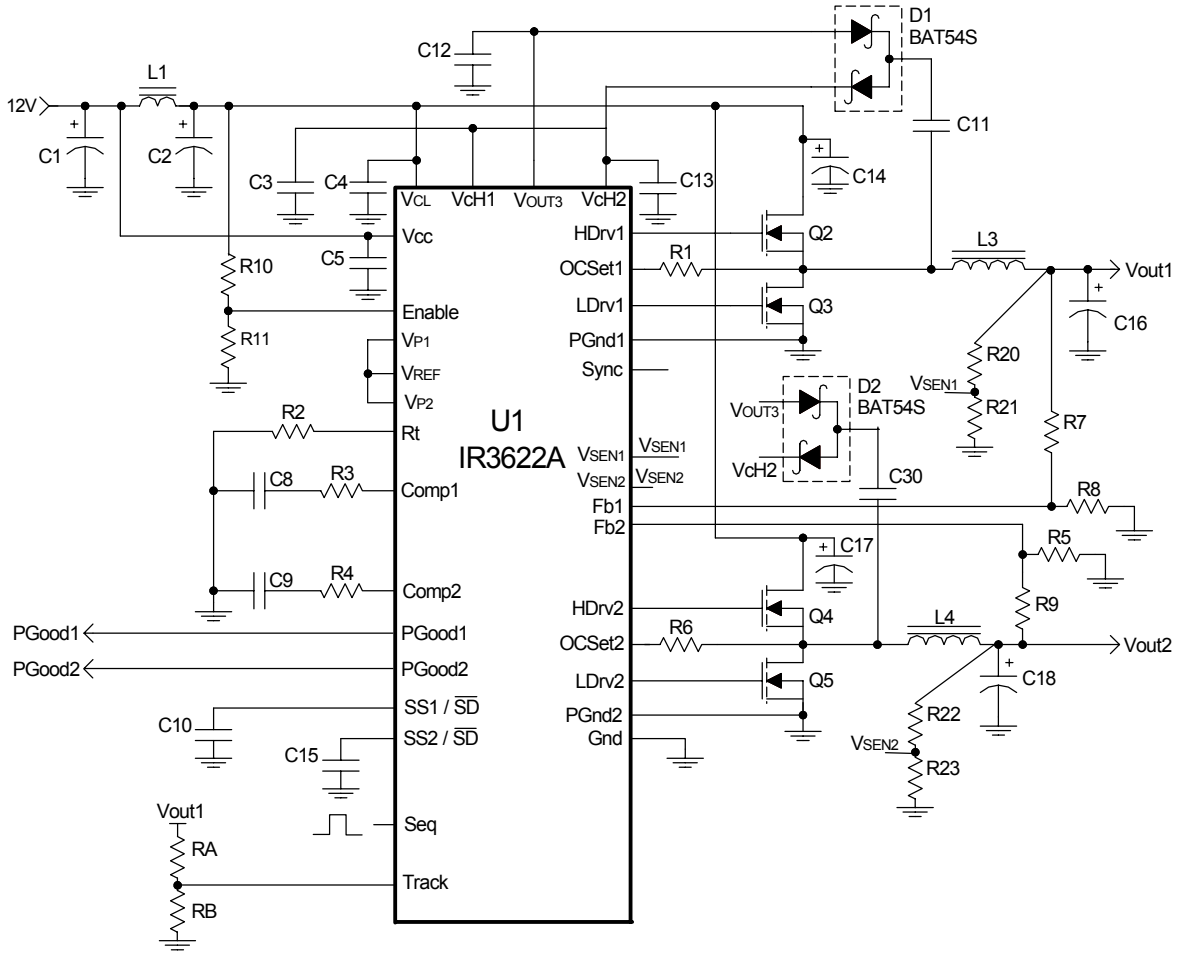


Fig. 24: Application circuit for Dual output application
Tracking and sequencing using Track pin

Note: To ensure correct start up Enable pin needs to be programmed (R10,R11) so the device turns on when the 12V rail is reached about 9-10V.

Track Pin	
Simultaneously	$R_A=R_9$, $R_B=R_5$
Ratiometric	$R_A=R_7$, $R_B=R_8$

Typical Application for Fully Buffered DIMM

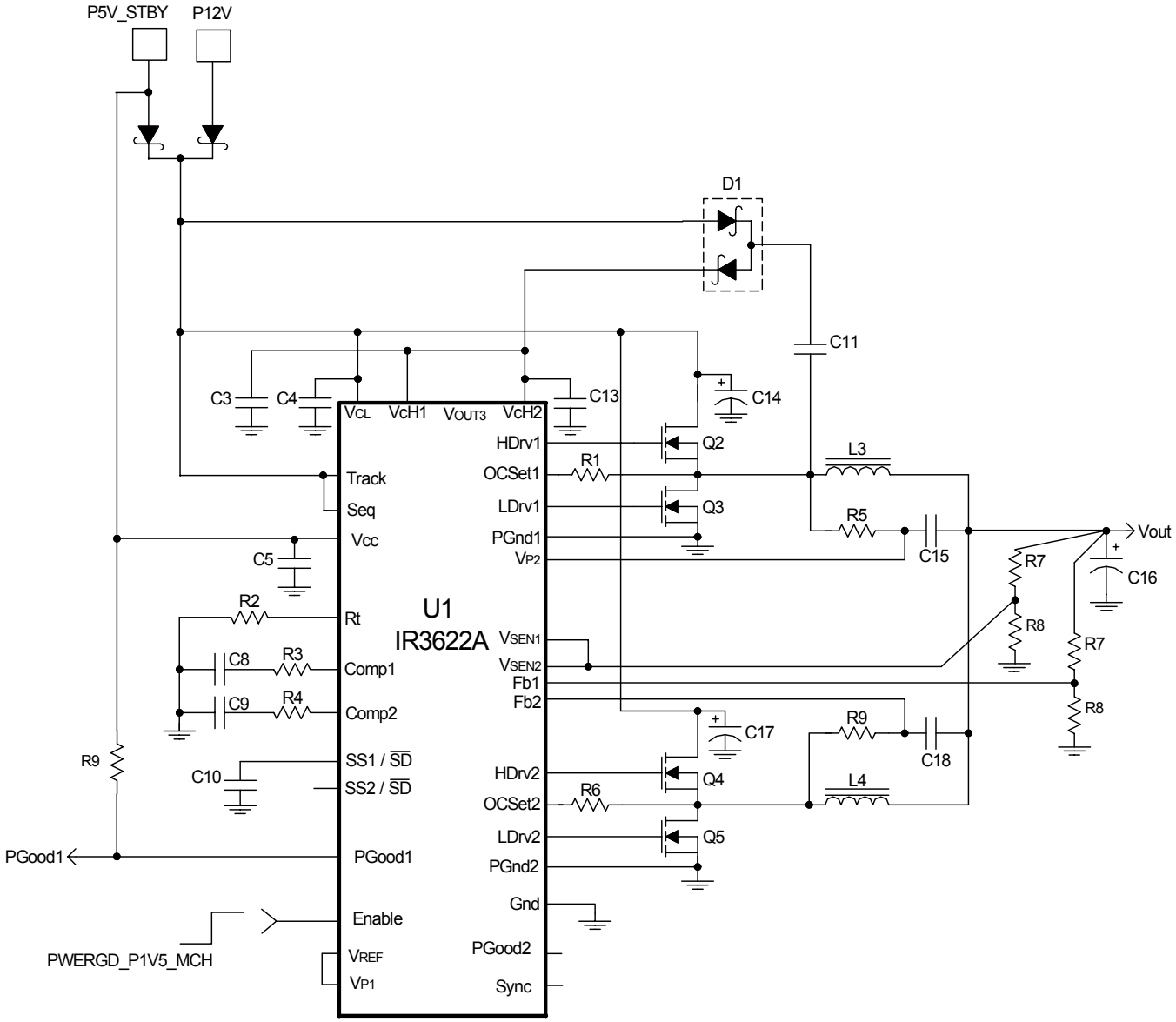


Fig. 25: Application circuit for FBD P1V8 VREG(40A)
P5V_P12V_STBY

Note: see Figure26 for start up/down waveforms

Typical start up /down waveforms for Fully Buffered DIMM

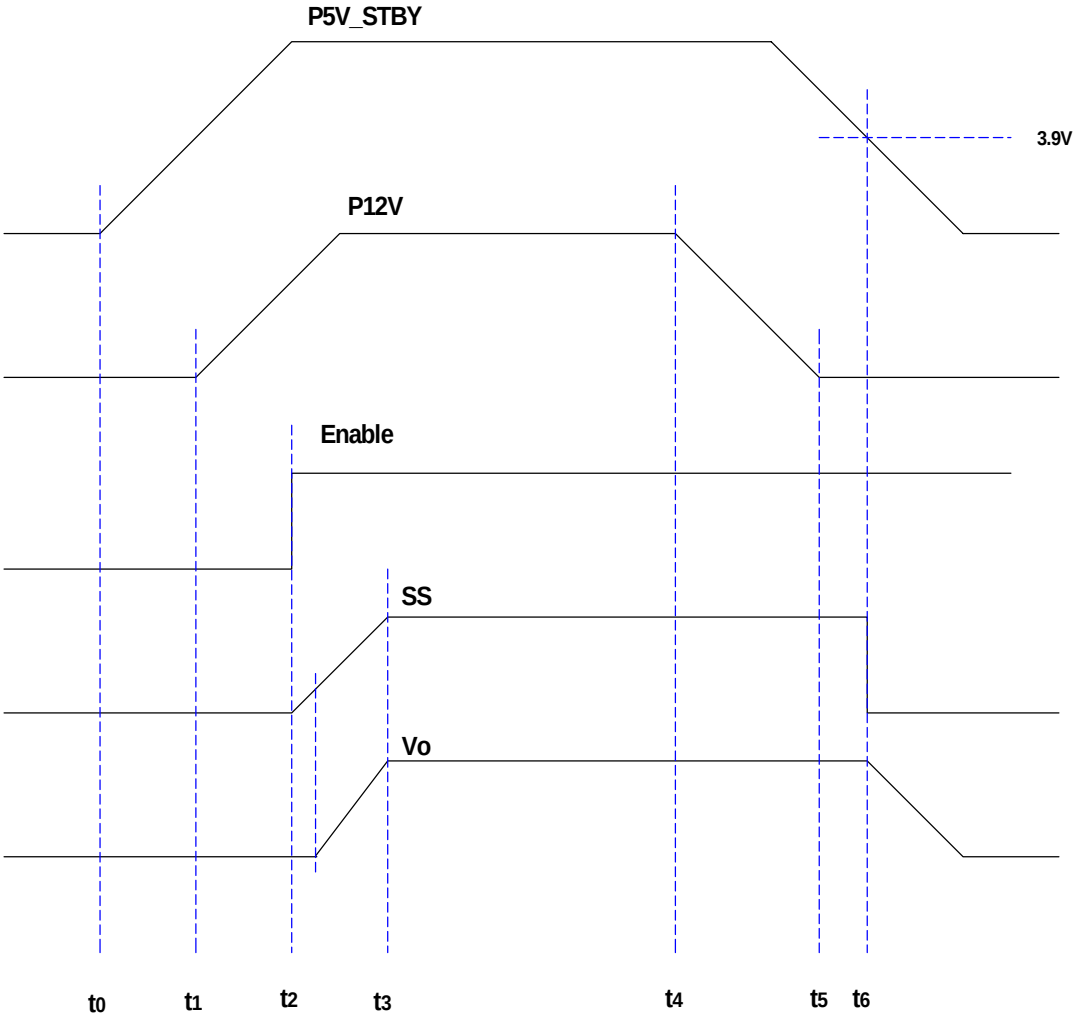


Fig. 26

t0: 5V standby ramps up
t1; 12V bus voltage ramps up
t2: Enable pin pulls high by Power Good Signal of P1V5_MCH regulator
t3: Soft start, Vo ramps up
t4: Vo reaches the set voltage
t4-t5: 12V rail shuts down, IC enters to standby mode (powered from 5V_STBY)
t6: 5V standby shuts down, Vcc<3.9V, IC shuts down

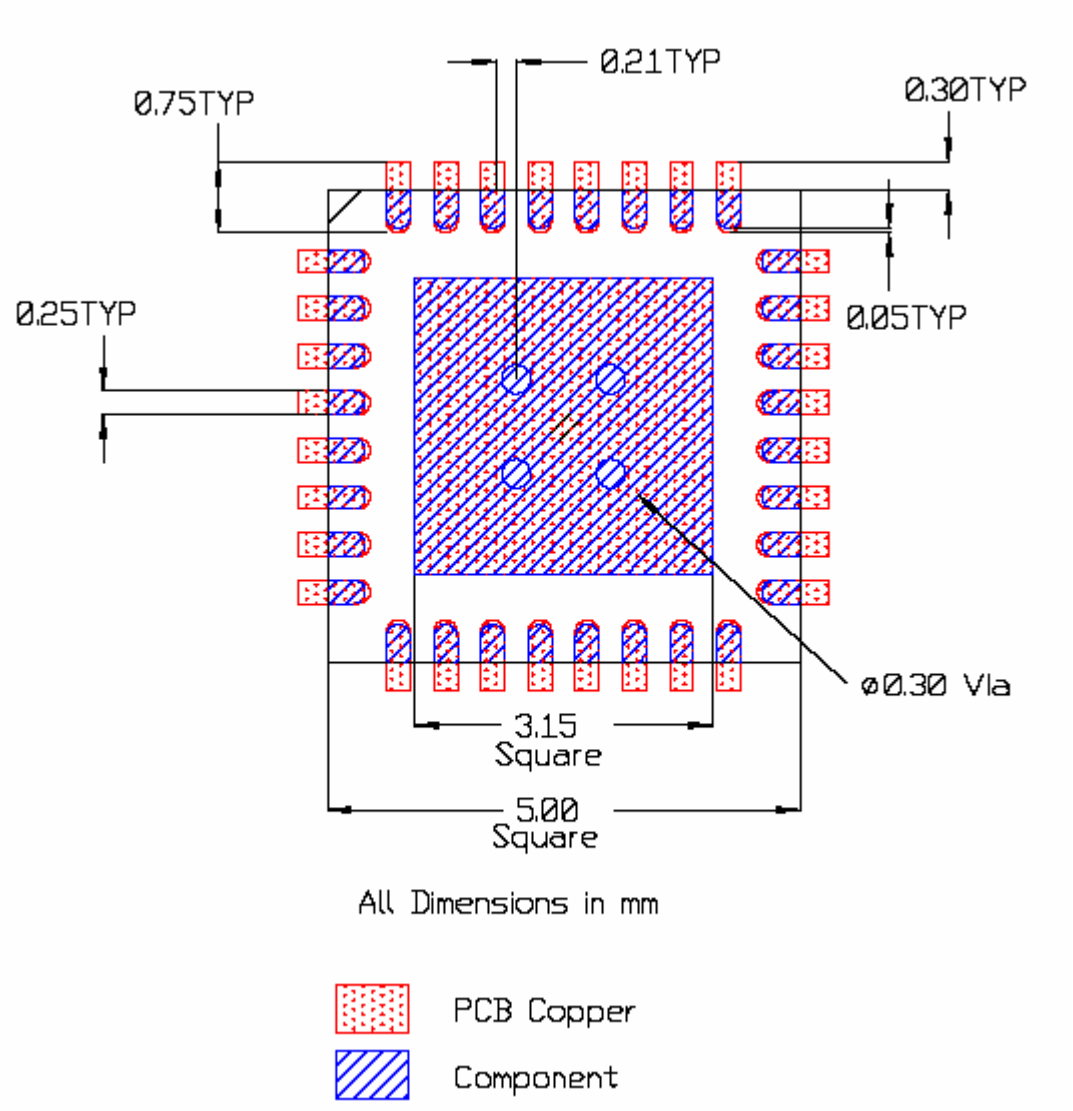
PCB Metal and Components Placement

▪ Lead land width should be equal to nominal part lead width. The minimum lead to lead spacing should be ≥ 0.2mm to minimize shorting.

▪ Lead land length should be equal to maximum part lead length + 0.3 mm outboard extension + 0.05mm inboard extension. The outboard extension ensures a large and inspectable toe fillet, and the inboard extension will accommodate any part misalignment and ensure a fillet.

▪ Center pad land length and width should be equal to maximum part pad length and width. However, the minimum metal to metal spacing should be ≥ 0.17mm for 2 oz. Copper (≥ 0.1mm for 1 oz. Copper and ≥ 0.23mm for 3 oz. Copper).

▪ A single 0.30mm diameter via shall be placed in the center of the pad land and connected to ground to minimize the noise effect on the IC.



Solder Resist

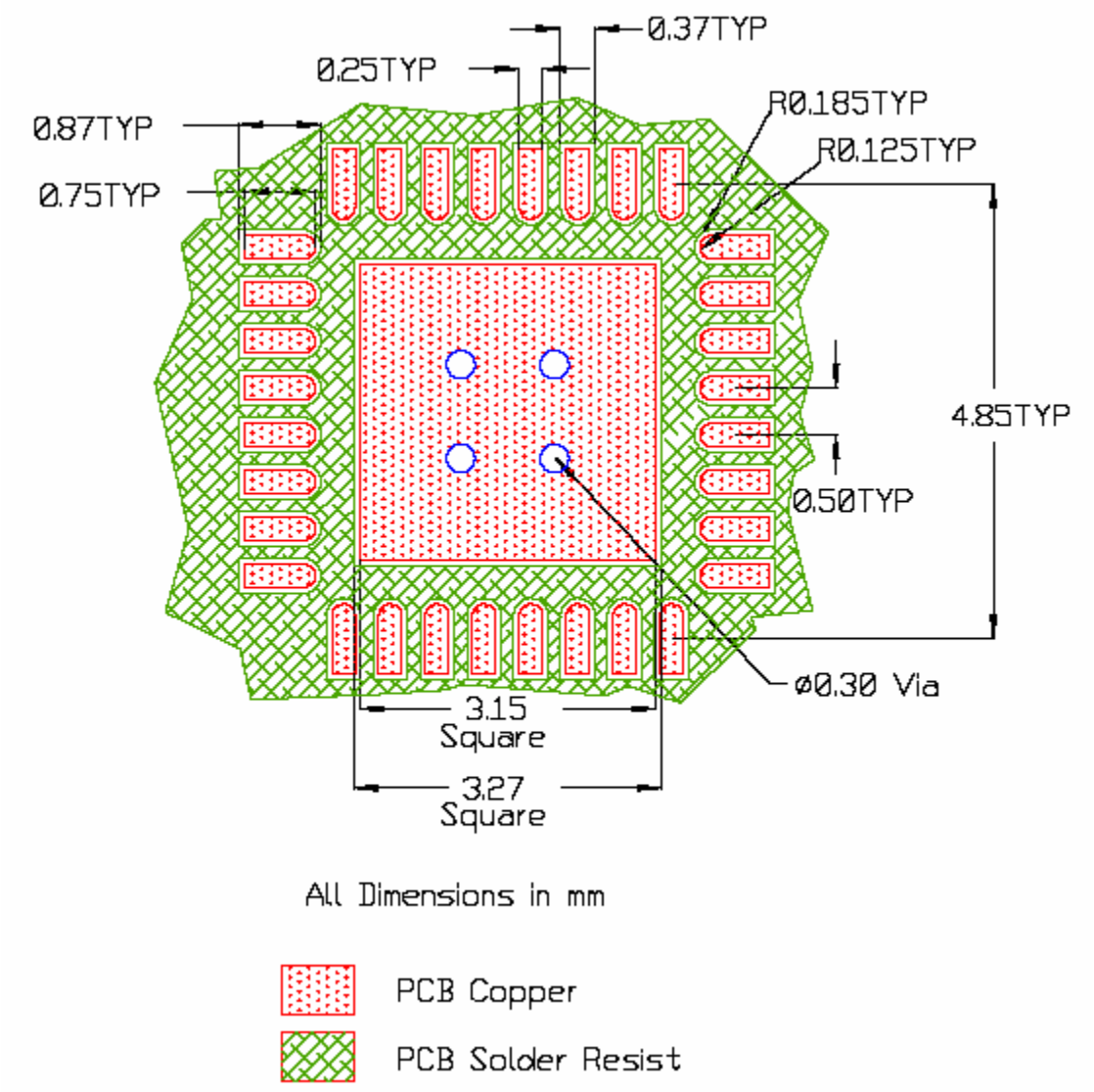
▪ The solder resist should be pulled away from the metal lead lands by a minimum of 0.06mm. The solder resist mis-alignment is a maximum of 0.05mm and it is recommended that the lead lands are all Non Solder Mask Defined (NSMD). Therefore pulling the S/R 0.06mm will always ensure NSMD pads.

▪ The minimum solder resist width is 0.13mm.
At the inside corner of the solder resist where the lead land groups meet, it is recommended to provide a fillet so a solder resist width of ≥ 0.17mm remains.

▪ The land pad should be Solder Mask Defined (SMD), with a minimum overlap of the solder resist onto the copper of 0.06mm to accommodate solder resist mis-alignment. In 0.5mm pitch cases it is allowable to have the solder resist opening for the land pad to be smaller than the part pad.

▪Ensure that the solder resist in-between the lead lands and the pad land is ≥ 0.15mm due to the high aspect ratio of the solder resist strip separating the lead lands from the pad land.

▪ The single via in the land pad should be tented or plugged from bottom boardside with solder resist.



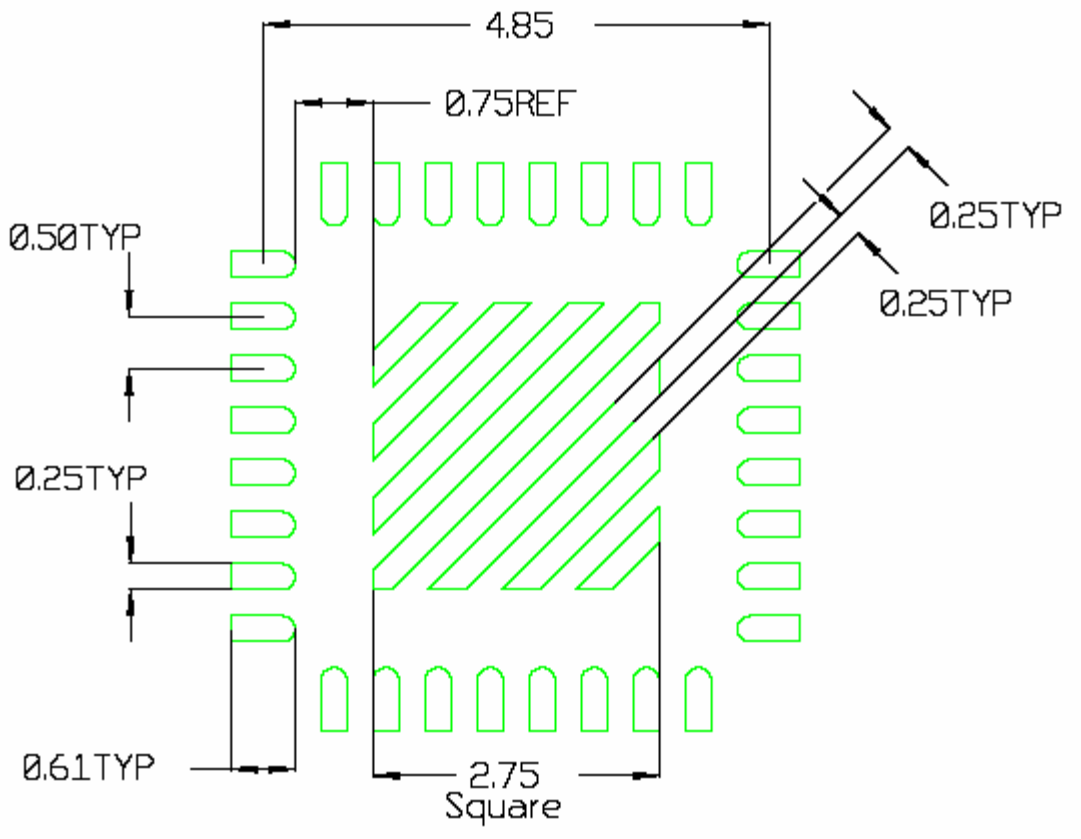
Stencil Design

▪ The stencil apertures for the lead lands should be approximately 80% of the area of the lead lands. Reducing the amount of solder deposited will minimize the occurrence of lead shorts. Since for 0.5mm pitch devices the leads are only 0.25mm wide, the stencil apertures should not be made narrower; openings in stencils < 0.25mm wide are difficult to maintain repeatable solder release.

▪ The stencil lead land apertures should therefore be shortened in length by 80% and centered on the lead land.

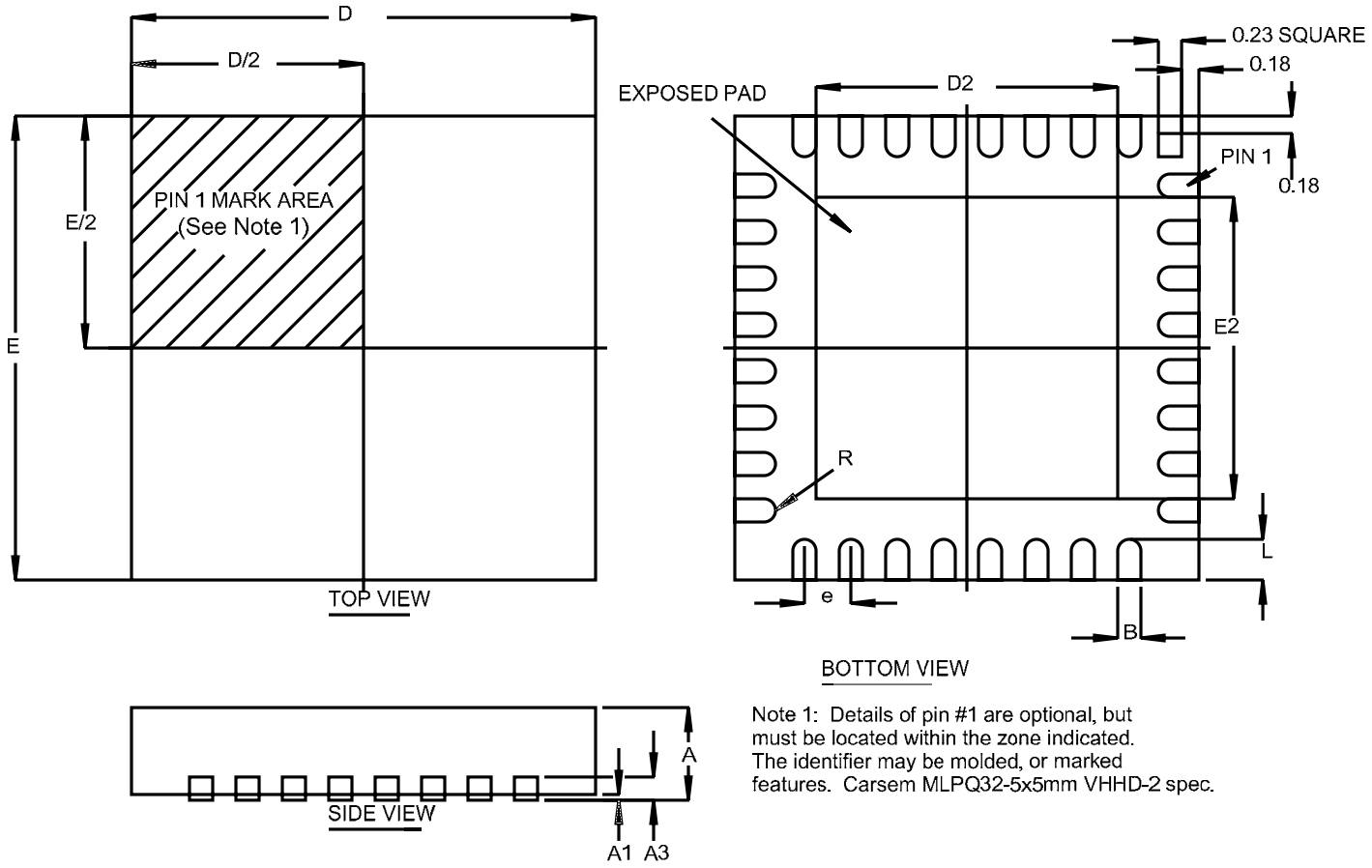
▪ The land pad aperture should be striped with 0.25mm wide openings and spaces to deposit approximately 50% area of solder on the center pad. If too much solder is deposited on the center pad the part will float and the lead lands will be open.

▪ The maximum length and width of the land pad stencil aperture should be equal to the solder resist opening minus an annular 0.2mm pull back to decrease the incidence of shorting the center land to the lead lands when the part is pushed into the solder paste.



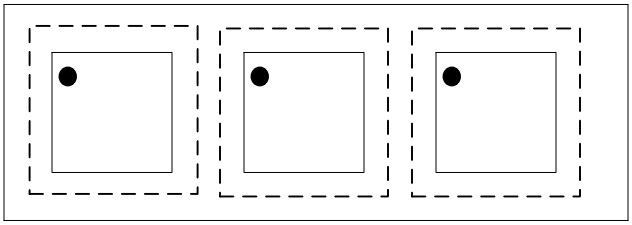
Stencil Aperture
All Dimensions In mm

(IR3622AM) MLPQ Package; 5x5-32 Lead



Note 1: Details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked features. Carsem MLPQ32-5x5mm VHHD-2 spec.

SYMBOL	32 PIN 5X5 MM		
DESIGN	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 REF	
B	0.18	0.23	0.30
D		5.00 BSC	
D2	3.00	3.15	3.25
E		5.00 BSC	
E2	3.00	3.15	3.25
e		0.50 BSC	
L	0.30	0.40	0.50
R	0.09	---	---



Feed Direction
Figure A

International
IOR Rectifier

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