Low Cost 6-Channel HD/SD Video Filter

ADA4420-6

FEATURES

Sixth-order filters
Transparent input sync tip clamp
−1 dB bandwidth of 26 MHz typical for HD
HD rejection @ 75 MHz: 48 dB typical
NTSC differential gain: 0.19%
NTSC differential phase: 0.76°
Rail-to-rail outputs
Low quiescent current: 32 mA typical
Disable feature
Output dc offset

APPLICATIONS

Set-top boxes
DVD players and recorders
HDTVs
Projectors
Personal video recorders

FUNCTIONAL BLOCK DIAGRAM

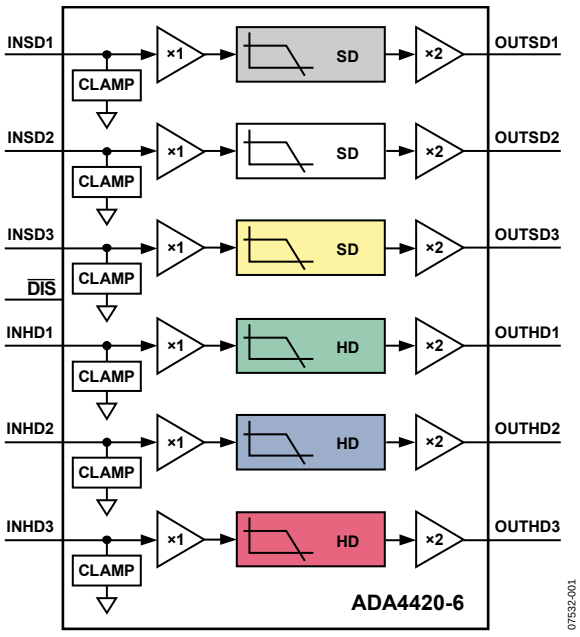

Figure 1.

GENERAL DESCRIPTION

The ADA4420-6 is a low cost video reconstruction filter specifically designed for consumer applications. It consists of six independent sixth-order Butterworth filters/buffers, three for standard definition (Y/C or CVBS) and three for high definition component signals (YPrPb or RGB).

The ADA4420-6 operates from a single 5 V supply and has a low quiescent current of 32 mA, making it ideal for applications where power consumption is critical. A disable feature allows for further power conservation by reducing the supply current to less than 8 µA typical when the device is not in use.

Each channel features a transparent sync tip clamp, allowing ac coupling of the inputs without requiring dc restoration.

The output drivers on the ADA4420-6 have rail-to-rail output capabilities with 6 dB gain. A built-in offset of 250 mV allows the outputs to be dc-coupled, eliminating the need for large coupling capacitors. Each output is capable of driving two 75 Ω doubly terminated cables.

The ADA4420-6 is available in either a 16-lead QSOP or a 20-lead TSSOP, and operates in the extended industrial temperature range of −40°C to +85°C.

Rev. A

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TABLE OF CONTENTS

REVISION HISTORY

5/11—Rev. 0 to Rev. A

Added 20-Lead TSSOP Package ..... Universal
Changes to General Description Section 1
Changes to Disable Assert Voltage, Disable Assert Time, Disable De-Assert Time Parameters 3
Changes to Table 3, Maximum Power Dissipation Section, and Figure 2 4
Added Figure 4 and Table 5 6
Changes to Figure 18, Figure 19, and Figure 20 10
Updated Outline Dimensions 13
Changes to Ordering Guide 14

8/08—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, V_O = 2.0 V p-p, R_L = 150 Ω, dc-coupled inputs, ac-coupled outputs, unless otherwise noted. See Figure 18, Figure 19, and Figure 20 for the test circuits.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL PERFORMANCE					
DC Voltage Gain	All channels	5.8	6.0	6.2	dB
Input Voltage Range, All Inputs			0 to 2.1		V
Output Voltage Range, All Outputs			0.25 to 4.6		V
Linear Output Current per Channel			30		mA
Filter Input Bias Current			1		µA
SD CHANNEL DYNAMIC PERFORMANCE					
−1 dB Bandwidth			8.6		MHz
−3 dB Bandwidth		8.5	10		MHz
Out-of-Band Rejection	f = 27 MHz	42	45		dB
Crosstalk	f = 1 MHz		−68		dB
Total Harmonic Distortion	f = 1 MHz, V_O = 1.4 V p-p, dc-coupled outputs		0.02		%
Signal-to-Noise Ratio	f = 100 kHz to 6 MHz, unweighted		70		dB
Propagation Delay			57		ns
Group Delay Variation	f = 100 kHz to 5 MHz		16		ns
Differential Gain	NTSC; ac-coupled inputs, dc-coupled outputs; see Figure 19		0.19		%
Differential Phase	NTSC; ac-coupled inputs, dc-coupled outputs; see Figure 19		0.76		Degrees
HD CHANNEL DYNAMIC PERFORMANCE					
−1 dB Bandwidth			26		MHz
−3 dB Bandwidth		27	31		MHz
Out-of-Band Rejection	f = 75 MHz	43	48		dB
Crosstalk	f = 1 MHz		−68		dB
Total Harmonic Distortion	f = 10 MHz, V_O = 1.4 V p-p, dc-coupled outputs		0.57		%
Signal-to-Noise Ratio	f = 100 kHz to 30 MHz, unweighted		66		dB
Propagation Delay			15		ns
Group Delay Variation	f = 100 kHz to 30 MHz		11		ns
DC CHARACTERISTICS					
Operating Voltage			4.75 to 5.25		V
Quiescent Supply Current	Active, $\overline{DIS}$ = 1		32	36	mA
	Disabled, $\overline{DIS}$ = 0		7	13	µA
PSRR	HD channel, referred to output	35	41		dB
	SD channel, referred to output	40	45		dB
Output DC Offset	All channels	135	250	375	mV
Disable Assert Voltage	$\overline{DIS}$ = 0 to 1			1.9	V
Disable Assert Time	$\overline{DIS}$ = 0 to 1		20		ns
Disable De-Assert Time	$\overline{DIS}$ = 1 to 0		450		ns
Disable Input Bias Current	Disabled, $\overline{DIS}$ = 0		−6.8		µA
Input-to-Output Isolation	Disabled, $\overline{DIS}$ = 0, f = 5 MHz		−96		dB

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	5.5 V
Power Dissipation	See Figure 2
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device soldered to a high thermal conductivity 4-layer (2s2p) circuit board, as described in EIA/JESD 51-7.

Table 3.

Package Type	θ_{JA}	θ_{JC}	Unit
16-Lead QSOP	105	23	°C/W
20-Lead TSSOP	143	45	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADA4420-6 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4420-6. Exceeding a junction temperature of 150°C for an extended time can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to load drive depends on the particular application. For each output, the power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. The power dissipated due to the loads is equal to the sum of the power dissipations due to each individual load. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA}. Figure 2 shows the maximum power dissipation in the package vs. the ambient temperature for the 16-lead QSOP (105°C/W) and the 20-lead TSSOP (143°C/W) on a JEDEC standard 4-layer board. θ_{JA} values are approximate.

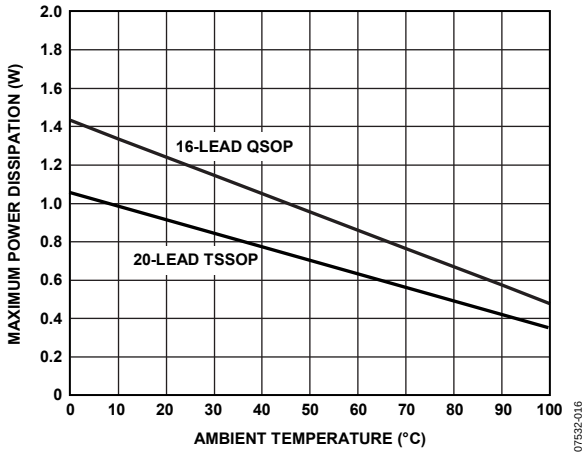


Figure 2. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

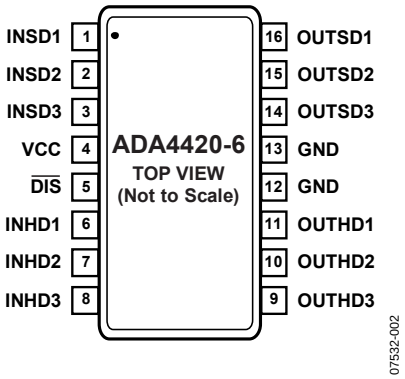


Figure 3. 16-Lead QSOP Pin Configuration

Table 4. 16-Pin QSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INSD1	Standard Definition Input 1
2	INSD2	Standard Definition Input 2
3	INSD3	Standard Definition Input 3
4	VCC	Power Supply
5	$\overline{\text{DIS}}$	Disable/Power-Down Input
6	INHD1	High Definition Input 1
7	INHD2	High Definition Input 2
8	INHD3	High Definition Input 3
9	OUTHD3	High Definition Output 3
10	OUTHD2	High Definition Output 2
11	OUTHD1	High Definition Output 1
12	GND	Ground
13	GND	Ground
14	OUTSD3	Standard Definition Output 3
15	OUTSD2	Standard Definition Output 2
16	OUTSD1	Standard Definition Output 1

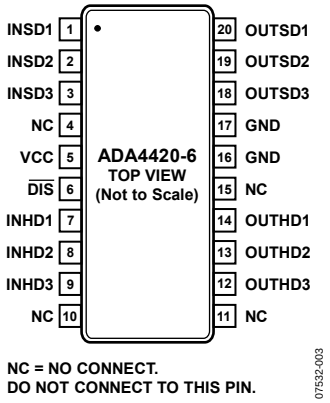


Figure 4. 20-Lead TSSOP Pin Configuration

Table 5. 20-lead TSSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INSD1	Standard Definition Input 1.
2	INSD2	Standard Definition Input 2.
3	INSD3	Standard Definition Input 3.
4	NC	Do not connect to this pin.
5	VCC	Power Supply.
6	$\overline{DIS}$	Disable/Power Down Input.
7	INHD1	High Definition Input 1.
8	INHD2	High Definition Input 2.
9	INHD3	High Definition Input 3.
10	NC	Do not connect to this pin.
11	NC	Do not connect to this pin.
12	OUTHD3	High Definition Output 3.
13	OUTHD2	High Definition Output 2.
14	OUTHD1	High Definition Output 1.
15	NC	No Connection.
16	GND	Ground.
17	GND	Ground.
18	OUTSD3	Standard Definition Output 3.
19	OUTSD2	Standard Definition Output 2.
20	OUTSD1	Standard Definition Output 1.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, V_O = 2.0 V p-p, R_L = 150 Ω, dc-coupled inputs, ac-coupled outputs, unless otherwise noted. See Figure 18, Figure 19, and Figure 20 for the test circuits.

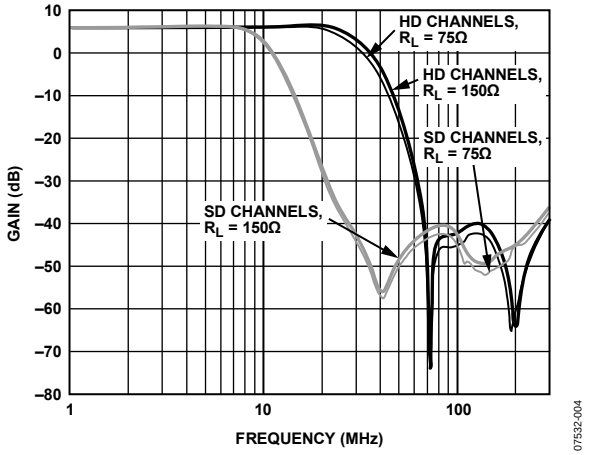


Figure 5. Frequency Response vs. Load (R_L)

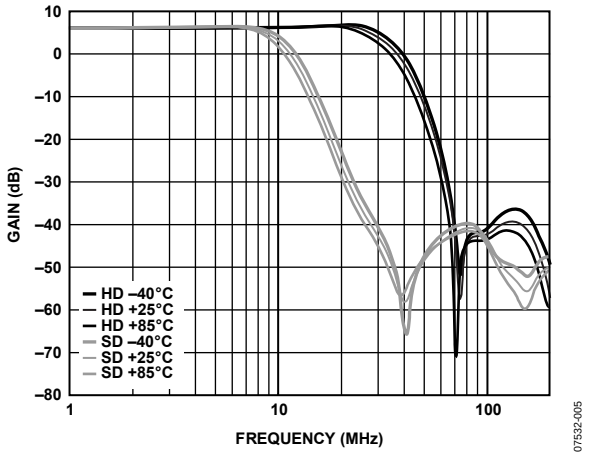


Figure 6. Frequency Response vs. Temperature

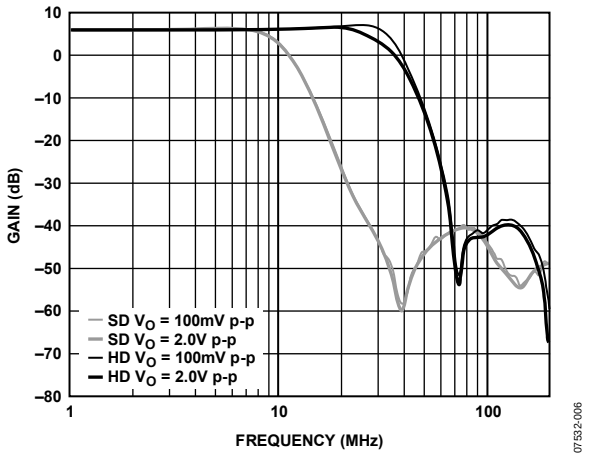


Figure 7. Frequency Response vs. Amplitude

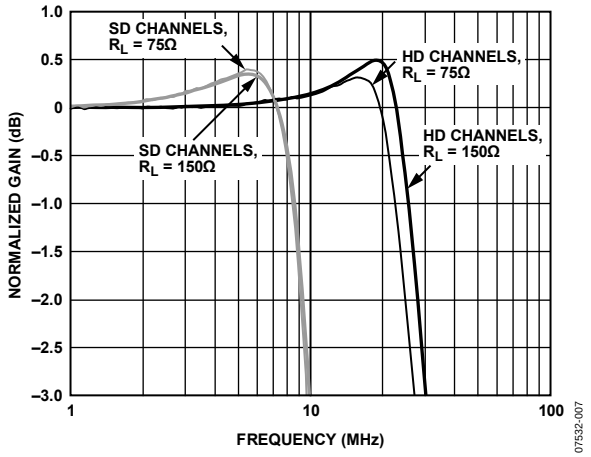


Figure 8. Flatness vs. Load (R_L)

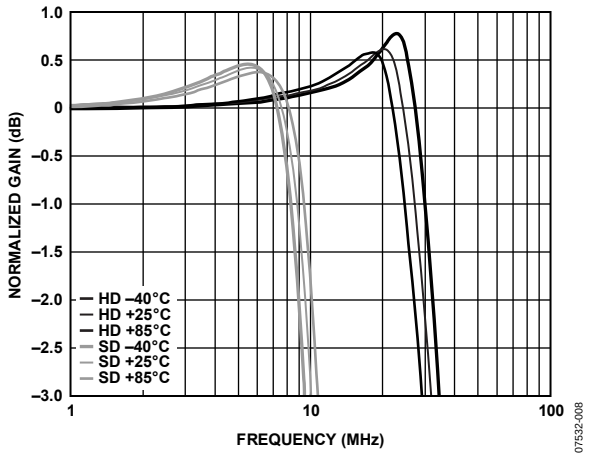


Figure 9. Flatness vs. Temperature

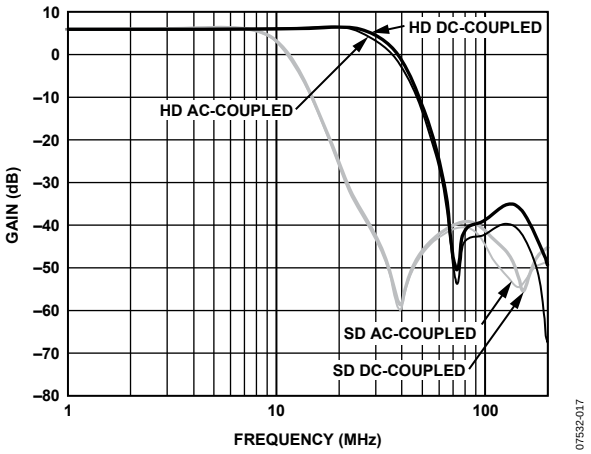


Figure 10. Frequency Response vs. Output Coupling

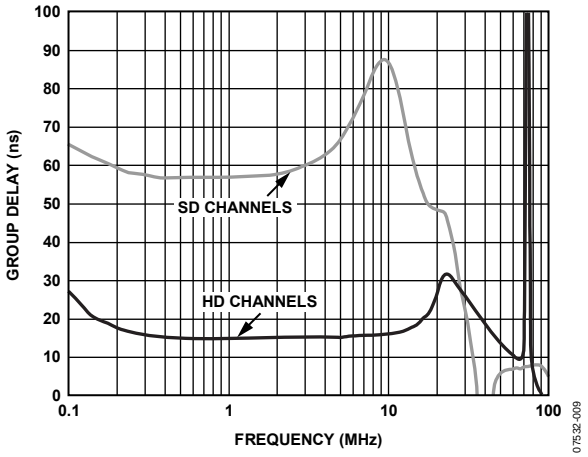


Figure 11. Group Delay vs. Frequency

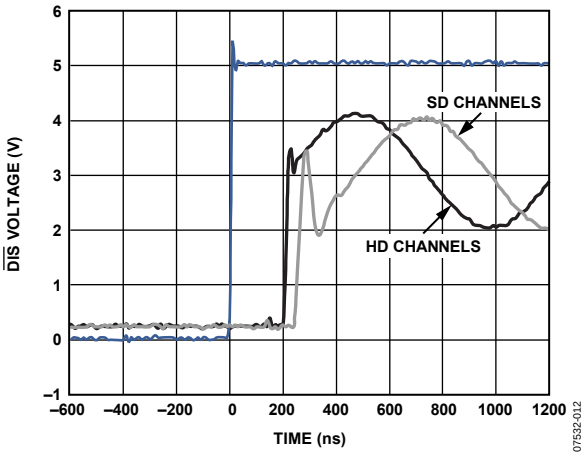


Figure 13. Enable Time

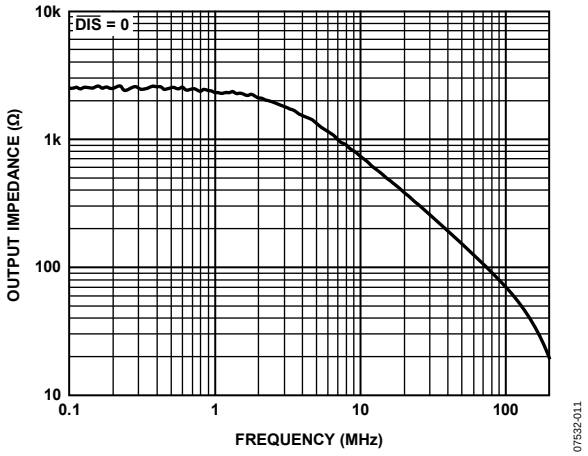


Figure 12. Output Impedance vs. Frequency

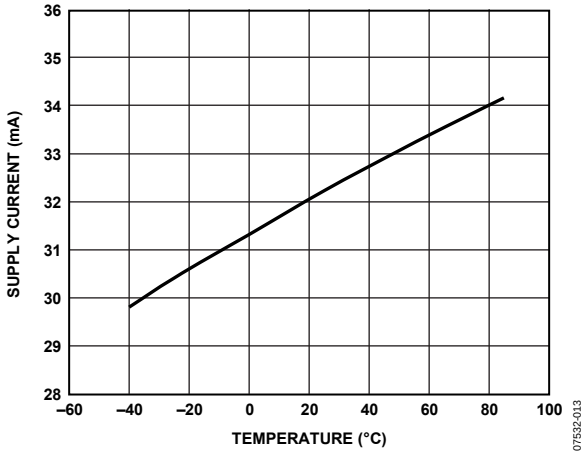


Figure 14. Supply Current vs. Temperature

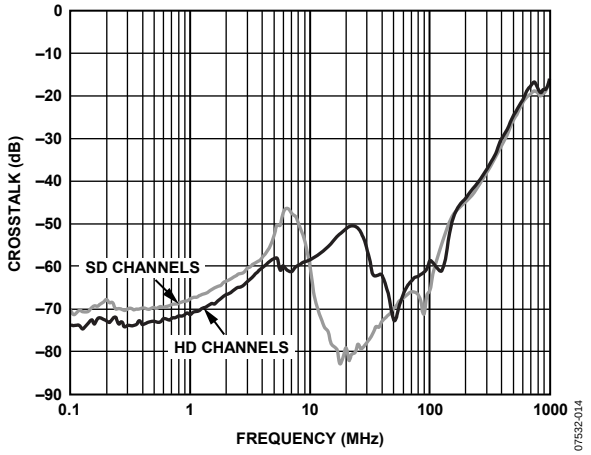


Figure 15. Crosstalk vs. Frequency

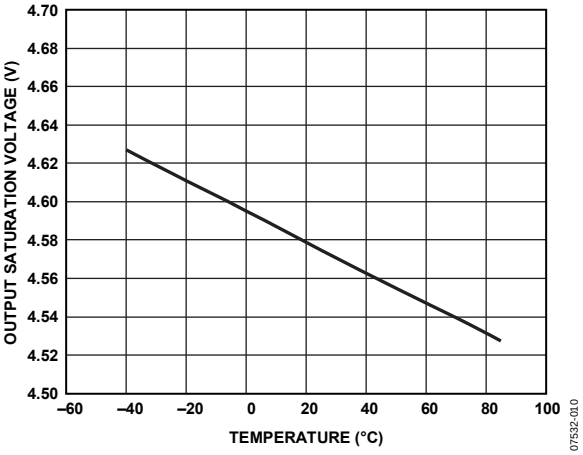


Figure 17. Output Saturation Voltage vs. Temperature

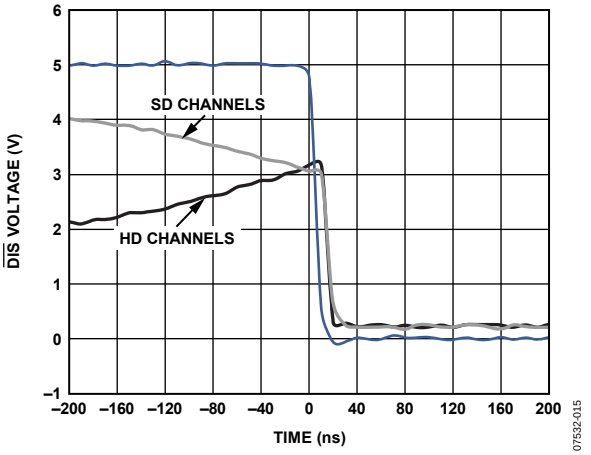


Figure 16. Disable Time

TEST CIRCUITS

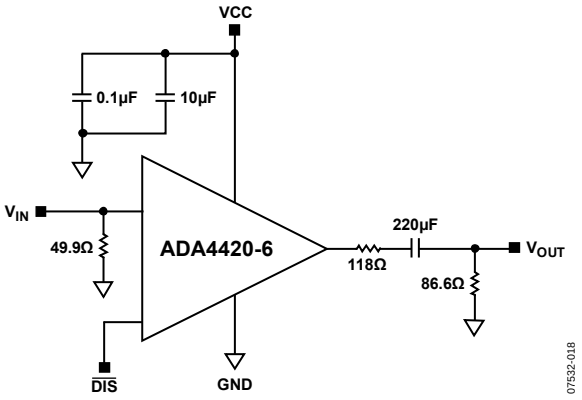


Figure 18. DC-Coupled Input, AC-Coupled Output

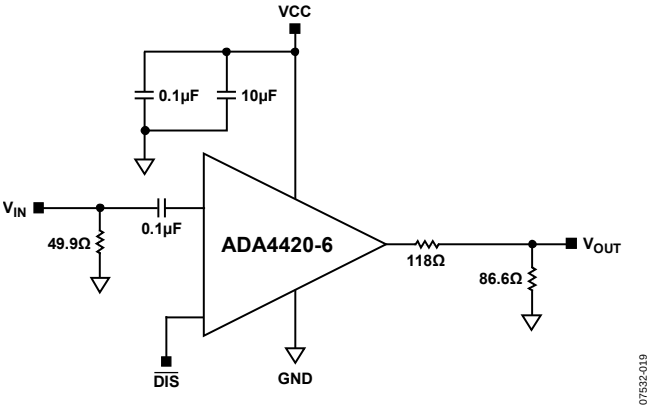


Figure 19. AC-Coupled Input, DC-Coupled Output

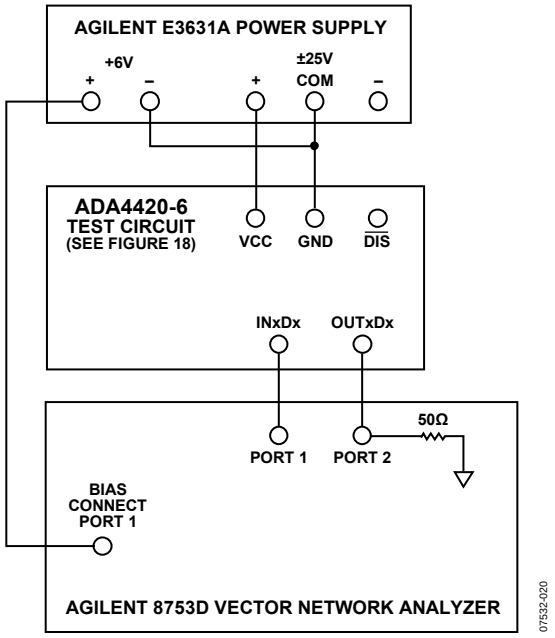


Figure 20. Test Circuit for Frequency Response and Group Delay

APPLICATIONS INFORMATION

OVERVIEW

With its high impedance inputs and high output drive, the ADA4420-6 is ideally suited to video reconstruction and anti-alias filtering applications. The high impedance inputs give designers flexibility with regard to how the input signals are terminated. Devices with DAC current source outputs that feed the ADA4420-6 can be loaded in whatever resistance provides the best performance, and devices with voltage outputs can be optimally terminated as well. The ADA4420-6 outputs can each drive up to two source-terminated, 75 Ω loads and; therefore, can directly drive the outputs from set-top boxes and DVDs without the need for a separate output buffer.

DISABLE

The ADA4420-6 includes a disable feature that can be used to save power when a particular device is not in use. When disabled, the ADA4420-6 typically draws only 7 μA from the supply. The disable feature is asserted by pulling the $\overline{\text{DIS}}$ pin low.

Table 6 summarizes the operation of the disable feature.

Table 6. Disable Function

$\overline{\text{DIS}}$ Pin Connection	Status
V_{CC} or Floating	Enabled
GND	Disabled

INPUT AND OUTPUT COUPLING

Inputs to the ADA4420-6 can be ac- or dc-coupled. For dc-coupled inputs, the signal must be completely contained within the input range of 0 V to 2.1 V. When using ac-coupled inputs, the lowest point of the signal is clamped to approximately 0 V. The ADA4420-6 outputs can be either ac- or dc-coupled.

When driving single ac-coupled loads in standard 75 Ω video distribution systems, a minimum capacitance of 220 μF is recommended to avoid line and field droop. There are two ac coupling options when driving two loads from one output. One option simply uses the same value capacitor on the second load, while the other option uses a common coupling capacitor that is at least twice the value used for the single load (see Figure 21 and Figure 22).

When driving two parallel 150 Ω loads (75 Ω effective load), the 3 dB bandwidth of the filters typically varies from that of the filters with a single 150 Ω load (see Figure 5).

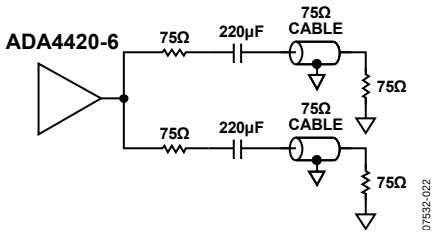


Figure 21. Driving Two AC-Coupled Loads with Two Coupling Capacitors

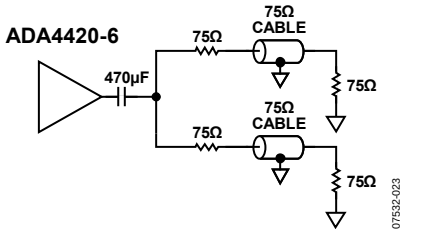


Figure 22. Driving Two AC-Coupled Loads with One Common Coupling Capacitor

PRINTED CIRCUIT BOARD (PCB) LAYOUT

As with all high speed applications, attention to the PCB layout is of paramount importance. When designing with the ADA4420-6, adhere to standard high speed layout practices. A solid ground plane is recommended, and surface-mount, ceramic power supply decoupling capacitors should be placed as close as possible to the supply pins. Connect all of the ADA4420-6 GND pins to the ground plane with traces that are as short as possible. Controlled impedance traces of the shortest length possible should be used to connect to the signal I/O pins and should not pass over any voids in the ground plane. A 75 Ω impedance level is typically used in video applications. When driving transmission lines, include series termination resistors on the signal outputs of the ADA4420-6.

When the ADA4420-6 receives its inputs from a device with current outputs, the required load resistor value for the output current is often different from the characteristic impedance of the signal traces. In this case, if the interconnections are short (<< 0.1 wavelength), the trace does not have to be terminated in its characteristic impedance. Traces of 75 Ω can be used in this instance, provided their lengths are an inch or two at most. This is easily achieved because the ADA4420-6 and the device feeding it are usually adjacent to each other, and connections can be made that are less than one inch in length.

VIDEO ENCODER RECONSTRUCTION FILTER

The ADA4420-6 is easily applied as a reconstruction filter at the DAC outputs of a video encoder. Figure 23 illustrates how to use the ADA4420-6 in this type of application following an ADV734x series video encoder, with a single-supply and ac-coupled outputs.

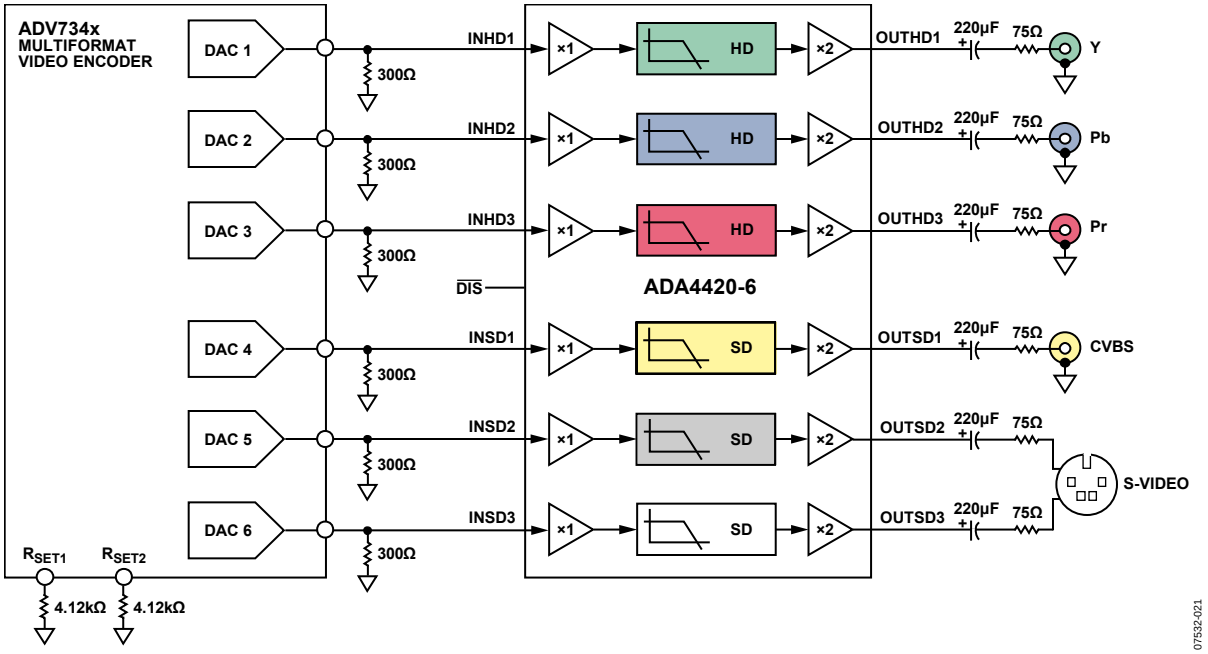
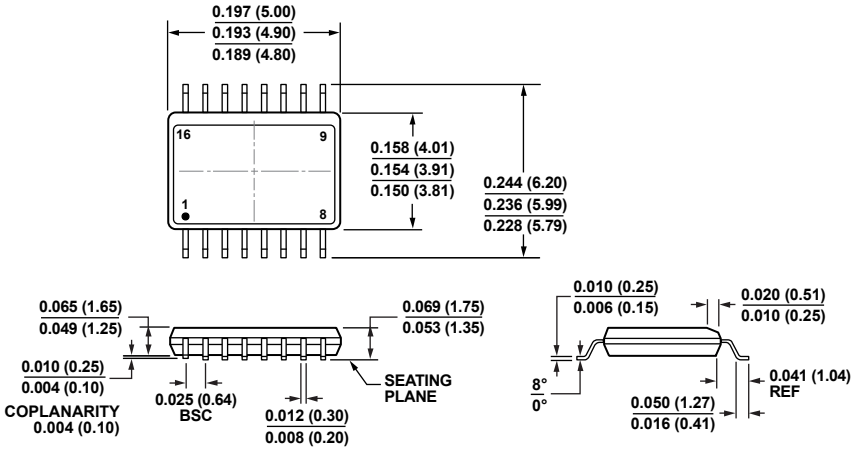


Figure 23. The ADA4420-6 Applied as a Reconstruction Filter Following an ADV734x Series Video Encoder

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-137-AB

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

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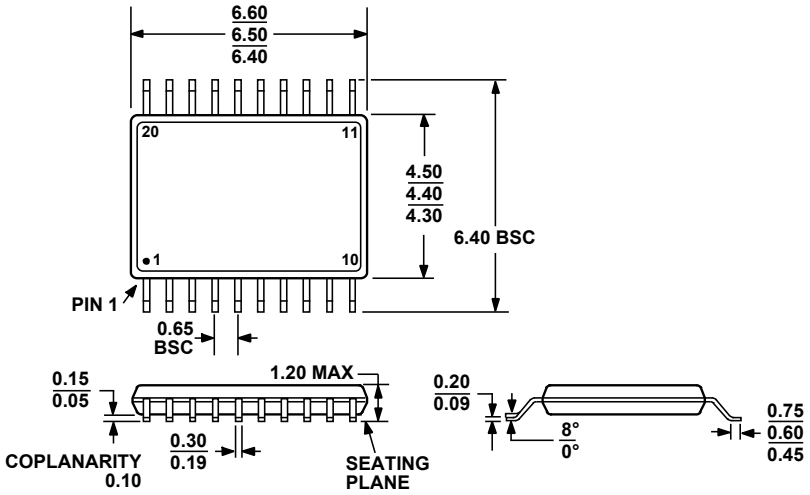
Figure 24. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 25. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADA4420-6ARQZ	−40°C to +85°C	16-Lead Shrink Small Outline Package (QSOP)	RQ-16	Tube (98)
ADA4420-6ARQZ-R7	−40°C to +85°C	16-Lead Shrink Small Outline Package (QSOP)	RQ-16	1,000
ADA4420-6ARQZ-RL	−40°C to +85°C	16-Lead Shrink Small Outline Package (QSOP)	RQ-16	2,500
ADA4420-6ARUZ	−40°C to +85°C	20-Lead Thin Shrink Small Outline Package (TSSOP)	RU-20	Tube (75)
ADA4420-6ARUZ-R7	−40°C to +85°C	20-Lead Thin Shrink Small Outline Package (TSSOP)	RU-20	1,000
ADA4420-6ARUZ-RL	−40°C to +85°C	20-Lead Thin Shrink Small Outline Package (TSSOP)	RU-20	2,500

[1] Z = RoHS Compliant Part.

NOTES

NOTES

D07532-0-5/11(A)