

1. Overview

The M16C/26A group (M16C/26A, M16C/26T) of single-chip microcomputers is built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and is packaged in a 42-pin and 48-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and a DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

There is a Normal-ver. for M16C/26A and T-ver. and v-ver. for M16C/26T.

1.1 Applications

Audio, cameras, office equipment, communications equipment, portable equipment,

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

1.2 Performance Outline

Table 1.1 lists performance outline of M16C/26A group (M16C/26A, M16C/26T) 48-pin device.

Table 1.2 lists performance outline of M16C/26A 42-pin device.

Table 1.1. Performance outline of M16C/26A group (48-pin device)(M16C/26A, M16C/26T)

Item		Performance
CPU	Number of basic instructions	91 instructions
	Shortest instruction	50 ns (f(BCLK)= 20MHz, Vcc= 3.0V to 5.5V) (M16C/26A, M16C/26T(T-ver.)) 100 ns (f(BCLK)= 10MHz, Vcc= 2.7V to 5.5V) (M16C/26A) 50 ns (f(BCLK)= 20MHz, Vcc= 4.2V to 5.5V -40 to 105°C) (M16C/26T(V-ver.)) 62.5 ns (f(BCLK)= 16MHz, Vcc= 4.2V to 5.5V -40 to 125°C) (M16C/26T(V-ver.))
	Operation mode	Single chip mode
	Address space	1M byte
	Memory capacity	ROM/RAM : See the product list
Peripheral function	Port	Input/Output : 39 lines
	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer
	Serial I/O	2 channels (UART, clock synchronous serial I/O) 1 channel (UART, clock synchronous, I ² C bus ¹ , or IEBus ²)
	A/D converter	10 bit A/D Converter : 1 circuit, 12 channels
	DMAC	2 channels
	CRC calculation circuit	2 polynomial (CRC-CCITT and CRC-16) with MSB/LSB selectable
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	20 internal and 8 external sources, 4 software sources, 7 levels
	Clock generation circuit	4 circuits Main clock(*), Sub-clock(*) On-chip oscillator, PLL frequency synthesizer (*)These circuit contain a built-in feedback resister.
	Oscillation stop detection	Main clock oscillation stop, re-oscillation detection function
Electrical Characteristics	Power supply voltage	Vcc=3.0V to 5.5V (f(BCLK)=20MHz) (M16C/26A) Vcc=2.7V to 5.5V (f(BCLK)=10MHz) Vcc=3.0V to 5.5V (M16C/26T(T-ver.)) Vcc=4.2V to 5.5V (M16C/26T(V-ver.))
	Power consumption	16mA (Vcc=5V, f(BCLK)=20MHz) 25 μA (Vcc=3V, f(BCLK)=f(X _{CIN})=32KHz on RAM) 1.8 μA (Vcc=3V, f(BCLK)=f(X _{CIN})=32KHz, in wait mode) 0.7 μA (Vcc=3V, when stop mode)
	Program/erase voltage	2.7V to 5.5V (M16C/26A) 3.0V to 5.5V (M16C/26T(T-ver.)) 4.2V to 5.5V (M16C/26T(V-ver.))
	Number of program/erase	100 times (Block A ,Block B : 10,000 times (option ³))
	Operating ambient temperature	-20 to 85°C / -40 to 85°C ⁴ (M16C/26A) -40 to 85°C (M16C/26T(T-ver.)) -40 to 105°C / -40 to 125°C (M16C/26T(V-ver.))
Package		48-pin plastic molded QFP

Notes:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. If you desire this option, please so specify.
4. See Table 1.6 for the operating ambient temperature.

Table 1.2. Performance outline of M16C/26A group (42-pin device) (M16C/26A)

Item		Performance
CPU	Number of basic instructions	91 instructions
	Shortest instruction	50 ns (f(BCLK)= 20MHz, Vcc= 3.0V to 5.5V) 100 ns (f(BCLK)= 10MHz, Vcc= 2.7V to 5.5V)
	Operation mode	Single chip mode
	Address space	1M byte
	Memory capacity	ROM/RAM : See the product list
Peripheral function	Port	Input/Output : 33 lines
	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer
	Serial I/O	1 channel (UART, clock synchronous serial I/O) 1 channel (UART, clock synchronous, I ² C bus ¹ , or IEBus ²)
	A/D converter	10 bit A/D Converter : 1 circuit, 10 channels
	DMAC	2 channels
	CRC calculation circuit	2 polynomial (CRC-CCITT and CRC-16) with MSB/LSB selectable
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	18 internal and 8 external sources, 4 software sources, 7 levels
	Clock generation circuit	4 circuits Main clock(*), Sub-clock(*) On-chip oscillator, PLL frequency synthesizer (*)These circuit contain a built-in feedback resistor.
	Oscillation stop detection	Main clock oscillation stop, re-oscillation detection function
	Low voltage detection circuit	Available
Electrical Characteristics	Power supply voltage	Vcc=3.0V to 5.5V (f(BCLK)=20MHz) Vcc=2.7V to 5.5V (f(BCLK)=10MHz)
	Power consumption	16mA (Vcc=5V, f(BCLK)=20MHz) 25 μ A (Vcc=3V, f(BCLK)=f(X _{CIN})=32KHz on RAM) 1.8 μ A (Vcc=3V, f(BCLK)=f(X _{CIN})=32KHz, in wait mode) 0.7 μ A (Vcc=3V, when stop mode)
Flash memory	Program/erase voltage	2.7V to 5.5V
	Number of program/erase	100 times(all area) or 1,000 times(program area)/10,000 times(data area) ³
Operating ambient temperature		-20 to 85°C / -40 to 85°C ³
Package		42-pin plastic molded SSOP

Notes:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. See Table 1.6 for the number of program/erase and the operating ambient temperature.

1.3 Block Diagram

Figure 1.1 is a block diagram of the M16C/26A group, 48-pin device.

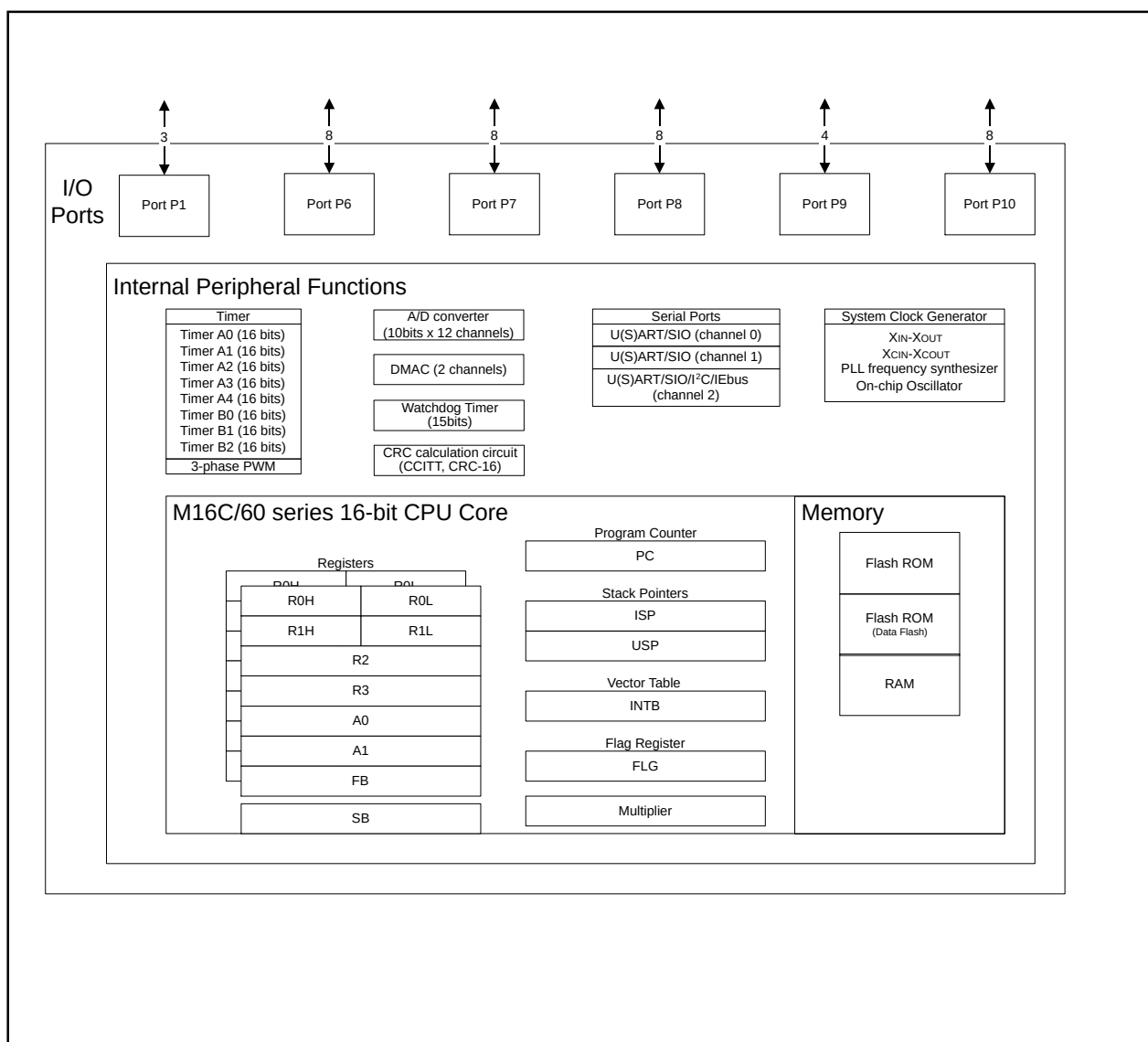


Figure 1.1. M16C/26A Group, 48-pin Block Diagram

The diagram illustrates the architecture of the M16C/60 series 16-bit CPU Core, organized into three main functional blocks:

- I/O Ports:** Located at the top, this block contains six ports: Port P1, Port P6, Port P7, Port P8, Port P9, and Port P10. Each port is connected to a central bus with a specific width: Port P1 (3 bits), Port P6 (4 bits), Port P7 (8 bits), Port P8 (8 bits), Port P9 (2 bits), and Port P10 (8 bits).
- Internal Peripheral Functions:** This central block contains various on-chip peripherals:
 - Timer:** Includes Timer A0 (16 bits), Timer A1 (16 bits), Timer A2 (16 bits), Timer A3 (16 bits), Timer A4 (16 bits), Timer B0 (16 bits), Timer B1 (16 bits), and Timer B2 (16 bits), along with a 3-phase PWM function.
 - A/D converter:** Provides 10bits x 10 channels.
 - DMAC:** Digital Macroe Address Controller with 2 channels.
 - Watchdog Timer:** 15bits.
 - CRC calculation circuit:** Supports CCITT and CRC-16.
 - Serial Ports:** Includes U(S)ART/SIO (channel 0) and U(S)ART/SIO/I²C/I²Sbus (channel 2).
 - System Clock Generator:** Features XIN-XOUT, XCIN-XCOUT, PLL frequency synthesizer, and On-chip Oscillator.
- M16C/60 series 16-bit CPU Core:** This block contains the core processing elements:
 - Registers:** A set of 16-bit registers including R0H/R0L, R1H/R1L, R2, R3, A0, A1, FB, and SB.
 - Program Counter (PC):** Holds the address of the next instruction.
 - Stack Pointers:** Includes Instruction Stack Pointer (ISP) and User Stack Pointer (USP).
 - Vector Table:** Contains interrupt vectors, starting with INTB.
 - Flag Register (FLG):** Holds status flags.
 - Multiplier:** A dedicated hardware multiplier.
- Memory:** Located on the right, this block contains:
 - Flash ROM:** Non-volatile memory for program storage.
 - Flash ROM (Data Flash):** Non-volatile memory for data storage.
 - RAM:** Random Access Memory for program execution.

1.4 Product List

Tables 1.3 to 1.5 list the M16C/28 group products and Figure 1.3 shows the type numbers, memory sizes and packages.

Table 1.3. Product List (1) -M16C/26A

As of Jun 2004

Type No.	ROM capacity	RAM capacity	Package type	Remarks
M30260M3A-XXXGP (D)	24K byte	1K byte	48P6Q	Mask ROM Version
M30260M4A-XXXGP (D)	32K byte	1K byte		
M30260M6A-XXXGP (D)	48K byte	2K byte		
M30260M8A-XXXGP (D)	64K byte	2K byte		
M30263M3A-XXXFP (D)	24K byte	1K byte	42P2R	
M30263M4A-XXXFP (D)	32K byte	1K byte		
M30263M6A-XXXFP (D)	48K byte	2K byte		
M30263M8A-XXXFP (D)	64K byte	2K byte		
M30260F3AGP (D)	24K + 4K byte	1K byte	48P6Q	Flash ROM Version
M30260F4AGP (D)	32K + 4K byte	1K byte		
M30260F6AGP (D)	48K + 4K byte	2K byte		
M30260F8AGP (D)	64K + 4K byte	2K byte		
M30263F3AFP (D)	24K + 4K byte	1K byte	42P2R	
M30263F4AFP (D)	32K + 4K byte	1K byte		
M30263F6AFP (D)	48K + 4K byte	2K byte		
M30263F8AFP (D)	64K + 4K byte	2K byte		

(P) : under planning

(D) : under development

Table 1.4. Product List (2) -M16C/26T T-ver.

As of Jun 2004

Type No.	ROM capacity	RAM capacity	Package type	Remarks
M30260M3T-XXXGP (P)	24K byte	1K byte	48P6Q	Mask ROM Version
M30260M4T-XXXGP (P)	32K byte	1K byte		
M30260M6T-XXXGP (P)	48K byte	2K byte		
M30260M8T-XXXGP (P)	64K byte	2K byte		
M30260F3TGP (D)	24K + 4K byte	1K byte	48P6Q	Flash ROM Version
M30260F4TGP (D)	32K + 4K byte	1K byte		
M30260F6TGP (D)	48K + 4K byte	2K byte		
M30260F8TGP (D)	64K + 4K byte	2K byte		

(P) : under planning

(D) : under development

NOTES: Specification of M16C/26T partly varies from the one of M16C/26A

Table 1.5. Product List (3) -M16C/26T V-ver.

As of Jun 2004

Type No.	ROM capacity	RAM capacity	Package type	Remarks
M30260M3V-XXXGP (P)	24K byte	1K byte	48P6Q	Mask ROM Version
M30260M4V-XXXGP (P)	32K byte	1K byte		
M30260M6V-XXXGP (P)	48K byte	2K byte		
M30260M8V-XXXGP (P)	64K byte	2K byte		
M30260F3VGP (D)	24K + 4K byte	1K byte	48P6Q	Flash ROM Version
M30260F4VGP (D)	32K + 4K byte	1K byte		
M30260F6VGP (D)	48K + 4K byte	2K byte		
M30260F8VGP (D)	64K + 4K byte	2K byte		

(P) : under planning

(D) : under development

NOTES: Specification of M16C/26T partly varies from the one of M16C/26A

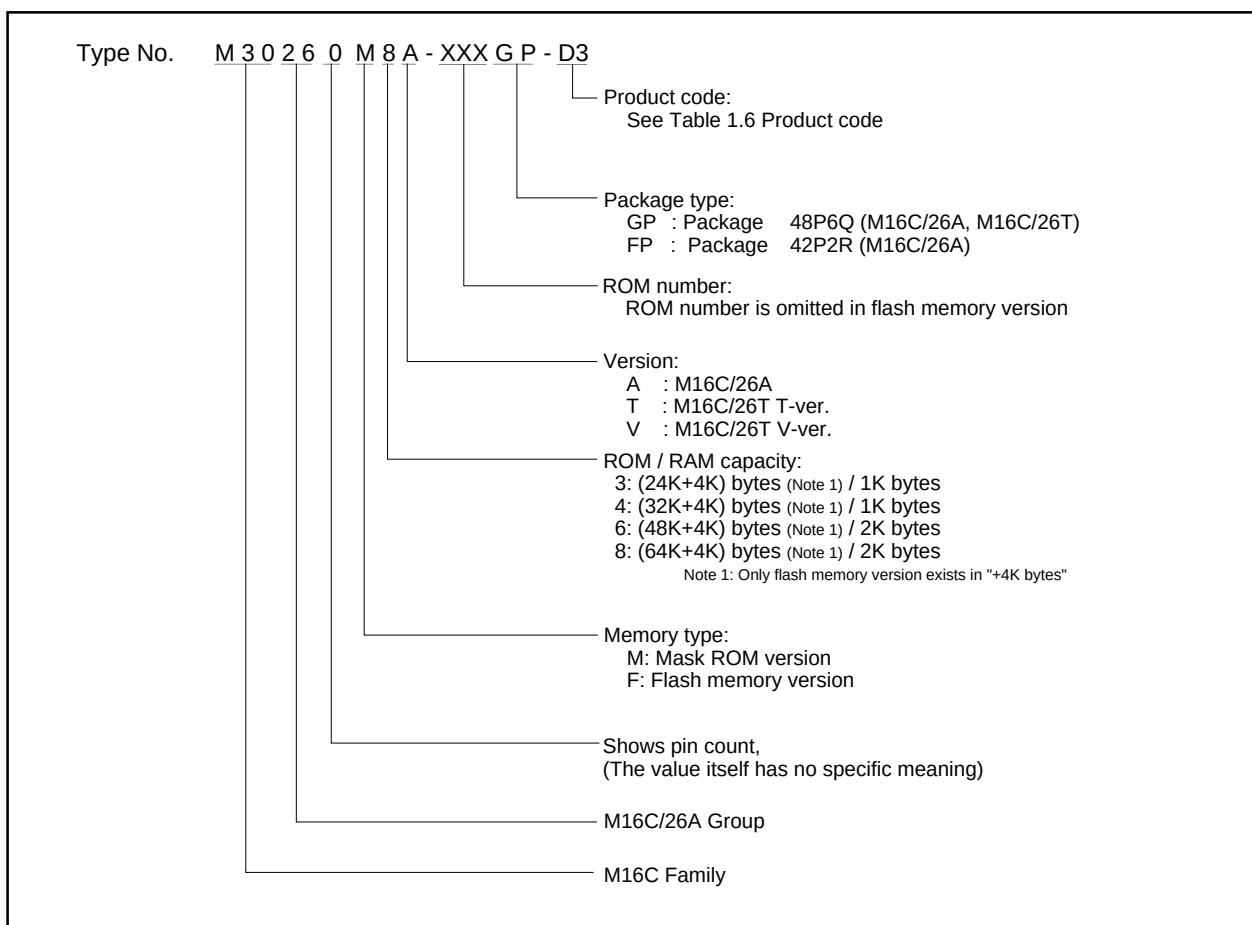


Figure 1.3. Type No., Memory Size, and Package

Table 1.6. Product code (Flash memory version, M16C/26A)

Product Code	Package	Internal ROM (Program area)		Internal ROM (Data area)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
D3	Lead-included	100	0°C to 60°C	100	0°C to 60°C	-40°C to 85°C
D5					-20°C to 85°C	
D7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
D9					-20°C to 85°C	-20°C to 85°C
U3	Lead-free	100		100	0°C to 60°C	-40°C to 85°C
U5					-20°C to 85°C	
U7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
U9					-20°C to 85°C	-20°C to 85°C

(MASK ROM version, M16C/26A)

Product Code	Package	Operating Ambient Temperature
D3	Lead-included	-40°C to 85°C
D5		-20°C to 85°C
U3	Lead-free	-40°C to 85°C
U5		-20°C to 85°C

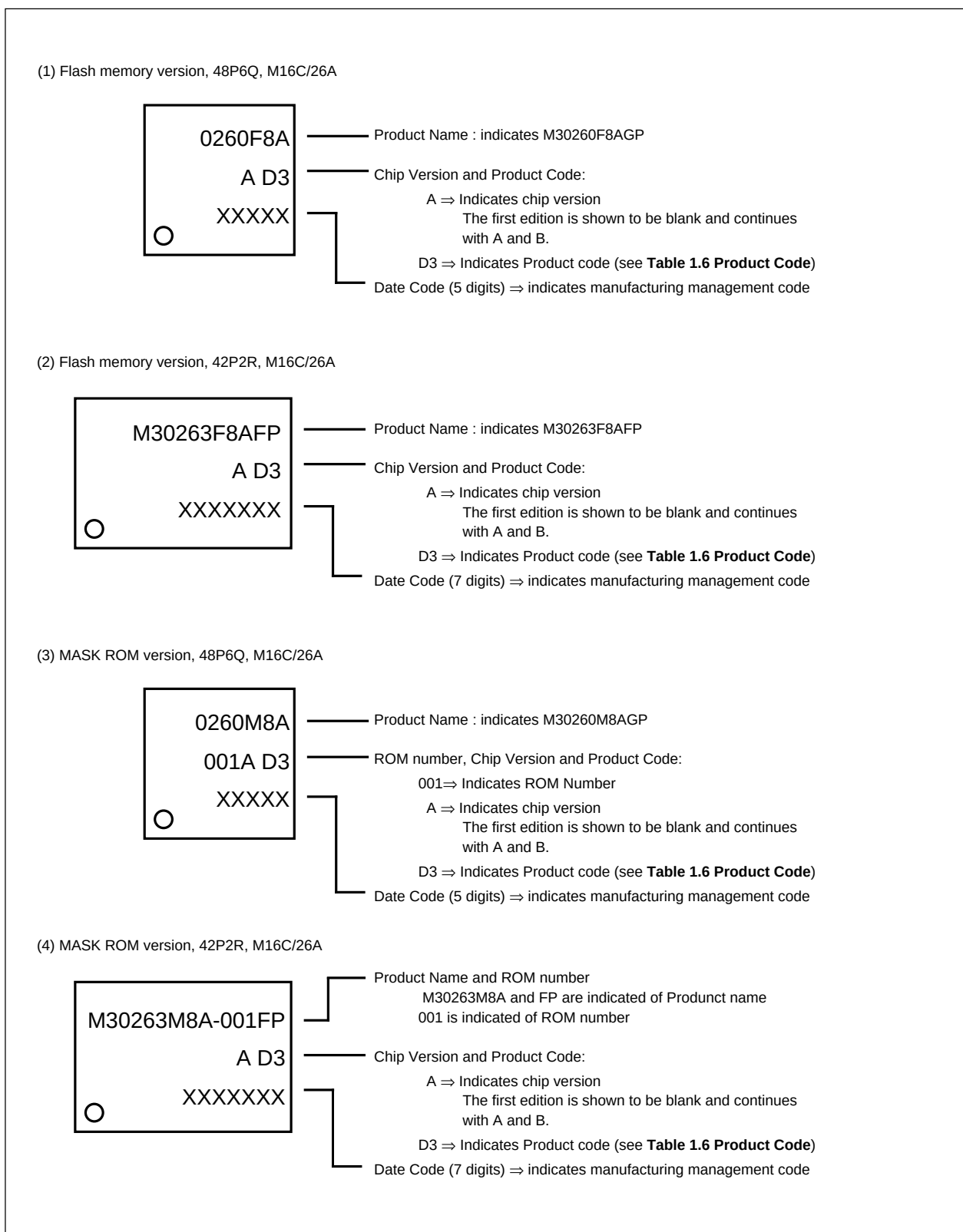


Figure 1.4. Marking Diagram of Flash Memory version for M16C/26A (Top View)

1.5 Pin Configuration

Figures 1.5 and 1.6 show the pin configurations (top view).

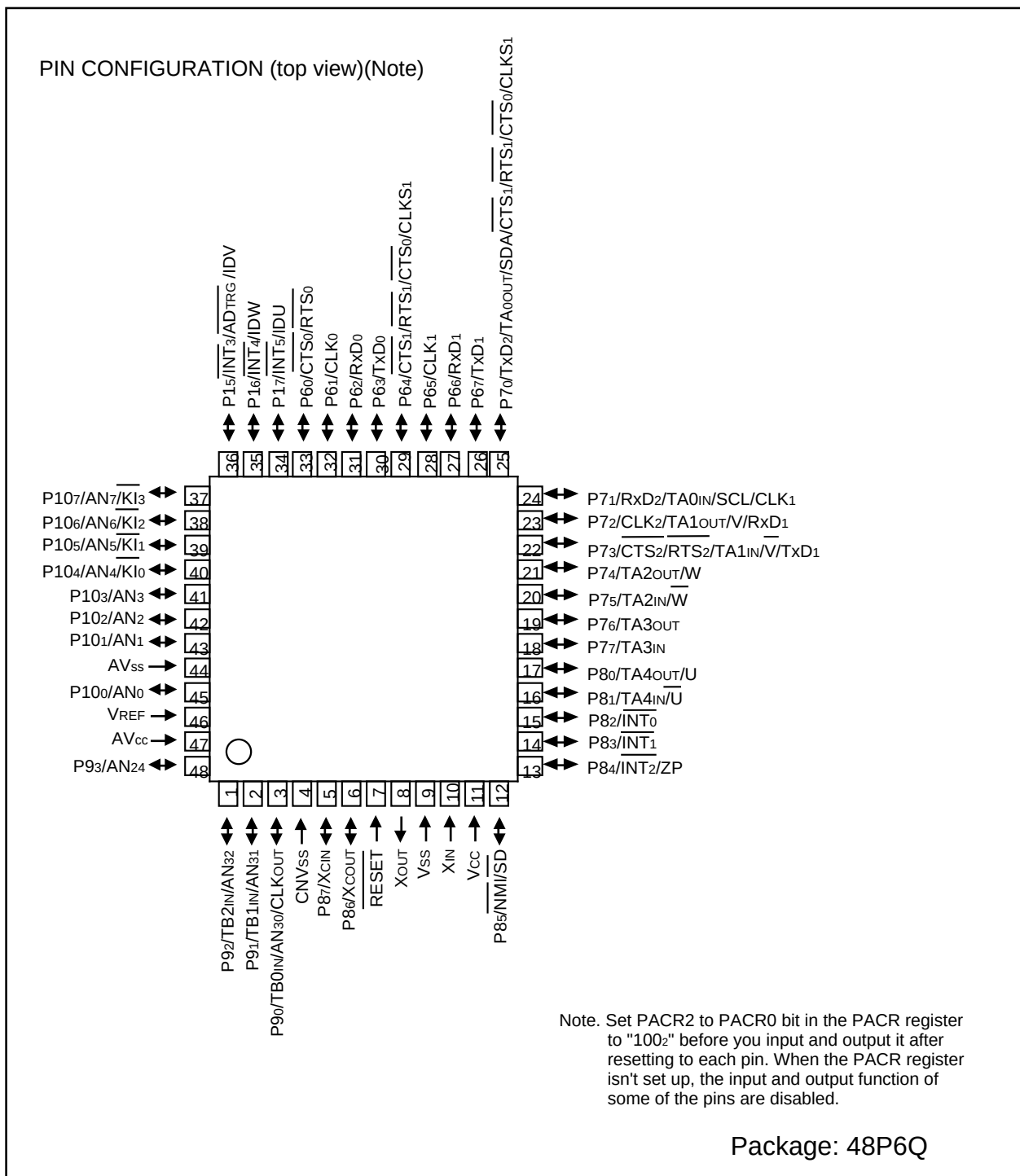


Figure 1.5. Pin Configuration (Top View) of M16C/26A Group, 48-pin Package

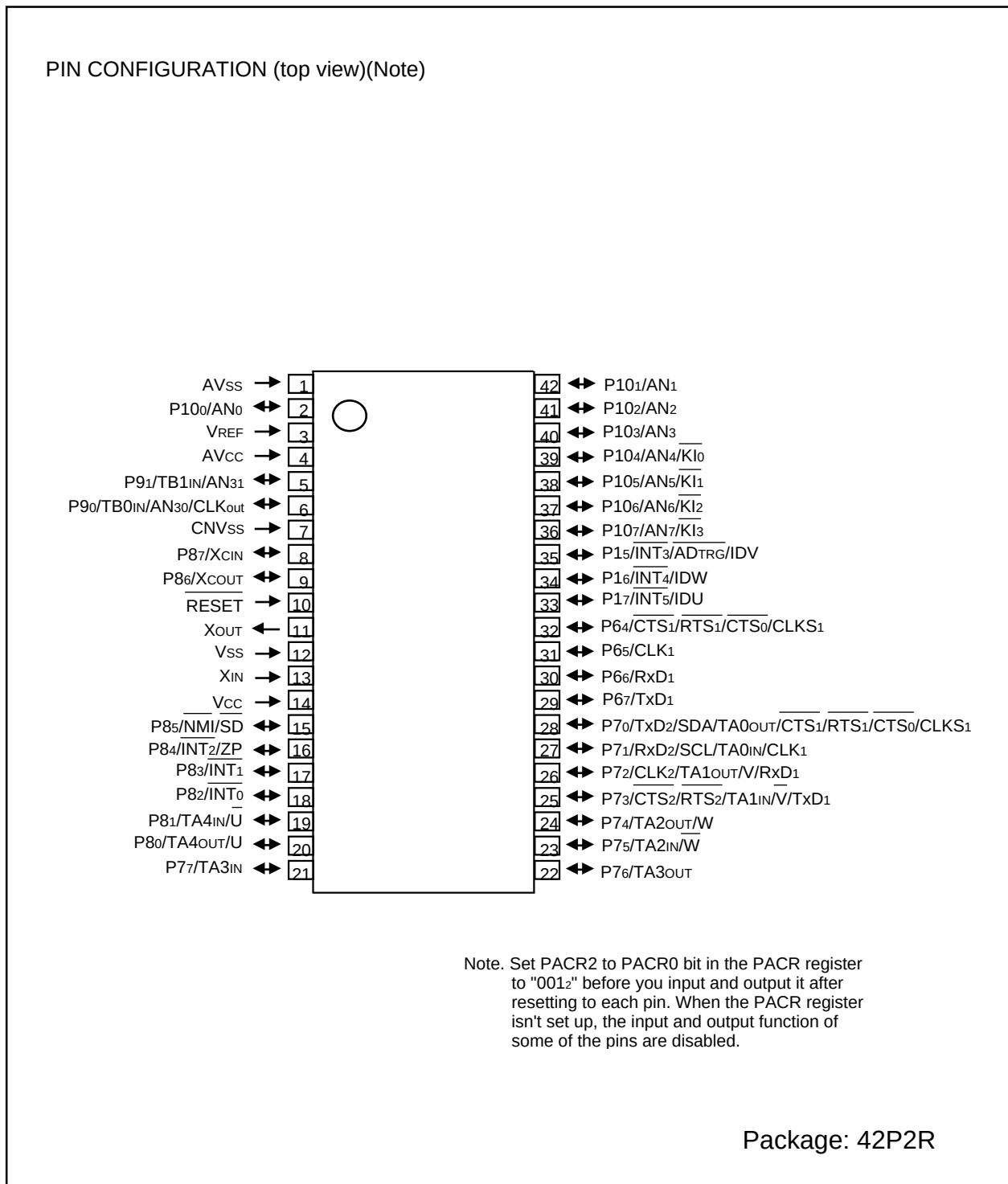


Figure 1.6. Pin Configuration (Top View) of M16C/26A Group, 42-pin Package

1.6 Pin Description

Table 1.6 and 1.7 describes the available pins.

Table 1.6. Pin Description(1)

Pin name	Signal name	I/O type	Function
V _{CC} , V _{SS}	Power supply input		Apply 0V to the V _{SS} pin, and the following voltage to the V _{CC} pin. 2.7 to 5.5V (M16C/26A) 3.0 to 5.5V (M16C/26T T-ver.) 4.2 to 5.5V (M16C/26T V-ver.)
CNV _{SS}	CNV _{SS}	Input	Connect this pin to V _{SS} .
RESET	Reset input	Input	"L" on this input resets the microcomputer.
X _{IN} X _{OUT}	Clock input Clock output	Input Output	These pins are provided for the main clock generating circuit input/output. Connect a ceramic resonator or crystal between the X _{IN} and the X _{OUT} pins. To use an externally derived clock, input it to the X _{IN} pin and leave the X _{OUT} pin open. If X _{IN} is not used (for external oscillator or external clock) connect X _{IN} pin to V _{CC} and leave X _{OUT} pin open.
AV _{CC}	Analog power supply input		This pin is a power supply input for the A/D converter. Connect this pin to V _{CC} .
AV _{SS}	Analog power supply input		This pin is a power supply input for the A/D converter. Connect this pin to V _{SS} .
V _{REF}	Reference Voltage input	Input	This pin is a reference voltage input for the A/D converter.
P1 ₅ ~P1 ₇	I/O port P1	Input/ output	This is an 3-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When used for input, a pull-up resistor option can be selected for the entire group of three pins. Additional software selectable secondary functions are: 1) P1 ₅ to P1 ₇ can be configured as external $\overline{\text{INT}}$ interrupt pins; 2) P1 ₅ to P1 ₇ can be configured as position-data-retain function input pins, and; 3) P1 ₅ can input a trigger for the A/D converter.
P6 ₀ ~P6 ₇	I/O port P6	Input/ output	This is an 8-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When used for input, a pull-up resistor option can be selected for the entire group of four pins. Pins in this port also function as UART0 and UART1 I/O, as selected by software. P6 ₀ to P6 ₃ are not available in the 42 pin version.
P7 ₀ ~P7 ₇	I/O port P7	Input/ output	This is an 8-bit I/O port equivalent to P6. P7 can also function as I/O for timer A0 to A3, as selected by software. Additional programming options are: P7 ₀ to P7 ₃ can assume UART1 I/O or UART2 I/O capabilities, and P7 ₂ to P7 ₅ can function as output pins for the three-phase motor control timer.

Table 1.7. Pin Description(2)

Pin name	Signal name	I/O type	Function
P8 ₀ ~P8 ₇	I/O port P8	Input/ output	This is an 8-bit I/O port equivalent to P6. Additional software-selectable secondary functions are: 1) P8 ₀ and P8 ₁ can act as either I/O for Timer A4, or as output pins for the three-phase motor control timer; 2) P8 ₂ to P8 ₄ can be configured as external $\overline{\text{INT}}$ interrupt pins. P8 ₄ can be used for Timer A Zphase function; 3) P8 ₅ can be used as $\overline{\text{NMI}}/\overline{\text{SD}}$. P8 ₅ can not be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to P8 ₅ after setting the direction register for P8 ₅ to "0" when the three-phase motor control is enabled, and; 4) P8 ₆ and P8 ₇ can serve as I/O pins for the sub-clock generation circuit. In this latter case, a quartz oscillator must be connected between P8 ₆ (X _{COU} T pin) and P8 ₇ (X _{CIN} pin).
P9 ₀ ~P9 ₃	I/O port P9	Input/ output	This is an 4-bit I/O port equivalent to P6. Additional software-selectable secondary functions are: 1) P9 ₀ to P9 ₂ can act as Timer B0~B2 input pins, and; 2) P9 ₀ to P9 ₃ can act as A/D converter input pins. P9 ₀ outputs a no-divide, divide-by-8 or divide-by-32 clock of X _{IN} or a clock of the same frequency as X _{CIN} as selected by program. P9 ₂ to P9 ₃ are not available in the 42 pin version.
P10 ₀ ~P10 ₇	I/O port P10	Input/ output	This is an 8-bit I/O port equivalent to P6. This port can also function as A/D converter input pins, as selected by software. Furthermore, P10 ₄ to P10 ₇ can also function as input pins for the key input interrupt function.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

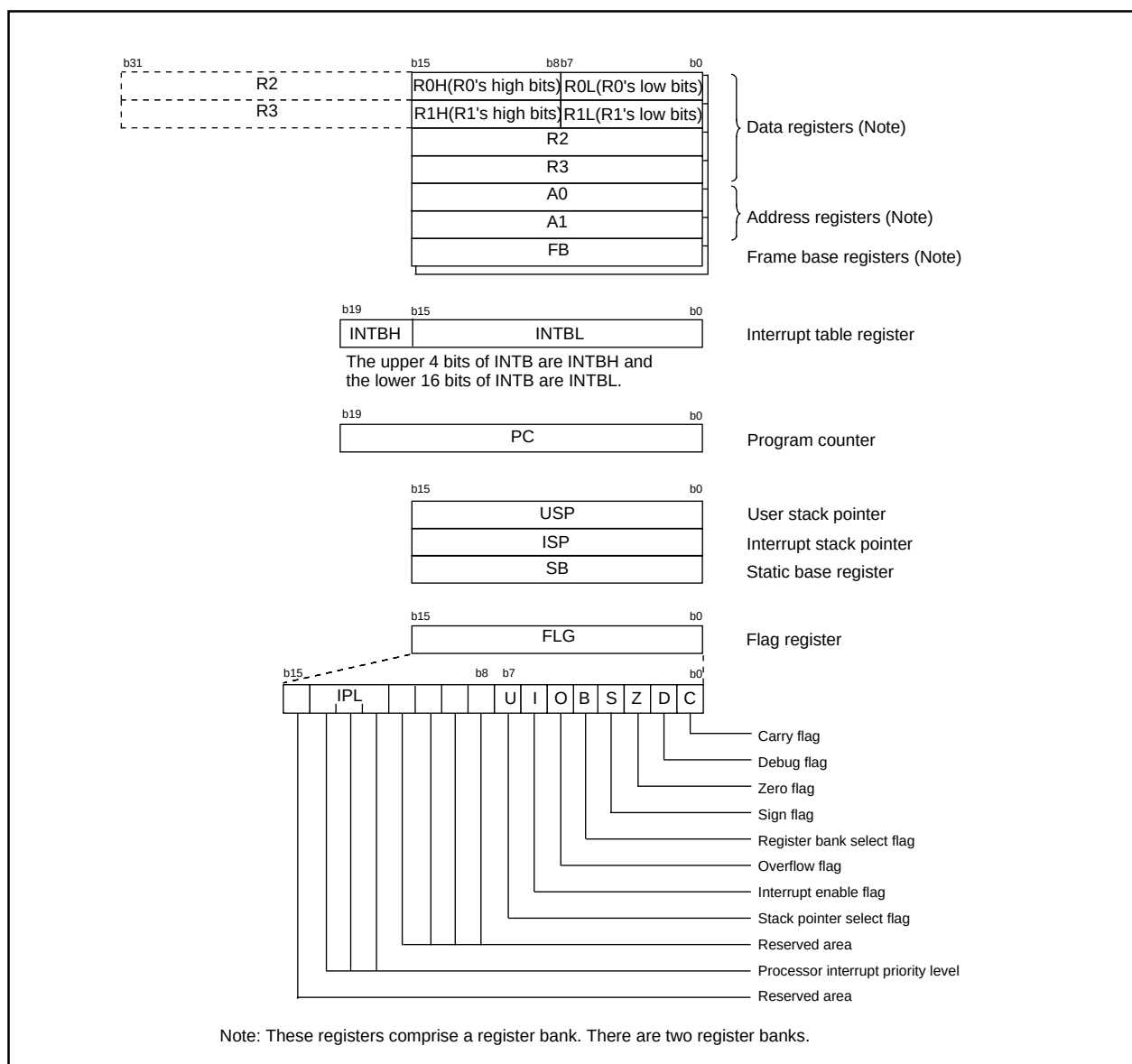


Figure 2.1. Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to "0".

2.8.3 Zero Flag (Z Flag)

This flag is set to "1" when an arithmetic operation resulted in 0; otherwise, it is "0".

2.8.4 Sign Flag (S Flag)

This flag is set to "1" when an arithmetic operation resulted in a negative value; otherwise, it is "0".

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is "0"; register bank 1 is selected when this flag is "1".

2.8.6 Overflow Flag (O Flag)

This flag is set to "1" when the operation resulted in an overflow; otherwise, it is "0".

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is "0", and are enabled when the I flag is "1". The I flag is cleared to "0" when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is "0"; USP is selected when the U flag is "1".

The U flag is cleared to "0" when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map. The linear address space of 1M bytes extends from address 00000₁₆ to FFFFF₁₆. The internal ROM is allocated in a lower address direction beginning with address FFFFF₁₆. For example, a 64-Kbyte internal ROM is allocated to the address from F0000₁₆ to FFFFF₁₆.

The fixed interrupt vector table is allocated to the address from FFFDC₁₆ to FFFFF₁₆. Therefore store the start address of each interrupt routine here. For details, refer to the "Interrupt".

These devices also contain two blocks of Flash ROM as Data Flash memory to store data. These two blocks of 2K bytes are located from 0F000₁₆ to 0FFFF₁₆ on all versions.

The internal RAM is allocated in an upper address direction beginning with address 00400₁₆. For example, a 1-Kbyte internal RAM is allocated to the address from 00400₁₆ to 007FF₁₆. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

The SFR is allocated to the address from 00000₁₆ to 003FF₁₆. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.

The special page vector table is allocated to the addresses from FFE00₁₆ to FFFDB₁₆. This vector is used by the JMPS or JSRS instruction. For details, refer to the "M16C/60 and M16C/20 Series Software Manual".

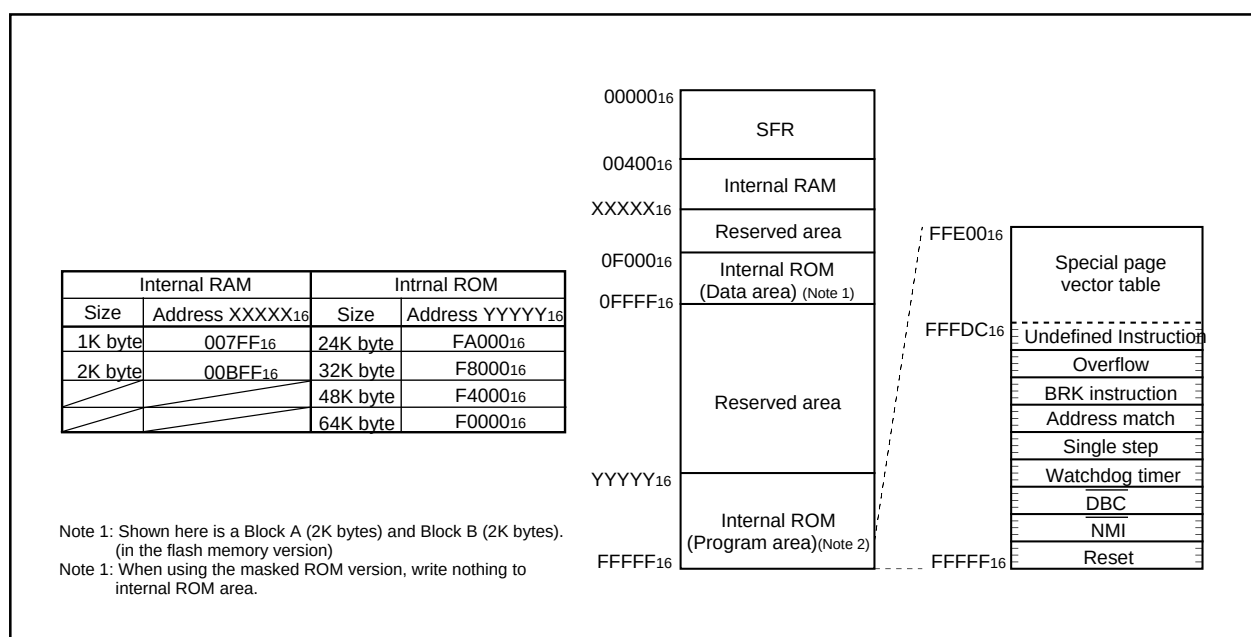


Figure 3.1. Memory Map

4. Special Function Register (SFR) Map

Address	Register	Symbol	After reset
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor mode register 0	PM0	00 ₁₆
0005 ₁₆	Processor mode register 1	PM1	00001000 ₂
0006 ₁₆	System clock control register 0	CM0	01001000 ₂
0007 ₁₆	System clock control register 1	CM1	00100000 ₂
0008 ₁₆			
0009 ₁₆	Address match interrupt enable register	AIER	XXXXXX00 ₂
000A ₁₆	Protect register	PBCR	XX000000 ₂
000B ₁₆			
000C ₁₆	Oscillation stop detection register (Note 2)	CM2	0X000010 ₂
000D ₁₆			
000E ₁₆	Watchdog timer start register	WDTS	?? ₁₆
000F ₁₆	Watchdog timer control register	WDC	00?????? ₂ (Note3)
0010 ₁₆	Address match interrupt register 0	RMAD0	00 ₁₆
0011 ₁₆			00 ₁₆
0012 ₁₆			X0 ₁₆
0013 ₁₆			
0014 ₁₆	Address match interrupt register 1	RMAD1	00 ₁₆
0015 ₁₆			00 ₁₆
0016 ₁₆			X0 ₁₆
0017 ₁₆			
0018 ₁₆			
0019 ₁₆	Voltage detection register 1 (Note 4,5)	VCR1	00001000 ₂
001A ₁₆	Voltage detection register 2 (Note 4,5)	VCR2	00 ₁₆
001B ₁₆			
001C ₁₆	PLL control register 0	PLC0	0001X010 ₂
001D ₁₆			
001E ₁₆	Processor mode register 2	PM2	XXX00000 ₂
001F ₁₆	Power supply down detection interrupt register (Note 5)	D4INT	00 ₁₆
0020 ₁₆	DMA0 source pointer	SAR0	?? ₁₆
0021 ₁₆			?? ₁₆
0022 ₁₆			X? ₁₆
0023 ₁₆			
0024 ₁₆	DMA0 destination pointer	DAR0	?? ₁₆
0025 ₁₆			?? ₁₆
0026 ₁₆			X? ₁₆
0027 ₁₆			
0028 ₁₆	DMA0 transfer counter	TCR0	?? ₁₆
0029 ₁₆			?? ₁₆
002A ₁₆			
002B ₁₆			
002C ₁₆	DMA0 control register	DM0CON	00000?00 ₂
002D ₁₆			
002E ₁₆			
002F ₁₆			
0030 ₁₆	DMA1 source pointer	SAR1	?? ₁₆
0031 ₁₆			?? ₁₆
0032 ₁₆			X? ₁₆
0033 ₁₆			
0034 ₁₆	DMA1 destination pointer	DAR1	?? ₁₆
0035 ₁₆			?? ₁₆
0036 ₁₆			X? ₁₆
0037 ₁₆			
0038 ₁₆	DMA1 transfer counter	TCR1	?? ₁₆
0039 ₁₆			?? ₁₆
003A ₁₆			
003B ₁₆			
003C ₁₆	DMA1 control register	DM1CON	00000?00 ₂
003D ₁₆			
003E ₁₆			
003F ₁₆			

Note 1: The blank areas are reserved and cannot be used by users.

Note 2: The CM20, CM21 and CM27 bits do not change at oscillation stop detection reset..

Note 3: The WDC5 bit is "0" (cold start) immediately after power-on. It can only be set to "1" in a program.

It is set to "0" when the input voltage at the VCC pin drops to Vdet2 or less while the VC25 bit in the VCR2 register is set to "1" (2V detection circuit enable).

Note 4: This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.

Note 5: This register can not use for M16C/26T

X : Nothing is mapped to this bit

? : Undefined

Address	Register	Symbol	After reset
0040 ₁₆			
0041 ₁₆			
0042 ₁₆			
0043 ₁₆			
0044 ₁₆	INT3 interrupt control register	INT3IC	XX00?000 ₂
0045 ₁₆			
0046 ₁₆			
0047 ₁₆			
0048 ₁₆	INT5 interrupt control register	INT5IC	XX00?000 ₂
0049 ₁₆	INT4 interrupt control register	INT4IC	XX00?000 ₂
004A ₁₆	UART2 Bus collision detection interrupt control register	BCNIC	XXXX?000 ₂
004B ₁₆	DMA0 interrupt control register	DM0IC	XXXX?000 ₂
004C ₁₆	DMA1 interrupt control register	DM1IC	XXXX?000 ₂
004D ₁₆	Key input interrupt control register	KUPIC	XXXX?000 ₂
004E ₁₆	A/D conversion interrupt control register	ADIC	XXXX?000 ₂
004F ₁₆	UART2 transmit interrupt control register	S2TIC	XXXX?000 ₂
0050 ₁₆	UART2 receive interrupt control register	S2RIC	XXXX?000 ₂
0051 ₁₆	UART0 transmit interrupt control register	S0TIC	XXXX?000 ₂
0052 ₁₆	UART0 receive interrupt control register	S0RIC	XXXX?000 ₂
0053 ₁₆	UART1 transmit interrupt control register	S1TIC	XXXX?000 ₂
0054 ₁₆	UART1 receive interrupt control register	S1RIC	XXXX?000 ₂
0055 ₁₆	TimerA0 interrupt control register	TA0IC	XXXX?000 ₂
0056 ₁₆	TimerA1 interrupt control register	TA1IC	XXXX?000 ₂
0057 ₁₆	TimerA2 interrupt control register	TA2IC	XXXX?000 ₂
0058 ₁₆	TimerA3 interrupt control register	TA3IC	XXXX?000 ₂
0059 ₁₆	TimerA4 interrupt control register	TA4IC	XXXX?000 ₂
005A ₁₆	TimerB0 interrupt control register	TB0IC	XXXX?000 ₂
005B ₁₆	TimerB1 interrupt control register	TB1IC	XXXX?000 ₂
005C ₁₆	TimerB2 interrupt control register	TB2IC	XXXX?000 ₂
005D ₁₆	INT0 interrupt control register	INT0IC	XX00?000 ₂
005E ₁₆	INT1 interrupt control register	INT1IC	XX00?000 ₂
005F ₁₆	INT2 interrupt control register	INT2IC	XX00?000 ₂
0060 ₁₆			
0061 ₁₆			
0062 ₁₆			
0063 ₁₆			
0064 ₁₆			
0065 ₁₆			
0066 ₁₆			
0067 ₁₆			
0068 ₁₆			
0069 ₁₆			
006A ₁₆			
006B ₁₆			
006C ₁₆			
006D ₁₆			
006E ₁₆			
006F ₁₆			
0070 ₁₆			
0071 ₁₆			
0072 ₁₆			
0073 ₁₆			
0074 ₁₆			
0075 ₁₆			
0076 ₁₆			
0077 ₁₆			
0078 ₁₆			
0079 ₁₆			
007A ₁₆			
007B ₁₆			
007C ₁₆			
007D ₁₆			
007E ₁₆			
007F ₁₆			

Note 1: The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Address	Register	Symbol	After reset
0080 ₁₆			
0081 ₁₆			
0082 ₁₆			
0083 ₁₆			
0084 ₁₆			
0085 ₁₆			
0086 ₁₆			
⋮			
01B0 ₁₆			
01B1 ₁₆			
01B2 ₁₆			
01B3 ₁₆	Flash memory control register 4 (Note 2)	FMR4	01000000 ₂
01B4 ₁₆			
01B5 ₁₆	Flash memory control register 1 (Note 2)	FMR1	000???0? ₂
01B6 ₁₆			
01B7 ₁₆	Flash memory control register 0 (Note 2)	FMR0	01 ₁₆
01B8 ₁₆			
01B9 ₁₆			
01BA ₁₆			
01BB ₁₆			
01BC ₁₆			
01BD ₁₆			
01BE ₁₆			
01BF ₁₆			
⋮			
0250 ₁₆			
0251 ₁₆			
0252 ₁₆			
0253 ₁₆			
0254 ₁₆			
0255 ₁₆			
0256 ₁₆			
0257 ₁₆			
0258 ₁₆			
0259 ₁₆			
025A ₁₆	Three phase protect control register	TPRC	00 ₁₆
025B ₁₆			
025C ₁₆	On-chip oscillator control register	ROCR	00000101 ₂
025D ₁₆	Pin assignment control register	PACR	00 ₁₆
025E ₁₆	Peripheral clock select register	PCLKR	00000011 ₂
025F ₁₆			
⋮			
0330 ₁₆			
0331 ₁₆			
0332 ₁₆			
0333 ₁₆			
0334 ₁₆			
0335 ₁₆			
0336 ₁₆			
0337 ₁₆			
0338 ₁₆			
0339 ₁₆			
033A ₁₆			
033B ₁₆			
033C ₁₆			
033D ₁₆			
033E ₁₆	NMI digital debounce register	NDDR	FF ₁₆
033F ₁₆	Port17 digital debounce register	P17DDR	FF ₁₆

Note 1: The blank areas are reserved and cannot be used by users.

Note 2: This register is included in the flash memory version.

X : Nothing is mapped to this bit

? : Undefined

Address	Register	Symbol	After reset
0340 ₁₆			
0341 ₁₆			
0342 ₁₆	Timer A1-1 register	TA11	?? ₁₆
0343 ₁₆			?? ₁₆
0344 ₁₆	Timer A2-1 register	TA21	?? ₁₆
0345 ₁₆			?? ₁₆
0346 ₁₆	Timer A4-1 register	TA41	?? ₁₆
0347 ₁₆			?? ₁₆
0348 ₁₆	Three phase PWM control register 0	INVC0	00 ₁₆
0349 ₁₆	Three phase PWM control register 1	INVC1	00 ₁₆
034A ₁₆	Three phase output buffer register 0	IDB0	00 ₁₆
034B ₁₆	Three phase output buffer register 1	IDB1	00 ₁₆
034C ₁₆	Dead time timer	DTT	?? ₁₆
034D ₁₆	Timer B2 Interrupt occurrence frequency set counter	ICTB2	X? ₁₆
034E ₁₆	Position-data-retain function control register	PDRF	XXXX0000 ₂
034F ₁₆			
0350 ₁₆			
0351 ₁₆			
0352 ₁₆			
0353 ₁₆			
0354 ₁₆			
0355 ₁₆			
0356 ₁₆			
0357 ₁₆			
0358 ₁₆	Port function control register	PFCR	00111111 ₂
0359 ₁₆			
035A ₁₆			
035B ₁₆			
035C ₁₆			
035D ₁₆			
035E ₁₆	Interrupt request cause select register 2	IFSR2A	XXXXXXX ₂
035F ₁₆	Interrupt request cause select register	IFSR	00 ₁₆
0360 ₁₆			
0361 ₁₆			
0362 ₁₆			
0363 ₁₆			
0364 ₁₆			
0365 ₁₆			
0366 ₁₆			
0367 ₁₆			
0368 ₁₆			
0369 ₁₆			
036A ₁₆			
036B ₁₆			
036C ₁₆			
036D ₁₆			
036E ₁₆			
036F ₁₆			
0370 ₁₆			
0371 ₁₆			
0372 ₁₆			
0373 ₁₆			
0374 ₁₆	UART2 special mode register 4	U2SMR4	00 ₁₆
0375 ₁₆	UART2 special mode register 3	U2SMR3	000X0X0X ₂
0376 ₁₆	UART2 special mode register 2	U2SMR2	X0000000 ₂
0377 ₁₆	UART2 special mode register	U2SMR	X0000000 ₂
0378 ₁₆	UART2 transmit/receive mode register	U2MR	00 ₁₆
0379 ₁₆	UART2 bit rate register	U2BRG	?? ₁₆
037A ₁₆	UART2 transmit buffer register	U2TB	??????? ₂
037B ₁₆			XXXXXXXX? ₂
037C ₁₆	UART2 transmit/receive control register 0	U2C0	00001000 ₂
037D ₁₆	UART2 transmit/receive control register 1	U2C1	00000010 ₂
037E ₁₆	UART2 receive buffer register	U2RB	??????? ₂
037F ₁₆			?????XX? ₂

Note 1 : The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit

? : Undefined

Address	Register	Symbol	After reset
0380 ₁₆	Count start flag	TABSR	00 ₁₆
0381 ₁₆	Clock prescaler reset flag	CPSRF	0XXXXXXX ₂
0382 ₁₆	One-shot start flag	ONSF	00 ₁₆
0383 ₁₆	Trigger select register	TRGSR	00 ₁₆
0384 ₁₆	Up-down flag	UDF	00 ₁₆
0385 ₁₆			
0386 ₁₆ 0387 ₁₆	Timer A0 register	TA0	?? ₁₆ ?? ₁₆
0388 ₁₆ 0389 ₁₆	Timer A1 register	TA1	?? ₁₆ ?? ₁₆
038A ₁₆ 038B ₁₆	Timer A2 register	TA2	?? ₁₆ ?? ₁₆
038C ₁₆ 038D ₁₆	Timer A3 register	TA3	?? ₁₆ ?? ₁₆
038E ₁₆ 038F ₁₆	Timer A4 register	TA4	?? ₁₆ ?? ₁₆
0390 ₁₆ 0391 ₁₆	Timer B0 register	TB0	?? ₁₆ ?? ₁₆
0392 ₁₆ 0393 ₁₆	Timer B1 register	TB1	?? ₁₆ ?? ₁₆
0394 ₁₆ 0395 ₁₆	Timer B2 register	TB2	?? ₁₆ ?? ₁₆
0396 ₁₆	Timer A0 mode register	TA0MR	00 ₁₆
0397 ₁₆	Timer A1 mode register	TA1MR	00 ₁₆
0398 ₁₆	Timer A2 mode register	TA2MR	00 ₁₆
0399 ₁₆	Timer A3 mode register	TA3MR	00 ₁₆
039A ₁₆	Timer A4 mode register	TA4MR	00 ₁₆
039B ₁₆	Timer B0 mode register	TB0MR	00??0000 ₂
039C ₁₆	Timer B1 mode register	TB1MR	00?X0000 ₂
039D ₁₆	Timer B2 mode register	TB2MR	00?X0000 ₂
039E ₁₆ 039F ₁₆	Timer B2 special mode register	TB2SC	X0000000 ₂
03A0 ₁₆	UART0 transmit/receive mode register	U0MR	00 ₁₆
03A1 ₁₆	UART0 bit rate register	U0BRG	?? ₁₆
03A2 ₁₆ 03A3 ₁₆	UART0 transmit buffer register	U0TB	??????? ₂ XXXXXXXX ₂
03A4 ₁₆	UART0 transmit/receive control register 0	U0C0	00001000 ₂
03A5 ₁₆	UART0 transmit/receive control register 1	U0C1	00000010 ₂
03A6 ₁₆ 03A7 ₁₆	UART0 receive buffer register	U0RB	??????? ₂ ?????XX ₂
03A8 ₁₆	UART1 transmit/receive mode register	U1MR	00 ₁₆
03A9 ₁₆	UART1 bit rate register	U1BRG	?? ₁₆
03AA ₁₆ 03AB ₁₆	UART1 transmit buffer register	U1TB	??????? ₂ XXXXXXXX ₂
03AC ₁₆	UART1 transmit/receive control register 0	U1C0	00001000 ₂
03AD ₁₆	UART1 transmit/receive control register 1	U1C1	00000010 ₂
03AE ₁₆ 03AF ₁₆	UART1 receive buffer register	U1RB	??????? ₂ ?????XX ₂
03B0 ₁₆	UART transmit/receive control register 2	UCON	X0000000 ₂
03B1 ₁₆			
03B2 ₁₆			
03B3 ₁₆			
03B4 ₁₆ 03B5 ₁₆	CRC snoop address register	CRCSAR	?? ₁₆ 00XXXX?? ₂
03B6 ₁₆ 03B7 ₁₆	CRC mode register	CRCMR	0XXXXXX0 ₂
03B8 ₁₆ 03B9 ₁₆	DMA0 request cause select register	DM0SL	00 ₁₆
03BA ₁₆ 03BB ₁₆	DMA1 request cause select register	DM1SL	00 ₁₆
03BC ₁₆ 03BD ₁₆	CRC data register	CRCD	?? ₁₆ ?? ₁₆
03BE ₁₆ 03BF ₁₆	CRC input register	CRCIN	?? ₁₆

Note 1 : The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit

? : Undefined

Address	Register	Symbol	After reset
03C0 ₁₆ 03C1 ₁₆	A/D register 0	AD0	??????? ₂ XXXXXX?? ₂
03C2 ₁₆ 03C3 ₁₆	A/D register 1	AD1	??????? ₂ XXXXXX?? ₂
03C4 ₁₆ 03C5 ₁₆	A/D register 2	AD2	??????? ₂ XXXXXX?? ₂
03C6 ₁₆ 03C7 ₁₆	A/D register 3	AD3	??????? ₂ XXXXXX?? ₂
03C8 ₁₆ 03C9 ₁₆	A/D register 4	AD4	??????? ₂ XXXXXX?? ₂
03CA ₁₆ 03CB ₁₆	A/D register 5	AD5	??????? ₂ XXXXXX?? ₂
03CC ₁₆ 03CD ₁₆	A/D register 6	AD6	??????? ₂ XXXXXX?? ₂
03CE ₁₆ 03CF ₁₆	A/D register 7	AD7	??????? ₂ XXXXXX?? ₂
03D0 ₁₆ 03D1 ₁₆			
03D2 ₁₆	A/D trigger control register	ADTRGCON	XXXX0000 ₂
03D3 ₁₆	A/D status register 0	ADSTAT0	0000X00 ₂
03D4 ₁₆ 03D5 ₁₆	A/D control register 2	ADCON2	00 ₁₆
03D6 ₁₆	A/D control register 0	ADCON0	00000??? ₂
03D7 ₁₆ 03D8 ₁₆	A/D control register 1	ADCON1	00 ₁₆
03D9 ₁₆ 03DA ₁₆			
03DB ₁₆ 03DC ₁₆			
03DD ₁₆ 03DE ₁₆			
03DF ₁₆ 03E0 ₁₆			
03E1 ₁₆	Port P1 register	P1	?? ₁₆
03E2 ₁₆ 03E3 ₁₆	Port P1 direction register	PD1	00 ₁₆
03E4 ₁₆ 03E5 ₁₆			
03E6 ₁₆ 03E7 ₁₆			
03E8 ₁₆ 03E9 ₁₆			
03EA ₁₆ 03EB ₁₆			
03EC ₁₆	Port P6 register	P6	?? ₁₆
03ED ₁₆	Port P7 register	P7	?? ₁₆
03EE ₁₆	Port P6 direction register	PD6	00 ₁₆
03EF ₁₆	Port P7 direction register	PD7	00 ₁₆
03F0 ₁₆	Port P8 register	P8	?? ₁₆
03F1 ₁₆	Port P9 register	P9	???X??? ₂
03F2 ₁₆	Port P8 direction register	PD8	00 ₁₆
03F3 ₁₆	Port P9 direction register	PD9	000X0000 ₂
03F4 ₁₆ 03F5 ₁₆	Port P10 register	P10	?? ₁₆
03F6 ₁₆	Port P10 direction register	PD10	00 ₁₆
03F7 ₁₆ 03F8 ₁₆			
03F9 ₁₆ 03FA ₁₆			
03FB ₁₆			
03FC ₁₆	Pull-up control register 0	PUR0	00 ₁₆
03FD ₁₆	Pull-up control register 1	PUR1	00 ₁₆
03FE ₁₆	Pull-up control register 2	PUR2	00 ₁₆
03FF ₁₆	Port control register	PCR	00 ₁₆

Note 1 :The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit

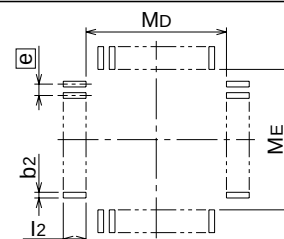
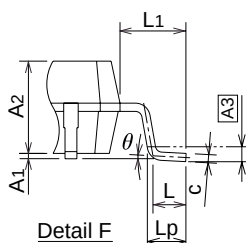
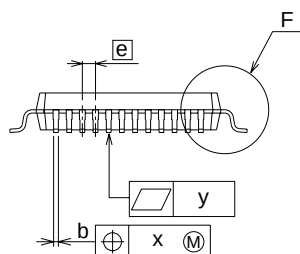
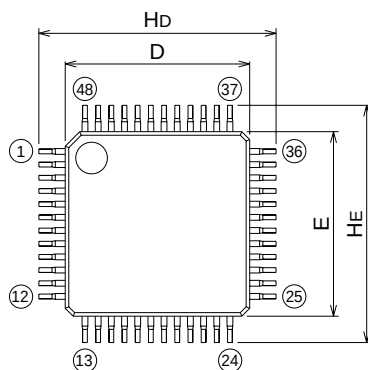
? : Undefined

5. Package

48P6Q-A Recommended

Plastic 48pin 7X7mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP48-P-77-0.50	—	—	Cu Alloy



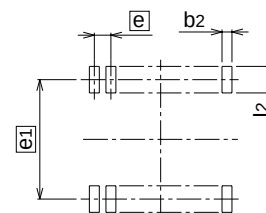
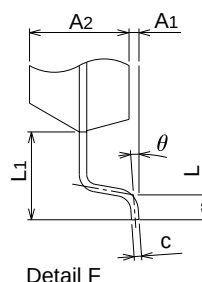
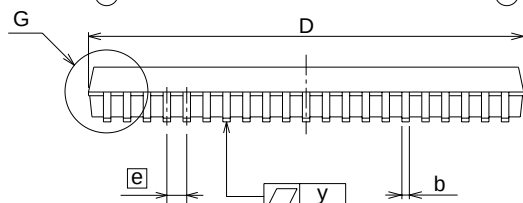
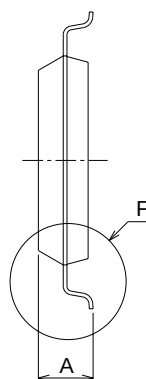
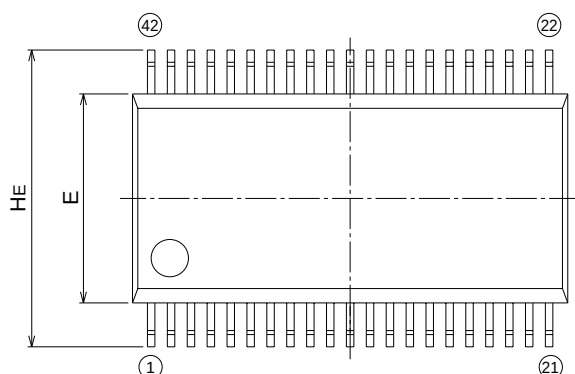
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A1	0	0.1	0.2
A2	—	1.4	—
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	—	0.5	—
Hd	8.8	9.0	9.2
HE	8.8	9.0	9.2
L	0.35	0.5	0.65
L1	—	1.0	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
x	—	—	0.08
y	—	—	0.1
theta	0°	—	8°
b2	—	0.225	—
l2	1.0	—	—
MD	—	7.4	—
ME	—	7.4	—

42P2R-E Recommended

Plastic 42pin 450mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP42-P-450-0.80	—	—	Cu Alloy+42 Alloy



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.4
A1	0.05	—	—
A2	—	2.0	—
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	17.3	17.5	17.7
E	8.2	8.4	8.6
e	—	0.8	—
HE	11.63	11.93	12.23
L	0.3	0.5	0.7
L1	—	1.765	—
Z	—	0.75	—
Z1	—	—	0.9
y	—	—	0.15
theta	0°	—	10°
b2	—	0.5	—
e1	—	11.43	—
l2	1.27	—	—

6. Functional differences

6.1 Functional differences between M16C/26A and M16C/26T

Item	M16C/26A	M16C/26T
Main Clock During and After Reset	Oscillating (Initial value of CM05 bit is set to “0” during and after reset)	Not oscillating (Initial value of CM05 bit is set to “1” during and after reset)
Voltage Detection Circuit (Function of 001916, 001A16, 001F16)	Available (Power supply detection register 1, Power supply detection register 2, Power supply down detection interrupt register)	Not available (Reserved register)
Package	48P6Q, 42P2R	48P6Q

Note. Since the emulator between the M16C/26A and M16C/29 group are same, all functions of M16C/29 are built in the emulator. When evaluating M16C/26A group, do not access to the SFR which is not built in M16C/26A group.

Refer to Hardware Manual about detail and electrical characteristics.

6.2 Functional differences between M16C/26A and M16C/26

Item	M16C/26A	M16C/26
Clock Generation Circuit	4 circuits (Main clock oscillation circuit, Sub clock oscillation circuit, On-chip oscillator, PLL frequency synthesizer)	3 circuits (Main clock oscillation circuit, Sub clock oscillation circuit, On-chip oscillator)
System Clock Source After Reset (Initial value of the CM21 bit in the CM2 register)	On-chip oscillator (Initial value "1" of CM21 bit)	Main clock (Initial value "0" of CM21 bit)
Internal RAM Retention limit Detection Circuit (The b5 bit in the VCR2 register)	Available (VC25 bit)	Not available (Reserved bit)
On-chip Oscillator Clock	Selectable (8MHz/1MHz/500KHz)	Fixed (1MHz)
PACR2 to PACR0 in the PACR Register	Necessary to set after reset 48pin:"1002", 42pin:"0012"	No PACR register
IFSR20 Bit in the IFSR2A Register	Necessary to set to "1" after reset	No IFSR2A register
External Interrupt	8 causes (INT2 added)	7 causes
13 pin (48-pin version) Function	INT2/ZP	IVcc
P70, P71	N-ch open drain output and CMOS output are selectable by S/W	N-ch open drain output
A/D Input Pin (48-pin version)	12 channels	8 channels
A/D Operation Mode	8 modes (single, repeat, single sweep, repeat sweep mode 0, repeat sweep mode 1, simultaneous sampling, delayed trigger mode 0, delayed trigger mode 1) 1 shunt current measurement function is available	5 modes (single, repeat, single sweep, repeat sweep mode 0, repeat sweep mode 1)
Timer B Operation Mode	5 modes (timer, event counter, pulse periods measurement, pulse width measurement, A/D trigger) 1 shunt current measurement function is available	4 modes (timer, event counter, pulse periods measurement, pulse width measurement)
CRC Calculation	Available (compatible to CRC-CCITT and CRC-16 methods)	Not available
Three-Phase Motor Control	•Waveform output/Switching port output by software is enabled •Position-data-retain function	•Waveform output/Switching port output by software is disabled •No position-data-retain function
Digital Debounce Function	This function is in the NMI/SD pin and INT5 pin	Not available
3 pin (48-pin version) Function	P90/CLKOUT/TB0IN/AN30 (CLKOUT: f1, f8, f32, and fc output)	P90/TB0IN
UART1 Compatible Pin	Switching to P64 to P67 or P70 to P73 is enabled	P64 to P67
Flash Memory Protect Function	Protection to blocks 0, 1 by FMR02 bit Protection to the blocks 0 to 3 by FMR16 bit	Protection to blocks 0,1 by FMR02 bit
Package	48P6Q, 42P2R	48P6Q

Note. Since the emulator between the M16C/26A and M16C/29 group are same, all functions of M16C/29 are built in the emulator. When evaluating M16C/26A group, do not access to the SFR which is not built in M16C/26A group.

Refer to Hardware Manual about detail and electrical characteristics.

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