ATPL230A

ATPL Series Power Line Communications Device

DATASHEET

Description

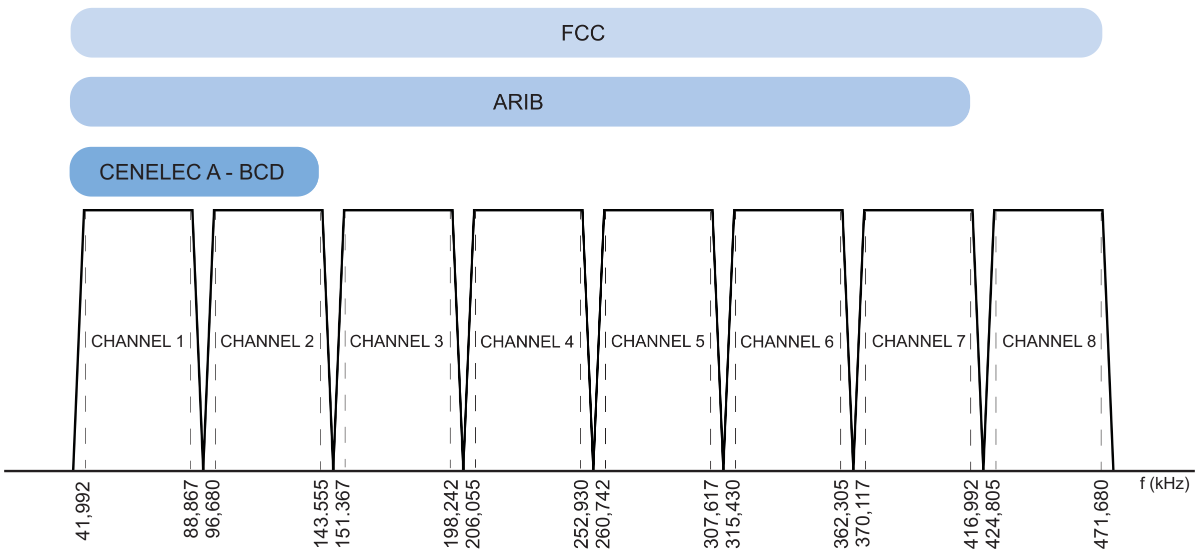
ATPL230A is a power line communications base band modem, compliant with the PHY layer of PRIME (Power Line Intelligent Metering Evolution) specification. PRIME is an open standard technology used for Smart Grid applications like Smart Metering, Industrial Lighting and Automation, Home Automation, Street Lighting, Solar Energy and PHEV Charging Stations.

ATPL230A PRIME device includes enhanced features such as additional robust modes and frequency band extension. ATPL230A is able to operate in independently selectable transmission bands up to 472 kHz, achieving baud rates ranging from 5.4 kbps up to 128.6 kbps.

ATPL230A has been conceived to be bundled with an external Atmel® MCU or MPU. Atmel provides a PRIME PHY layer library which is used by the external MCU/MPU to take control of ATPL230A PHY layer device.

1. Features

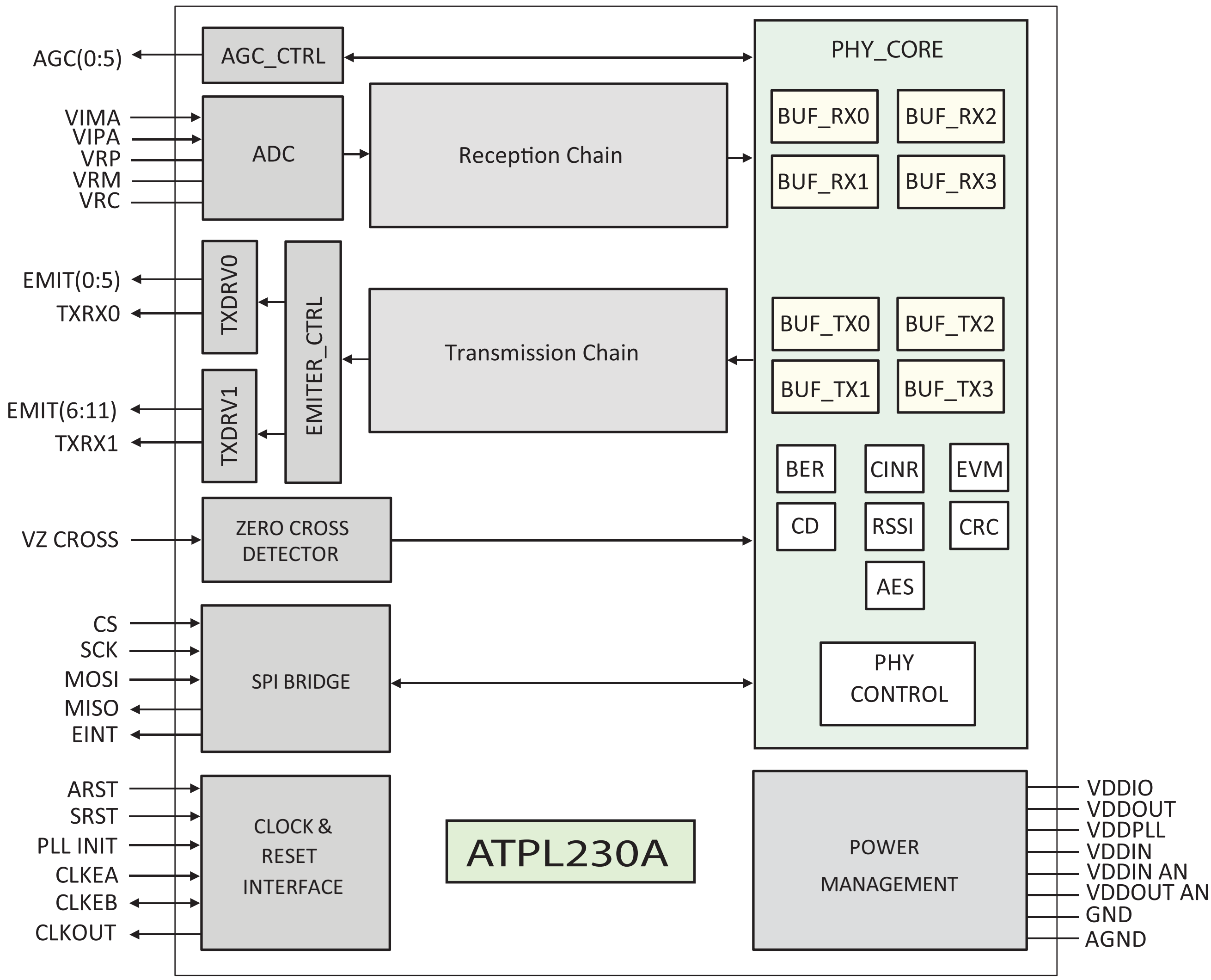
- Modem
  - Power Line Carrier Modem for 50 Hz and 60 Hz mains
  - 97-carriers OFDM PRIME compliant
  - DBPSK, DQPSK, D8PSK modulation schemes available
  - Additional enhanced modes available: DBPSK Robust and DQPSK Robust
  - Eight selectable channels between 42kHz and 472kHz available. Only one channel can be active at a time



  - Baud rate Selectable: 5.4 to 128.6 kbps
  - Four dedicated buffers for transmission/reception
  - Up to 124.6 dBµVrms injected signal against PRIME load
  - Up to 79.6 dB of dynamic range in PRIME networks
- Automatic Gain Control and continuous amplitude tracking in signal reception
- Class D switching power amplifier control
- Integrated 1.2V LDO regulator to supply analog functions
- Medium Access Control co-processor features
  - Viterbi soft decoding and PRIME CRC calculation
  - 128-bit AES encryption
  - Channel sensing and collision pre-detection

2. Block Diagram

Figure 2-1. ATPL230A Functional Block Diagram



3. Signal Description

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Power Supplies					
VDDIO	3.3V digital supply. Digital power supply must be decoupled by external capacitors	Power			3.0V to 3.6V
VDDIN	3.3V Digital LDO input supply	Power			3.0V to 3.6V
VDDIN AN	3.3V Analog LDO input supply	Power			3.0V to 3.6V
VDDOUT AN	1.2V Analog LDO output. A capacitor in the range 0.1µF - 10µF must be connected to each pin	Power			1.2V
VDDOUT	1.2V Digital LDO output. A capacitor in the range 0.1µF - 10µF must be connected to each pin	Power			1.2V
VDDPLL	1.2V PLL supply. It must be decoupled by a 100nF external capacitor, and connected to VDDOUT through a filter (Cut off frequency: 25kHz)	Power			1.2V
GND(1)	Digital Ground	Power			
AGND(1)	Analog Ground	Power			
Clocks, Oscillators and PLLs					
CLKEA(2)	External Clock Oscillator • CLKEA must be connected to one terminal of a crystal (when a crystal is being used) or used as input for external clock signal	Input		VDDIO	
CLKEB(2)	External Clock Oscillator • CLKEB must be connected to one terminal of a crystal (when a crystal is being used) or must be floating when an external clock signal is connected through CLKEA	I/O		VDDIO	
CLKOUT	10MHz External Clock Output	Output		VDDIO	
Reset/Test					
ARST	Asynchronous Reset	Input	Low	VDDIO	Internal pull up(3)
SRST	Synchronous Reset	Input	Low	VDDIO	Internal pull up(3)
PLL INIT	PLL Initialization Signal	Input	Low	VDDIO	Internal pull up(3)
PPLC (PRIME Power Line Communications) Transceiver					
EMIT [0:11](4)	PLC Tri-state Transmission ports	Output		VDDIO	
AGC [0:5]	Automatic Gain Control: • These digital tri-state outputs are managed by AGC hardware logic to drive external circuitry when input signal attenuation is needed	Output		VDDIO	

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage reference	Comments
TXRX0	Analog Front-End Transmission/Reception for TXDRV0 • This digital output is used to modify external coupling behavior in Transmission/Reception. The suitable value depends on the external circuitry configuration. The polarity of this pin can be inverted by software.	Output		VDDIO	
TXRX1	Analog Front-End Transmission/Reception for TXDRV1 • This digital output is used to modify external coupling behavior in Transmission/Reception. The suitable value depends on the external circuitry configuration. The polarity of this pin can be inverted by software.	Output		VDDIO	
VZ CROSS(5)	Mains Zero-Cross Detection Signal: • This input detects the zero-crossing of the mains voltage	Input		VDDIO	Internal pull down(3)
VIMA	Negative Differential Voltage Input	Input		VDDOUT AN	
VIPA	Positive Differential Voltage Input	Input		VDDOUT AN	
VRP	Internal Reference “Plus” Voltage. Connect an external decoupling capacitor between VRP and VRM (1nF - 100nF)	Output		VDDOUT AN	
VRM	Internal Reference “Minus” Voltage. Connect an external decoupling capacitor between VRP and VRM (1nF - 100nF)	Output		VDDOUT AN	
VRC	Common-mode Voltage. Bypass to analog ground with an external decoupling capacitor (100pF - 1nF)	Output		VDDOUT AN	
Serial Peripheral Interface - SPI					
CS	SPI CS • SPI bridge Slave Select	Input	Low	VDDIO	Internal pull up(3)
SCK	SPI SCK • SPI bridge Clock signal	Input		VDDIO	Internal pull up(3)
MOSI	SPI MOSI • SPI bridge Master Out Slave In	Input		VDDIO	Internal pull up(3)
MISO	SPI MISO • SPI bridge Master In Slave Out	Output		VDDIO	
EINT	PHY Layer External Interrupt	Output	Low	VDDIO	

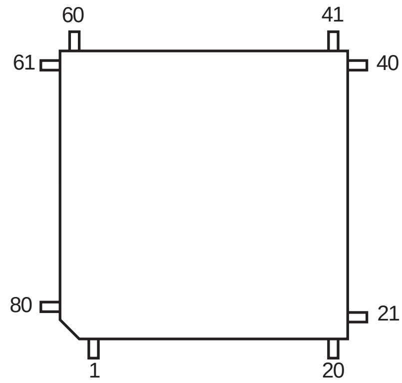
Notes: 1. Separate pins are provided for GND and AGND grounds. Layout considerations should be taken into account to reduce interference. Ground pins should be connected as shortly as possible to the system ground plane. For more details about EMC Considerations, please refer to AVR040 application note.

2. The crystal should be located as close as possible to CLKEA and CLKEB pins. See Table 10-7 on page 112.
3. See Table 10-5 on page 109.
4. Different configurations allowed depending on external topology and net behavior.
5. Depending on whether an isolated or a non-isolated power supply is being used, isolation of this pin should be taken into account in the circuitry design. Please refer to the Reference Design for further information.

4. Package and Pinout

4.1 80-Lead LQFP Package Outline

Figure 4-1. Orientation of the 80-Lead LQFP Package



4.2 80-Lead LQFP Pinout

Table 4-1. 80 - Lead LQFP Pinout

1	NC	21	VDDIO	41	GND	61	GND
2	NC	22	NC	42	EMIT8	62	AGND
3	NC	23	CLKOUT	43	EMIT9	63	VDDOUT AN
4	ARST	24	CS	44	EMIT10	64	VIMA
5	PLL INIT	25	SCK	45	EMIT11	65	VIPA
6	GND	26	MOSI	46	VDDIO	66	VDDOUT AN
7	CLKEA	27	MISO	47	GND	67	AGND
8	GND	28	VDDIO	48	VDDOUT	68	VRP
9	CLKEB	29	GND	49	TXRX0	69	VRM
10	VDDIO	30	EMIT0	50	TXRX1	70	VRC
11	GND	31	EMIT1	51	GND	71	VDDIN AN
12	VDDPLL	32	EMIT2	52	AGC2	72	AGND
13	GND	33	EMIT3	53	AGC5	73	AGND
14	VDDIN	34	VDDIO	54	AGC1	74	VDDIN AN
15	VDDIN	35	GND	55	AGC4	75	GND
16	GND	36	EMIT4	56	AGC0	76	VDDIO
17	VDDOUT	37	EMIT5	57	AGC3	77	VZ CROSS
18	GND	38	EMIT6	58	VDDIO	78	NC
19	NC	39	EMIT7	59	GND	79	NC
20	SRST	40	VDDIO	60	EINT	80	NC

5. Analog Front-End

5.1 PLC coupling circuitry description

Atmel PLC coupling reference designs have been designed to achieve high performance, low cost and simplicity.

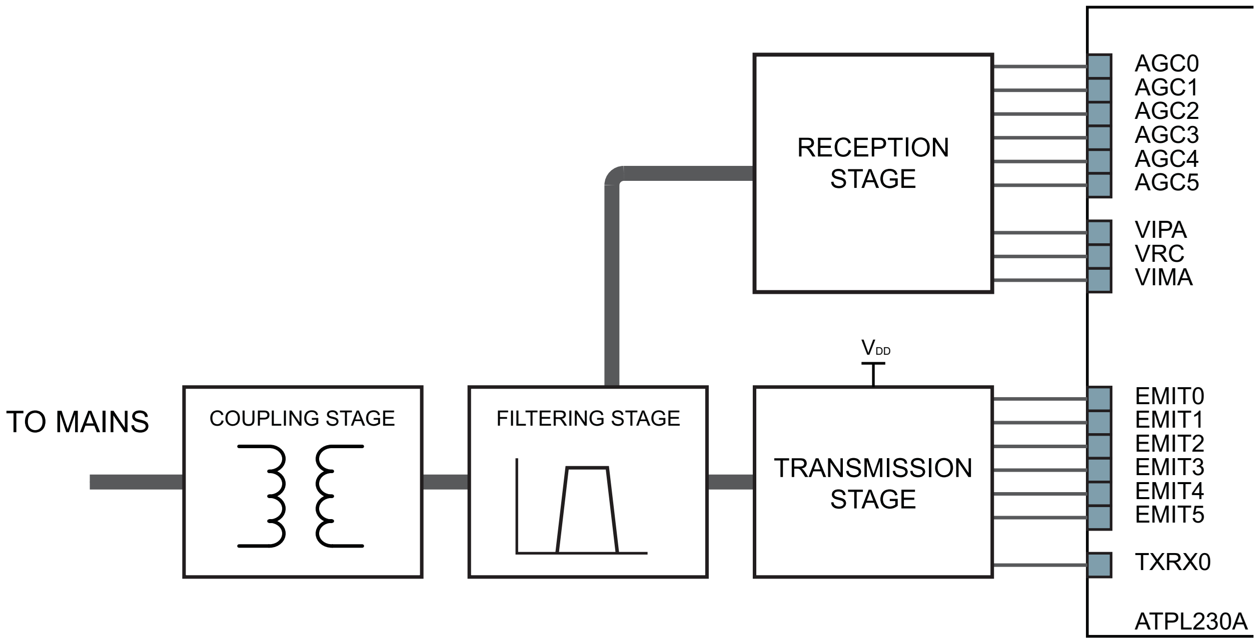
With these values on mind, Atmel has developed a set of PLC couplings covering frequencies up to 472 kHz compliant with different applicable regulations.

Atmel PLC technology is purely digital and does not require external DAC/ADC, thus simplifying the external required circuitry. Generally Atmel PLC coupling reference designs make use of few passive components plus a Class D amplification stage for transmission.

All PLC coupling reference designs are generally composed by the same sub-circuits:

- Transmission Stage
- Reception Stage
- Filtering Stage
- Coupling Stage

Figure 5-1. PLC coupling block diagram



A particular reference design can contain more than one sub-circuit of the same kind (i.e.: two transmission stages).

5.1.1 Transmission Stage

The transmission stage adapts the EMIT signals and amplifies them if required. It can be composed by:

- Driver: A group of resistors which adapt the EMIT signals to either control the Class-D amplifier or to be filtered by the next stage.
- Amplifier: If required, a Class-D amplifier which generates a square waveform from 0 to V_{DD} is included.
- Bias and protection: A couple of resistors and a couple of Schottky barrier diodes provide a DC component and provide protection from received disturbances.

Transmission stage shall be always followed by a filtering stage.

5.1.2 Filtering Stage

The filtering stage is composed by band-pass filters which have been designed to achieve high performance in field deployments complying at the same time with the proper normative and standards.

The in-band flat response filtering stage does not distort the injected signal, reduces spurious emission to the limits set by the corresponding regulation and blocks potential interferences from other transmission channels.

The filtering stage has three aims:

- Band-pass filtering of high frequency components of the square waveform generated by the transmission stage
- Adapt Input/Output impedances for optimal reception/transmission. This is controlled by TXRX signals
- In some cases, Band-pass filtering for received signals

When the system is intended to be connected to a physical channel with high voltage or which is not electrically referenced to the same point then the filtering stage must be always followed by a coupling stage.

5.1.3 Coupling Stage

The coupling stage blocks the DC component of the line to/from which the signal is injected/received (i.e.: 50/60 Hz of the mains). This is carried out by a high voltage capacitor.

Coupling stage could also electrically isolate the coupling circuitry from the external world by means of a 1:1 transformer.

5.1.4 Reception Stage

The reception stage adapts the received analog signal to be properly captured by the ATPL230A internal reception chain. Reception circuit is independent of the PLC channel which is being used. It basically consists of:

- Anti aliasing filter (RC Filter)
- Automatic Gain Control (AGC) circuit
- Driver of the internal ADC

The AGC circuit avoids distortion on the received signal that may arise when the input signal is high enough to polarize the protective diodes in direct region.

The driver to the internal ADC comprises a couple of resistors and a couple of capacitors. This driver provides a DC component and adapts the received signal to be properly converted by the internal reception chain.

5.1.5 Generic PLC Coupling

Please consider that this is a generic PLC Coupling design for a particular application please refer to Atmel doc43052 "PLC Coupling Reference Designs".

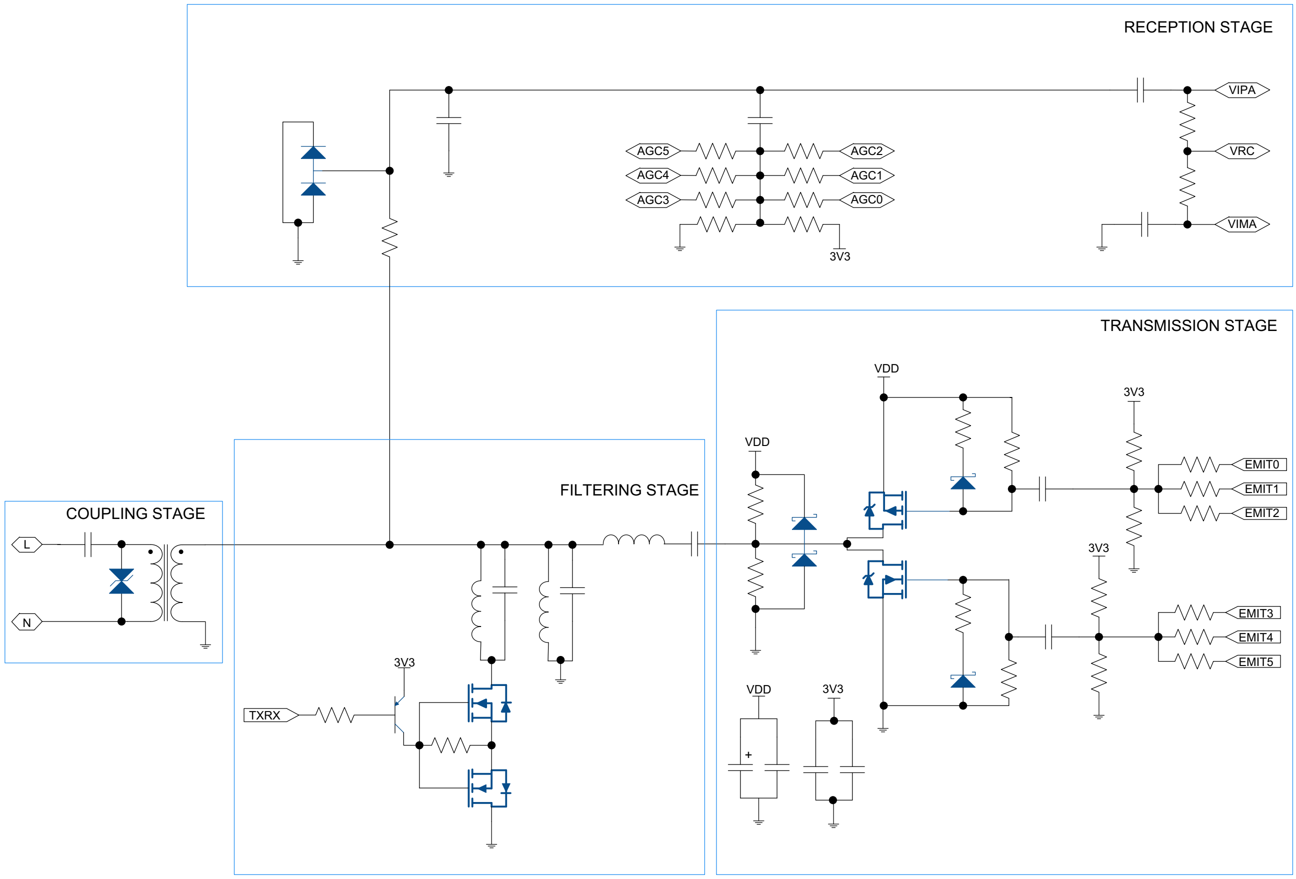


Figure 5-2. PLC Coupling block diagram detailed

5.2 ATPLCOUP reference designs

Atmel provides PLC coupling reference designs for different applications and frequency bands up to 500 kHz. Please refer to Atmel doc43052 "PLC Coupling Reference Designs" for a detailed description.

5.3 Zero-crossing detection

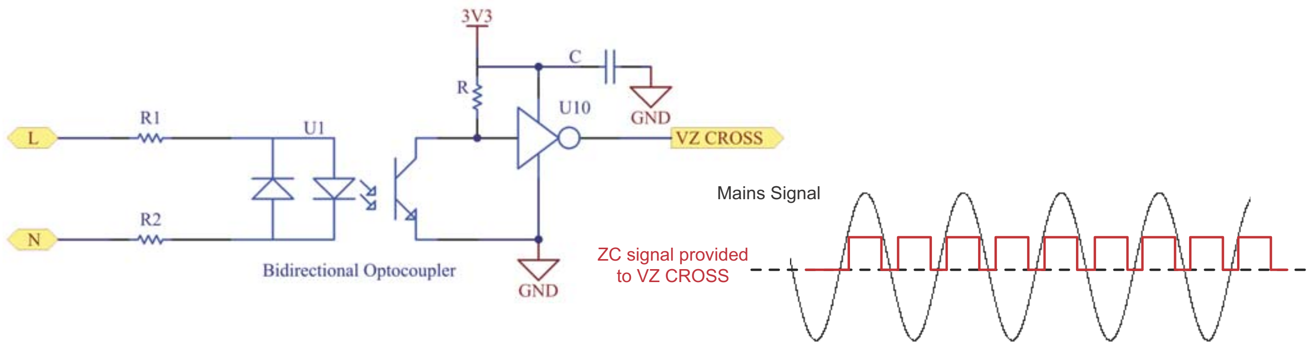
5.3.1 Overview

Zero Crossing Detector block works predicting future zero crossings of the Mains signal in function of its past zero crossings. To achieve this, the system embeds a configurable Input Signal Management (ISM) block and a PLL, both of which manage Zero Crossing Detector Input Signal to calculate Zero Crossing Output Flag. The zero-cross detection of waves of 50 Hz and 60 Hz with ±10% of error is supported.

The PLL block interprets its input signal such a way that it indicates a zero cross in the middle of a positive pulse. It is important to note that depending on the external circuit implementing the Zero Crossing Detector Input Signal this interpretation is not always correct. Thus, for some cases it is required to transform the Input Signal in a signal where the middle of a positive pulse corresponds to a truly zero cross. This transformation is implemented through the Input Signal Management (ISM) block, configured by MODE_INV and MODE_REP fields in ZC_CONFIG register.

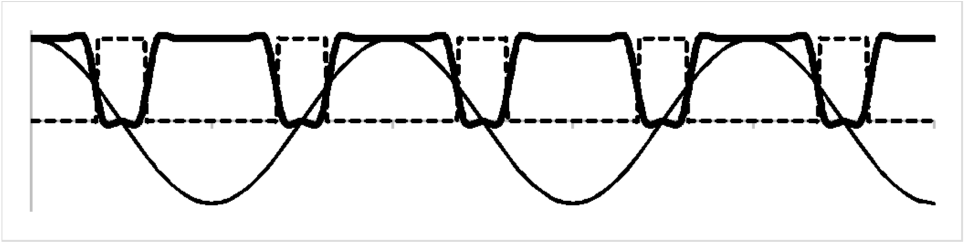
Zero Crossing Detector Input Signal (VZ CROSS) must fulfil some requirements. The first requirement is that VZ CROSS signal must be a pulse train with a duty cycle being >60% or <40% (polarity is configurable). In addition, if we have to detect ascent or descent zero-crossing, the Zero Crossing Detector Input Signal period must be equal than the period of the wave we need to obtain zero-crossing. Ascent and descent Zero Crossing Detection are configured by setting MODE_MUX and MODE_ASC fields in ZC_CONFIG register.

Figure 5-3. Typical circuit, using a bidirectional optocoupler and a Schmitt trigger



The input signal "VZ CROSS" (wider line) generated by this circuit for Zero Cross Detection of the wave "L"-"N" (finer line) is plotted in next figure. The digital signal at output of Input Signal Management (ISM) is plotted in Figure 5-4.

Figure 5-4. Digital signal (dashed line) at output of Input Signal Management (ISM) internal block

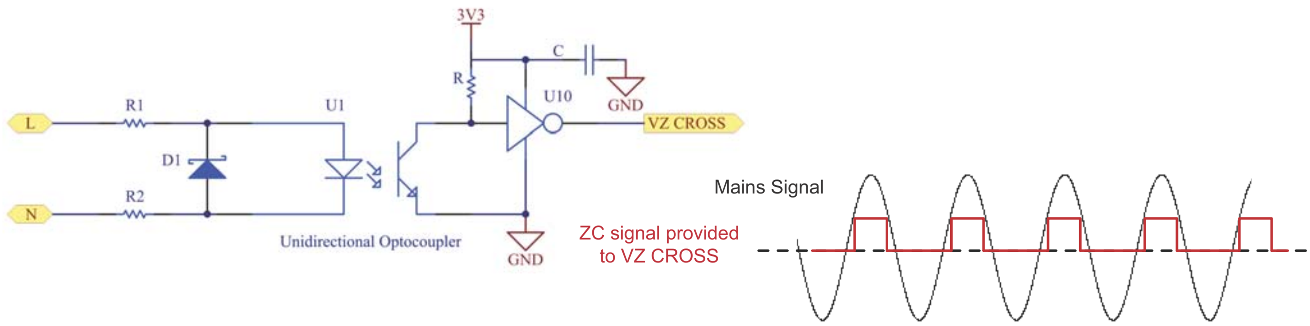


For this circuit, Zero Cross Internal registers should be configured this way:

ZC_CONFIG.MODE_MUX = '0'
ZC_CONFIG.MODE_ASC = '0'
ZC_CONFIG.MODE_INV = '1'
ZC_CONFIG.MODE_REP = '0'
ZC_FILTER.ZC_FILTER_BP = '0'

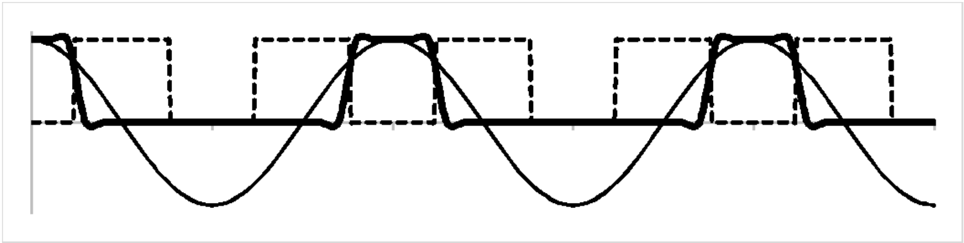
Some situations (for example in some protocols needing to differentiate rising/falling edges in mains signal) could require only ascent (or descent) mains signal zero-crossings to be detected. When we have to detect ascent or descent Zero-Cross of the wave (finer line), the circuit should generate an input signal "VZ CROSS" (wider line) with the same period, as specified in next figure. This could be easily implemented by using an unidirectional optocoupler or a Zener diode topology in the external circuitry.

Figure 5-5. Typical circuit, using a unidirectional optocoupler and a Schmitt trigger



The digital signal at output of Input Signal Management (ISM) is plotted in Figure 5-6.

Figure 5-6. Digital signal (dashed line) at output of Input Signal Management (ISM) internal block



For this case, Zero Cross Internal registers should be configured this way:

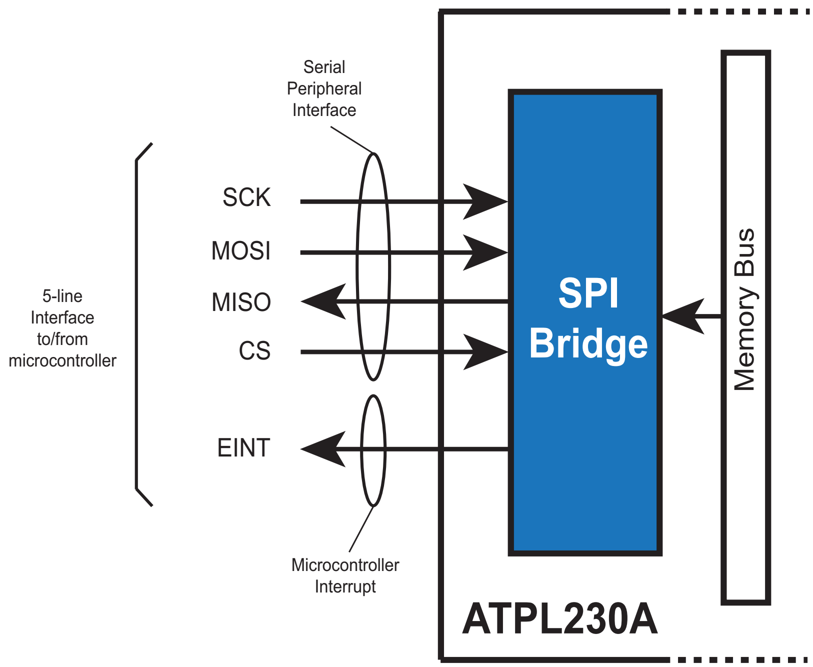
ZC_CONFIG.MODE_MUX = '1'
ZC_CONFIG.MODE_ASC = '0'(ascent) or '1'(descent)
ZC_CONFIG.MODE_INV = '1'
ZC_CONFIG.MODE_REP = '1'
ZC_FILTER.ZC_FILTER_BP = '0'

See register description in Section 9.3.7.2 "Zero Crossing Configuration Register" and Section 9.3.7.3 "Zero Crossing Filter Register".

6. SPI Controller

ATPL230A has been conceived to be easily managed by an external microcontroller through a 5-line interface. This interface is comprised of a 4-line standard Serial Peripheral Interface (SPI) and an additional line used as interrupt from the ATPL230A to the external microcontroller. A diagram is shown below.

Figure 6-1. SPI Controller Block Diagram

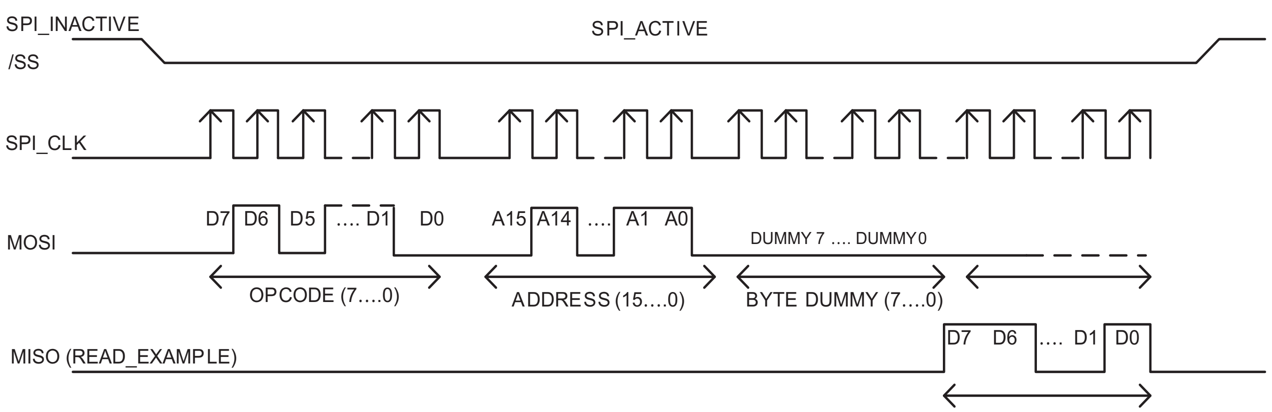


By means of this SPI interface, an external microcontroller can access the ATPL230A and can carry out "write", "write_rep", "read" and "mask" operations. All the "Peripheral Registers" in ATPL230A are reachable via the SPI interface, thus the microcontroller can fully manage and control the ATPL230A (PHY layer, MAC co-processing, etc).

6.1 Serial Peripheral Interface

The Serial Peripheral Interface Bus or SPI bus is a synchronous serial data link standard. Devices communicate in master/slave mode where the master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip select) lines.

Figure 6-2. SPI Communication Example in ATPL230A



The ATPL230A SPI allows an external device (working as a master), to communicate with the ATPL230A (working as a slave). Below is a brief description of the SPI signals:

- **CS, Chip Select (pin no.24):** This input enables/disables the slave SPI. The ATPL230A is configured to work always as a slave. When disabled (CS pin is tied high), the other SPI signals (SCK, MOSI and MISO) are not taken into account.

  CS = '0': SPI enabled.

  CS = '1': SPI disabled.

- **SCK, Serial Peripheral Interface Clock (pin no.25):** In reception (master slave), data is read from MOSI line in the rising edge of the SPI clock. In transmission (slave master), data is released to MISO in the falling edge of the SPI clock.

  It is recommended not to work with clock frequencies above 10MHz.

  This input only will be taken into account when CS='0'.

- **MOSI, Master Out Slave In (pin no.26):** MOSI is the slave's data input line. Data is read from MOSI line in the rising edge of SCK.

  This input only will be taken into account when CS='0'.

- **MISO, Master In Slave Out (pin no.27):** MISO is the slave's data output line. Data is released to MISO in the falling edge of SCK.

Furthermore, ATPL230A SPI bridge uses an additional line to send interrupts to the host CPU:

- **EINT (pin no.60):** This signal is an interrupt from ATPL230A PHY layer to the microcontroller.

  In reception, every time a PLC message is received, the PHY Layer generates two interrupts. One of them when the physical header is correctly received (two first symbols), and the other one when the message is completely received.

  In transmission, an interrupt will be generated every time a complete message has been sent.

  This signal is low level active.

6.2 SPI Operation

When establishing a SPI communication (CS line is set to '0' by the master), the first byte sent through MOSI line corresponds to the operation code. Four different operation types are defined over ATPL230A SPI. The operation codes are shown in the following table:

Table 6-1. Operation Codes

Operation	Mask type	OpCode
Read	---	0x63
Write	---	0x2A
Mask	AND	0x4C
	OR	0x71
	XOR	0x6D
Write_rep	---	0x1E

Following the operation code, the second and third bytes correspond to the SRAM address (16-bit address). Depending on the operation code, the master will "read data from"/"write data to"/"mask data in"/"write some data to" that address.

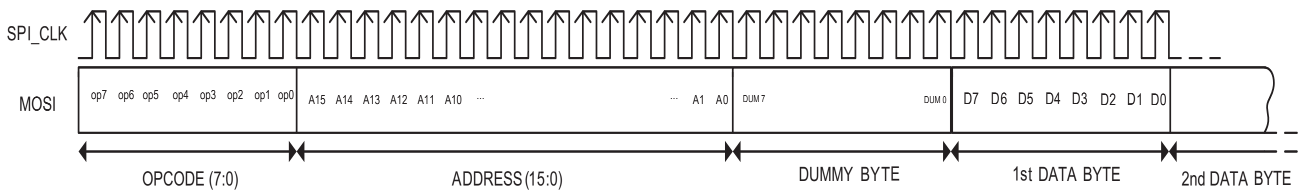
After the address, a dummy byte is sent.

Following the dummy byte, n data bytes (where n ≥ 1) are sent/received:

- If the operation code corresponds to a write operation in memory, the first data byte will be written in the specified address. If more data bytes are sent, they will be written in subsequent memory positions.
- If the operation code corresponds to a read operation from memory, the ATPL230A will output the data byte in MISO line. If the master continues sending SCK cycles, subsequent memory positions will be written in MISO line by the slave.
- If the operation code corresponds to a mask operation (AND, OR, XOR), the master will send the byte mask that have to be applied to the byte located at the specified address memory. If the master continues sending bytes, they will be applied as masks to the bytes stored in subsequent memory positions.
- If the operation code corresponds to a write_rep operation in memory, the dummy byte is changed by a number between 0x00 and 0xFF, called OFFSET_ADDRESS. Data bytes will be written from ADDRESS to ADDRESS+OFFSET_ADDRESS. For example, if OFFSET_ADDRESS = 0x04, the five first data bytes will be written between ADDRESS and ADDRESS+4, and then, the sixth data byte, will be written in ADDRESS, the seventh in ADDRESS+1, and so on. It is used to fill the some memories in PHY Layer (Chirp, Angle and IIR).

Bytes will be always sent with the most significant bit first.

Figure 6-3. SPI Frame Example



7. Peripheral Registers

A total of 768 bytes are reserved on-chip to allocate the system peripheral registers.

A detailed description of each peripheral register can be found in its corresponding section. On the next pages, there is a list of all of them.

Table 7-1. Register Mapping

Address	Register	Name	Access	Reset
0xFD00 - 0xFD03	TX Time Registers	TXRXBUF_EMITIME_TX0	Read/Write	0x00..00
0xFD04 - 0xFD07		TXRXBUF_EMITIME_TX1	Read/Write	0x00..00
0xFD08 - 0xFD0B		TXRXBUF_EMITIME_TX2	Read/Write	0x00..00
0xFD0C - 0xFD0F		TXRXBUF_EMITIME_TX3	Read/Write	0x00..00
0xFD10 - 0xFD11	TX Post-activation Time TxRx Registers	TXRXBUF_TXRX_TA_TX0	Read/Write	0x0000
0xFD12 - 0xFD13		TXRXBUF_TXRX_TA_TX1	Read/Write	0x0000
0xFD14 - 0xFD15		TXRXBUF_TXRX_TA_TX2	Read/Write	0x0000
0xFD16 - 0xFD17		TXRXBUF_TXRX_TA_TX3	Read/Write	0x0000
0xFD18 - 0xFD19	TX Pre-activation Time TxRx Registers	TXRXBUF_TXRX_TB_TX0	Read/Write	0x0000
0xFD1A - 0xFD1B		TXRXBUF_TXRX_TB_TX1	Read/Write	0x0000
0xFD1C - 0xFD1D		TXRXBUF_TXRX_TB_TX2	Read/Write	0x0000
0xFD1E - 0xFD1F		TXRXBUF_TXRX_TB_TX3	Read/Write	0x0000
0xFD20	Global Amplitude Registers	TXRXBUF_GLBL_AMP_TX0	Read/Write	0xFF
0xFD21		TXRXBUF_GLBL_AMP_TX1	Read/Write	0xFF
0xFD22		TXRXBUF_GLBL_AMP_TX2	Read/Write	0xFF
0xFD23		TXRXBUF_GLBL_AMP_TX3	Read/Write	0xFF
0xFD24	Signal Amplitude Registers	TXRXBUF_SGNL_AMP_TX0	Read/Write	0x60
0xFD25		TXRXBUF_SGNL_AMP_TX1	Read/Write	0x60
0xFD26		TXRXBUF_SGNL_AMP_TX2	Read/Write	0x60
0xFD27		TXRXBUF_SGNL_AMP_TX3	Read/Write	0x60
0xFD28	Chirp Amplitude Registers	TXRXBUF_CHIRP_AMP_TX0	Read/Write	0x60
0xFD29		TXRXBUF_CHIRP_AMP_TX1	Read/Write	0x60
0xFD2A		TXRXBUF_CHIRP_AMP_TX2	Read/Write	0x60
0xFD2B		TXRXBUF_CHIRP_AMP_TX3	Read/Write	0x60
0xFD2C - 0xFD2F	TX Timeout Registers	TXRXBUF_TIMEOUT_TX0	Read/Write	0x000124F8
0xFD30 - 0xFD33		TXRXBUF_TIMEOUT_TX1	Read/Write	0x000124F8
0xFD34 - 0xFD37		TXRXBUF_TIMEOUT_TX2	Read/Write	0x000124F8
0xFD38 - 0xFD3B		TXRXBUF_TIMEOUT_TX3	Read/Write	0x000124F8
0xFD3C	TX Configuration Registers	TXRXBUF_TXCONF_TX0	Read/Write	0xA0
0xFD3D		TXRXBUF_TXCONF_TX1	Read/Write	0xA0
0xFD3E		TXRXBUF_TXCONF_TX2	Read/Write	0xA0
0xFD3F		TXRXBUF_TXCONF_TX3	Read/Write	0xA0
0xFD40 - 0xFD41	TX Initial Address Registers	TXRXBUF_INITAD_TX0	Read/Write	0x0000
0xFD42 - 0xFD43		TXRXBUF_INITAD_TX1	Read/Write	0x0000
0xFD44 - 0xFD45		TXRXBUF_INITAD_TX2	Read/Write	0x0000
0xFD46 - 0xFD47		TXRXBUF_INITAD_TX3	Read/Write	0x0000

Table 7-1. Register Mapping

Address	Register	Name	Access	Reset
0xFD48 - 0xFD49	Reserved	-	-	0x0000
0xFD4A - 0xFD4B		-	-	0x0000
0xFD4C - 0xFD4D		-	-	0x0000
0xFD4E - 0xFD4F		-	-	0x0000
0xFD50 - 0xFD51	TX Result Register	TXRXBUF_RESULT_TX	Read-only	0x1111
0xFD52	TX Interrupts Register	TXRXBUF_TX_INT	Read-only	0x00
0xFD53	Reserved	-	-	0x00
0xFD54		-	-	0x00
0xFD55		-	-	0x00
0xFD56		-	-	0x00
0xFD57	BER SOFT Average Error Registers	TXRXBUF_BERSOFT_AVG_RX0	Read-only	0x00
0xFD58		TXRXBUF_BERSOFT_AVG_RX1	Read-only	0x00
0xFD59		TXRXBUF_BERSOFT_AVG_RX2	Read-only	0x00
0xFD5A		TXRXBUF_BERSOFT_AVG_RX3	Read-only	0x00
0xFD5B	BER SOFT Maximum Error Registers	TXRXBUF_BERSOFT_MAX_RX0	Read-only	0x00
0xFD5C		TXRXBUF_BERSOFT_MAX_RX1	Read-only	0x00
0xFD5D		TXRXBUF_BERSOFT_MAX_RX2	Read-only	0x00
0xFD5E		TXRXBUF_BERSOFT_MAX_RX3	Read-only	0x00
0xFD5F	Reserved	-	-	0x00
0xFD60		-	-	0x00
0xFD61		-	-	0x00
0xFD62		-	-	0x00
0xFD63	BER HARD Average Error Registers	TXRXBUF_BERHARD_AVG_RX0	Read-only	0x00
0xFD64		TXRXBUF_BERHARD_AVG_RX1	Read-only	0x00
0xFD65		TXRXBUF_BERHARD_AVG_RX2	Read-only	0x00
0xFD66		TXRXBUF_BERHARD_AVG_RX3	Read-only	0x00
0xFD67	BER HARD Maximum Error Registers	TXRXBUF_BERHARD_MAX_RX0	Read-only	0x00
0xFD68		TXRXBUF_BERHARD_MAX_RX1	Read-only	0x00
0xFD69		TXRXBUF_BERHARD_MAX_RX2	Read-only	0x00
0xFD6A		TXRXBUF_BERHARD_MAX_RX3	Read-only	0x00
0xFD6B	Minimum RSSI Registers	TXRXBUF_RSSIMIN_RX0	Read-only	0x00
0xFD6C		TXRXBUF_RSSIMIN_RX1	Read-only	0x00
0xFD6D		TXRXBUF_RSSIMIN_RX2	Read-only	0x00
0xFD6E		TXRXBUF_RSSIMIN_RX3	Read-only	0x00
0xFD6F	Average RSSI Registers	TXRXBUF_RSSIAVG_RX0	Read-only	0x00
0xFD70		TXRXBUF_RSSIAVG_RX1	Read-only	0x00
0xFD71		TXRXBUF_RSSIAVG_RX2	Read-only	0x00
0xFD72		TXRXBUF_RSSIAVG_RX3	Read-only	0x00
0xFD73	Maximum RSSI Registers	TXRXBUF_RSSIMAX_RX0	Read-only	0x00
0xFD74		TXRXBUF_RSSIMAX_RX1	Read-only	0x00
0xFD75		TXRXBUF_RSSIMAX_RX2	Read-only	0x00
0xFD76		TXRXBUF_RSSIMAX_RX3	Read-only	0x00

Table 7-1. Register Mapping

Address	Register	Name	Access	Reset
0xFD77	Minimum CINR Registers	TXRXBUF_CINRMIN_RX0	Read-only	0x00
0xFD78		TXRXBUF_CINRMIN_RX1	Read-only	0x00
0xFD79		TXRXBUF_CINRMIN_RX2	Read-only	0x00
0xFD7A		TXRXBUF_CINRMIN_RX3	Read-only	0x00
0xFD7B	Average CINR Registers	TXRXBUF_CINRAVG_RX0	Read-only	0x00
0xFD7C		TXRXBUF_CINRAVG_RX1	Read-only	0x00
0xFD7D		TXRXBUF_CINRAVG_RX2	Read-only	0x00
0xFD7E		TXRXBUF_CINRAVG_RX3	Read-only	0x00
0xFD7F	Maximum CINR Registers	TXRXBUF_CINRMAX_RX0	Read-only	0x00
0xFD80		TXRXBUF_CINRMAX_RX1	Read-only	0x00
0xFD81		TXRXBUF_CINRMAX_RX2	Read-only	0x00
0xFD82		TXRXBUF_CINRMAX_RX3	Read-only	0x00
0xFD83 - 0xFD86	RX Time Registers	TXRXBUF_RECTIME_RX0	Read-only	0x00..00
0xFD87 - 0xFD8A		TXRXBUF_RECTIME_RX1	Read-only	0x00..00
0xFD8B - 0xFD8E		TXRXBUF_RECTIME_RX2	Read-only	0x00..00
0xFD8F - 0xFD92		TXRXBUF_RECTIME_RX3	Read-only	0x00..00
0xFD93 - 0xFD96	Zero-Cross Time Registers	TXRXBUF_ZCT_RX0	Read-only	0x00..00
0xFD97 - 0xFD9A		TXRXBUF_ZCT_RX1	Read-only	0x00..00
0xFD9B - 0xFD9E		TXRXBUF_ZCT_RX2	Read-only	0x00..00
0xFD9F - 0xFDA2		TXRXBUF_ZCT_RX3	Read-only	0x00..00
0xFDA3 - 0xFDA4	Header EVM Registers	TXRXBUF_EVM_HD_RX0	Read-only	0x0000
0xFDA5 - 0xFDA6		TXRXBUF_EVM_HD_RX1	Read-only	0x0000
0xFDA7 - 0xFDA8		TXRXBUF_EVM_HD_RX2	Read-only	0x0000
0xFDA9 - 0xFDAA		TXRXBUF_EVM_HD_RX3	Read-only	0x0000
0xFDAB - 0xFDAC	Payload EVM Registers	TXRXBUF_EVM_PYLD_RX0	Read-only	0x0000
0xFDAD - 0xFDAE		TXRXBUF_EVM_PYLD_RX1	Read-only	0x0000
0xFDAF - 0xFDB0		TXRXBUF_EVM_PYLD_RX2	Read-only	0x0000
0xFDB1 - 0xFDB2		TXRXBUF_EVM_PYLD_RX3	Read-only	0x0000
0xFDB3 - 0xFDB6	Accumulated Header EVM Registers	TXRXBUF_EVM_HDACUM_RX0	Read-only	0x00..00
0xFDB7 - 0xFDBA		TXRXBUF_EVM_HDACUM_RX1	Read-only	0x00..00
0xFDBB - 0xFDBE		TXRXBUF_EVM_HDACUM_RX2	Read-only	0x00..00
0xFDBF - 0xFDC2		TXRXBUF_EVM_HDACUM_RX3	Read-only	0x00..00
0xFDC3 - 0xFDC6	Accumulated Payload EVM Registers	TXRXBUF_EVM_PYLACUM_RX0	Read-only	0x00..00
0xFDC7 - 0xFDCA		TXRXBUF_EVM_PYLACUM_RX1	Read-only	0x00..00
0xFDCB - 0xFDCE		TXRXBUF_EVM_PYLACUM_RX2	Read-only	0x00..00
0xFDCF - 0xFDD2		TXRXBUF_EVM_PYLACUM_RX3	Read-only	0x00..00
0xFDD3	Buffer Selection Register	TXRXBUF_SELECT_BUFF_RX	Read/Write	0x00
0xFDD4	RX Interrupts Register	TXRXBUF_RX_INT	Read/Write	0x00
0xFDD5	RX Configuration Register	TXRXBUF_RXCONF	Read/Write	0x02

Table 7-1. Register Mapping

Address	Register	Name	Access	Reset
0xFDD6 - 0xFDD7	RX Initial Address Registers	TXRXBUF_INITAD_RX0	Read/Write	0x0000
0xFDD8 - 0xFDD9		TXRXBUF_INITAD_RX1	Read/Write	0x0000
0xFDDA - 0xFDDB		TXRXBUF_INITAD_RX2	Read/Write	0x0000
0xFDDC - 0xFDDD		TXRXBUF_INITAD_RX3	Read/Write	0x0000
0xFDDE - 0xFDE1	Reserved	-	-	0x00..00
0xFDE2 - 0xFDE5	Reserved	-	-	0x00..00
0xFDE6	Reserved	-	-	0x00
0xFDE7		-	-	0x00
0xFDE8		-	-	0x00
0xFDE9		-	-	0x00
0xFDEA - 0xFDEB	Reserved	-	-	0x0000
0xFDEC - 0xFDED		-	-	0x0000
0xFDEE - 0xFDEF		-	-	0x0000
0xFDF0 - 0xFDF1		-	-	0x0000
0xFDF2	Robust TX Control Register	TXRXBUF_TXCONF_ROBO_CTL	Read/Write	0x00
0xFDF3	Robust RX Mode Register	TXRXBUF_RXCONF_ROBO_MODE	Read-only	0x00
0xFDF4 - 0xFDF7	Reserved	-	-	0x00..00
0xFDF8 - 0xFDF9	Reserved	-	-	0x0000
0xFDFA	Reserved	-	-	0xE0
0xFDFB	Branch Selection Register	TXRXBUF_TXCONF_SELBRANCH	Read/Write	0x00
0xFDFC	Reserved	-	-	0x00
0xFDFD	Reserved	-	-	0x00
0xFDFE	Reserved	-	-	0x00
0xFDFF	Reserved	-	-	0x00
0xFE2A	PHY Layer Special Function Register	PHY_SFR	Read/Write	0x87
0xFE2C	System Configuration Register	SYS_CONFIG	Read/Write	0x04
0xFE30	Reserved	-	-	0x00
0xFE31		-	-	0x00
0xFE32		-	-	0x00
0xFE33		-	-	0x00
0xFE34		-	-	0x00
0xFE35		-	-	0x00
0xFE36		-	-	0x00
0xFE37		-	-	0x00
0xFE38	Reserved	-	-	0x40
0xFE39		-	-	0x40
0xFE3A		-	-	0x40
0xFE3B		-	-	0x40

Table 7-1. Register Mapping

Address	Register	Name	Access	Reset
0xFE3C	Reserved	-	-	0x10
0xFE3D		-	-	0x10
0xFE3E		-	-	0x10
0xFE3F		-	-	0x10
0xFE47 - 0xFE4A	PHY Layer Timer Register	TIMER_BEACON_REF	Read-only	0x00..00
0xFE53 - 0xFE55	Reserved	-	-	0x000200
0xFE57	Reserved	-	-	0x1E
0xFE5C	Reserved	-	-	0x0C
0xFE5D		-	-	0x18
0xFE5F		-	-	0x26
0xFE60		-	-	0x2B
0xFE62 - 0xFE67	Sub Network Address Register	SNA	Read/Write	0x00..00
0xFE68	Reserved	-	-	0x5F
0xFE69 - 0xFE6A	Reserved	-	-	0xFFFF
0xFE6B - 0xFE6C		-	-	0xFFFF
0xFE6D - 0xFE6E		-	-	0xFFFF
0xFE6F - 0xFE70		-	-	0xFFFF
0xFE71 - 0xFE72		-	-	0xFFFF
0xFE73	Reserved	-	-	0x56
0xFE7D - 0xFE7E	Reserved	-	-	0x814C
0xFE7F	Reserved	-	-	0x00
0xFE80 - 0xFE81	Reserved	-	-	0x0000
0xFE8F	Reserved	-	-	0x03
0xFE90	TXRX Polarity Selector Register	AFE_CTL	Read/Write	0x00
0xFE91	Reserved	-	-	0x1E
0xFE92	Reserved	-	-	0x28
0xFE94	PHY Layer Error Counter Register	PHY_ERRORS	Read/Write	0x00
0xFE9D	Reserved	-	-	0x21
0xFE9E	Reserved	-	-	0x05
0xFE9F	Reserved	-	-	0x60
0xFEA0	Reserved	-	-	0x60
0xFEA1	Reserved	-	-	0x60
0xFEA2	Reserved	-	-	0x60
0xFEA3 - 0xFEA6	Reserved	-	-	0x77777777
0xFEAB - 0xFEAC	Reserved	-	-	0x5508
0xFEAD - 0xFEAE	Reserved	-	-	0x3C20
0xFEAF	Reserved	-	-	0x00
0xFEB0	Reserved	-	-	0x00
0xFEB4	Reserved	-	-	0x00
0xFEB5 - 0xFEB6	Reserved	-	-	0x0066

Table 7-1. Register Mapping

Address	Register	Name	Access	Reset
0xFEB7	Reserved	-	-	0x00
0xFEBA - 0xFEBB	CRC32 Errors Counter Register	ERR_CRC32_MAC	Read-only	0x0000
0xFEBC - 0xFEBD	CRC8 Errors Counter Register	ERR_CRC8_MAC	Read-only	0x0000
0xFEC0 - 0xFEC1	CRC8 HD Errors Counter Register	ERR_CRC8_MAC_HD	Read-only	0x0000
0xFEC2 - 0xFEC3	CRC8 PHY Errors Counter Register	ERR_CRC8_PHY	Read-only	0x0000
0xFEC4	False Positive Configuration Register	FALSE_POSITIVE_CONFIG	Read/Write	0x10
0xFEC5 - 0xFEC6	False Positive Counter Register	FALSE_POSITIVE	Read-only	0x0000
0xFEC8	Reserved	-	-	0x3F
0xFEC9	Reserved	-	-	0x3F
0xFECA	Reserved	-	-	0x3F
0xFECB	Reserved	-	-	0x3F
0xFECC	Reserved	-	-	0x3F
0xFECD	Reserved	-	-	0x3F
0xFECE - 0xFECF	Reserved	-	-	0x0000
0xFED3	Reserved	-	-	0x40
0xFED5 - 0xFED6	Reserved	-	-	0x0000
0xFEDB	Reserved	-	-	0x00
0xFEDC - 0xFEDF	Reserved	-	-	0x00..00
0xFEE0	Reserved	-	-	0x02
0xFEE4 - 0xFEE5	Reserved	-	-	0x0000
0xFEE6 - 0xFEE7	Reserved	-	-	0x0000
0xFEE8	Reserved	-	-	0x00
0xFEE9	Reserved	-	-	0xFF
0xFEEA	Reserved	-	-	0x04
0xFEEB	Reserved	-	-	0x08
0xFEEC	Reserved	-	-	0x0C
0xFEED	Reserved	-	-	0x14
0xFEEE	Reserved	-	-	0x00
0xFEEF	Reserved	-	-	0x03
0xFEF0	Reserved	-	-	0x00
0xFEF1	Reserved	-	-	0x17
0xFEF2	Reserved	-	-	0x18
0xFEF3	Reserved	-	-	0x23
0xFEF4	CRC PRIMEPLUS Configuration Register	PRIMEPLUS_CRC_CONFIG	Read/Write	0x14
0xFEF5 - 0xFEF6	CRC PRIMEPLUS Polynomial Register	PRIMEPLUS_CRC_POLY	Read/Write	0x080F
0xFEF7 - 0xFEF8	CRC PRIMEPLUS Reset Value Register	PRIMEPLUS_CRC_RST	Read/Write	0x0000

Table 7-1. Register Mapping

Address	Register	Name	Access	Reset
0xFEFA - 0xFEFD	Channel Selector Register	CTPS	Read/Write	0x000150C7
0xFEFE	Reserved	-	-	0x00
0xFF00 - 0xFF07	Reserved	-	-	0x411A1803 73D6893C
0xFF09 - 0xFF0A	Reserved	-	-	0x0EA5
0xFF0E - 0xFF11	Peripheral CRC Polynomial Register	VCRC_POLY	Read/Write	0x04C11DB7
0xFF12 - 0xFF15	Peripheral CRC Reset Value Register	VCRC_RST	Read/Write	0x00..00
0xFF16	Peripheral CRC Configuration Register	VCRC_CONF	Read/Write	0xC3
0xFF17	Peripheral CRC Input Register	VCRC_INPUT	Read/Write	0x00
0xFF18	Peripheral CRC Control Register	VCRC_CTL	Read/Write	0x00
0xFF19 - 0xFF1C	Peripheral CRC Value Register	VCRC_CRC	Read-only	0x00..00
0xFF1E	Zero Crossing Configuration Register	ZC_CONFIG	Read/Write	0x00
0xFF1F - 0xFF20	Reserved	-	-	0x051E
0xFF21 - 0xFF22	Reserved	-	-	0x8000
0xFF23	Zero Crossing Filter Register	ZC_FILTER	Read/Write	0xB2
0xFF24 - 0xFF27	Reserved	-	-	0x00030D40
0xFF28 - 0xFF2B	Reserved	-	-	0x00..00
0xFF2D	Reserved	-	-	0x01
0xFF33 - 0xFF36	Reserved	-	-	0x00..00
0xFF37 - 0xFF38	Reserved	-	-	0x0000
0xFF39	Reserved	-	-	0x14
0xFF3A	Reserved	-	-	0x80
0xFF3B	Reserved	-	-	0x70
0xFF3C	Reserved	-	-	0xC8
0xFF3D	Reserved	-	-	0x0A
0xFF3E	Reserved	-	-	0x02
0xFF3F	Reserved	-	-	0x04
0xFF40	Reserved	-	-	0x01
0xFF41	Reserved	-	-	0x01
0xFF42	Reserved	-	-	0x27
0xFF43	Reserved	-	-	0x0A
0xFF4C	Reserved	-	-	0xA8
0xFF51	Reserved	-	-	0x99
0xFF52	Reserved	-	-	0xC0
0xFF53	Reserved	-	-	0x00
0xFF54	Reserved	-	-	0x03
0xFF55	Reserved	-	-	0x99
0xFF56	Reserved	-	-	0x99

Table 7-1. **Register Mapping**

Address	Register	Name	Access	Reset
0xFF57	Reserved	-	-	0xFF
0xFF58	Reserved	-	-	0x33
0xFF5E - 0xFF5F	Reserved	-	-	0x0000
0xFF61	Reserved	-	-	0x00
0xFF62	Reserved	-	-	0x10
0xFF63 - 0xFF64	Reserved	-	-	0x00BF
0xFF65 - 0xFF66	Reserved	-	-	0x03E8
0xFF67 - 0xFF68	Reserved	-	-	0x0400
0xFF69 - 0xFF6A	Reserved	-	-	0x0F20
0xFF6B - 0xFF6C	Reserved	-	-	0x01EE
0xFF6D - 0xFF6E	Reserved	-	-	0x00BF
0xFF6F - 0xFF70		-	-	0x0160
0xFF71 - 0xFF72		-	-	0x02F0
0xFF73 - 0xFF74		-	-	0x0450
0xFF75	Reserved	-	-	0x68
0xFF76	Reserved	-	-	0x80
0xFF77	Reserved	-	-	0x3B
0xFF78 - 0xFF79	Reserved	-	-	0x0000
0xFF7A - 0xFF7F	Reserved	-	-	0x00..00
0xFF80	Reserved	-	-	0x00
0xFF81	Reserved	-	-	0x30
0xFF82 - 0xFF83	Reserved	-	-	0x0600
0xFF84	Reserved	-	-	0x58
0xFF85	Reserved	-	-	0x99
0xFF86	Reserved	-	-	0x79
0xFF87 - 0xFF88	Reserved	-	-	0x0021
0xFF89	Reserved	-	-	0x03
0xFF8A	Reserved	-	-	0x01
0xFF8B	Reserved	-	-	0x02
0xFF8C	Reserved	-	-	0x04
0xFF8D	Reserved	-	-	0x7F
0xFF8E	Reserved	-	-	0x00
0xFF92	Reserved	-	-	0x14
0xFF93	Reserved	-	-	0x11
0xFF94	Reserved	-	-	0x80
0xFF95	Reserved	-	-	0x00
0xFF96	Reserved	-	-	0x00
0xFF97	Reserved	-	-	0x70
0xFF98	Reserved	-	-	0xC8
0xFF99	Reserved	-	-	0x0A
0xFF9A	Reserved	-	-	0x02
0xFF9B	Reserved	-	-	0x04

Table 7-1. Register Mapping

Address	Register	Name	Access	Reset
0xFF9C	Reserved	-	-	0x01
0xFF9D	Reserved	-	-	0x01
0xFF9E	Reserved	-	-	0x27
0xFF9F	Reserved	-	-	0x0A
0xFFA0 - 0xFFAF	Peripheral AES Key Register	AES_KEY	Read/Write	0x00..00
0xFFB0 - 0xFFBF	Peripheral AES Data Field Register	AES_DATA	Read/Write	0x00..00
0xFFC0	Peripheral AES Control Register	AES_CTL	Read/Write	0x04
0xFFE2 - 0xFFE3	Reserved	-	-	0x0424
0xFFE4 - 0xFFE5		-	-	0x0424
0xFFE6 - 0xFFE7		-	-	0x0424
0xFFE8 - 0xFFE9		-	-	0x0424
0xFFEA - 0xFFEB		-	-	0x0424
0xFFEC - 0xFFED		-	-	0x0424
0xFFEE - 0xFFEF		-	-	0x0424
0xFFF0 - 0xFFF1		-	-	0x0424
0xFFF2 - 0xFFF3		-	-	0x0424
0xFFF4 - 0xFFF5		-	-	0x0424
0xFFF6 - 0xFFF7		-	-	0x0424
0xFFF8 - 0xFFF9		-	-	0x0424

8. MAC Coprocessor

ATPL230A accelerators can be used to perform PRIME MAC-specific tasks by hardware, decreasing CPU load from the external MCU/MPU. For that purpose, Cyclic Redundance Check (CRC) and AES128 encryption blocks are available in ATPL230A.

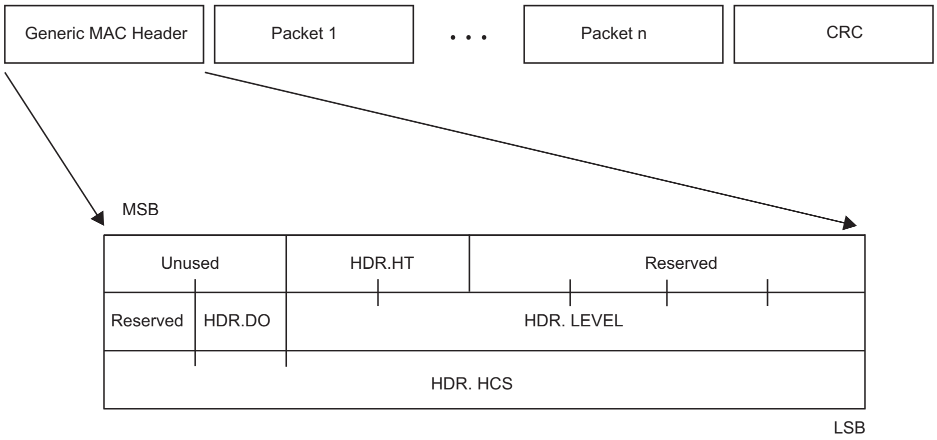
Please refer to Atmel doc43048 "Atmel PRIME Implementation" for Atmel software package detailed description and functionality.

8.1 Cyclic Redundancy Check (CRC)

8.1.1 PRIME v1.3 CRC

There are three types of MAC PDUs (generic, promotion and beacon) for different purposes, and each one has its own specific CRC. There is a hardware implementation of every CRC type calculated by the MAC layer. This CRC hardware-calculation is enabled by default. Note that the CRC included at the physical layer is also a hardware implementation available (enabled by default).

Figure 8-1. Example: Generic MAC PDU format and generic MAC header detail



In transmission all CRC bytes are real-time calculated and the last bytes of the MAC PDU are overwritten with these values, (provided that the field HT in the first byte of the MAC header in transmission data is equal to the corresponding MAC PDU type).

In reception the CRC bytes are also real-time calculated and these bytes are checked with the last bytes of the MAC PDU. If the CRC is not correct, then an error flag is activated, the complete frame is discarded, and the corresponding error counter is increased. These counters allow the MAC layer to take decisions according to error ratio.

For the Generic MAC PDU, there is an 8-bit CRC in the Generic MAC header, which corresponds to PRIME HDR.HCS. In reception, if this CRC doesn't check successfully, the current frame is discarded and no interruption is generated.

This works in the same way as CRC for the PHY layer (CRC Ctrl, located in the PHY header, see PRIME specification for further information).

There is another CRC for the Generic MAC PDU which is the last field of the GPDU. It is 32 bits long and it is used to detect transmission errors. The CRC shall cover the concatenation of the SNA with the GPDU except for the CRC field itself. In reception, if the CRC is not successful then an internal flag is set and the error counter is increased.

For the Promotion Needed PDU there is an 8-bit CRC, calculated with the first 13 bytes of the header. In reception, if this CRC is not correct, then an internal flag is set and the corresponding error counter is increased.

For the Beacon PDU there is a 32-bit CRC calculated with the same algorithm as the one defined for the CRC of the Generic MAC PDU. This CRC shall be calculated over the complete BPDU except for the CRC field itself. In reception, if this CRC is not successful, then an internal flag is set and the same error counter used for GPDU is increased. The hardware used for this CRC is the same as the one used for GPDU.

8.1.2 Configurable CRC calculation

PRIME v1.3 version fixes the polynomial to calculate the CRCs. In case that these polynomials were modified, the CRC peripheral would be used. It is used as a peripheral unit, accessible using the system peripheral registers.

For example, to configure it for PRIME CRC8:

X^8 + X^2 + X + 1

VCRC_POLY = 0x00000007

VCRC_RST = 0x00000000

VCRC_CONF = 0xC0

And to configure it for PRIME CRC32:

x^32 + x^26 + x^23 + x^22 + x^16 + x^12 + x^11 + x^10 + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1

VCRC_POLY = 0x04C11DB7

VCRC_RST = 0x00000000

VCRC_CONF = 0xC3

A different set of registers can also be used to set CRC parameters:

X^12 + X^11 + X^3 + X^2 + X + 1

PRIMEPLUS_CRC_POLY = 0x080F

PRIMEPLUS_CRC_RST = 0x0000

PRIMEPLUS_CRC_CONFIG = 0x14

8.2 Advanced Encryption Standard (AES)

One of the additional security functionalities to PRIME v1.3 is the 128-bit AES encryption of data. ATPL230A includes a hardware implementation of this block, as a peripheral unit.

In transmission, data must be encrypted previously to the use of the PHY_DATA request primitive (see PRIME specification), in an independent way (note that Beacon PDU, Promotion PDU and Generic MAC header, as well as several control packets, are not encrypted).

In reception, data passed by the PHY layer is already encrypted and must be decrypted in a subsequent process.

To encrypt a data package with corresponding KEY, the process is as follows:

1. Write the KEY (128 bits long) in AES_KEY register. This step is only needed if a new key is going to be used (due to a key change or to a reset operation).
2. Write the 128 bits of data to be encrypted in AES_DATA register.
3. Set to ‘1’ the CIPHER control bit in AES_CTL register and then set to ‘1’ the START control bit to start the operation. This step could be realized as an atomic operation writing 0x03.
4. Wait until the READY bit in AES_CTL register becomes ‘1’ automatically. This bit indicates when the operation is completed.
5. After that, the encrypted (coded) data package is automatically stored in AES_DATA register.

On the other hand, to decrypt a data package with corresponding KEY, the process is as follows:

1. Write the KEY (128 bits long) in AES_KEY register. This step is only needed if a new key is going to be used (due to a key change or to a reset operation).
2. Write the 128 bits of encrypted data in AES_DATA register.
3. Set to ‘0’ the CIPHER control bit in AES_CTL register and then set to ‘1’ the START control bit to start the operation. This step could be realized as an atomic operation writing 0x02.
4. Wait until the READY bit in AES_CTL register becomes ‘1’ automatically. This bit indicates when the operation is completed.
5. After that, the decrypted (decoded) data package is automatically stored in AES_DATA register.

8.3 MAC Coprocessor Registers

8.3.1 CRC Registers

8.3.1.1 Sub Network Address Register

Name: SNA

Address: 0xFE62 – 0xFE67

Access: Read/Write

Reset: 0x00..00

47	46	45	44	43	42	41	40
SNA (47:40)							

39	38	37	36	35	34	33	32
SNA (39:32)							

31	30	29	28	27	26	25	24
SNA (31:24)							

23	22	21	20	19	18	17	16
SNA (23:16)							

15	14	13	12	11	10	9	8
SNA (15:8)							

7	6	5	4	3	2	1	0
SNA (7:0)							

This register stores the 48-bit Sub Network Address. Physical layer uses it to calculate the CRC's.

8.3.1.2 CRC32 Errors Counter Register

Name: ERR_CRC32_MAC

Address: 0xFEBA (MSB) – 0xFEBB (LSB)

Access: Read-only

Reset: 0x0000

15	14	13	12	11	10	9	8
ERR_CRC32_MAC (15:8)							
7	6	5	4	3	2	1	0
ERR_CRC32_MAC (7:0)							

This register stores the number of received PRIME v1.3 packets (Beacon and generic) with an error in the CRC32 MAC field of the payload, since the last physical layer reset. Only a physical layer reset initializes the register.

Note: Once the register has reached its maximum value, a new error causes the register to roll over.

8.3.1.3 CRC8 Errors Counter Register

Name: ERR_CRC8_MAC

Address: 0xFEBC (MSB) – 0xFEBD (LSB)

Access: Read-only

Reset: 0x0000

15	14	13	12	11	10	9	8
ERR_CRC8_MAC (15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ERR_CRC8_MAC (7:0)							

This register stores the number of received PRIME v1.3 packets (Promotion) with an error in the CRC8 MAC field of the payload, since the last physical layer reset. Only a physical layer reset initializes the register.

Note: Once the register has reached its maximum value, a new error causes the register to roll over.

8.3.1.4 CRC8 HD Errors Counter Register

Name: ERR_CRC8_MAC_HD

Address: 0xFEC0 (MSB) – 0xFEC1 (LSB)

Access: Read-only

Reset: 0x0000

15	14	13	12	11	10	9	8
ERR_CRC8_MAC_HD (15:8)							
7	6	5	4	3	2	1	0
ERR_CRC8_MAC_HD (7:0)							

This register stores the number of received PRIME v1.3 packets with an error in the CRC8 MAC field of the header, since the last physical layer reset. Only a physical layer reset initializes the register.

Note: Once the register has reached its maximum value, a new error causes the register to roll over.

8.3.1.5 CRC8 PHY Errors Counter Register

Name: ERR_CRC8_PHY

Address: 0xFEC2 (MSB) – 0xFEC3 (LSB)

Access: Read-only

Reset: 0x0000

15	14	13	12	11	10	9	8
ERR_CRC8_PHY (15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ERR_CRC8_PHY (7:0)							

This register stores the number of received PRIME v1.3 packets with an error in the CRC8 PHY field of the header, since the last physical layer reset. Only a physical layer reset initializes the register.

Note: Once the register has reached its maximum value, a new error causes the register to roll over.

8.3.1.6 CRC PRIMEPLUS Configuration Register

Name: PRIMEPLUS_CRC_CONFIG

Address: 0xFEF4

Access: Read/Write

Reset: 0x14

7	6	5	4	3	2	1	0
-	-	-	FB_TYPE	WIDTH			

PRIMEPLUS_CRC_CONFIG register allows the user to configure feedback type and width of the PRIME v1.4 mode physical CRC computation algorithm.

- **FB_TYPE:**

  '0': Computation procedure must end with extra bytes with value zero added to the data ones (User added).

  '1': Extra bytes addition is not required.

- **WIDTH (3:0):**

  Represents the grade of the polynomial used by the algorithm.

WIDTH (3:0)	Polynomial bits
0	8
1	9
2	10
3	11
4	12
5	13
6	14
7	15
>7	16

8.3.1.7 CRC PRIMEPLUS Polynomial Register

Name: PRIMEPLUS_CRC_POLY

Address: 0xFEF5 (MSB) – 0xFEF6 (LSB)

Access: Read/Write

Reset: 0x080F

15	14	13	12	11	10	9	8
PRIMEPLUS_CRC_POLY (15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRIMEPLUS_CRC_POLY (7:0)							

This register allows the PRIME v1.4 mode physical CRC polynomial configuration. Each bit of the register represents a grade coefficient selected by its position into the register. For example the reset value 0x080F corresponds to the polynomial X^12 + X^11 + X^3 + X^2 + X + 1. In this polynomial the active coefficients are 12, 11, 3, 2, 1, 0. The most significant coefficient (12) represents the polynomial grade and is implemented by the algorithm feedback so it is not included in the register. With the other coefficients we calculate the register value needed as follows: 2^11 + 2^3 + 2^2 + 2^1 + 2^0 = 2063 = 0x080F.

8.3.1.8 CRC PRIMEPLUS Reset Value Register

Name: PRIMEPLUS_CRC_RST

Address: 0xFEF7 (MSB) – 0xFEF8 (LSB)

Access: Read/Write

Reset: 0x0000

15	14	13	12	11	10	9	8
PRIMEPLUS_CRC_RST (15:8)							
7	6	5	4	3	2	1	0
PRIMEPLUS_CRC_RST (7:0)							

This register stores the initial value of the PRIME v1.4 mode physical CRC computation algorithm.

8.3.1.9 Peripheral CRC Polynomial Register

Name: VCRC_POLY

Address: 0xFF0E (MSB) – 0xFF11 (LSB)

Access: Read/Write

Reset: 0x04C11DB7

31	30	..	..	..	..	1	0
VCRC_POLY (31:0)							

This is a 32 bits register used to store the CRC polynomial mathematical expression. Each register bit location represents an exponential degree of the polynomial. Meaning that, for a register value of 0x04C11DB7; the corresponding polynomial expression is x^32 + x^26 + x^23 + x^22 + x^16 + x^12 + x^11 + x^10 + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1. Note that, the first exponential degree (x^32) is taken by the feedback of the circuit itself.

To configure the system in CRC mode, the bit VCRC_POLY(0) must be set to ‘1’. Otherwise, if VCRC_POLY(0) is set to ‘0’ the system works in LFSR (Linear Feedback Shift Register) mode.

8.3.1.10 Peripheral CRC Reset Value Register

Name: VCRC_RST

Address: 0xFF12 (MSB) – 0xFF15 (LSB)

Access: Read/Write

Reset: 0x00000000

31	30	..	..	..	..	1	0
VCRC_RST (31:0)							

This is a 32 bits register used to store the initial value to start calculating the CRC. This value is fixed by either the CRC used or by the protocol implemented.

8.3.1.11 Peripheral CRC Configuration Register

Name: VCRC_CONF

Address: 0xFF16

Access: Read/Write

Reset: 0xC3

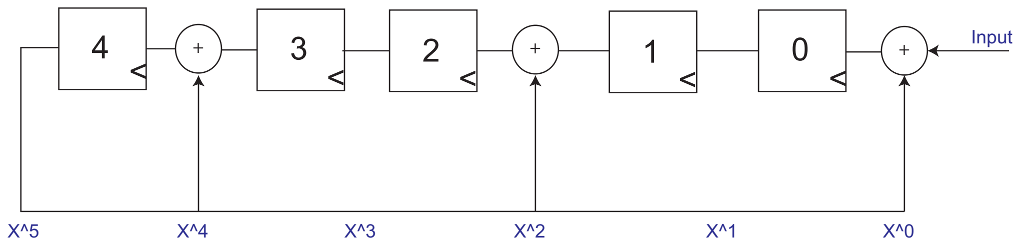
7	6	5	4	3	2	1	0
FB_TYPE	MSBF	MIRRORED32	MIRRORED8	CIN	COUT	WIDTH1	WIDTH0

This is an 8 bits register used to configure different CRC´s and LFSR´s. This register contains the following control bits:

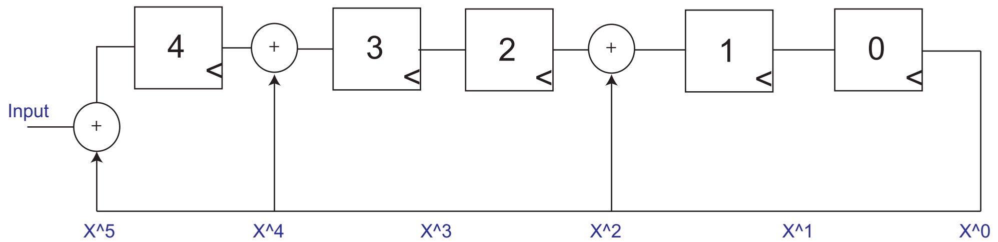
- **FB_TYPE:**

  Configures desired circuit feedback type

  '0': Select circuit feedback type as below.



  '1': Select circuit feedback type as below.



- **MSBF:**

  Allows to choose byte calculation mode

  '0': Select the least significant bit (LSB) first to start calculations.

  '1': Select the most significant bit (MSB) first to start calculations.

- **MIRRORED8:**

  Allows to flip (turn over) the desired CRC size (bytes) in the 32-bit VCRC_CRC register configured by WIDTH1 and WIDTH0 bits.

  '0': No flipping is performed and the 32-bit VCRC_CRC register will remain unalterable as below.

  '1': Flip the desired CRC size (bytes) in the 32-bit VCRC_CRC register configured by the control bits WIDTH1 and WIDTH0. For example, if control bits WIDTH1 and WIDTH0 are both set to '1' (CRC size = 4, see link table), it will flip the four blocks of bytes in the register. In another case when CRC size = 3 (WIDTH1='1' and WIDTH0='0'), it will flip the first three blocks of bytes (beginning from less significant byte) in the register ignoring the last byte.

- **MIRRORED32:**

  Allows byte shifting in the 32-bit VCRC_CRC register.

  ‘0’: No byte shifting is performed and the entire 32-bit VCRC_CRC register will remain unalterable as below.

  ‘1’: The 32-bit VCRC_CRC register is reorganized by shifting the four blocks of bytes. Meaning that, in a byte the MSB will become the LSB. After this command, the VCRC_CRC register will look as below. Both control bits MIRRORED32 AND MIRRORED8 can be set to ‘1’ to obtain the two results simultaneously.

- **CIN:**

  Complement (opposite) the INPUT byte of the VCRC_INPUT register

  ‘0’: Disable complement.

  ‘1’: Enable complement.

- **COUT:**

  Complement (opposite) the OUTPUT byte of the VCRC_INPUT register

  ‘0’: Disable complement.

  ‘1’: Enable complement.

- **WIDTH(1:0):**

  Select CRC size in bytes:

WIDTH(1:0)	CRC size [Bytes]
“00”	1
“01”	2
“10”	3
“11”	4

8.3.1.12 Peripheral CRC Input Register

Name: VCRC_INPUT

Address: 0xFF17

Access: Read/Write

Reset: 0x00

7	6	5	4	3	2	1	0
VCRC_INPUT (7:0)							

This is an 8 bits register used to write the input bytes for CRC calculations. Each time a byte has been written in this register, the VCRC block detects the byte automatically and initiates the operation adding this new byte to previous calculations.

8.3.1.13 Peripheral CRC Control Register

Name: VCRC_CTL

Address: 0xFF18

Access: Read/Write

Reset: 0x00

7	6	5	4	3	2	1	0
0	0	0	BUSY	0	0	0	RESTART

The VCRC_CTL register contains the following control bits:

- **BUSY:**
  - '0': VCRC block is ready to receive a new data byte.
  - '1': VCRC block is busy performing calculations. Unable to write in VCRC_INPUT register.

- **RESTART:**

  Configures desired circuit feedback type:
  - '0': Reset disable. After a reset, RESTART bit is set to '0' automatically after a period of time.
  - '1': Reset enable. Delete the actual VCRC_CRC register value and does not affect configuration registers.

8.3.1.14 Peripheral CRC Value Register

Name: VCRC_CRC

Address: 0xFF19 (MSB) – 0xFF1C (LSB)

Access: Read-only

Reset: 0x00000000

31	30	..	..	..	..	1	0
VCRC_CRC (31:0)							

This is a 32 bits register containing the final computed CRC value. The value in this register depends on the CRC size (bytes) selected in the control bits WIDTH1 and WIDTH0.

8.3.2 AES Registers

8.3.2.1 Peripheral AES Key Register

Name: AES_KEY

Address: 0xFFA0 (MSB) – 0xFFAF (LSB)

Access: Read/Write

Reset: 0x00..00

127	126	..	..	..	..	1	0
AES_KEY (127:0)							

The register AES_KEY is used to store the 128 bits “KEY” of the encryption algorithm.

8.3.2.2 Peripheral AES Data Field Register

Name: AES_DATA

Address: 0xFFB0 (MSB) – 0xFFBF (LSB)

Access: Read/Write

Reset: 0x00..00

127	126	..	..	..	..	1	0
AES_DATA (127:0)							

AES_DATA register is used to store the encrypted/decrypted data. The size of the data packet for an encryption/decryption operation is always 128 bits.

8.3.2.3 Peripheral AES Control Register

Name: AES_CTL

Address: 0xFFC0

Access: Read/Write

Reset: 0x04

7	6	5	4	3	2	1	0
-	-	-	RESET	-	READY	START	CIPHER

The register AES_CTL contains some bits for control operation purposes.

- **RESET:**

  Initializes the AES block:

  ‘0’: Reset disabled.

  ‘1’: Reset enabled.

- **READY:**

  Indicates the encryption/decryption ongoing operation:

  ‘0’: Indicates encryption/decryption ongoing operation.

  ‘1’: Indicates encryption/decryption operation is done.

- **START:**

  Initialize encrypt/decrypt process:

  ‘1’: Start selected functional mode. Automatically set to ‘0’ after process begins.

- **CIPHER:**

  Configures functional mode:

  ‘0’: AES block is in decrypt (decode) mode.

  ‘1’: AES block is in encrypt (code) mode.

8.3.3 MAC Info Registers

8.3.3.1 BER SOFT Average Error Registers

Name: TXRXBUF_BERSOFT_AVG_RX0
Address: 0xFD57
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERSOFT_AVG_RX0							

After a message is received in BUF_RX0, this register stores the logarithm of the number of accumulated errors regarding the number of received bits, using Viterbi soft* decision. In PRIME v1.4 mode, it is calculated from the arithmetic average of the accumulated errors in each one of the four replicated symbols. The value is cleared by hardware each time a new message is received in BUF_RX0.

Name: TXRXBUF_BERSOFT_AVG_RX1
Address: 0xFD58
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERSOFT_AVG_RX1							

After a message is received in BUF_RX1, this register stores the logarithm of the number of accumulated errors regarding the number of received bits, using Viterbi soft* decision. In PRIME v1.4 mode, it is calculated from the arithmetic average of the accumulated errors in each one of the four replicated symbols. The value is cleared by hardware each time a new message is received in BUF_RX1.

Name: TXRXBUF_BERSOFT_AVG_RX2
Address: 0xFD59
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERSOFT_AVG_RX2							

After a message is received in BUF_RX2, this register stores the logarithm of the number of accumulated errors regarding the number of received bits, using Viterbi soft* decision. In PRIME v1.4 mode, it is calculated from the arithmetic average of the accumulated errors in each one of the four replicated symbols. The value is cleared by hardware each time a new message is received in BUF_RX2.

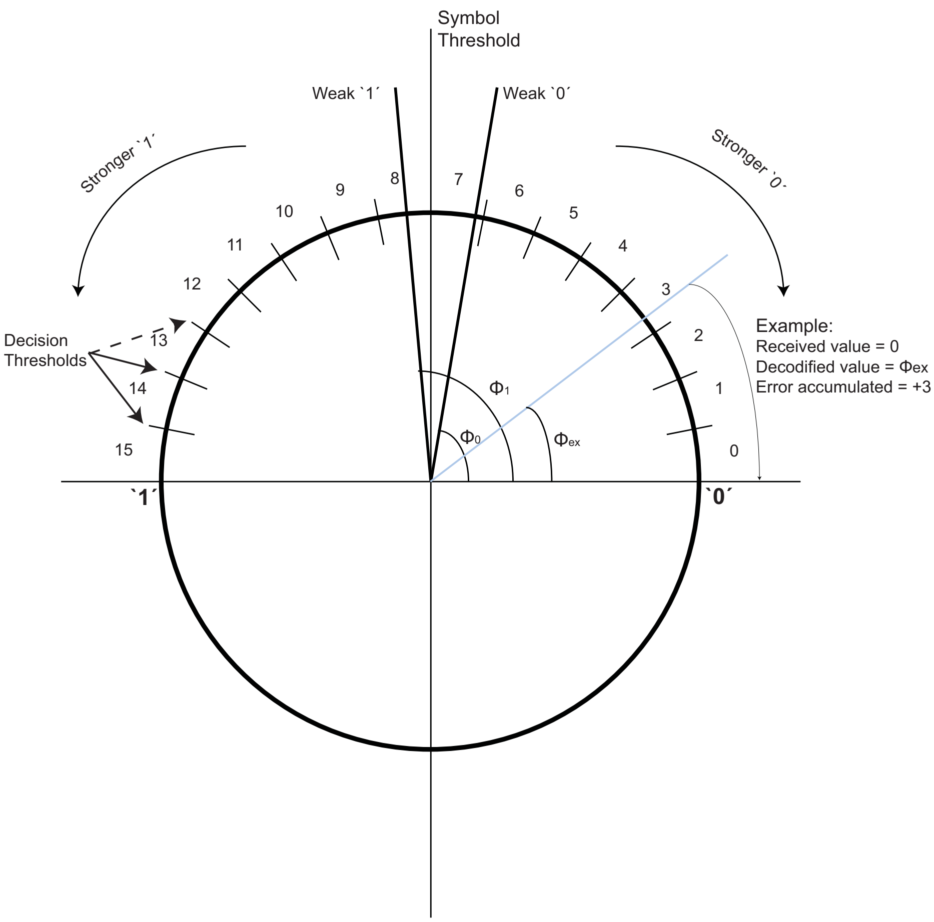
Name: TXRXBUF_BERSOFT_AVG_RX3
Address: 0xFD5A
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERSOFT_AVG_RX3							

After a message is received in BUF_RX3, this register stores the logarithm of the number of accumulated errors regarding the number of received bits, using Viterbi soft* decision. In PRIME v1.4 mode, it is calculated from the arithmetic average of the accumulated errors in each one of the four replicated symbols. The value is cleared by hardware each time a new message is received in BUF_RX3.

** Viterbi Soft Decision: in "soft" decision there are sixteen decision levels. Once decodified, a strong '0' is represented by a value of "0", while a strong '1' is represented by a value of "15". The rest of values are intermediate, so "7" is used to represent a weak '0' and "8" represents a weak '1'. Soft decision calculates the error in one bit received as the distance in decision levels between the value received (a value in the range 0 to 15) and the corrected one (0 or 15).*

Figure 8-2. Example of Viterbi Soft detection decision levels in a BPSK constellation



8.3.3.2 BER SOFT Maximum Error Registers

Name: TXRXBUF_BERSOFT_MAX_RX0
Address: 0xFD5B
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERSOFT_MAX_RX0							

Used only in PRIME v1.4 mode. After a message is received in BUF_RX0, this register stores the logarithm of the maximum error of the four replicated symbols, regarding the number of received bits, using Viterbi soft* decision. The value is cleared by hardware each time a new message is received in BUF_RX0.

Name: TXRXBUF_BERSOFT_MAX_RX1
Address: 0xFD5C
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERSOFT_MAX_RX1							

Used only in PRIME v1.4 mode. After a message is received in BUF_RX1, this register stores the logarithm of the maximum error of the four replicated symbols, regarding the number of received bits, using Viterbi soft* decision. The value is cleared by hardware each time a new message is received in BUF_RX1.

Name: TXRXBUF_BERSOFT_MAX_RX2
Address: 0xFD5D
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERSOFT_MAX_RX2							

Used only in PRIME v1.4 mode. After a message is received in BUF_RX2, this register stores the logarithm of the maximum error of the four replicated symbols, regarding the number of received bits, using Viterbi soft* decision. The value is cleared by hardware each time a new message is received in BUF_RX2.

Name: TXRXBUF_BERSOFT_MAX_RX3
Address: 0xFD5E
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERSOFT_MAX_RX3							

Used only in PRIME v1.4 mode. After a message is received in BUF_RX3, this register stores the logarithm of the maximum error of the four replicated symbols, regarding the number of received bits, using Viterbi soft* decision. The value is cleared by hardware each time a new message is received in BUF_RX3.

8.3.3.3 BER HARD Average Error Registers

Name: TXRXBUF_BERHARD_AVG_RX0
Address: 0xFD63
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERHARD_AVG_RX0							

After a message is received in BUF_RX0, this register stores the logarithm of the number of accumulated errors regarding the number of received bits, using Viterbi hard* decision. In PRIME v1.4 mode, it is calculated from the arithmetic average of the accumulated errors in each one of the four replicated symbols. The value is cleared by hardware each time a new message is received in BUF_RX0.

Name: TXRXBUF_BERHARD_AVG_RX1
Address: 0xFD64
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERHARD_AVG_RX1							

After a message is received in BUF_RX1, this register stores the logarithm of the number of accumulated errors regarding the number of received bits, using Viterbi hard* decision. In PRIME v1.4 mode, it is calculated from the arithmetic average of the accumulated errors in each one of the four replicated symbols. The value is cleared by hardware each time a new message is received in BUF_RX1.

Name: TXRXBUF_BERHARD_AVG_RX2
Address: 0xFD65
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERHARD_AVG_RX2							

After a message is received in BUF_RX2, this register stores the logarithm of the number of accumulated errors regarding the number of received bits, using Viterbi hard* decision. In PRIME v1.4 mode, it is calculated from the arithmetic average of the accumulated errors in each one of the four replicated symbols. The value is cleared by hardware each time a new message is received in BUF_RX2.

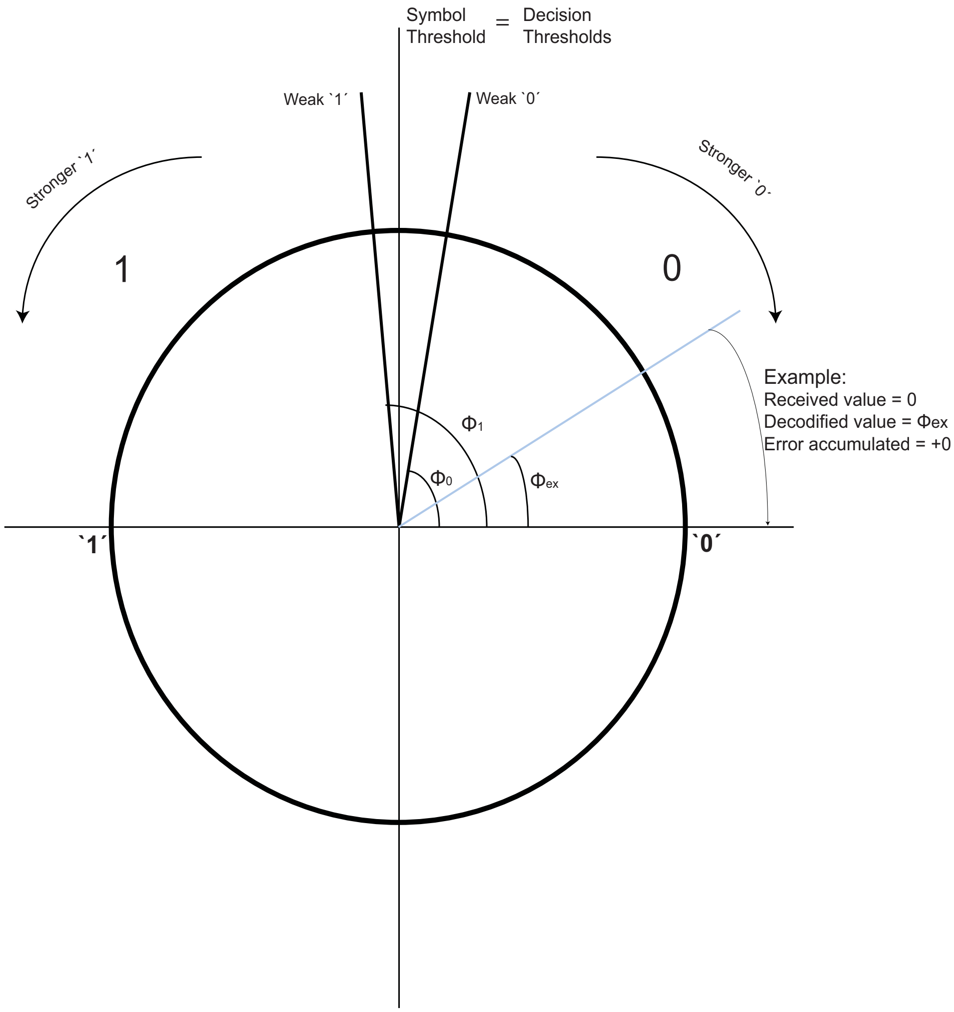
Name: TXRXBUF_BERHARD_AVG_RX3
Address: 0xFD66
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERHARD_AVG_RX3							

After a message is received in BUF_RX3, this register stores the logarithm of the number of accumulated errors regarding the number of received bits, using Viterbi hard* decision. In PRIME v1.4 mode, it is calculated from the arithmetic average of the accumulated errors in each one of the four replicated symbols. The value is cleared by hardware each time a new message is received in BUF_RX3.

** Viterbi Hard Decision: in “hard” detection there are only two decision levels. If the received value is different than the corrected one, the error value taken is “1”. Otherwise, the error value taken is “0”.*

Figure 8-3. Example of Viterbi Hard detection decision levels in a BPSK constellation



8.3.3.4 BER HARD Maximum Error Registers

Name: TXRXBUF_BERHARD_MAX_RX0
Address: 0xFD67
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERHARD_MAX_RX0							

Used only in PRIME v1.4 mode. After a message is received in BUF_RX0, this register stores the logarithm of the maximum error of the four replicated symbols, regarding the number of received bits, using Viterbi hard* decision. The value is cleared by hardware each time a new message is received in BUF_RX0.

Name: TXRXBUF_BERHARD_MAX_RX1
Address: 0xFD68
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERHARD_MAX_RX1							

Used only in PRIME v1.4 mode. After a message is received in BUF_RX1, this register stores the logarithm of the maximum error of the four replicated symbols, regarding the number of received bits, using Viterbi hard* decision. The value is cleared by hardware each time a new message is received in BUF_RX1.

Name: TXRXBUF_BERHARD_MAX_RX2
Address: 0xFD69
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERHARD_MAX_RX2							

Used only in PRIME v1.4 mode. After a message is received in BUF_RX2, this register stores the logarithm of the maximum error of the four replicated symbols, regarding the number of received bits, using Viterbi hard* decision. The value is cleared by hardware each time a new message is received in BUF_RX2.

Name: TXRXBUF_BERHARD_MAX_RX3
Address: 0xFD6A
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERHARD_MAX_RX3							

Used only in PRIME v1.4 mode. After a message is received in BUF_RX3, this register stores the logarithm of the maximum error of the four replicated symbols, regarding the number of received bits, using Viterbi hard* decision. The value is cleared by hardware each time a new message is received in BUF_RX3.

8.3.3.5 False Positive Configuration Register

Name: FALSE_POSITIVE_CONFIG

Address: 0xFEC4

Access: Read/Write

Reset: 0x10

7	6	5	4	3	2	1	0
-	-	ERR_CRC8_MAC_HD	ERR_PROTOCOL	ERR_LEN	ERR_PAD_LEN	ERR_PDU	ERR_SP

Through FALSE_POSITIVE_CONFIG register the user is able to configure FALSE_POSITIVE register behavior. When a flag of this register is set to '1', the correspondent field of the packet is included in the false positive computation algorithm. False positive algorithm is only enabled in PRIME v1.3 mode. See "False Positive Counter Register"

- **ERR_CRC8_MAC_HD:**

  Bad CRC8 MAC value (The one located at the header part of the packet).

- **ERR_PROTOCOL:**

  Unsupported protocol field.

- **ERR_LEN:**

  Invalid LEN field value. LEN field is located in the PRIME PPDU header and it defines the length of the payload (after coding) in OFDM symbols. See PRIME specification for further details about PPDU structure.

- **ERR_PAD_LEN:**

  Invalid PAD_LEN value. PAD_LEN field is located in the PRIME PPDU header and it defines the length of the PAD field (after coding) in bytes. See PRIME specification for further details about PPDU structure.

- **ERR_PDU:**

  Unsupported Header Type.

- **ERR_SP:**

  Unsupported Security Protocol.

8.3.3.6 False Positive Counter Register

Name: FALSE_POSITIVE

Address: 0xFEC5 (MSB) – 0xFEC6 (LSB)

Access: Read-only

Reset: 0x0000

15	14	13	12	11	10	9	8
FALSE_POSITIVE (15:8)							
7	6	5	4	3	2	1	0
FALSE_POSITIVE (7:0)							

This register holds the number of received PRIME v1.3 packets with a good CRC8_PHY value but with an unsupported value in any of the fields indicated by FALSE_POSITIVE_CONFIG register. Only a physical layer reset initializes the register.

Note: Once the register has reached its maximum value, a new error causes the register to roll over.

9. PRIME PHY Layer

9.1 Overview

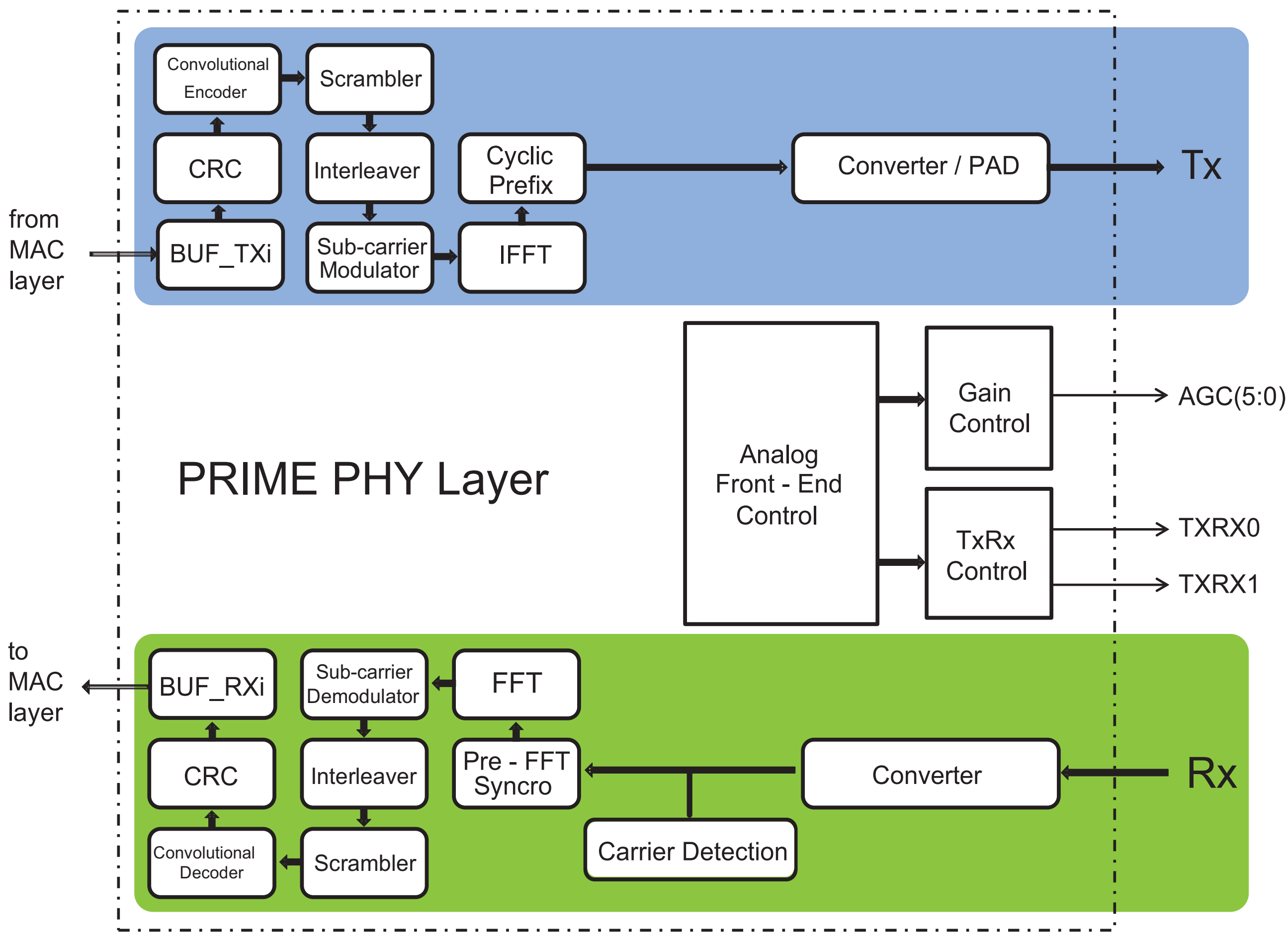
The physical layer consists of a hardware implementation of the enhanced PRIME Physical Layer Entity, which is an Orthogonal Frequency Division Multiplexing (OFDM) system in the 42 kHz to 472 kHz frequency band. This PHY layer transmits and receives MPDUs (MAC Protocol Data Unit) between neighbor nodes.

From the transmission point of view, the PHY layer receives its inputs from the MAC (Medium Access Control) layer. At the end of transmission branch, data is output to the physical channel.

On the reception side, the PHY layer receives its inputs from the physical channel, and at the end of reception branch, the data flows to the MAC layer.

A PHY layer block diagram is shown below:

Figure 9-1. PHY Layer Block Diagram



The diagram can be divided in five sub-blocks: TxRx buffers, Transmission branch, Reception branch, Analog Front End control and Carrier Detection.

9.1.1 TxRx Buffers

There are 4 dedicated buffers for transmission (BUF_TX0, BUF_TX1, BUF_TX2 and BUF_TX3) and 4 dedicated buffers for reception (BUF_RX0, BUF_RX1, BUF_RX2, BUF_RX3). The main features are shown below:

Table 9-1. TxRx Buffers features

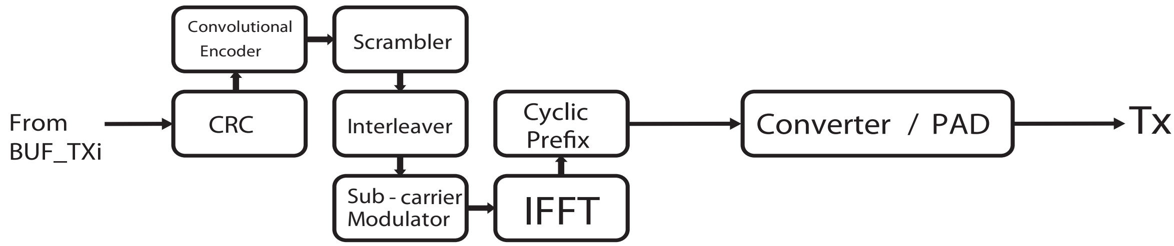
BUF_TXi	BUF_RXi
• Size configurable • Number of buffers enabled configurable • Start time forced or programmed • Transmission can be forced regardless of the carrier detection and frames reception • Transmission parameters configurable • Error detector	• Size configurable • Number of buffers enabled configurable • Enable/Disable interrupts • Parameters saved (BER, RSSI, CINR…)

9.1.2 Transmission Branch

PHY layer takes data to be sent from BUF_TXi. The Cyclic Redundancy Check (CRC) fields are hardware-generated in real time, and properly appended to the transmission data. The rest of the chain is hardware-wired, and performs automatically all the tasks needed to send data according to PRIME specifications.

In the following figure, the block diagram of the transmission branch is shown.

Figure 9-2. Transmission Branch



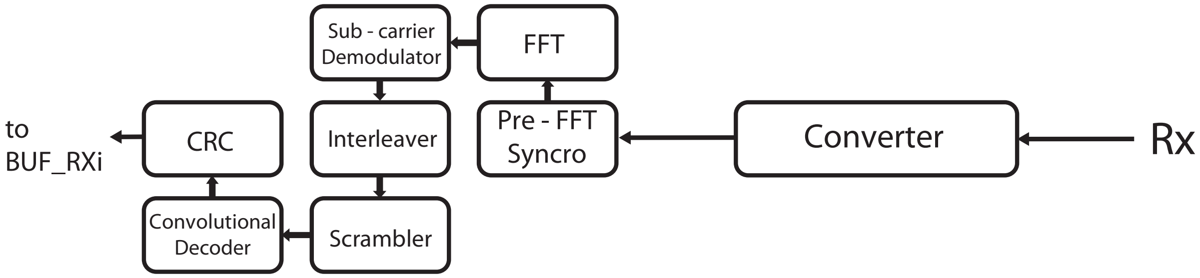
The output is differential modulated using a DBPSK/DQPSK/D8PSK scheme. After modulation, IFFT (Inverse Fourier Transform) block and cyclic prefix block allow to implement an OFDM scheme.

A Converter and a Power Amplifier Driver is the last block in the transmission branch. This block is responsible for adjusting the signal to reach the best transmission efficiency, thus reducing consumption and power dissipation.

9.1.3 Reception Branch

The reception branch performs automatically all the tasks needed to process received data. PHY layer delivers data to MAC layer through the BUF_RXi.

Figure 9-3. Reception Branch



9.1.4 Analog Front End control

9.1.4.1 Gain control

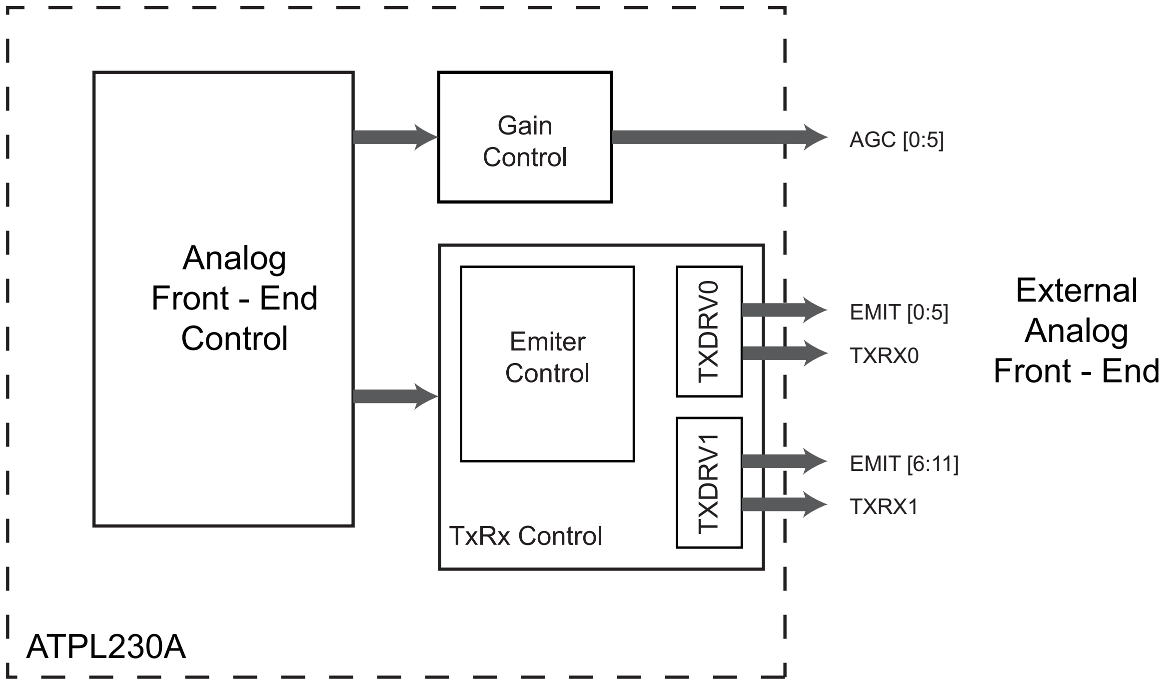
This block implements an Automatic Gain Control (AGC) which attenuates the PLC input signal via activating some outputs of the ATPL230A, so there is no saturation and therefore no distortion in the OFDM signal.

There are 6 outputs of the ATPL230A controlled by this peripheral. AGC0, AGC1, AGC2, AGC3, AGC4 and AGC5. Please see reference design for further information and recommended external circuitry values.

9.1.4.2 TxRx control

This block modifies the configuration of the external Analog Front End by means of TXRX outputs. There are two TXRX outputs, one for each TXDRV. These digital outputs are used to modify external filter conditions between transmission and reception. To allow different external circuitry topologies, the polarity of both signals can be inverted by hardware (see "TXRX Polarity Selector Register").

Figure 9-4. TxRx control block diagram



See reference design for further information about TxRx control.

9.1.5 Carrier Detection

Looking for an easy detection of incoming messages, the PRIME specification defines a carrier detection algorithm that shall be based on preamble detection and header recognition. ATPL230A implements by hardware a set of detection techniques to control access to medium, thus improving frame synchronization in reception and decreasing collision ratio in transmission.

9.2 PHY parameters

A complete description of the PRIME PHY Layer can be found in PRIME specification. Please refer to the PRIME specification provided by the PRIME Alliance in www.prime-alliance.org

PRIME specifies a complete set of primitives to manage the PHY Layer, and the PHY-SAP (PHY Service Access Point) from MAC layer. Doc43048 "Atmel PRIME Implementation" integrates all these functions, making them transparent to the final user and simplifying the management.

9.3 PHY Layer Registers

9.3.1 PHY Configuration Registers

9.3.1.1 PHY Layer Special Function Register

Name: PHY_SFR

Address: 0xFE2A

Access: Read/Write

Reset: 0x87

7	6	5	4	3	2	1	0
BCH_ERR	CD	UMD	-	-	-	-	INT_PHY

- **BCH_ERR: Busy Channel Error Flag**

  This bit is cleared to ‘0’ by hardware to indicate the presence of an OFDM signal at the transmission instant. Otherwise, this field value is ‘1’.

  This bit is used for returning a result of “Busy Channel” in the PHY_DATA confirm primitive (see PRIME specification).

- **CD: Carrier Detect bit**

  This bit is set to ‘1’ by hardware when an OFDM signal is detected, and it is active during the whole reception.

  This bit is used in channel access (CSMA-CA algorithm) for performing channel-sensing.

- **UMD: Unsupported Modulation Scheme flag**

  This flag is set to ‘1’ by hardware every time a header with correct CRC is received, but the PROTOCOL field in this header indicates a modulation scheme not supported by the system.

- **INT_PHY: Physical Layer interruption**

  This bit is internally connected to the EINT pin.

  It is Low level active and it is set to '0' by the PHY layer to trigger an interrupt in the external host.

  In reception, every time a PLC message is received, the PHY layer generates two interrupts. One of them when the physical header is correctly received (two first symbols), and the other one when the message is completely received.

  In transmission, an interrupt will be generated every time a complete message has been sent.

  The signal is cleared by writing '1' in the bit PHY_SFR(0).

9.3.1.2 Channel selector Register

Name: CTPS

Address: 0xFEFA (MSB) – 0xFEFD (LSB)

Access: Read/Write

Reset: 0x000150C7

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	CTPS (24)
23	22	21	20	19	18	17	16
CTPS(23:16)							
15	14	13	12	11	10	9	8
CTPS(15:8)							
7	6	5	4	3	2	1	0
CTPS(7:0)							

Configures the channel:

Value	Name	Description
0x000150C7	CHANNEL1	42 - 89 kHz
0x00026A44	CHANNEL2	97 - 144 kHz
0x000383C1	CHANNEL3	151 - 198 kHz
0x00049D3D	CHANNEL4	206 - 253 kHz
0x0005B6BA	CHANNEL5	261 - 308 kHz
0x0006D036	CHANNEL6	315 - 362 kHz
0x0007E9B3	CHANNEL7	370 - 417 kHz
0x00090330	CHANNEL8	425 - 472 kHz

9.3.2 RX Buffers Registers

9.3.2.1 RX Time Registers

Name: TXRXBUF_RECTIME_RX0
Address: 0xFD83 – 0xFD86
Access: Read-only
Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_RECTIME_RX0 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_RECTIME_RX0 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_RECTIME_RX0 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_RECTIME_RX0 (7:0)							

Reception Time in Buffer 0.

Name: TXRXBUF_RECTIME_RX1
Address: 0xFD87 – 0xFD8A
Access: Read-only
Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_RECTIME_RX1 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_RECTIME_RX1 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_RECTIME_RX1 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_RECTIME_RX1 (7:0)							

Reception Time in Buffer 1.

Name: TXRXBUF_RECTIME_RX2
Address: 0xFD8B – 0xFD8E
Access: Read-only
Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_RECTIME_RX2 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_RECTIME_RX2 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_RECTIME_RX2 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_RECTIME_RX2 (7:0)							

Reception Time in Buffer 2.

Name: TXRXBUF_RECTIME_RX3
Address: 0xFD8F – 0xFD92
Access: Read-only
Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_RECTIME_RX3 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_RECTIME_RX3 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_RECTIME_RX3 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_RECTIME_RX3 (7:0)							

Reception Time in Buffer 3.

When there has been a reception, these registers show when it happened.

9.3.2.2 Buffer Selection Register

Name: TXRXBUF_SELECT_BUFF_RX

Address: 0xFDD3

Access: Read/Write

Reset: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	SB3	SB2	SB1	SB0

Select Reception Buffer: It is used to establish what reception buffers are active.

- **SB0: Select Buffer 0**

  0: Disable Buffer

  1: Enable Buffer

- **SB1: Select Buffer 1**

  0: Disable Buffer

  1: Enable Buffer

- **SB2: Select Buffer 2**

  0: Disable Buffer

  1: Enable Buffer

- **SB3: Select Buffer 3**

  0: Disable Buffer

  1: Enable Buffer

9.3.2.3 RX Interrupts Register

Name: TXRXBUF_RX_INT

Address: 0xFDD4

Access: Read/Write

Reset: 0x00

7	6	5	4	3	2	1	0
PI_RX3	PI_RX2	PI_RX1	PI_RX0	HI_RX3	HI_RX2	HI_RX1	HI_RX0

Interrupt Reception Register: When there is some issue with the reception, the micro is warned and then micro tests what buffer is affected through this register.

- **PI_RX3: Notice Payload Interrupt Reception Buffer 3**
- **PI_RX2: Notice Payload Interrupt Reception Buffer 2**
- **PI_RX1: Notice Payload Interrupt Reception Buffer 1**
- **PI_RX0: Notice Payload Interrupt Reception Buffer 0**
- **HI_RX3: Notice Header Interrupt Reception Buffer 3**
- **HI_RX2: Notice Header Interrupt Reception Buffer 2**
- **HI_RX1: Notice Header Interrupt Reception Buffer 1**
- **HI_RX0: Notice Header Interrupt Reception Buffer 0**

9.3.2.4 RX Configuration Register

Name: TXRXBUF_RXCONF

Address: 0xFDD5

Access: Read/Write

Reset: 0x02

7	6	5	4	3	2	1	0
DIS_RX3	DIS_RX2	DIS_RX1	DIS_RX0	NEXT_BUF		EH	MS

This register permits us configure/know several features in reception:

- Disable an active reception interrupt.
- Knowing what buffer will be the next to be written.
- Enable/disable header interruptions.
- Activate/deactivate the overwrite mode in buffer reception when a reception is received.

- **DIS_RX3: Disable Interrupt Buffer 3**

  0: Enabled

  1: Disabled

- **DIS_RX2: Disable Interrupt Buffer 2**

  0: Enabled

  1: Disabled

- **DIS_RX1: Disable Interrupt Buffer 1**

  0: Enabled

  1: Disabled

- **DIS_RX0: Disable Interrupt Buffer 0**

  0: Enabled

  1: Disabled

- **NEXT_BUF: It shows the next buffer which will be written**

  0: Buffer 0

  1: Buffer 1

  2: Buffer 2

  3: Buffer 3

- **EH: Disable header interruptions**

  0: Disabled

  1: Enabled

- **MS: Enable overwrite mode**

  0: Disabled

  1: Enabled

9.3.2.5 RX Initial Address Registers

Name: TXRXBUF_INITAD_RX0
Address: 0xFDD6 - 0xFDD7
Access: Read/Write
Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_INITAD_RX0 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_INITAD_RX0 (7:0)							

Initial Address of Reception Buffer 0.

Name: TXRXBUF_INITAD_RX1
Address: 0xFDD8 - 0xFDD9
Access: Read/Write
Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_INITAD_RX1 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_INITAD_RX1 (7:0)							

Initial Address of Reception Buffer 1.

Name: TXRXBUF_INITAD_RX2
Address: 0xFDDA - 0xFDDB
Access: Read/Write
Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_INITAD_RX2 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_INITAD_RX2 (7:0)							

Initial Address of Reception Buffer 2.

Name: TXRXBUF_INITAD_RX3
Address: 0xFDDC - 0xFDDD
Access: Read/Write
Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_INITAD_RX3 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_INITAD_RX3 (7:0)							

Initial Address of Reception Buffer 3.

These four registers contain four pointers to the beginning of the respective Rx buffer in peripheral memory (buffer 0 to 3). This way, buffers are configurable in both size and position.

9.3.2.6 Robust RX Mode Register

Name: TXRXBUF_RXCONF_ROBO_MODE

Address: 0xFDF3

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
RC_RX3		RC_RX2		RC_RX1		RC_RX0	

This register shows the reception mode of each RX buffer:

- **RC_RX0:** Buffer 0 reception mode.
- **RC_RX1:** Buffer 1 reception mode.
- **RC_RX2:** Buffer 2 reception mode.
- **RC_RX3:** Buffer 3 reception mode.

Value	Name	Description
0	PRIME 1.3	Mode PRIME v1.3
1	Reserved	Reserved
2	PRIME 1.4	PRIME v1.4 reception mode
3	PRIME 1.4 c	PRIME v1.4 reception backwards compatible mode

9.3.3 RX Info Registers

9.3.3.1 Minimum RSSI Registers

Name: TXRXBUF_RSSIMIN_RX0

Address: 0xFD6B

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIMIN_RX0							

This register stores the minimum RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX0. The measurement is done at symbol level. The value is stored in dB.

Name: TXRXBUF_RSSIMIN_RX1

Address: 0xFD6C

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIMIN_RX1							

This register stores the minimum RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX1. The measurement is done at symbol level. The value is stored in dB.

Name: TXRXBUF_RSSIMIN_RX2

Address: 0xFD6D

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIMIN_RX2							

This register stores the minimum RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX2. The measurement is done at symbol level. The value is stored in dB.

Name: TXRXBUF_RSSIMIN_RX3

Address: 0xFD6E

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIMIN_RX3							

This register stores the minimum RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX3. The measurement is done at symbol level. The value is stored in dB.

9.3.3.2 Average RSSI Registers

Name: TXRXBUF_RSSIAVG_RX0

Address: 0xFD6F

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIAVG_RX0							

This register stores the average RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX0. The measurement is done at symbol level. The value is stored in dB.

Name: TXRXBUF_RSSIAVG_RX1

Address: 0xFD70

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIAVG_RX1							

This register stores the average RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX1. The measurement is done at symbol level. The value is stored in dB.

Name: TXRXBUF_RSSIAVG_RX2

Address: 0xFD71

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIAVG_RX2							

This register stores the average RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX2. The measurement is done at symbol level. The value is stored in dB.

Name: TXRXBUF_RSSIAVG_RX3

Address: 0xFD72

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIAVG_RX3							

This register stores the average RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX3. The measurement is done at symbol level. The value is stored in dB.

9.3.3.3 Maximum RSSI Registers

Name: TXRXBUF_RSSIMAX_RX0

Address: 0xFD73

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIMAX_RX0							

This register stores the maximum RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX0. The measurement is done at symbol level. The value is stored in dB.

Name: TXRXBUF_RSSIMAX_RX1

Address: 0xFD74

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIMAX_RX1							

This register stores the maximum RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX1. The measurement is done at symbol level. The value is stored in dB.

Name: TXRXBUF_RSSIMAX_RX2

Address: 0xFD75

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIMAX_RX2							

This register stores the maximum RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX2. The measurement is done at symbol level. The value is stored in dB.

Name: TXRXBUF_RSSIMAX_RX3

Address: 0xFD76

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIMAX_RX3							

This register stores the maximum RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX3. The measurement is done at symbol level. The value is stored in dB.

9.3.3.4 Minimum CINR Registers

Name: TXRXBUF_CINRMIN_RX0

Address: 0xFD77

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_CINRMIN_RX0							

This register stores the minimum CINR (Carrier to Interference + Noise ratio) value measured in the last message received in BUF_RX0. The measurement is done at symbol level. The value is stored in ¼ dB steps.

Name: TXRXBUF_CINRMIN_RX1

Address: 0xFD78

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_CINRMIN_RX1							

This register stores the minimum CINR (Carrier to Interference + Noise ratio) value measured in the last message received in BUF_RX1. The measurement is done at symbol level. The value is stored in ¼ dB steps.

Name: TXRXBUF_CINRMIN_RX2

Address: 0xFD79

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_CINRMIN_RX2							

This register stores the minimum CINR (Carrier to Interference + Noise ratio) value measured in the last message received in BUF_RX2. The measurement is done at symbol level. The value is stored in ¼ dB steps.

Name: TXRXBUF_CINRMIN_RX3

Address: 0xFD7A

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_CINRMIN_RX3							

This register stores the minimum CINR (Carrier to Interference + Noise ratio) value measured in the last message received in BUF_RX3. The measurement is done at symbol level. The value is stored in ¼ dB steps.

9.3.3.5 Average CINR Registers

Name: TXRXBUF_CINRAVG_RX0

Address: 0xFD7B

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_CINRAVG_RX0							

This register stores the average CINR (Carrier to Interference + Noise ratio) value measured in the last message received in BUF_RX0. The measurement is done at symbol level. The value is stored in ¼ dB steps.

Name: TXRXBUF_CINRAVG_RX1

Address: 0xFD7C

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_CINRAVG_RX1							

This register stores the average CINR (Carrier to Interference + Noise ratio) value measured in the last message received in BUF_RX1. The measurement is done at symbol level. The value is stored in ¼ dB steps.

Name: TXRXBUF_CINRAVG_RX2

Address: 0xFD7D

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_CINRAVG_RX2							

This register stores the average CINR (Carrier to Interference + Noise ratio) value measured in the last message received in BUF_RX2. The measurement is done at symbol level. The value is stored in ¼ dB steps.

Name: TXRXBUF_CINRAVG_RX3

Address: 0xFD7E

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_CINRAVG_RX3							

This register stores the average CINR (Carrier to Interference + Noise ratio) value measured in the last message received in BUF_RX3. The measurement is done at symbol level. The value is stored in ¼ dB steps.

9.3.3.6 Maximum CINR Registers

Name: TXRXBUF_CINRMAX_RX0

Address: 0xFD7F

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_CINRMAX_RX0							

This register stores the maximum CINR (Carrier to Interference + Noise ratio) value measured in the last message received in BUF_RX0. The measurement is done at symbol level. The value is stored in ¼ dB steps.

Name: TXRXBUF_CINRMAX_RX1

Address: 0xFD80

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_CINRMAX_RX1							

This register stores the maximum CINR (Carrier to Interference + Noise ratio) value measured in the last message received in BUF_RX1. The measurement is done at symbol level. The value is stored in ¼ dB steps.

Name: TXRXBUF_CINRMAX_RX2

Address: 0xFD81

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_CINRMAX_RX2							

This register stores the maximum CINR (Carrier to Interference + Noise ratio) value measured in the last message received in BUF_RX2. The measurement is done at symbol level. The value is stored in ¼ dB steps.

Name: TXRXBUF_CINRMAX_RX3

Address: 0xFD82

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_CINRMAX_RX3							

This register stores the maximum CINR (Carrier to Interference + Noise ratio) value measured in the last message received in BUF_RX3. The measurement is done at symbol level. The value is stored in ¼ dB steps.

9.3.3.7 Header EVM Registers

Name: TXRXBUF_EVM_HD_RX0

Address: 0xFDA3 - 0xFDA4

Access: Read-only

Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_EVM_HD_RX0 (15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXRXBUF_EVM_HD_RX0 (7:0)							

This register stores the maximum EVM (Error Vector Magnitude) measured in the reception of the last message header in BUF_RX0. The 7 msb, TXRXBUF_EVM_HD_RX0 (15:9), represent the integer part in %, being the TXRXBUF_EVM_HD_RX0 (8:0) bits the fractional part if more precision were required.

This register is used by the physical layer for being in accordance with PRIME specification.

Name: TXRXBUF_EVM_HD_RX1

Address: 0xFDA5 - 0xFDA6

Access: Read-only

Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_EVM_HD_RX1 (15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXRXBUF_EVM_HD_RX1 (7:0)							

This register stores the maximum EVM (Error Vector Magnitude) measured in the reception of the last message header in BUF_RX1. The 7 msb, TXRXBUF_EVM_HD_RX1 (15:9), represent the integer part in %, being the TXRXBUF_EVM_HD_RX1 (8:0) bits the fractional part if more precision were required.

This register is used by the physical layer for being in accordance with PRIME specification.

Name: TXRXBUF_EVM_HD_RX2

Address: 0xFDA7 - 0xFDA8

Access: Read-only

Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_EVM_HD_RX2 (15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXRXBUF_EVM_HD_RX2 (7:0)							

This register stores the maximum EVM (Error Vector Magnitude) measured in the reception of the last message header in BUF_RX2. The 7 msb, TXRXBUF_EVM_HD_RX2 (15:9), represent the integer part in %, being the TXRXBUF_EVM_HD_RX2 (8:0) bits the fractional part if more precision were required.

This register is used by the physical layer for being in accordance with PRIME specification.

Name: TXRXBUF_EVM_HD_RX3

Address: 0xFDA9 - 0xFDAA

Access: Read-only

Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_EVM_HD_RX3 (15:8)							

7	6	5	4	3	2	1	0
TXRXBUF_EVM_HD_RX3 (7:0)							

This register stores the maximum EVM (Error Vector Magnitude) measured in the reception of the last message header in BUF_RX3. The 7 msb, TXRXBUF_EVM_HD_RX3 (15:9), represent the integer part in %, being the TXRXBUF_EVM_HD_RX3 (8:0) bits the fractional part if more precision were required.

This register is used by the physical layer for being in accordance with PRIME specification.

9.3.3.8 Payload EVM Registers

Name: TXRXBUF_EVM_PYLD_RX0

Address: 0xFDAB - 0xFDAC

Access: Read-only

Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_EVM_PYLD_RX0 (15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXRXBUF_EVM_PYLD_RX0 (7:0)							

This register stores the maximum EVM (Error Vector Magnitude) measured in the reception of the last message payload in BUF_RX0. The 7 msb, TXRXBUF_EVM_PYLD_RX0 (15:9), represent the integer part in %, being the TXRXBUF_EVM_PYLD_RX0 (8:0) bits the fractional part if more precision were required.

Name: TXRXBUF_EVM_PYLD_RX1

Address: 0xFDAD - 0xFDAE

Access: Read-only

Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_EVM_PYLD_RX1 (15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXRXBUF_EVM_PYLD_RX1 (7:0)							

This register stores the maximum EVM (Error Vector Magnitude) measured in the reception of the last message payload in BUF_RX1. The 7 msb, TXRXBUF_EVM_PYLD_RX1 (15:9), represent the integer part in %, being the TXRXBUF_EVM_PYLD_RX1 (8:0) bits the fractional part if more precision were required.

Name: TXRXBUF_EVM_PYLD_RX2

Address: 0xFDAF - 0xFDB0

Access: Read-only

Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_EVM_PYLD_RX2 (15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXRXBUF_EVM_PYLD_RX2 (7:0)							

This register stores the maximum EVM (Error Vector Magnitude) measured in the reception of the last message payload in BUF_RX2. The 7 msb, TXRXBUF_EVM_PYLD_RX2 (15:9), represent the integer part in %, being the TXRXBUF_EVM_PYLD_RX2 (8:0) bits the fractional part if more precision were required.

Name: TXRXBUF_EVM_PYLD_RX3

Address: 0xFDB1 - 0xFDB2

Access: Read-only

Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_EVM_PYLD_RX3 (15:8)							

7	6	5	4	3	2	1	0
TXRXBUF_EVM_PYLD_RX3 (7:0)							

This register stores the maximum EVM (Error Vector Magnitude) measured in the reception of the last message payload in BUF_RX3. The 7 msb, TXRXBUF_EVM_PYLD_RX3 (15:9), represent the integer part in %, being the TXRXBUF_EVM_PYLD_RX3 (8:0) bits the fractional part if more precision were required.

9.3.3.9 Accumulated Header EVM Registers

Name: TXRXBUF_EVM_HDACUM_RX0

Address: 0xFDB3 - 0xFDB6

Access: Read-only

Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_EVM_HDACUM_RX0 (20:13)							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXRXBUF_EVM_HDACUM_RX0 (12:5)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXRXBUF_EVM_HDACUM_RX0 (4:0)					0	0	0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0

When receiving an OFDM symbol, the total sum of all its individual carriers EVMs (Error Vector Magnitude) is calculated in order to further calculate the average EVM value. This register stores the maximum total sum between the two OFDM symbols received in the last message header in BUF_RX0.

Name: TXRXBUF_EVM_HDACUM_RX1

Address: 0xFDB7 - 0xFDBA

Access: Read-only

Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_EVM_HDACUM_RX1 (20:13)							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXRXBUF_EVM_HDACUM_RX1 (12:5)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXRXBUF_EVM_HDACUM_RX1 (4:0)					0	0	0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0

When receiving an OFDM symbol, the total sum of all its individual carriers EVMs (Error Vector Magnitude) is calculated in order to further calculate the average EVM value. This register stores the maximum total sum between the two OFDM symbols received in the last message header in BUF_RX1.

Name: TXRXBUF_EVM_HDACUM_RX2

Address: 0xFDBB - 0xFDBE

Access: Read-only

Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_EVM_HDACUM_RX2 (20:13)							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXRXBUF_EVM_HDACUM_RX2 (12:5)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXRXBUF_EVM_HDACUM_RX2 (4:0)					0	0	0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0

When receiving an OFDM symbol, the total sum of all its individual carriers EVMs (Error Vector Magnitude) is calculated in order to further calculate the average EVM value. This register stores the maximum total sum between the two OFDM symbols received in the last message header in BUF_RX2.

Name: TXRXBUF_EVM_HDACUM_RX3

Address: 0xFDBF - 0xFDC2

Access: Read-only

Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_EVM_HDACUM_RX3 (20:13)							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXRXBUF_EVM_HDACUM_RX3 (12:5)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXRXBUF_EVM_HDACUM_RX3 (4:0)					0	0	0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0

When receiving an OFDM symbol, the total sum of all its individual carriers EVMs (Error Vector Magnitude) is calculated in order to further calculate the average EVM value. This register stores the maximum total sum between the two OFDM symbols received in the last message header in BUF_RX3.

9.3.3.10 Accumulated Payload EVM Registers

Name: TXRXBUF_EVM_PYLACUM_RX0

Address: 0xFDC3 - 0xFDC6

Access: Read-only

Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_EVM_PYLACUM_RX0 (20:13)							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXRXBUF_EVM_PYLACUM_RX0 (12:5)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXRXBUF_EVM_PYLACUM_RX0 (4:0)					0	0	0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0

When receiving an OFDM symbol, the total sum of all its individual carriers EVMs (Error Vector Magnitude) is calculated in order to further calculate the average EVM value. This register stores the maximum total sum between the two OFDM symbols received in the last message payload in BUF_RX0.

Name: TXRXBUF_EVM_PYLACUM_RX1

Address: 0xFDC7 - 0xFDCA

Access: Read-only

Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_EVM_PYLACUM_RX1 (20:13)							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXRXBUF_EVM_PYLACUM_RX1 (12:5)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXRXBUF_EVM_PYLACUM_RX1 (4:0)					0	0	0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0

When receiving an OFDM symbol, the total sum of all its individual carriers EVMs (Error Vector Magnitude) is calculated in order to further calculate the average EVM value. This register stores the maximum total sum between the two OFDM symbols received in the last message payload in BUF_RX1.

Name: TXRXBUF_EVM_PYLACUM_RX2

Address: 0xFDCB - 0xFDCE

Access: Read-only

Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_EVM_PYLACUM_RX2 (20:13)							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXRXBUF_EVM_PYLACUM_RX2 (12:5)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXRXBUF_EVM_PYLACUM_RX2 (4:0)					0	0	0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0

When receiving an OFDM symbol, the total sum of all its individual carriers EVMs (Error Vector Magnitude) is calculated in order to further calculate the average EVM value. This register stores the maximum total sum between the two OFDM symbols received in the last message payload in BUF_RX2.

Name: TXRXBUF_EVM_PYLACUM_RX3

Address: 0xFDCF - 0xFDD2

Access: Read-only

Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_EVM_PYLACUM_RX3 (20:13)							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXRXBUF_EVM_PYLACUM_RX3 (12:5)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXRXBUF_EVM_PYLACUM_RX3 (4:0)					0	0	0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	0	0	0	0	0	0	0

When receiving an OFDM symbol, the total sum of all its individual carriers EVMs (Error Vector Magnitude) is calculated in order to further calculate the average EVM value. This register stores the maximum total sum between the two OFDM symbols received in the last message payload in BUF_RX3.

9.3.4 TX Config Registers

9.3.4.1 Global Amplitude Registers

Name: TXRXBUF_GLBL_AMP_TX0
Address: 0xFD20
Access: Read/Write
Reset: 0xFF

7	6	5	4	3	2	1	0
TXRXBUF_GLBL_AMP_TX0							

Being “Amax” the maximum voltage reachable in the external driver MOS couple, this register sets the global amplitude for the transmitted frame (chirp+header+payload), when BUF_TX0 is used, following this formula:

$$FinalAmplitude = A\max * \left(\frac{TXRXBUF\_GLBL\_AMP\_TX0}{255} \right)$$

Name: TXRXBUF_GLBL_AMP_TX1
Address: 0xFD21
Access: Read/Write
Reset: 0xFF

7	6	5	4	3	2	1	0
TXRXBUF_GLBL_AMP_TX1							

Being “Amax” the maximum voltage reachable in the external driver MOS couple, this register sets the global amplitude for the transmitted frame (chirp+header+payload), when BUF_TX1 is used, following this formula:

$$FinalAmplitude = A\max * \left(\frac{TXRXBUF\_GLBL\_AMP\_TX1}{255} \right)$$

Name: TXRXBUF_GLBL_AMP_TX2
Address: 0xFD22
Access: Read/Write
Reset: 0xFF

7	6	5	4	3	2	1	0
TXRXBUF_GLBL_AMP_TX2							

Being “Amax” the maximum voltage reachable in the external driver MOS couple, this register sets the global amplitude for the transmitted frame (chirp+header+payload), when BUF_TX2 is used, following this formula:

$$FinalAmplitude = A\max * \left(\frac{TXRXBUF\_GLBL\_AMP\_TX2}{255} \right)$$

Name: TXRXBUF_GLBL_AMP_TX3

Address: 0xFD23

Access: Read/Write

Reset: 0xFF

7	6	5	4	3	2	1	0
TXRXBUF_GLBL_AMP_TX3							

Being "Amax" the maximum voltage reachable in the external driver MOS couple, this register sets the global amplitude for the transmitted frame (chirp+header+payload), when BUF_TX3 is used, following this formula:

$$FinalAmplitude = A\max * \left(\frac{TXRXBUF\_GLBL\_AMP\_TX3}{255} \right)$$

9.3.4.2 Signal Amplitude Registers

Name: TXRXBUF_SGNL_AMP_TX0
Address: 0xFD24
Access: Read/Write
Reset: 0x60

7	6	5	4	3	2	1	0
TXRXBUF_SGNL_AMP_TX0							

This register stores the amplitude value for the transmitted frame (only header+payload; chirp not affected), when BUF_TX0 is used. If this value is equal to 0xFF, the header+payload transmitted are not attenuated. If this register is equal to 0x00, the header+payload are nullified.

Name: TXRXBUF_SGNL_AMP_TX1
Address: 0xFD25
Access: Read/Write
Reset: 0x60

7	6	5	4	3	2	1	0
TXRXBUF_SGNL_AMP_TX1							

This register stores the amplitude value for the transmitted frame (only header+payload; chirp not affected), when BUF_TX1 is used. If this value is equal to 0xFF, the header+payload transmitted are not attenuated. If this register is equal to 0x00, the header+payload are nullified.

Name: TXRXBUF_SGNL_AMP_TX2
Address: 0xFD26
Access: Read/Write
Reset: 0x60

7	6	5	4	3	2	1	0
TXRXBUF_SGNL_AMP_TX2							

This register stores the amplitude value for the transmitted frame (only header+payload; chirp not affected), when BUF_TX2 is used. If this value is equal to 0xFF, the header+payload transmitted are not attenuated. If this register is equal to 0x00, the header+payload are nullified.

Name: TXRXBUF_SGNL_AMP_TX3
Address: 0xFD27
Access: Read/Write
Reset: 0x60

7	6	5	4	3	2	1	0
TXRXBUF_SGNL_AMP_TX3							

This register stores the amplitude value for the transmitted frame (only header+payload; chirp not affected), when BUF_TX3 is used. If this value is equal to 0xFF, the header+payload transmitted are not attenuated. If this register is equal to 0x00, the header+payload are nullified.

9.3.4.3 Chirp Amplitude Registers

Name: TXRXBUF_CHIRP_AMP_TX0
Address: 0xFD28
Access: Read/Write
Reset: 0x60

7	6	5	4	3	2	1	0
TXRXBUF_CHIRP_AMP_TX0							

This register stores the amplitude value for the transmitted chirp (header and payload not affected), when BUF_TX0 is used. If this value is equal to 0xFF, the chirp transmitted is not attenuated. If this register is equal to 0x00, the chirp is nullified.

Name: TXRXBUF_CHIRP_AMP_TX1
Address: 0xFD29
Access: Read/Write
Reset: 0x60

7	6	5	4	3	2	1	0
TXRXBUF_CHIRP_AMP_TX1							

This register stores the amplitude value for the transmitted chirp (header and payload not affected), when BUF_TX1 is used. If this value is equal to 0xFF, the chirp transmitted is not attenuated. If this register is equal to 0x00, the chirp is nullified.

Name: TXRXBUF_CHIRP_AMP_TX2
Address: 0xFD2A
Access: Read/Write
Reset: 0x60

7	6	5	4	3	2	1	0
TXRXBUF_CHIRP_AMP_TX2							

This register stores the amplitude value for the transmitted chirp (header and payload not affected), when BUF_TX2 is used. If this value is equal to 0xFF, the chirp transmitted is not attenuated. If this register is equal to 0x00, the chirp is nullified.

Name: TXRXBUF_CHIRP_AMP_TX3
Address: 0xFD2B
Access: Read/Write
Reset: 0x60

7	6	5	4	3	2	1	0
TXRXBUF_CHIRP_AMP_TX3							

This register stores the amplitude value for the transmitted chirp (header and payload not affected), when BUF_TX3 is used. If this value is equal to 0xFF, the chirp transmitted is not attenuated. If this register is equal to 0x00, the chirp is nullified.

9.3.5 TX Buffers Registers

9.3.5.1 TX Time Registers

Name: TXRXBUF_EMITIME_TX0
Address: 0xFD00 - 0xFD03
Access: Read/Write
Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_EMITIME_TX0 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_EMITIME_TX0 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_EMITIME_TX0 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_EMITIME_TX0 (7:0)							

Transmission time of Buffer 0.

Name: TXRXBUF_EMITIME_TX1
Address: 0xFD04 - 0xFD07
Access: Read/Write
Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_EMITIME_TX1 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_EMITIME_TX1 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_EMITIME_TX1 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_EMITIME_TX1 (7:0)							

Transmission time of Buffer 1.

Name: TXRXBUF_EMITIME_TX2
Address: 0xFD08 - 0xFD0B
Access: Read/Write
Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_EMITIME_TX2 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_EMITIME_TX2 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_EMITIME_TX2 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_EMITIME_TX2 (7:0)							

Transmission time of Buffer 2.

Name: TXRXBUF_EMITIME_TX3
Address: 0xFD0C - 0xFD0F
Access: Read/Write
Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_EMITIME_TX3 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_EMITIME_TX3 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_EMITIME_TX3 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_EMITIME_TX3 (7:0)							

Transmission time of Buffer 3.

These registers contain the time value (referenced to the 20-bit PHY layer global timer) when a programmed transmission in the corresponding buffer shall begin.

9.3.5.2 TX Post-activation Time TxRx Registers

Name: TXRXBUF_TXRX_TA_TX0
Address: 0xFD10 - 0xFD11
Access: Read/Write
Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_TXRX_TA_TX0 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_TXRX_TA_TX0 (7:0)							

Post-activation time TxRx of Buffer 0.

Name: TXRXBUF_TXRX_TA_TX1
Address: 0xFD12 - 0xFD13
Access: Read/Write
Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_TXRX_TA_TX1 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_TXRX_TA_TX1 (7:0)							

Post-activation time TxRx of Buffer 1.

Name: TXRXBUF_TXRX_TA_TX2
Address: 0xFD14 - 0xFD15
Access: Read/Write
Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_TXRX_TA_TX2 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_TXRX_TA_TX2 (7:0)							

Post-activation time TxRx of Buffer 2.

Name: TXRXBUF_TXRX_TA_TX3
Address: 0xFD16 - 0xFD17
Access: Read/Write
Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_TXRX_TA_TX3 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_TXRX_TA_TX3 (7:0)							

Post-activation time TxRx of Buffer 3.

The user can modify these registers to set the period of time to maintain active (according to polarity) TXRX output signals once a transmission has finished. This parameter is useful to improve the external coupling transient response. When automatic TxRx has been selected, in these registers must be set this time for the suitable buffer.

9.3.5.3 TX Pre-activation Time TxRx Registers

Name: TXRXBUF_TXRX_TB_TX0
Address: 0xFD18 - 0xFD19
Access: Read/Write
Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_TXRX_TB_TX0 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_TXRX_TB_TX0 (7:0)							

Pre-activation time TxRx of Buffer 0.

Name: TXRXBUF_TXRX_TB_TX1
Address: 0xFD1A - 0xFD1B
Access: Read/Write
Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_TXRX_TB_TX1 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_TXRX_TB_TX1 (7:0)							

Pre-activation time TxRx of Buffer 1.

Name: TXRXBUF_TXRX_TB_TX2
Address: 0xFD1C - 0xFD1D
Access: Read/Write
Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_TXRX_TB_TX2 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_TXRX_TB_TX2 (7:0)							

Pre-activation time TxRx of Buffer 2.

Name: TXRXBUF_TXRX_TB_TX3
Address: 0xFD1E - 0xFD1F
Access: Read/Write
Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_TXRX_TB_TX3 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_TXRX_TB_TX3 (7:0)							

Pre-activation time TxRx of Buffer 3.

The user can modify these registers to specify the period of time to set active (according to polarity) TXRX output signals before a transmission starts. This parameter is useful to improve the external coupling transient response. When automatic TxRx has been selected, in these registers must be set this time for the suitable buffer.

9.3.5.4 TX Timeout Registers

Name: TXRXBUF_TIMEOUT_TX0
Address: 0xFD2C - 0xFD2F
Access: Read/Write
Reset: 0x000124F8

31	30	29	28	27	26	25	24
TXRXBUF_TIMEOUT_TX0 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_TIMEOUT_TX0 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_TIMEOUT_TX0 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_TIMEOUT_TX0 (7:0)							

Timeout Buffer 0.

Name: TXRXBUF_TIMEOUT_TX1
Address: 0xFD30 - 0xFD33
Access: Read/Write
Reset: 0x000124F8

31	30	29	28	27	26	25	24
TXRXBUF_TIMEOUT_TX1 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_TIMEOUT_TX1 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_TIMEOUT_TX1 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_TIMEOUT_TX1 (7:0)							

Timeout Buffer 1.

Name: TXRXBUF_TIMEOUT_TX2
Address: 0xFD34 - 0xFD37
Access: Read/Write
Reset: 0x000124F8

31	30	29	28	27	26	25	24
TXRXBUF_TIMEOUT_TX2 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_TIMEOUT_TX2 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_TIMEOUT_TX2 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_TIMEOUT_TX2 (7:0)							

Timeout Buffer 2.

Name: TXRXBUF_TIMEOUT_TX3
Address: 0xFD38 - 0xFD3B
Access: Read/Write
Reset: 0x000124F8

31	30	29	28	27	26	25	24
TXRXBUF_TIMEOUT_TX3 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_TIMEOUT_TX3 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_TIMEOUT_TX3 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_TIMEOUT_TX3 (7:0)							

Timeout Buffer 3.

Transmission timeout. Maximum period of time that the PHY layer shall wait before discarding a frame that is waiting to be transmitted.

9.3.5.5 TX Configuration Registers

Name: TXRXBUF_TXCONF_TX0

Address: 0xFD3C

Access: Read/Write

Reset: 0xA0

7	6	5	4	3	2	1	0
-	TRS0	ATR0	-	FE0	EB0	DC0	DR0

- **TRS0: TxRx established by software in buffer 0.** TxRx established by software for activated/deactivated TXRX signal before/after each transmission to work properly transistors when this feature has been selected.

  0: Disabled

  1: Enabled

- **ATR0: TxRx control mode in buffer 0.** Establishing software/hardware control of TXRX signal for transmitting.

  1**:** by hardware

  0: by software

- **FE0: Transmission forced/unforced in buffer 0.** When force transmission is required, if it is possible (Carrier Detection or Reception are in course and not disable) and suitable buffer is enabled, a transmission is immediately started.

  0: Transmission unforced

  1: Transmission forced

- **EB0: Buffer 0 enabled/disabled in buffer 0.** Enable buffer that it has been required.

  0: Disabled

  1: Enabled

- **DC0: Carrier Detect enabled/disabled for transmission in buffer 0.** Starting transmission though carrier detection is in course.

  0: Enabled

  1: Disabled

- **DR0: Reception enabled/disabled for transmission in buffer 0.** Starting transmission though reception is in course.

  0: Enabled

  1: Disabled

Name: TXRXBUF_TXCONF_TX1

Address: 0xFD3D

Access: Read/Write

Reset: 0xA0

7	6	5	4	3	2	1	0
-	TRS1	ATR1	-	FE1	EB1	DC1	DR1

- **TRS1: TxRx established by software in buffer 1.** TxRx established by software for activated/deactivated TXRX signal before/after each transmission to work properly transistors when this feature has been selected.

  0: Disabled

  1: Enabled

- **ATR1: TxRx control mode in buffer 1.** Establishing software/hardware control of TXRX signal for transmitting.

  1: by hardware

  0: by software

- **FE1: Transmission forced/unforced in buffer 1.** When force transmission is required, if it is possible (Carrier Detection or Reception are in course and not disable) and suitable buffer is enabled, a transmission is immediately started.

  0: Transmission unforced

  1: Transmission forced

- **EB1: Buffer 0 enabled/disabled in buffer 1.** Enable buffer that it has been required.

  0: Disabled

  1: Enabled

- **DC1: Carrier Detect enabled/disabled for transmission in buffer 1.** Starting transmission though carrier detection is in course.

  0: Enabled

  1: Disabled

- **DR1: Reception enabled/disabled for transmission in buffer 1.** Starting transmission though reception is in course.

  0: Enabled

  1: Disabled

Name: TXRXBUF_TXCONF_TX2

Address: 0xFD3E

Access: Read/Write

Reset: 0xA0

7	6	5	4	3	2	1	0
-	TRS2	ATR2	-	FE2	EB2	DC2	DR2

- **TRS2: TxRx established by software in buffer 2.** TxRx established by software for activated/deactivated TXRX signal before/after each transmission to work properly transistors when this feature has been selected.

  0: Disabled

  1: Enabled

- **ATR2: TxRx control mode in buffer 2.** Establishing software/hardware control of TXRX signal for transmitting.

  1**:** by hardware

  0: by software

- **FE2: Transmission forced/unforced in buffer 2.** When force transmission is required, if it is possible (Carrier Detection or Reception are in course and not disable) and suitable buffer is enabled, a transmission is immediately started.

  0: Transmission unforced

  1: Transmission forced

- **EB2: Buffer 0 enabled/disabled in buffer 2.** Enable buffer that it has been required.

  0: Disabled

  1: Enabled

- **DC2: Carrier Detect enabled/disabled for transmission in buffer 2.** Starting transmission though carrier detection is in course.

  0: Enabled

  1: Disabled

- **DR2: Reception enabled/disabled for transmission in buffer 2.** Starting transmission though reception is in course.

  0: Enabled

  1: Disabled

Name: TXRXBUF_TXCONF_TX3

Address: 0xFD3F

Access: Read/Write

Reset: 0xA0

7	6	5	4	3	2	1	0
-	TRS3	ATR3	-	FE3	EB3	DC3	DR3

- **TRS3: TxRx established by software in buffer 3.** TxRx established by software for activated/deactivated TXRX signal before/after each transmission to work properly transistors when this feature has been selected.

  0: Disabled

  1: Enabled

- **ATR3: TxRx control mode in buffer 3.** Establishing software/hardware control of TXRX signal for transmitting.

  1**:** by hardware

  0: by software

- **FE3: Transmission forced/unforced in buffer 3.** When force transmission is required, if it is possible (Carrier Detection or Reception are in course and not disable) and suitable buffer is enabled, a transmission is immediately started.

  0: Transmission unforced

  1: Transmission forced

- **EB3: Buffer 0 enabled/disabled in buffer 3.** Enable buffer that it has been required.

  0: Disabled

  1: Enabled

- **DC3: Carrier Detect enabled/disabled for transmission in buffer 3.** Starting transmission though carrier detection is in course.

  0: Enabled

  1: Disabled

- **DR3: Reception enabled/disabled for transmission in buffer 3.** Starting transmission though reception is in course.

  0: Enabled

  1: Disabled

9.3.5.6 TX Initial Address Registers

Name: TXRXBUF_INITAD_TX0
Address: 0xFD40 - 0xFD41
Access: Read/Write
Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_INITAD_TX0 (15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXRXBUF_INITAD_TX0 (7:0)							

Initial Address of Transmission Buffer 0.

Name: TXRXBUF_INITAD_TX1
Address: 0xFD42 - 0xFD43
Access: Read/Write
Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_INITAD_TX1 (15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXRXBUF_INITAD_TX1 (7:0)							

Initial Address of Transmission Buffer 1.

Name: TXRXBUF_INITAD_TX2
Address: 0xFD44 - 0xFD45
Access: Read/Write
Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_INITAD_TX2 (15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXRXBUF_INITAD_TX2 (7:0)							

Initial Address of Transmission Buffer 2.

Name: TXRXBUF_INITAD_TX3
Address: 0xFD46 - 0xFD47
Access: Read/Write
Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_INITAD_TX3 (15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXRXBUF_INITAD_TX3 (7:0)							

Initial Address of Transmission Buffer 3.

These four registers contain four pointers to the beginning of the respective Tx buffer in peripheral memory (buffer 0 to 3). This way, buffers are configurable in both size and position.

9.3.5.7 TX Result Register

Name: TXRXBUF_RESULT_TX

Address: 0xFD50 - 0xFD51

Access: Read-only

Reset: 0x1111

15	14	13	12	11	10	9	8
-	ET_TX1			-	ET_TX0		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	ET_TX3			-	ET_TX2		

This register stores the transmission status of each buffer.

Value	Name	Description
0	ET0_TX	Transmission in process
1	ET1_TX	Successful transmission
2	ET2_TX	Wrong Length
3	ET3_TX	Busy Channel
4	ET4_TX	Previous transmission in process
5	ET5_TX	Reception transmission in process
6	ET6_TX	Invalid Scheme
7	ET7_TX	Timeout

9.3.5.8 TX Interrupts Register

Name: TXRXBUF_TX_INT

Address: 0xFD52

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
-	-	-	HI_N	HI_TX3	HI_TX2	HI_TX1	HI_TX0

Interrupt register of Transmission and Noise buffers:

- **HI_N: Notice Interrupt Noise Buffer**
- **HI_TX3: Notice Interrupt Transmission Buffer 3**
- **HI_TX2: Notice Interrupt Transmission Buffer 2**
- **HI_TX1: Notice Interrupt Transmission Buffer 1**
- **HI_TX0: Notice Interrupt Transmission Buffer 0**

When there is some issue with the transmission or noise reception, the micro is warned and then micro tests what buffer is affected through this register.

9.3.5.9 Robust TX Control Register

Name: TXRXBUF_TXCONF_ROBO_CTL

Address: 0xFDF2

Access: Read/Write

Reset: 0x00

7	6	5	4	3	2	1	0
RC3		RC2		RC1		RC0	

This register sets the transmission mode of each TX buffer

- **RC0: Buffer 0 transmission mode**
- **RC1: Buffer 1 transmission mode**
- **RC2: Buffer 2 transmission mode**
- **RC3: Buffer 3 transmission mode**

Value	Name	Description
0	PRIME 1.3	Mode PRIME v1.3
1	Reserved	Reserved
2	PRIME 1.4	PRIME v1.4 transmission mode
3	PRIME 1.4 c	PRIME v1.4 transmission backwards compatible mode

9.3.6 AFE Configuration Registers

9.3.6.1 Branch Selection Register

Name: TXRXBUF_TXCONF_SELBRANCH

Address: 0xFDFB

Access: Read/Write

Reset: 0x00

7	6	5	4	3	2	1	0
BR2_TX3	BR1_TX3	BR2_TX2	BR1_TX2	BR2_TX1	BR1_TX1	BR2_TX0	BR1_TX0

- **BR1_TX0: Enable/Disable EMIT(0:5) output pins, when BUF_TX0 is used**

  1: Enabled

  0: Disabled

- **BR2_TX0: Enable/Disable EMIT(6:11) output pins, when BUF_TX0 is used**

  1: Enabled

  0: Disabled

- **BR1_TX1: Enable/Disable EMIT(0:5) output pins, when BUF_TX1 is used**

  1: Enabled

  0: Disabled

- **BR2_TX1: Enable/Disable EMIT(6:11) output pins, when BUF_TX1 is used**

  1: Enabled

  0: Disabled

- **BR1_TX2: Enable/Disable EMIT(0:5) output pins, when BUF_TX2 is used**

  1: Enabled

  0: Disabled

- **BR2_TX2: Enable/Disable EMIT(6:11) output pins, when BUF_TX2 is used**

  1: Enabled

  0: Disabled

- **BR1_TX3: Enable/Disable EMIT(0:5) output pins, when BUF_TX3 is used**

  1: Enabled

  0: Disabled

- **BR2_TX3: Enable/Disable EMIT(6:11) output pins, when BUF_TX3 is used**

  1: Enabled

  0: Disabled

9.3.6.2 TXRX Polarity Selector Register

Name: AFE_CTL

Address: 0xFE90

Access: Read/Write

Reset: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	-	-	TXRX1_POL	TXRX0_POL

- **TXRX1_POL: TXRX1 pin polarity control**

  0: TXRX1 pin output = ‘0’ in transmission and ‘1’ in reception.

  1: TXRX1 pin output = ‘1’ in transmission and ‘0’ in reception.

- **TXRX0_POL: TXRX0 pin polarity control**

  0: TXRX0 pin output = ‘0’ in transmission and ‘1’ in reception.

  1: TXRX0 pin output = ‘1’ in transmission and ‘0’ in reception.

9.3.7 Zero-crossing Registers

9.3.7.1 Zero-Cross Time Registers

Name: TXRXBUF_ZCT_RX0

Address: 0xFD93 - 0xFD96

Access: Read-only

Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_ZCT_RX0 (31:24)							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXRXBUF_ZCT_RX0 (23:16)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXRXBUF_ZCT_RX0 (15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXRXBUF_ZCT_RX0 (7:0)							

Instant in time at which the last zero-cross event took place, at the end of the last message received in BUF_RX0. It is expressed in 10 µs steps. It is set by hardware and is a read-only register. This register is used by the physical layer for being in accordance with PRIME specification.

Name: TXRXBUF_ZCT_RX1

Address: 0xFD97 - 0xFD9A

Access: Read-only

Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_ZCT_RX1 (31:24)							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXRXBUF_ZCT_RX1 (23:16)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXRXBUF_ZCT_RX1 (15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXRXBUF_ZCT_RX1 (7:0)							

Instant in time at which the last zero-cross event took place, at the end of the last message received in BUF_RX1. It is expressed in 10 µs steps. It is set by hardware and is a read-only register. This register is used by the physical layer for being in accordance with PRIME specification.

Name: TXRXBUF_ZCT_RX2

Address: 0xFD9B - 0xFD9E

Access: Read-only

Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_ZCT_RX2 (31:24)							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXRXBUF_ZCT_RX2 (23:16)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXRXBUF_ZCT_RX2 (15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXRXBUF_ZCT_RX2 (7:0)							

Instant in time at which the last zero-cross event took place, at the end of the last message received in BUF_RX2. It is expressed in 10 μs steps. It is set by hardware and is a read-only register. This register is used by the physical layer for being in accordance with PRIME specification.

Name: TXRXBUF_ZCT_RX3

Address: 0xFD9F - 0xFDA2

Access: Read-only

Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_ZCT_RX3 (31:24)							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TXRXBUF_ZCT_RX3 (23:16)							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TXRXBUF_ZCT_RX3 (15:8)							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TXRXBUF_ZCT_RX3 (7:0)							

Instant in time at which the last zero-cross event took place, at the end of the last message received in BUF_RX3. It is expressed in 10 μs steps. It is set by hardware and is a read-only register. This register is used by the physical layer for being in accordance with PRIME specification.

9.3.7.2 Zero Crossing Configuration Register

Name: ZC_CONFIG

Address: 0xFF1E

Access: Read/Write

Reset: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	MODE_REP	MODE_INV	MODE_ASC	MODE_MUX

- **MODE_REP: Repetition Mode**

  '0': No effect.

  '1': Zero Crossing Detector Input Signal period is down by half.

- **MODE_INV: Inversion Mode**

  '0': No effect.

  '1': Zero Crossing Detector Input Signal is inverted.

- **MODE_ASC: Ascent-Descent Mode**

  '0': If MODE_MUX is 1, Ascent Zero Crossing.

  '1': If MODE_MUX is 1, Descent Zero Crossing.

- **MODE_MUX: Zero Crossing Mode**

  '0': Selection of both ascent and descent zero-crossing.

  '1': Selection of ascent or descent zero-crossing.

9.3.7.3 Zero Crossing Filter Register

Name: ZC_FILTER

Address: 0xFF23

Access: Read/Write

Reset: 0xB2

7	6	5	4	3	2	1	0
ZC_FILTER_BP	ZC_FILTER_NUM [6:0]						

- **ZC_FILTER_BP: Zero Crossing Input Signal Filter Enable**

  ‘0’: Filter enabled.

  ‘1’: Filter not enabled.

- **ZC_FILTER_NUM [6:0]: Zero Crossing Input Signal Filter Parameter**

  Time (counted in number of clock cycles) that the Zero Crossing Input Signal (1-bit) must be constant to set that value as the input signal for Zero Crossing Detection. Used to refuse fast transitions in Zero Crossing Input Signal.

9.3.8 Other Registers

9.3.8.1 System Configuration Register

Name: SYS_CONFIG

Address: 0xFE2C

Access: Read/Write

Reset: 0x04

7	6	5	4	3	2	1	0
-	-	-	-	CONV_PD	-	-	PHY_RST

- **CONV_PD: Converter Power Down**

Microcontroller can activate internal converter power down mode by setting this bit. When internal converter is in power down mode, the system is unable to receive.

This bit is high-level active.

- **PHY_RST: Physical Layer Reset**

This bit resets the Physical layer. To perform a Physical layer reset cycle, microcontroller must set this bit to ‘1’ and then must clear it to ‘0’.

9.3.8.2 PHY Layer Timer Register

Name: TIMER_BEACON_REF

Address: 0xFE47 - 0xFE4A

Access: Read-only

Reset: 0x00000000

31	30	29	28	27	26	25	24
TIMER_BEACON_REF (31:24)							

23	22	21	20	19	18	17	16
TIMER_BEACON_REF (23:16)							

15	14	13	12	11	10	9	8
TIMER_BEACON_REF (15:8)							

7	6	5	4	3	2	1	0
TIMER_BEACON_REF (7:0)							

Timer for the physical layer, which consists of a free-running clock measured in 10 µs steps.

It indefinitely increases a unit each 10 microseconds, overflowing back to 0.

It is set by hardware and is a read-only register.

This register is used by the physical layer for being in accordance with PRIME specification.

9.3.8.3 PHY Layer Error Counter Register

Name: PHY_ERRORS

Address: 0xFE94

Access: Read/Write

Reset: 0x00

7	6	5	4	3	2	1	0
-	-	-	PHY_ERRORS				

The system stores in these bits the number of times that a Physical layer error has occurred. This counter can be cleared to zero. The value stored in this register is cleared every time the register is read.

10. Electrical characteristics

10.1 Absolute Maximum Ratings

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions given in the Recommended Operating Conditions section. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

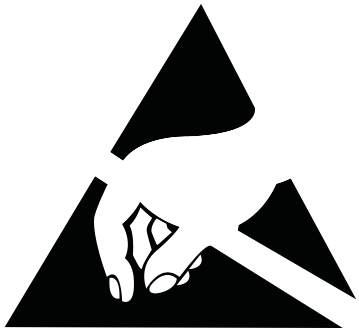
Table 10-1. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	VDDIO	-0.5 to 4.0	V
Input Voltage	VI	-0.5 to VDDIO +0.5 (≤ 4.0V)	
Output Voltage	VO	-0.5 to VDDIO +0.5 (<4.0V)	
Storage Temperature	T_{ST}	-55 to 125	ºC
Junction Temperature	T_J	-40 to 125	
Output Current[(1)]	IO	±10[(2)]	mA

Notes: 1. DC current that continuously flows for 10ms or more, or average DC current.

2. Applies to all the pins except EMIT pins. EMIT pins should be only used according to circuit configurations recommended by Atmel.

ATTENTION observe EDS precautions



Precautions for handling electrostatic sensitive devices should be taken into account to avoid malfunction. Charged devices and circuit boards can discharge without detection.

10.2 Recommended Operating Conditions

Table 10-2. Recommended Operating Conditions

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Supply Voltage	VDDIO	3.00	3.30	3.60	V
	VDDIN AN	3.00	3.30	3.60	
	VDDIN	3.00	3.30	3.60	
	VDDPLL	1.08	-	1.32	
Junction Temperature	T_J	-40	25	125	ºC
Ambient Temperature	T_A	-40	-	85	

Table 10-3. Thermal Data

Parameter	Symbol	Conditions		LQFP80	Unit
		PCB Layers	Air Speed		
Thermal resistance junction-to-ambient steady state	$R_{Theta-ja}$	2	0 m/s	64	ºC/W
			1 m/s	56	
			3 m/s	48	
		4	0 m/s	43	
			1 m/s	40	
			3 m/s	36	

Theta-ja is calculated based on a standard JEDEC defined environment and is not reliable indicator of a device's thermal performance in a non-JEDEC environment. The customer should always perform their own calculations/simulations to ensure that their system's thermal performance is sufficient.

10.3 Electrical Pinout

Table 10-4. 80 - Lead LQFP Electrical Pinout

Pin No	Pin Name	I/O	I(mA)	Res	HY	Pin No	Pin Name	I/O	I(mA)	Res	HY
1	NC	-	-	-	-	41	GND	P	-	-	-
2	NC	-	-	-	-	42	EMIT8	OT	± X	-	-
3	NC	-	-	-	-	43	EMIT9	OT	± X	-	-
4	ARST	I	-	PU	Y	44	EMIT10	OT	± X	-	-
5	PLL INIT	I	-	PU	Y	45	EMIT11	OT	± X	-	-
6	GND	P	-	-	-	46	VDDIO	P	-	-	-
7	CLKEA	I	-	-	-	47	GND	P	-	-	-
8	GND	P	-	-	-	48	VDDOUT	P	-	-	-
9	CLKEB	I/O	-	-	-	49	TXRX0	O	± 8	-	-
10	VDDIO	P	-	-	-	50	TXRX1	O	± 8	-	-
11	GND	P	-	-	-	51	GND	P	-	-	-
12	VDDPLL	P	-	-	-	52	AGC2	OT	± 8	-	-
13	GND	P	-	-	-	53	AGC5	OT	± 8	-	-
14	VDDIN	P	-	-	-	54	AGC1	OT	± 6	-	-
15	VDDIN	P	-	-	-	55	AGC4	OT	± 6	-	-
16	GND	P	-	-	-	56	AGC0	OT	± 4	-	-
17	VDDOUT	P	-	-	-	57	AGC3	OT	± 4	-	-
18	GND	P	-	-	-	58	VDDIO	P	-	-	-
19	NC	-	-	-	-	59	GND	P	-	-	-
20	SRST	I	-	PU	Y	60	EINT	O	± 4	-	-
21	VDDIO	P	-	-	-	61	GND	P	-	-	-
22	NC	-	-	-	-	62	AGND	P	-	-	-
23	CLKOUT	O	± 8	-	-	63	VDDOUT AN	P	-	-	-
24	CS	I	-	PU	Y	64	VIMA	I	-	-	-
25	SCK	I	-	PU	Y	65	VIPA	I	-	-	-
26	MOSI	I	-	PU	Y	66	VDDOUT AN	P	-	-	-
27	MISO	OT	± 4	-	-	67	AGND	P	-	-	-
28	VDDIO	P	-	-	-	68	VRP	O	-	-	-
29	GND	P	-	-	-	69	VRM	O	-	-	-
30	EMIT0	OT	± X	-	-	70	VRC	O	-	-	-
31	EMIT1	OT	± X	-	-	71	VDDIN AN	P	-	-	-
32	EMIT2	OT	± X	-	-	72	AGND	P	-	-	-
33	EMIT3	OT	± X	-	-	73	AGND	P	-	-	-
34	VDDIO	P	-	-	-	74	VDDIN AN	P	-	-	-
35	GND	P	-	-	-	75	GND	P	-	-	-
36	EMIT4	OT	± X	-	-	76	VDDIO	P	-	-	-
37	EMIT5	OT	± X	-	-	77	VZ CROSS	I	-	PD	Y
38	EMIT6	OT	± X	-	-	78	NC	-	-	-	-
39	EMIT7	OT	± X	-	-	79	NC	-	-	-	-
40	VDDIO	P	-	-	-	80	NC	-	-	-	-

I/O = pin direction:	I = input, O = output, T = tri-state, P = power
I(mA) = nominal current:	+ = source, - = sink, X = fixed by external resistor. See "V-I curves"
Res = pin pull up/pull down resistor:	PU = pull up, PD = pull down (15 - 70 kΩ, typical 33 kΩ)
HY = Input Hysteresis:	Y = yes

10.4 DC Characteristics

Table 10-5. ATPL230A DC Characteristics

Parameter	Condition	Symbol	Rating			Unit
			Min	Typ	Max	
Supply Voltage		VDDIO	3.00	3.30	3.60	V
H-level Input Voltage (3.3V CMOS)		VIH	2.0	-	VDDIO +0.3	
L-level Input Voltage (3.3V CMOS)		VIL	-0.3	-	0.8	
H-level Output Voltage	3.3V I/O IOH= -100 µA	VOH	VDDIO -0.2	-	VDDIO	
L-level Output Voltage	3.3V I/O IOL= 100 µA	VOL	0	-	0.2	
H-level Output V - I Characteristics	3.3V I/O VDDIO=3.3±0.3	IOH	See "V-I curves" section			mA
L-level Output V - I Characteristics	3.3V I/O VDDIO=3.3±0.3	IOL	See "V-I curves" section			
Internal Pull-up Resistor[1]	3.3V I/O	Rpu	15	33	70	kΩ
Internal Pull-down Resistor[1]	3.3V I/O	Rpd	15	33	70	

Note: 1. Only applicable to pins with internal pulling.

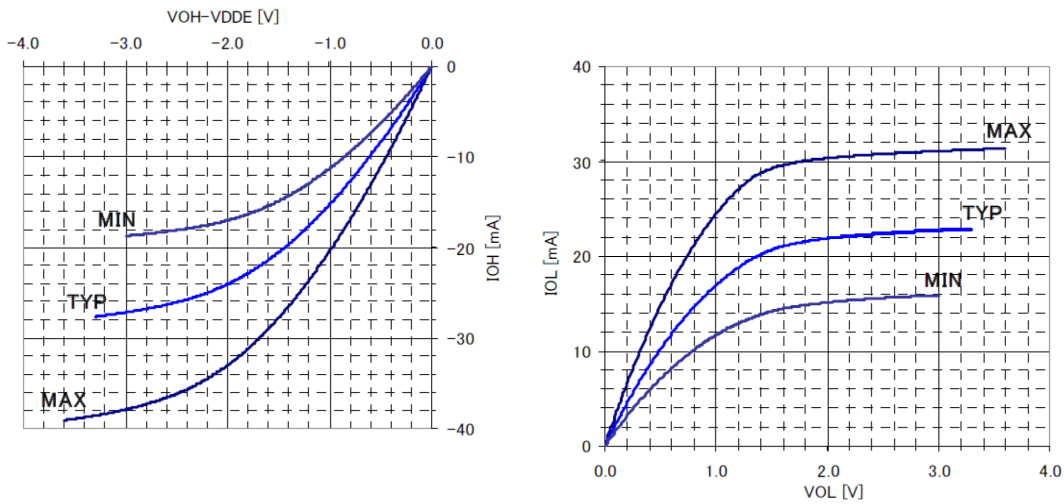
10.4.1 V-I curves

V-I Characteristics 3.3V standard CMOS IO L, M type

Apply to pins MISO, EINT, AGC0, AGC3

Condition:	MIN	Process = Slow	T_J = 125°C	VDDIO = 3.0V
	TYP	Process = Typical	T_J = 25°C	VDDIO = 3.3V
	MAX	Process = Fast	T_J = -40°C	VDDIO = 3.6V

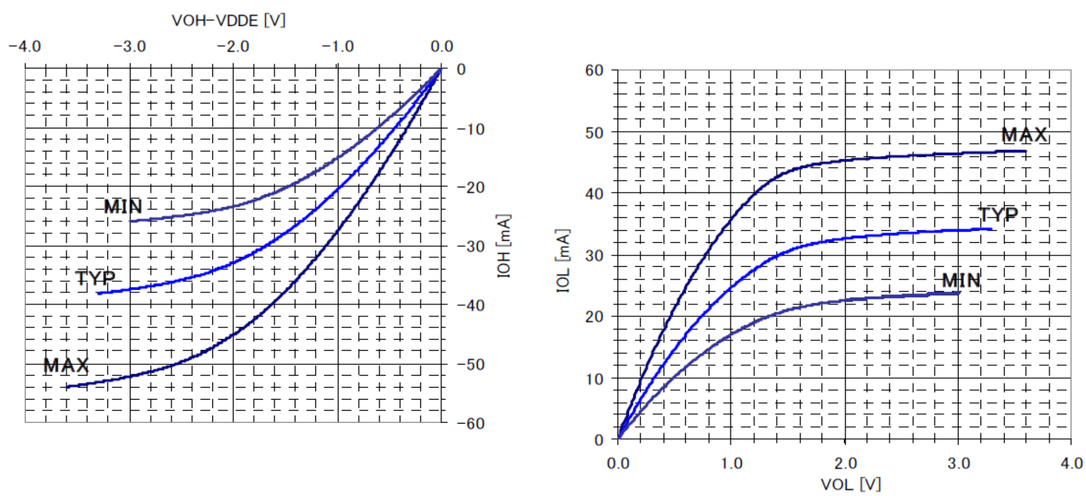
Figure 10-1. V-I curves for pins MISO, EINT, AGC0, AGC3



Apply to pins AGC1, AGC4

Condition:	MIN	Process = Slow	T_J = 125°C	VDDIO = 3.0V
	TYP	Process = Typical	T_J = 25°C	VDDIO = 3.3V
	MAX	Process = Fast	T_J = -40°C	VDDIO = 3.6V

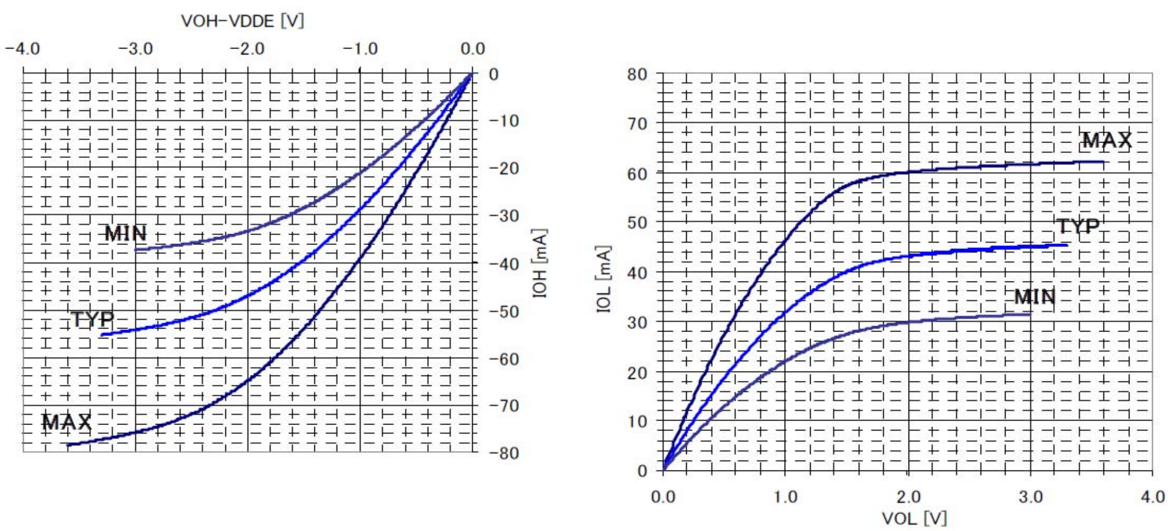
Figure 10-2. V-I curves for pins AGC1, AGC4



Apply to pins CLKOUT, TXRX0, TXRX1, AGC2, AGC5

Condition:	MIN	Process = Slow	T_J = 125°C	VDDIO = 3.0V
	TYP	Process = Typical	T_J = 25°C	VDDIO = 3.3V
	MAX	Process = Fast	T_J = -40°C	VDDIO = 3.6V

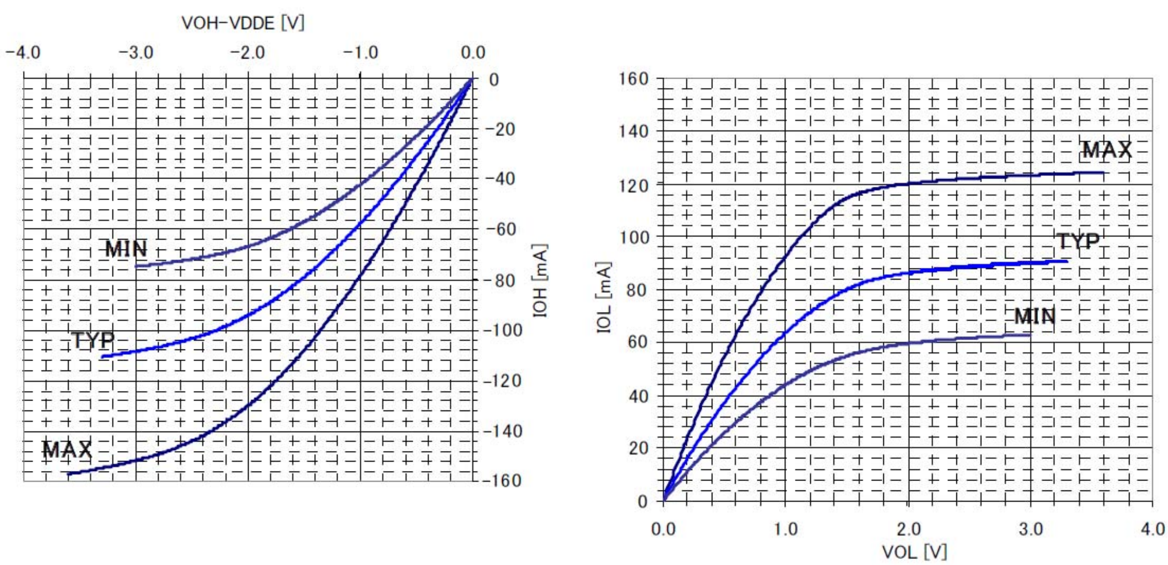
Figure 10-3. V-I curves for pins CLKOUT, TXRX0, TXRX1, AGC2, AGC5



Apply to pins EMIT [0:11]

Condition:	MIN	Process = Slow	T_J = 125°C	VDDIO = 3.0V
	TYP	Process = Typical	T_J = 25°C	VDDIO = 3.3V
	MAX	Process = Fast	T_J = -40°C	VDDIO = 3.6V

Figure 10-4. V-I curves for pins EMIT [0:11]



10.5 Power Consumption

Table 10-6. Power Consumption

Parameter	Condition	Symbol	Rating			Unit
			Min	Typ	Max	
Power Consumption	T_J = 25ºC VDDIO = 3.3V VDDIN = 3.3V VDDIN AN = 3.3V	P_{25}	- -	160	- -	mW
Power Consumption (worst case)	T_J = 125ºC VDDIO = 3.6V VDDIN = 3.6V VDDIN AN = 3.6V	P_{125}	- -	- -	270	

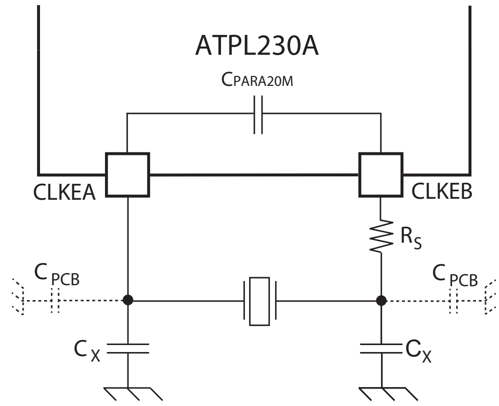
10.6 Oscillator

Table 10-7. ATPL230A 20 MHz Crystal Oscillator Characteristics

Parameter	Test Condition	Symbol	Rating			Unit
			Min	Typ	Max	
Crystal Oscillator frequency	Fundamental	X_{tal}	20			MHz
External Oscillator Capacitance(2)(3)		C_{XTAL}	-	18	-	pF
External capacitor on CLKEA and CLKEB(2)(3)		C_X	-	27	-	
Internal parasitic capacitance	Between CLKEA and CLKEB	$C_{PARA20M}$	-	4	-	
H-level Input Voltage		XVIH	2	-	VDDIO +0.3	V
L-level Input Voltage		XVIL	-0.3	-	0.8	
External Oscillator Parallel Resistance		Rp	not needed			Ω
External Oscillator Series Resistance		Rs	-	220	-	

Notes:
1. The crystal should be located as close as possible to CLKEB and CLKEA pins.
2. Recommended value for C_X is 27 pF and Rs 220 Ω. These values may depend on the specific crystal characteristics and PCB layout. See example below. For further information please refer to Atmel doc43084 "Crystal Selection Guidelines" application note.
3. As a requirement of PRIME specification, the System Clock tolerance from which transmit frequency and symbol timing are derived shall be ± 50 ppm maximum. Crystal Stability/Tolerance/Ageing values must be selected according to standard PRIME requirements.

Figure 10-5. 20 MHz Crystal Oscillator Schematic



$$C_X = 2 \times (C_{XTAL} - C_{PARA20M} - C_{PCB} / 2)$$

where C_{PCB} is the ground referenced parasitic capacitance of the printed circuit board (PCB) on CLKEA and CLKEB tracks.

As a practical example, taking the following crystal part number:

Manufacturer: TXC CORPORATION

Part Number: 9C-20.000MAAJ-T

Frequency: 20.000 MHz

Tolerance: 30 ppm (as low as possible to fullfil PRIME specification requirements)

C_{XTAL} = 18 pF

Working in a typical layout / substrate with C_{PCB} = 1 pF

The value of the external capacitors on CLKEA and CLKEB should be C_X = 2 x (18 - 4 - 0.5) = 27 pF

It is strongly recommended to use capacitors with the lowest temperature stability possible. In this practical example, a suitable part number could be:

Manufacturer: MURATA

Part Number: GRM1885C1H270FA01D

Capacitance: 27 pF

Tolerance: 1 %

Dielectric: C0G / NP0 (0 drift)

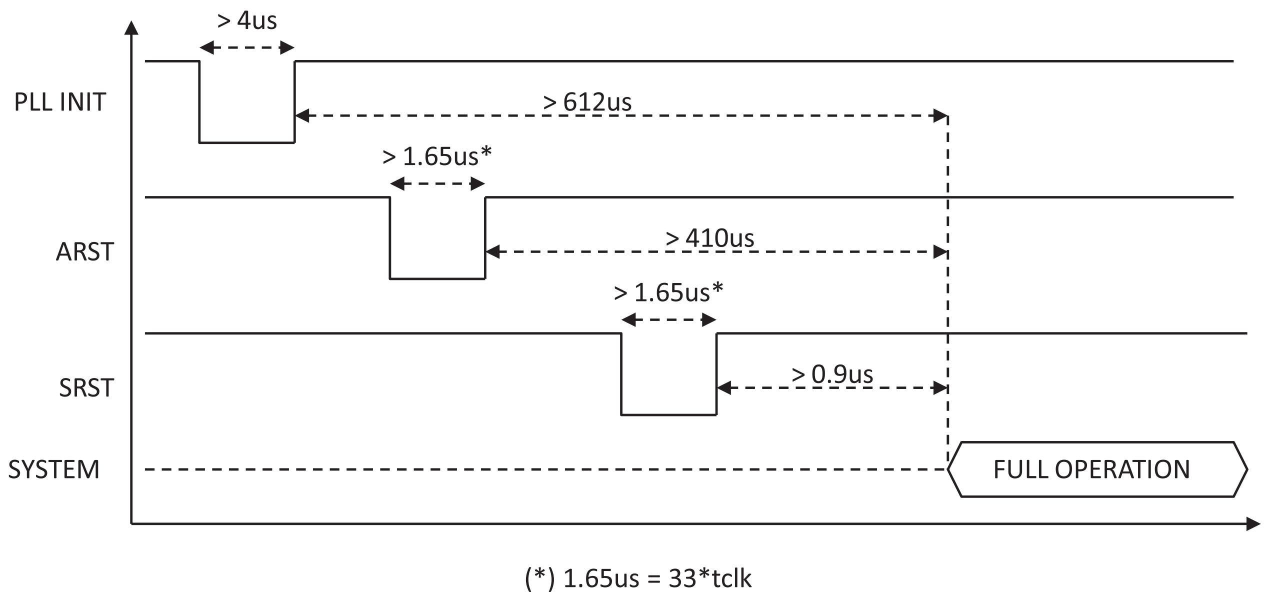
10.7 Power On Considerations

During power-on, PLL INIT pin should be tied to ground during 4 µs at least, in order to ensure proper system start up. After releasing PLL INIT, the system will start no later than 612 µs.

After power-up system can be restarted by means of low active pulse (min 1.65 µs) in ARST or SRST. System full operation starts after 410 µs (ARST pulse) or after 0.9 µs (SRST pulse).

In case of simultaneous tie down of more than one initialization pin the longest time for operation must be respected.

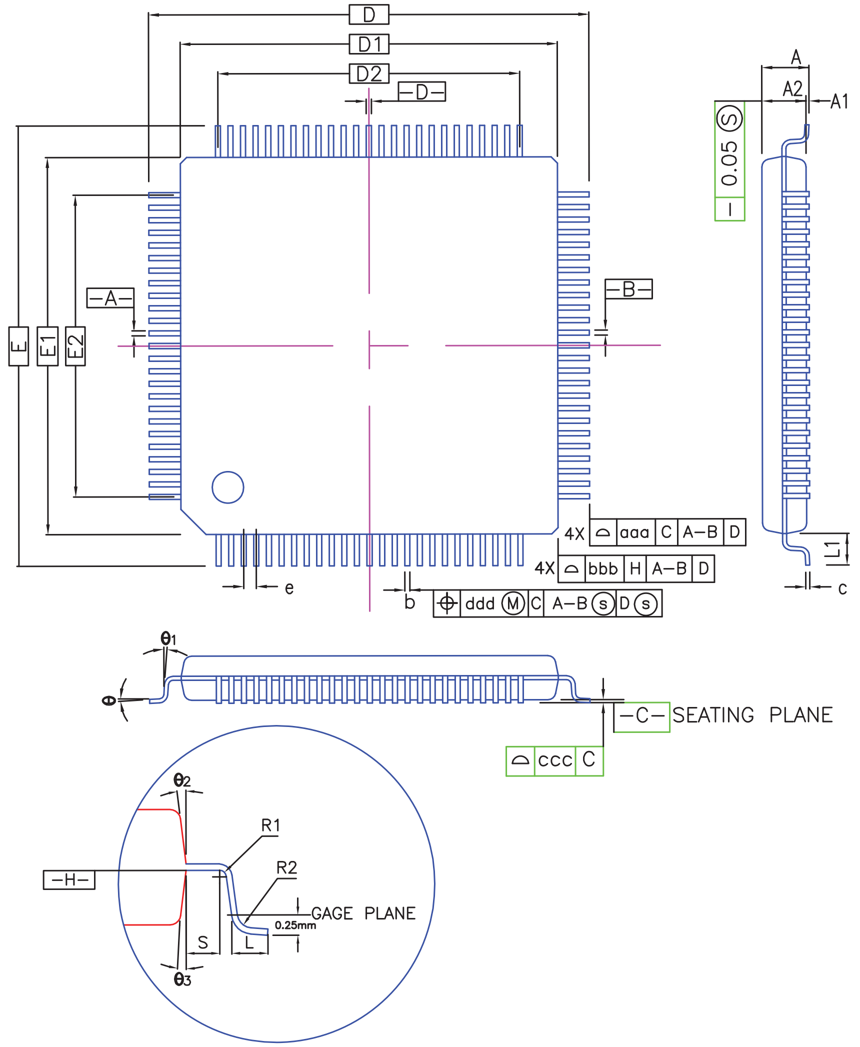
Figure 10-6. PLL INIT initialization diagram



11. Mechanical Characteristics

11.1 LQFP80 Mechanical Characteristics

Figure 11-1. 80 LQFP package dimensions



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	14.00 BSC.			0.551 BSC.		
D1	12.00 BSC.			0.472 BSC.		
E	14.00 BSC.			0.551 BSC.		
E1	12.00 BSC.			0.472 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	80L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	9.50			0.374		
E2	9.50			0.374		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Table 11-1. LQFP Package Reference

JEDEC Drawing Reference	MS-026

Table 11-2. LQFP Package Characteristics

Moisture Sensitivity Level	3

This package respects the recommendations of the NEMI User Group.

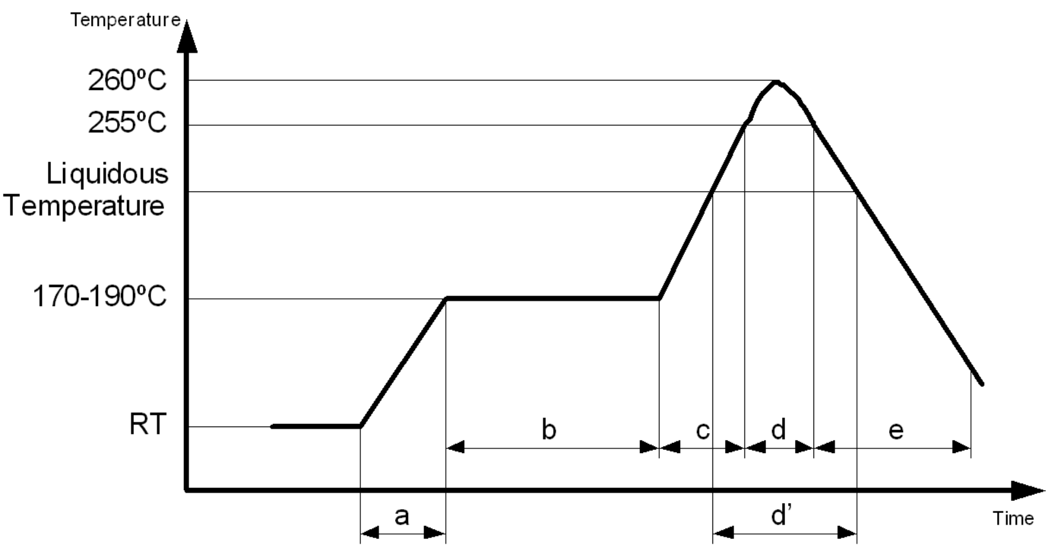
12. Recommended mounting conditions

12.1 Conditions of Standard Reflow

Table 12-1. Conditions of Standard Reflow

Items	Contents	
Method	IR (Infrared Reflow) / Convection	
Times	2	
Floor Life	Before unpacking	Please use within 2 years after production
	From unpacking to second reflow	Within 8 days
	In case over period of floor life	Baking with 125ºC +/- 3ºC for 24hrs +2hrs/-0hrs is required. Then please use within 8 days (please remember baking is up to 2 times).
Floor Life Condition	Between 5ºC and 30ºC and also below 70% RH required. (It is preferred lower humidity in the required temp. range).	

Figure 12-1. LQFP80 package soldering profile



Note: H rank: 260ºC Max

a: Average ramp-up rate: 1ºC/s to 4ºC/s

b: Preheat & Soak: 170ºC to 190ºC, 60s to 180s

c: Average ramp-up rate: 1ºC/s to 4ºC/s

d: Peak temperature: 260ºC Max, up to 255ºC within 10s

d': Liquidous temperature: Up to 230ºC within 40s or
Up to 225ºC within 60s or
Up to 220ºC within 80s

e: Cooling: Natural cooling or forced cooling

12.2 Manual Soldering

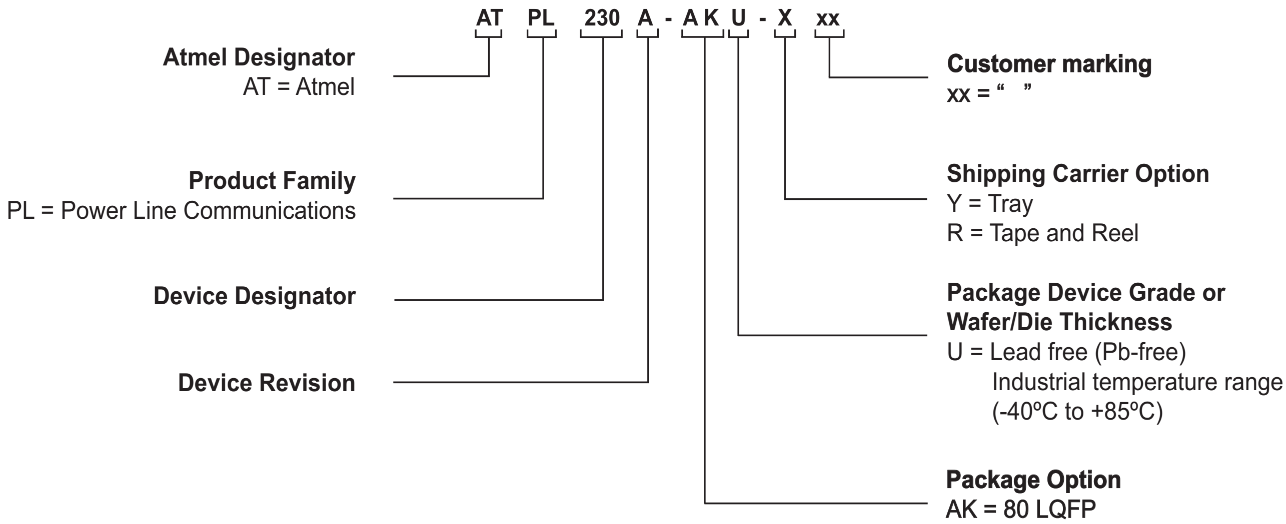
Table 12-2. Manual Soldering

Items	Contents	
Floor life	Before unpacking	Please use within 2 years after production
	From unpacking to Manual Soldering	Within 2 years after production (No control required for moisture adsorption because it is partial heating)
Floor life condition	Between 5°C and 30°C and also below 70% RH required. (It is preferred lower humidity in the required temp. range).	
Solder Condition	Temperature of soldering iron: Max 400°C, Time: Within 5 seconds/pin *Be careful for touching package body with iron	

13. Ordering Information

Table 13-1. Ordering Information

Atmel Ordering Code	Package	Package Type	Temperature Range
ATPL230A-AKU-Y	80 LQFP	Pb-Free	Industrial (-40ºC to 85ºC)
ATPL230A-AKU-R	80 LQFP	Pb-Free	Industrial (-40ºC to 85ºC)



14. Revision History

In the table that follows, the most recent version of the document appears first.

Doc Rev. 43053	Comments	Change Request Ref.
J	**Analog Front-End** Figure 5-3 and Figure 5-5: updated.	
I	**Analog Front-End** Section 5.3 ”Zero-crossing detection”: updated. **Peripheral Registers** Added the following registers: “Zero Crossing Configuration” and “Zero Crossing Filter” **PRIME PHY Layer** Added Section 9.3.7.2 ”Zero Crossing Configuration Register” and Section 9.3.7.3 ”Zero Crossing Filter Register”.	
H	**Analog Front-End** Section 5.2 ”ATPLCOUP reference designs” modified.	
G	Format changes according to new templates.	
F	Chapters order redefined. Deleted Section “Power Considerations”: the information of this section is in Section 3. ”Signal Description”. Modified Section 5. ”Analog Front-End” (was “PLC coupling circuitry description”). Changed “PRIME + Robust” by “PRIME v1.4”. **Electrical Characteristics** Section 10.6 ”Oscillator” updated: modified Figure 10-5, added equation and information after the figure. Table 10-7 updated: added the values of C_{XTAL} and $C_{PARA20M}$. Modified the notes below the table. **Ordering Information** Table 13-1: added new Atmel Ordering Code “ATPL230A-AKU-R”.	
E	**MAC Coprocessor** Removed the following registers: “0xFD53, 0xFD54, 0xFD55, 0xFD56, 0xFD5F, 0xFD60, 0xFD61 and 0xFD62”. Updated Section 8.3.3.3 ”BER HARD Average Error Registers”. **Mechanical Characteristics** Table 11-1,Table 11-2 added.	

Doc Rev. 43053	Comments	Change Request Ref.
D	Minor changes. **Signal Description** CLKOUT: “20 MHz CLK Output” changed to “10 MHz External Clock Output”. **SPI Controller** Chapter added. **MAC Coprocessor** “Address: 0xFE62 - 0xFE67” changed to “Address: 0xFEBA (MSB) - 0xFEBB (LSB)” in Section 8.3.1.2 ”CRC32 Errors Counter Register”. **PRIME PHY Layer** “Reset: 0x000000” changed to “Reset: 0x00000000” in Section 9.3.3.9 ”Accumulated Header EVM Registers”. “Reset: 0x000000” changed to “Reset: 0x00000000” in Section 9.3.3.10 ”Accumulated Payload EVM Registers”. “Reset: 0x00000000” changed to “Reset: 0x000124F8” in Section 9.3.5.4 ”TX Timeout Registers”. “Reset: 0x0000” changed to “Reset: 0x1111” in Section 9.3.5.7 ”TX Result Register”.	
C	“GND” changed to “AGND” in the following pins: 62, 67, 72 and 73. Changed the description of “VDDIN AN” in Section 3. ”Signal Description”.	
B	Update Package.	
A	First Issue.	

Table of Contents

Enabling Unlimited Possibilities®

Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**