System Requirements for Software:

The HSP50216 / ISL5216 evaluation board requires an IBM PC compatible computer with an available parallel interface (printer) port or Universal Serial Bus (USB) port. A 120 MHz Pentium or faster CPU and 800x600 or higher screen resolution is recommended. The supported operating systems and interface types are shown below. The USB interface (USBINTERFACE-DBEVAL1) is a daughterboard which connects to the HSP50216 / ISL5216 evaluation board. Up to 8 evaluation boards may be connected to a computer's USB interface using these daughterboards. Only one evaluation board may be connected to a parallel port.

Operating System	Parallel Port	USB Port
MS Windows 95	X	
MS WIndows 98	X	X
MS Windows NT 4	X	
MS Windows 2000	X	X

Software Installation:

Windows 95 / Windows 98 using parallel port:

1. Run the self-extracting zip exe file 216SETUP.EXE
2. Provide a path for the program and data files. A directory called HSP50216 will be created under the path provided. The default path is C:\.
3. Click "Unzip".
4. Start the evaluation board software by double-clicking or running HSP50216.EXE.

Windows NT 4 / Windows 2000 using parallel port:

1. Log into the computer using an account with administrator access.
2. Run the self-extracting zip exe file 216SETUP.EXE
3. Provide a path for the program and data files. A directory called HSP50216 will be created under the path provided. The default path is C:\.
4. Click "Unzip".
5. Run port95nt.exe (Scientific Software Tools, Inc.'s DriverLINX installer program) and follow the on-screen instructions. This installs drivers used by the evaluation board software to access I/O ports. Information on this driver is available on SST's website at http://www.sstnet.com.
6. Start the evaluation board software by double-clicking or running HSP50216.EXE.

Windows 98 using USB port:

1. Run the self-extracting zip exe file 216SETUP.EXE
2. Provide a path for the program and data files. A directory called HSP50216 will be created under the path provided. The default path is C:\.
3. Click "Unzip".
4. Set the 3 binary address switches on the USB daughterboard to a unique address (0 - 7).
5. Connect the USB daughterboard to the computer's USB port.
6. When the "Add New Hardware Wizard" box appears, click "Next".
7. Verify that "Search for the best driver for your device. (Recommended)" is checked and click "Next".
8. Click "Specify a location" and enter the path to the HSP50216 directory created above (default of "C:\HSP50216"), click "Next".
9. Verify driver file search finds "Intersil HSP50216 / ISL5216 Eval Board (no firmware)", click Next.
10. Click "Finish".
11. Start the evaluation board software by double-clicking or running HSP50216.EXE.

Windows 2000 using USB port:

1. Log into the computer using an account with administrator access.
2. Run the self-extracting zip exe file 216SETUP.EXE
3. Provide a path for the program and data files. A directory called HSP50216 will be created under the path provided. The default path is C:\.
4. Click "Unzip".
5. Set the 3 binary address switches on the USB daughterboard to a unique address (0 - 7).
6. Connect the USB daughterboard to the computer's USB port.
7. When "Found New Hardware Wizard" appears, click "Next"

8. Verify that "Search for a suitable driver for my device (recommended)" is checked and click "Next".

9. Click "Specify a location" and click "Next".

10. Enter the path to the HSP50216 directory created above (default of "C:\HSP50216") and click "Next".

11. Click "Finish" and reboot the computer if asked.

12. Start the evaluation board software by double-clicking or running HSP50216.EXE.

Windows NT 4 and Windows 2000 installations (parallel or USB) require an administrator account to install the necessary drivers. Once installed, user accounts will be able to access the hardware.

Evaluation Board Hardware Configuration:

For parallel port connections, the port should be configured for ECP-mode. This option is often available in the computer's BIOS settings.

Jumper Settings: JP7

Evaluation board JP7 pins 7 and 9 should be shorted to connect the HSP50216/ISL5216's SYNCO to SYNCI (on ST-116 boards, this is J10 pins 7 and 9). JP1 should be set for the desired clock source: pins 1 and 2 if the clock is provided on J4 (parallel input bus C) or J2 (LVDS bus A), or pins 2 and 3 if the clock source is the on-board 32 MHz oscillator.

Power:

The board uses 5V DC power at up to approximately 1A. On the cable provided for connecting to a power supply, the wire with the white stripe is the +5 volt lead (center conductor is positive). There are 3.3V and 2.5V regulators on the board to supply the HSP50216 (3.3V) / ISL5216 (3.3V and 2.5V) and other 3.3V devices. Note that the ST-116 boards use an HSP50216 and have only the 3.3V regulator.

Inputs:

The I/O busses have receivers/drivers with 5V tolerant I/Os, however, pins connected directly to the HSP50216/ISL5216 ARE NOT 5V tolerant.

Inputs J4 (parallel input bus C) and J5 (parallel input bus D) are compatible with the pinout of the HSP50215EVAL. The JP4 (LVDS bus A) and JP5 (LVDS bus B) inputs are high speed serial inputs using National Semiconductor's "ChannelLink" serial LVDS parts. On the ST-116, these are referred to as J2 and J3 respectively.

Due to the difficulty in aligning the clocks for the two types of inputs, it is expected that one or the other input type will be used at a time but not both.

The clock for parallel port inputs J4 and J5 comes in on the J4 connector. The clock for LVDS inputs JP4 and JP5 comes in on the JP4 connector (J2 for the ST-116 board). The input clock is distributed using a PLL-based zero delay buffer. This part (and therefore the board) has a minimum input clock rate of 20 MHz.

DAC outputs

A dual 12-bit D/A (Intersil HI5828) is provided for observing the output signals on an oscilloscope or spectrum analyzer. It outputs to phono-plug J7 and 3-pin header J8. The initial build of the ST-116 boards has a series capacitor in the D/A output path that limits the low frequency response to J7 and J8. This has been replaced in later ST-116 boards with a zero ohm resistor. The ISL5216EVAL1 board has J7 capacitively coupled and J8 DC coupled.

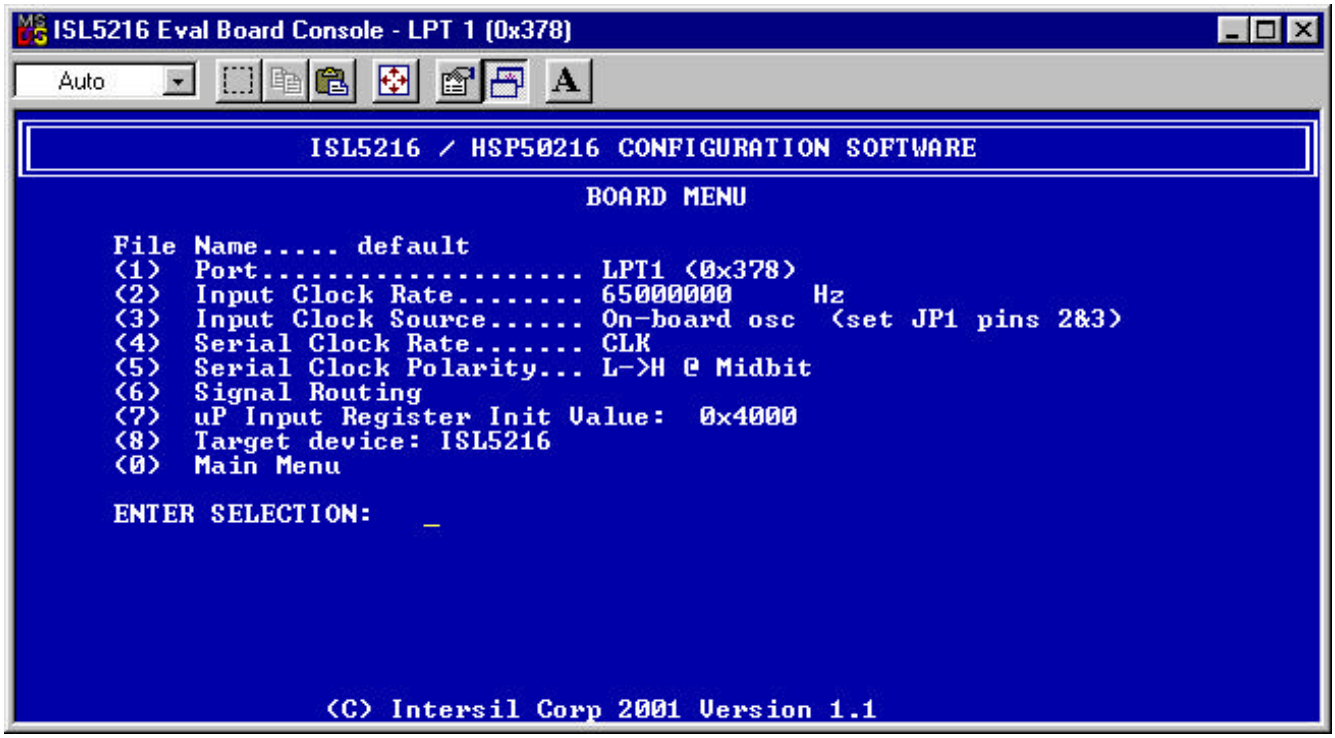
Note that when using the resampler or interpolation halfband filters, the spacing between samples can be uneven and will time-distort the DAC signals. The FIFO delay in the 216 may need to be adjusted for optimum analog performance, but normally a setting of "AUTO" in the software will provide the correct FIFO delay. The FIFO was intended mainly to spread output samples from the interpolation halfband filters. It can partially de-jitter the resampler or resampler plus one interpolation halfband filter combination, but the FIFO is not deep enough to de-jitter a resampler/2-IHBF combination.

A note on rates:

For testing with non-real-time signals, the clock rate and sample rate in the menus do not have to match the input clock for the board. For example, the clocks in the menus can be set to 65 MHz while the clock for the board is actually 32 MHz (the on-board oscillator frequency). The frequencies in the displays and calculated register values will reflect the menu clock rates.

Tutorial and Overview:

Select main menu item 1 for the board menu to set the port, clock settings and target device (HSP50216 or ISL5216).



Port and Input Clock Source options apply only to the evaluation board. These settings may be ignored if an evaluation board will not be connected. The software can be used to generate register files even without an evaluation board. In this case, use main menu option 10 (“compute register value files”) followed by option 14 ("generate batch file") to create a file containing all the register data needed for the configuration. The data in this file may be imported into the user's own loader software.

Port: this setting is used to specify how the evaluation board is connected to the computer. Enter 1, 2, or 3 for LPT1, LPT2, or LPT3, respectively, or the base address in hex for a non-standard parallel port (for example, enter "0x290" for a parallel port at 290H). For a USB interface, enter -0 to -7 for USB board addresses of 0 through 7.

Input Clock Rate: clock rate of the HSP50216 in Hz. As stated above in "A note on rates", this frequency does not need to be the actual clock rate on the eval board. It is used in register calculations, to report configuration warnings, and to report frequencies in run and display mode. Enter the rate of the clock that will be used in the final application.

Input clock source: selects between on-board oscillator (32 MHz), JP4 / J2 (LVDS) clock input or J4 (parallel bus) clock input as the HSP50216/ISL5216 clock source. Note that a change to JP1 may also be required when changing this.

Serial Clock Rate and Serial Clock Polarity affect the SCLK (serial output clock) timing. These should be set for CLK and L->H @ Midbit (default settings) when targeting the evaluation board for testing, but may be set as needed when generating register files for a final design.

Target Device puts the software into either an HSP50216 or ISL5216 mode. This setting affects certain menu choices (those related to ISL5216-specific features) and the generation of register files. Default setting is ISL5216 - this must be changed when targeting an HSP50216.

Other options in this menu are described in the Signal Routing and Common Chip Setup (Board Menu) section.

Note that the title bar of the console window (“ISL5216 Eval Board Console - LPT1 (0x378)” in this example) shows the currently selected target device and port.

Select 0 from the board menu to return to the main menu.

If an evaluation board is connected, select option 17 from the main menu to initialize it. Board initialization consists of programming the FPGA and configuring the clock buffers according to the settings made in the board menu. After successful board initialization, the HSP50216 is ready for register loading. Note that "Port" and "Input Clock Source" from the Board Menu (above) must be correctly set before the board can be initialized.

At this point, main menu options 2 through 6 would be used to enter configuration data such as input and output formats, filter types and decimations, coefficient file locations, etc. These menus are described in detail below. The no-file-loaded defaults will generate a configuration that produces an output. These defaults are a good starting point for most configurations.

To calculate the register values from the current configuration data, select option 10 from the main menu. A set of files is produced with file extensions of ".r0", ".r1", ".r2", ".r3" and ".rtp" for channels 0, 1, 2, 3 and the global registers, respectively. These files contain the actual values to be loaded into the device for the given configuration (refer to the HSP50216 or ISL5216 datasheet for the recommended configuration procedure). They are human-readable text files with each line containing a 16 bit integer register number and a 32 bit integer value, both in hex. Additionally, an ".sta" report file is created to summarize FIR engine clock and memory usage - information which is useful in determining whether longer filters can be implemented. During register value computation, error messages will appear if certain device limitations are exceeded. After returning to the main menu, the ".sta" file can be opened with any text viewer (such as Notepad) to determine how to correct the problem. The initial file prefix for the six files described above is "default". This is changed when the configuration data are saved (main menu option 9) or loaded (main menu option 8).

After computing register files, option 14 from the main menu may be used to generate a single file containing all the information necessary to program the HSP50216 / ISL5216 in the order stated in the datasheet's recommended configuration procedure.

Once the register values are calculated, select main menu item 12 to configure the part. The ".r0", ".r1", ".r2", ".r3" and ".rtp" files created above are downloaded to the HSP50216 / ISL5216 and a SYNCO is generated. Normally JP7 (J10 on the ST-116) pins 7 and 9 are shorted so that SYNCO is connected directly to SYNCI, enabling inputs and synchronizing blocks programmed to respond to SYNCI.

Main menu item 13 ("Run and Display") provides the graphics window shown below to collect and display the output samples. While running, the evaluation board hardware captures 256 sample snapshots which are then transferred to the computer for FFT computation and display. The text at the bottom of the window lists the key functions available -

"1": toggles peak on / off

"2": toggles average on / off

"3": toggles current (real-time) FFT on / off

"4": resets peak trace

"5": resets average trace

"6": toggles between the two AGC loop gains

"A"-"D": selects the serial output to monitor (if other than D, it must be sync'd to D) . N/A in polyphase mode.

The left and right arrow keys step the carrier center frequency. The up and down arrow keys increase or decrease the step size (amount carrier frequency changes when left/right arrow keys are pressed). The step size range is 2^N FFT bins with N = 0 to 8.

Details of all the menus and their parameters are now presented. In general, the minimal procedure for configuring the evaluation board is as follows:

1.Set Port, Input Clock Source settings and Target Device in Signal Routing and Common Chip Setup (Board Menu)

2.Enter configuration parameters using main menu items 1 - 6. For single channel configurations on the evaluation board, use channel 3 and outputs SD1D/SD2D.

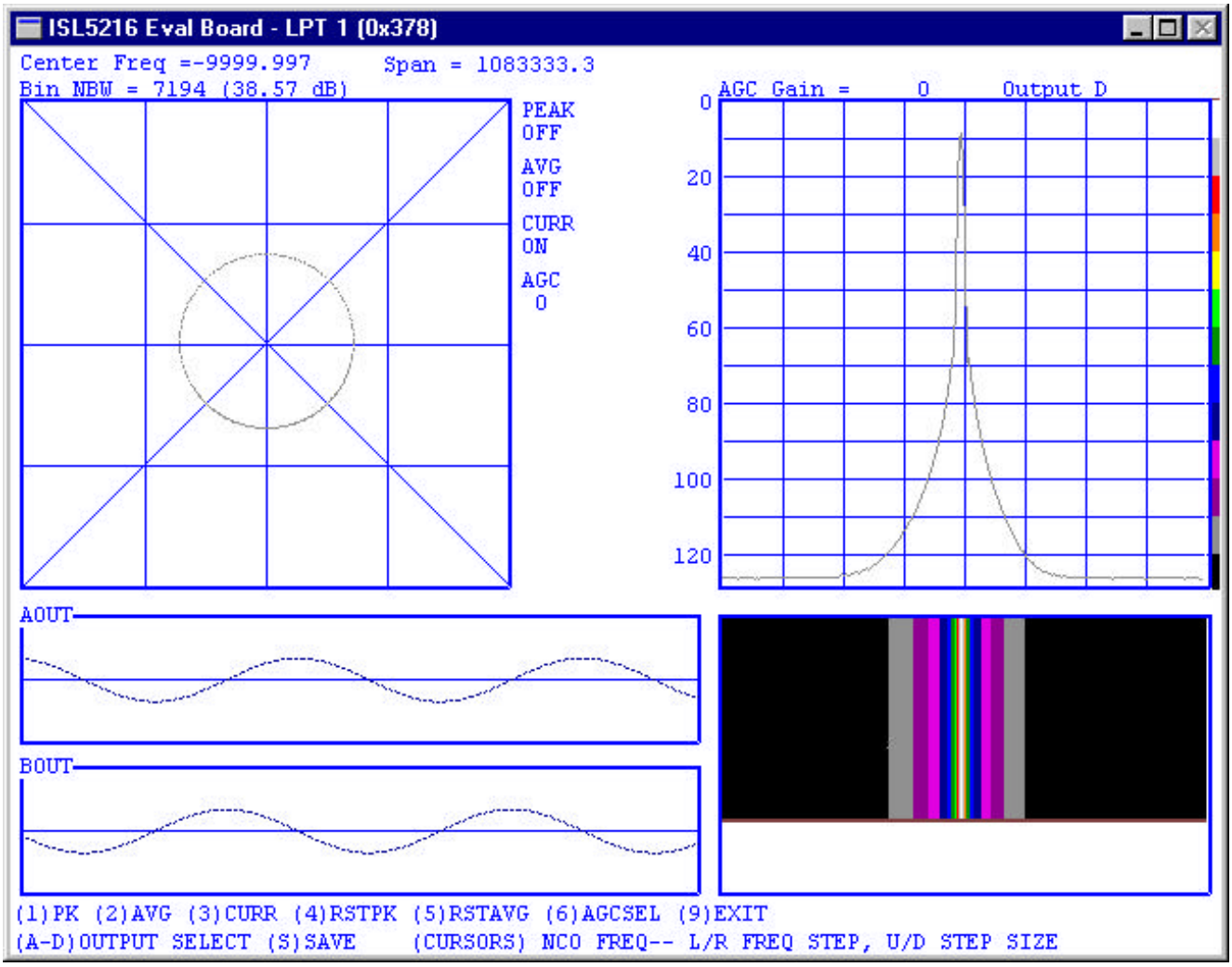
3.Initialize the board (main menu option # 17).

4.Compute register files (main menu option # 10).

5.Download the register files to the evaluation board's HSP50216 / ISL5216 (main menu option # 12).

6.Select Run and Display (main menu option # 13) to view the 216's output.

Remember to select main menu options 10 and 12 (in that order) following any change to a parameter. These steps are needed to recompute the registers and load the new data into the device.



Main menu functions:

Signal Routing and Common Chip Setup

This menu allows the following parameters to be set: evaluation board port, input clock rate and source, serial output clock rate and polarity, channel-to-channel signal routing (for channel cascading and polyphasing), microprocessor test (input) register value, and target device. See details in the "Signal Routing and Common Chip Setup" section.

Input Level Detector

This menu provides settings related to the input level detector. See details in "Input Level Detector" section.

Channel n Menu

These menus are used to configure channel data paths (NCO frequency, CIC and FIR options), AGCs, serial output options, and SYNC input responses. See details in "Data Path Menu", "AGC Menu", "Serial Output Menu" and "Sync Menu" sections.

Copy Channel Configuration

This command is useful for duplicating a channel's configuration. Channel 0 could be configured, for example, and then copied to channels 1, 2, and 3. Note that in copying a channel all parameters associated with that channel are copied, including items as input sources and serial outputs. After copying a channel be sure to update the copy, changing input and output parameters as needed.

Load Configuration File

Enter the full path or path relative to the program directory of the root name of the desired configuration. A configuration consists of .0, .1, .2, .3 and .TOP files in addition to the .IMP impulse response files and possibly one or more imported filter files. These files contain all the necessary information to communicate with the evaluation board and to generate the 216's register files. The .0, .1, .2, .3 and .TOP files are all preceded by the same root name. For example, enter "rx1" to open the rx1.0, rx1.1, rx1.2, rx1.3 and rx1.top files in the program directory or "c:\mydesigns\rx1" if they are under the "c:\mydesigns" directory.

Save Configuration File

As above but for saving the configuration.

Compute Register Value Files

This command generates the actual register data needed to configure the HSP50216 / ISL5216.

It produces a set of files with extensions of ".r0", ".r1", ".r2", ".r3" and ".rtp" for channels 0, 1, 2, 3 and the global registers, respectively. These files contain the actual values to be loaded into the device for the given configuration (refer to the HSP50216 or ISL5216 datasheet for the recommended configuration procedure). They are human-readable text files with each line having a 16 bit integer register number and a 32 bit integer value, both in hex. Additionally, an ".sta" report file is created to summarize FIR engine clock and memory usage - information which is useful in determining whether longer filter impulse responses can be used. During register value computation, error messages will appear if certain device limitations are exceeded. After returning to the main menu, the ".sta" file can be opened to determine how to correct the problem. The initial file prefix for the six files described above is "default". This is changed when the configuration data are saved (main menu option 9) or loaded (main menu option 8).

Data Collection & Display Settings

This menu provides capturing of output data to a file and frequency sweeps of the CIC and FIR filters. It also holds the "bits captured per sample" and "polyphase mode" parameters used in run & display and capture data modes. See "Data Collection & Display Settings" section for details.

Program Eval Board

Downloads the ".r0", ".r1", ".r2", ".r3" and ".rtp" files created by "Compute Register Value Files" above to the evaluation board and generates a SYNCO. Normally JP7 (J10 on the ST-116) pins 7 and 9 are shorted so that SYNCO is connected directly to SYNCI, enabling inputs and synchronizing blocks programmed to respond to SYNCI.

Run and Display

Provides real-time graphical display of output data in time and frequency domains as well as an I vs. Q constellation plot. See Run and Display section for details.

Generate Batch File

Generates a batch file containing the device register data. Select "Compute Register Value Files" (main menu option # 10) prior to using this option.

The batch file produced is of the following format:

wr216 <reserved> <reserved> <register address> <register value>

The register addresses and associated values are presented in the order recommended by the "mP Read/Write Procedures" section of the HSP50216 and ISL5216 datasheets.

Test Menu

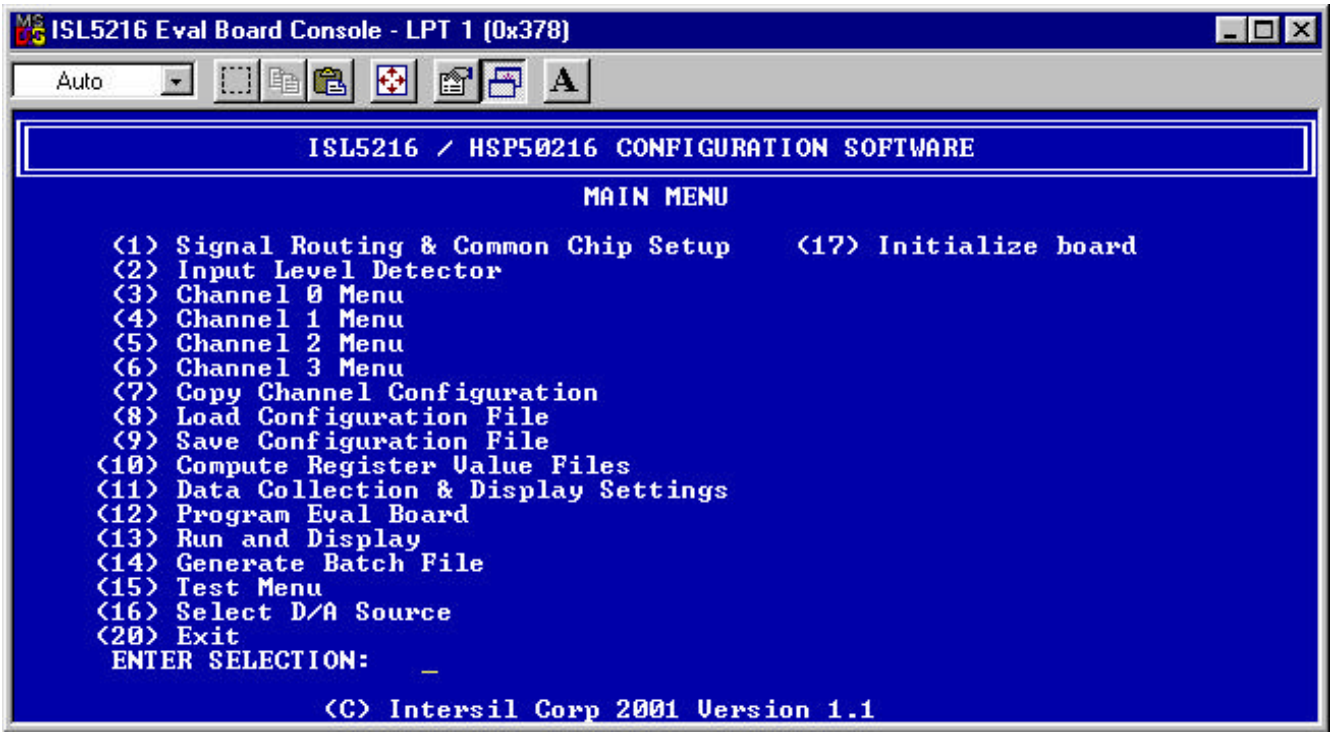
This menu provides functions for testing the evaluation board and HSP50216 / ISL5216 chip. See "Test Menu" section for details.

Select D/A Source

Sets the evaluation board's dual channel D/A source to outputs SD1A/SD2A, SD1B/SD2B, SD1C/SD2C, or SD1D/SD2D (default). The appropriate output SYNC line is also selected so that, unlike in "run and dispay" and data capture modes, the selected output need not be synchronized with output D.

Initialize Board

Downloads FPGA bitstream to the evaluation board and configures clock buffers according to the clock source setting in "Signal Routing and Common Chip Setup" menu. This step must be performed before register data can be downloaded to the chip.



Signal Routing & Common Chip Setup (Main menu option # 1):

Port

This parameter is used to specify how the evaluation board is connected to the computer. Enter 1, 2, or 3 for LPT1, LPT2, or LPT3, respectively, or the base address in hex for a non-standard parallel port (for example, enter "0x290" for a parallel port at 290H). For a USB interface, enter -0 to -7 for USB board addresses of 0 through 7. If not targeting the evaluation board, this may be ignored.

Input Clock Rate

Specifies the clock rate of the HSP50216 / ISL5216 in Hz. This frequency does not necessarily have to be the actual clock rate provided to the evaluation board (see input clock source below). It is used in register calculations, to report configuration warnings, and to report frequencies in run and display mode. Enter the rate of the clock that will be used in the final application.

Input Clock Source

Selects between on-board oscillator (32 MHz), JP4 / J2 (LVDS) clock input or J4 (parallel bus) clock input as the HSP50216/ISL5216 clock source. Note that a change to JP1 may also be required when changing this. The software

will indicate the proper position of JP1 for the desired clock source.

Serial Clock Rate

Sets bits 2:0 of register F803H to set SCLK (serial output data clock) to CLK, CLK/2, CLK/4, CLK/8, or CLK/16. This should be set for CLK when targeting the evaluation board, but may be set as needed when generating register files for a final design.

Serial Clock Polarity

Sets bit 3 of register F803H to make clock transition from low to high or high to low at the center of data bits. This should be set for L->H @ Midbit (default setting) when targeting the evaluation board, but may be set as needed when generating register files for a final design.

Signal Routing

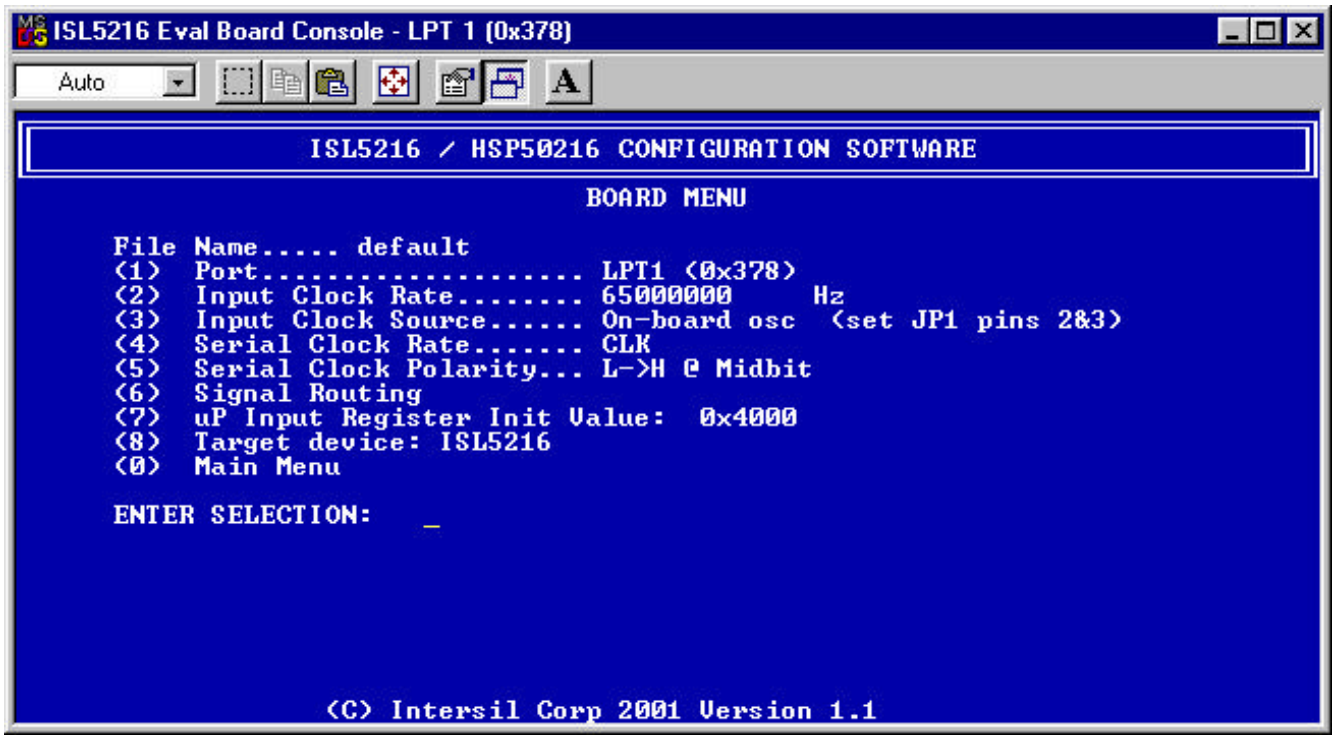
Brings up signal routing screen for channel cascading and polyphasing. See Signal Routing section.

uP Input Register Init Value

Loads a value into the microprocessor test input register (F807H).

Target Device

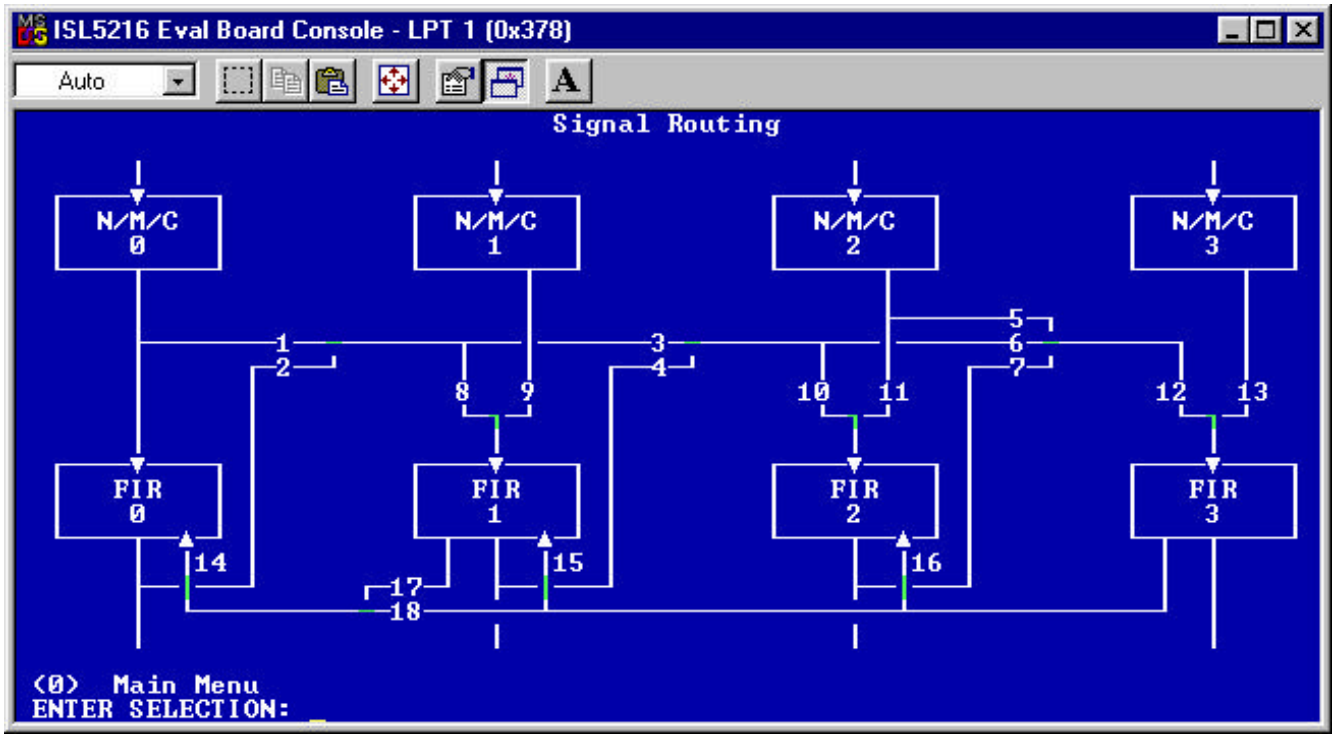
Places the software into either HSP50216 or ISL5216 mode. This setting affects certain menu choices (those related to ISL5216-specific features) and register value calculations. Note that the console window title bar shows the currently selected target device (“ISL5216 Eval Board Console” or “HSP50216 Eval Board Console”). Default value is ISL5216.



Signal Routing (Signal Routing & Common Chip Setup menu option # 6):

This screen controls the HSP50216 / ISL5216 global write address register F801H (bus routing control). This allows channels to be cascaded or polyphased to increase bandwidth or allow for more filter taps. In the screen below, for example, all 4 channels are combined into a single polyphase filter. Selections 1 - 13 change the signal routing while selections 14 - 18 control the AGC routing. In this case, channel 0's NCO / mixer / CIC output to all 4 filter compute engines (FIR0 - FIR3). Channel 3's AGC sets the gain for channels 0, 1 and 2 by way of paths 14, 18, 15, and 16. Paths 14, 15, and 16 may be toggled on or off as desired, allowing channels to control their own gains. Entering 0 from this screen returns to the board menu.

Do not select paths 2, 4, or 7 unless channel cascading is intended. These settings override the output path options in the Data Path menus. Select 1, 3 and 6 (default settings) unless channels are being cascaded.



Input Level Detector (Main menu option # 2):

The input level detector provides a way of measuring the signal level at the input to the HSP50216 / ISL5216 - this is useful for determining how much of the A/D converter's dynamic range is being used to provide gain or attenuation.

Input Source

selects between input busses A, B, C, D and the microprocessor test register as the input to the level detector. When the test register is used as the input source, three enable options are available: enabled (one input per clock), disabled (no input), or pulsed (one input per write to F808H).

Input Format

Option 2 selects whether input values are interpreted as two's complement or offset binary (see GWA = F804H bit 10).

Option 3 selects between fixed point or one of several floating point input modes. The choices available depends upon the selected target device, with the HSP50216 offering a subset of the modes available on the ISL5216. For ISL5216-specific floating point modes, the user may limit the gain range to something less than the 42 dB, 18 dB or 6 dB maximums for 3, 2 and 1 exponent bits (this is done to allow for larger CIC decimations in the datapaths - see datapath section for more information). The software prompts for the desired gain range (0 dB to the maximum, in 6 dB steps) following the floating point selection. See ISL5216 datasheet GWA = F804H bits 9:7 and 20:16 for details.

Demux Delay

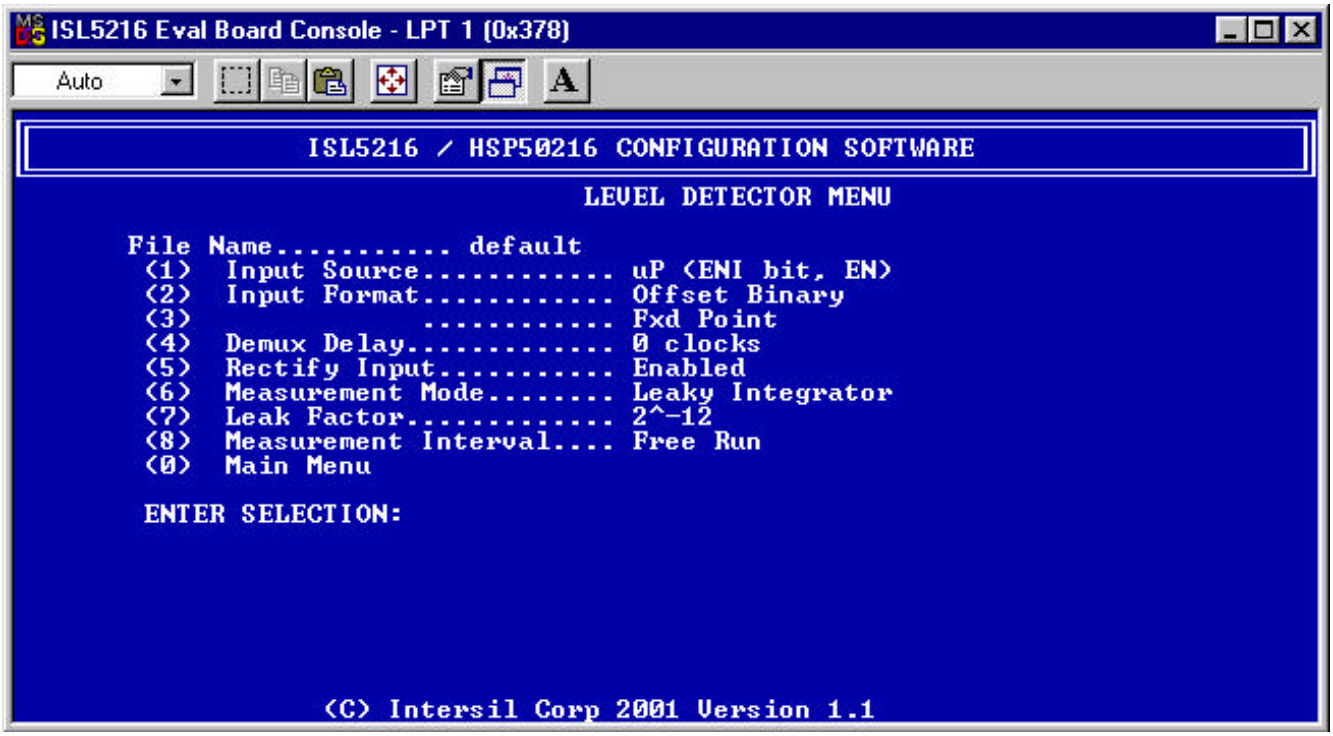
Used for signals which are time multiplexed onto an input bus. This parameter sets GWA register F804H bits 6:4.

Rectify Input

Sets F805H bit 21 (ones complement of 16 bit data after formatting) when enabled.

Measurement Mode

Sets Leaky Integrator, Peak Detector, or Integrator mode for measuring the input level. In leaky integrator mode, the level is calculated according to Yn = Xn + Yn-1 (1 - A), where A is the Leak Factor. Peak Detector and Integrator modes run over a number of samples determined by Measurement Interval. See GWA = F805H.



Data Path Menu (Channel menu option # 1):

The data path menu configures the channel input, NCO frequency, filtering and decimation.

INPUT

Sample Rate

Sample rate in Hertz into the mixer. This should normally be set to the chip's clock rate.

Input Source

selects between input busses A, B, C, D and the microprocessor test register as the input to the level detector. When the test register is used as the input source, three enable options are available: enabled (one input per clock), disabled (no input), or pulsed (one input per write to F808H).

Input Format

Option 3 selects whether input values are interpreted as two's complement or offset binary and real or complex (ISL5216 only). For complex mode, the user is prompted for the I and Q sample timing (Q samples are presented one or two clocks after I samples) and the upper sideband / lower sideband select bit. See ISL5216 datasheet, IWA = *000H bits 24:22.

Option 4 selects between fixed point or one of several floating point input modes. The choices available depends upon the selected target device, with HSP50216 offering a subset of the modes available on the ISL5216. The new ISL5216 floating point modes make use of the CIC's input barrel shifter to provide up to a maximum of 42 dB of gain range for modes with 3 exponent bits, 18 dB of range for those with 2 exponent bits, and 6 dB for the 16 bit mantissa / 1 bit exponent mode. Adding gain to the signal, however, places a limit on the maximum available decimation in the CIC. For this reason, the ISL5216 allows the exponent to saturate at a level less than the maximums provided above (see datasheet IWA = *000H bits 20:18 description). This permits gain range to be traded off for a larger CIC decimation. The software prompts for the desired gain range (0 dB to the maximum, in 6 dB steps) following the floating point selection.

Input Mode

Selects between Gated and Interpolated mode. In gated mode a sample is taken on each clock that the ENIx (input enable) is active. In interpolated mode a sample is taken on each clock and zeros are inserted when ENIx is inactive.

PN Generator

Allows -18 to -108 dBFS of pseudo-random noise to be added to the signal following mixing (see datasheet IWA register *001H - PN Gain Register).

Demux Delay

Used for signals which are time multiplexed onto an input bus. This parameter sets IWA register *000H bits 6:4.

CARRIER NCO

Center Freq

Sets carrier NCO register (IWA register *005H) according to:

Carrier NCO register = -1 * (Center Freq) * 232 / (input sample rate)

Phase Offset

In HSP50216 mode, this sets carrier phase shift bits (8:6) of IWA register *004H. Legal range is -180° to 315° in 45° increments.

In ISL5216 mode, *004H bits 8:6 are set to zero and *01CH bits 15:0 are set. Legal range is -180° to 360°.

Offset Freq

Sets the carrier offset frequency bits (2:0) of IWA register *004H allowing serial offsetting (tracking) of the carrier frequency via input bus D pins. Options are 8, 16, 24, 32 bits or disabled.

CIC FILTER

CIC Order

Controls bypassing of integrator / comb pairs. Available range is 0 - 5, with 0 bypassing all stages and 5 bypassing none. Typical setting is 5. See datasheet for frequency response curves for various CIC orders.

Decimation

Sets CIC decimation. Total decimation is the product of CIC decimation and FIR decimations.

FILTERING

This section specifies FIR filter compute engine parameters.

Spec Type

Specifies "basic" or "imported" filter type. A basic filter in the context of this software is one with the structure

FIR1 -> FIR2 -> FIR3 -> RESAMPLER -> IHBF1 -> IHBF2

where IHBF refers to interpolating halfband filter and any of the filters may be bypassed.

These filter entries become steps in the filter compute engine's instruction RAM. A bypassed filter is simply omitted from the filter program. The configuration illustrated in the screen shot below, for example, would generate 3 instructions. The first and last steps are always "wait for samples" and "loop to step 0", respectively. The only filter not bypassed below is "Filter 1" which is set as HB5, a halfband #5 filter. This becomes instruction number 1 (2nd step of the 3 step program). The basic filter structure is flexible enough to accommodate most filter designs.

In special cases, the "imported" filter type may be selected allowing the full flexibility of the HSP50216 / ISL5216 to be utilized. When this is set, options 14 - 26 disappear (no longer applicable) and options 27 (Filter Program) and 28 (decimation) appear. Filter Program is the name of the imported filter file which contains the register contents to import. Its format is similar to that of the .r0 - .r3 files except that the 1st three lines are ignored to allow for comments. Decimation is simply the decimation of the imported filter. Imported filters are often used to extract all the performance possible for such wideband applications as CDMA 2000 and UMTS.

Filter n (n = 1, 2 or 3)

Specifies the filter type: coefficient file (see File Desciptions and Formats section for details), one of 4 built-in halfband filters, or bypassed (no filter). Note that halfband filter #4 (HB4) is supplied as a coefficient file due to an error in the HB4 coefficient ROM. If the HB4 filter is needed, use the HB4.IMP coefficient file instead of the HB4 selection.

Decimation (for Filter n)

Decimation for the associated filter. Enter 1 for no change in sample rate after filtering.

Resampler

Enables or disables the resampler step. The resampler allows decimation by a non-integer value between 1 and 4. For example, a resampler input rate of 1 MHz could be resampled to 270833.333 KHz (a decimation of about 3.692).

Rate (Resampler)

Resampler output rate. The resampler's decimation (input rate / output rate) should be between 1 and 4.

Offset Freq (Resampler)

Sets the carrier offset frequency bits (14:12) of IWA register *00AH allowing serial offsetting (tracking) of the timing (resampler) NCO via input bus D pins. Options are 8, 16, 24, 32 bits or disabled.

Interp HBF

Sets the number of interpolating halfband filters to run. Options are 0 (no interpolation), 1 (IHBF #1 only), or 2 (IHBF #1 and IHBF #2). Each IHBF provides an interpolation of 2, providing an interpolation of 2 or 4 for selections 1 and 2, respectively.

Output Path

Sets bits 26:25 (path) and 24 (enable output strobe) of the FIR instruction word to select the destination of the filter compute engine's output data. Option 0 ("Direct w/o Serial Output") selects path 2 (bypass FIFO/AGC) but disables the output strobe - this is used for cascading the channel's output to another channel's filter compute engine input. Option 1 ("Direct w/ Serial Output") selects path 2 (bypass FIFO/AGC) and enables the output strobe. Option 2 ("via FIFO/AGC") selects path 1 (FIFO/AGC) and enables the output strobe. Unless cascading channels, this is normally set to option 2.

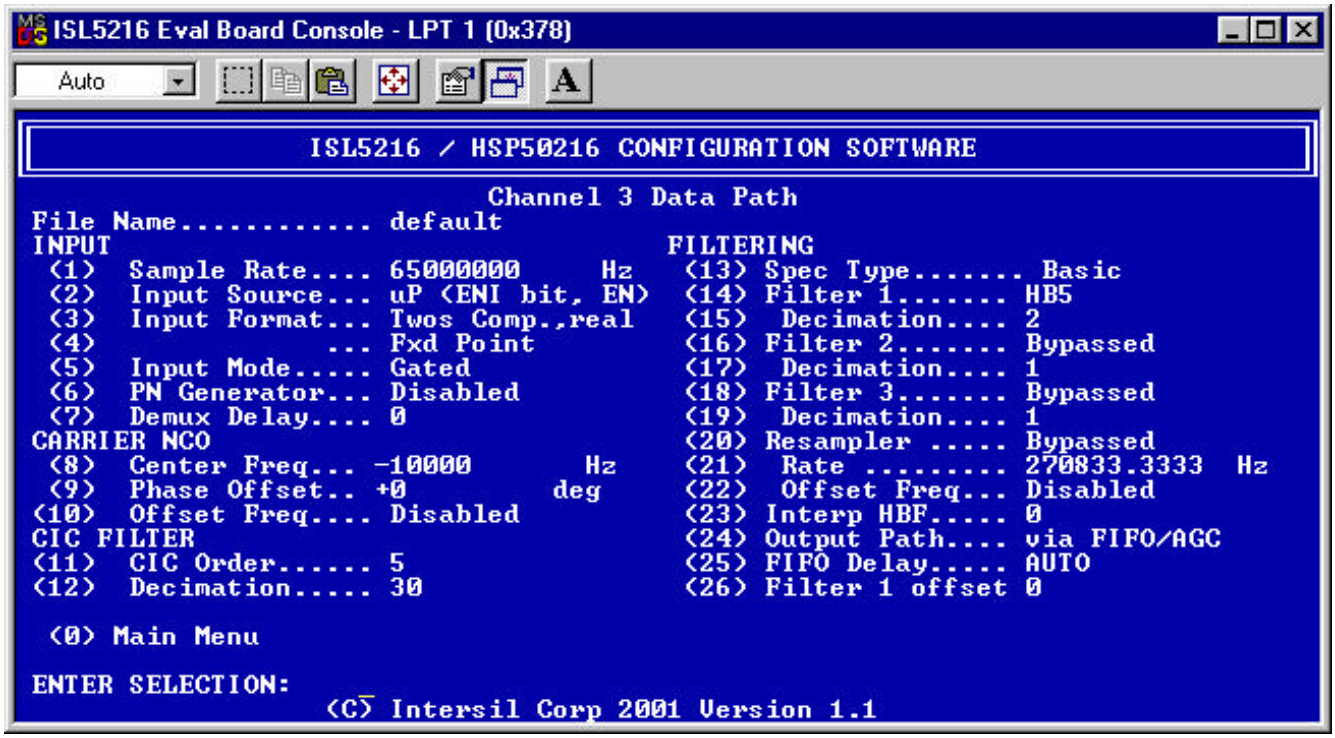
Note that option 2 is overridden by the signal routing screen (option 6 from the Board Menu).

FIFO Delay

Sets FIFODelay bits (11:0) of register *00AH. This is used to provide maximal spacing between samples from the filter compute engine before arrival at the output formatter. A setting of AUTO (-1) uses the default value of decimation - 1 except when interpolating halfband filters are used with the resampler. In this case the resampler's output rate is taken to be its input rate for the calculation. AUTO should be used for most configurations.

Filter 1 offset

Sets Filter Start Offset Register (*00BH) for the filter at instruction step # 1 (first filter in the sequence, i.e., FIR 1). This parameter is used for polyphase and systolic filter arrays. Each branch of the array, a channel's filter compute engine, receives the same data from a mixer output but is offset by 1 or more samples. This setting is used to specify that offset. The default value of 0 causes no offset. Enter -1 to offset by 1 sample, -2 to offset by 2 samples, etc. The value should normally be negative. For compatibility with the evaluation board software (which collects samples from output D to output A), make channel 3's output the most offset (largest negative number) and channel 2, 1 or 0's offset 0 for the case of a 2, 3 or 4 branch filter. This assumes channel 3's output is routed to output D, 2's to output C, 1's to output B and 0's to output A.



AGC Menu (Channel menu option # 2):

The AGC menu configures a channel's AGC mode, threshold value, gain limits and slew rates.

OUTPUT LEVEL

Threshold

Sets register *012H according to the expression

AGC threshold register = 1.646760258 * 8192.0 * 10 (threshold / 20)

where threshold is in dB relative to full scale (dBFS).

This is the target value of the AGC - it is used by the error detector to determine the gain.

LIMITS

Sets the upper and lower limits of the AGC. To disable the AGC, set the minimum and maximum gain to the same value.

Minimum Gain

Sets register *011H bits 15:0. This is the lowest gain provided by the AGC.

Maximum Gain

Sets register *011H bits 31:16. This is the highest gain provided by the AGC.

SLEW RATES

Slew Rate 0 (Attack)

Sets bits 15:8 of register *010H according to the C code below. This controls the maximum step size in mean mode, and the fixed step size in mean mode. The setting is in terms of dB of change per filter compute engine output. A faster output rate, for example, requires a lower dB / output to get the same dB/unit time slew rate. The attack setting affects how quickly the AGC decreases its gain when the received signal amplitude increases.

```
// c-code for computing AGC loop attack/decay gain register values

maxslew = ;  // 1 for mean mode, 3 for median mode

if (agcslew > 0.0)

{

    temp1dbl = ceil( log10(0.00000001 + agcslew / maxslew)

    / log10(2.0)) );if (temp1dbl > 0.0) temp1dbl = 0.0;

    temp2dbl =   (agcslew / maxslew) / pow(2.0, temp1dbl);

    if (temp2dbl > 0.9375) temp2dbl = 0.9375;

    reg010h |= (0x000000f0 & (((long int) (temp1dbl + 15.0))
    << 4));

    reg010h |= (0x0000000f & (((long int) (temp2dbl * 16.0))
    ));

}
```

Slew Rate 0 (Decay)

As above but sets bits 31:24 of *010H. The decay setting affects how quickly the AGC increases its gain when the received signal amplitude decreases.

Slew Rate 1 (Attack)

As in Slew Rate 0 (Attack), but sets bits 7:0 of *010H. Slew Rate 1 settings are accessed by setting bit 10 of register *013H (not directly supported by this software).

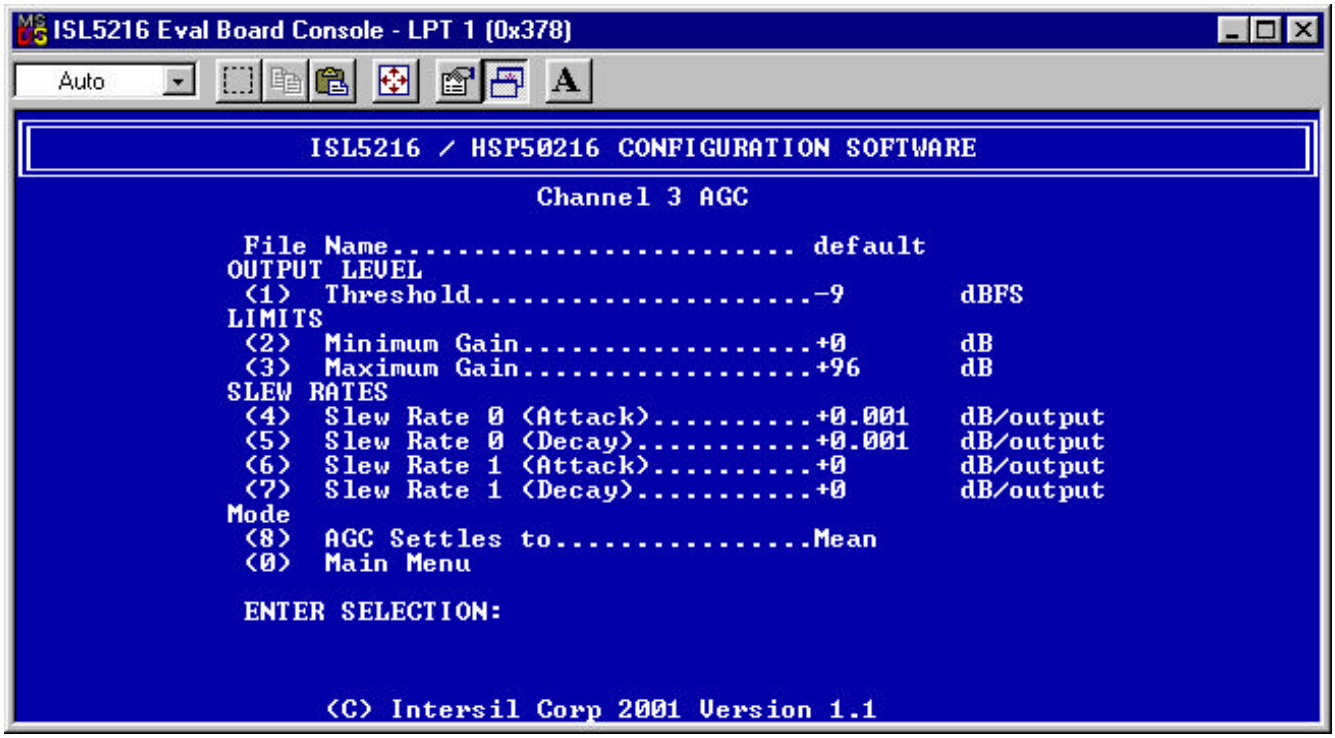
Slew Rate 1 (Decay)

As in Slew Rate 0 (Decay) but sets bits 23:16 of *010H.

MODE

AGC Settles to

Selects either mean or median mode for AGC operation. In mean mode, the AGC step size is variable and the AGC settles asymptotically to the threshold value. In median mode, the AGC step size is fixed causing settling to occur faster and more predictably at the expense of additional AM distortion after settling.



Serial Output Menu (Channel menu option # 3):

Sync Active

Sets register *014H bit 28 to make the output SYNC signal (SYNCA, SYNCB, SYNCC, or SYNCD) low or high when active. Set for the default of High when using the evaluation board.

Sync Position

Sets register *014H bits 25:24 to set the position of the sync pulse relative to the output data. Options are Early (sync pulse occurs the serial clock period before the first data bit of the serial word), Late (sync pulse occurs the serial clock period after the last data bit of the serial word) or coincident (sync pulse occurs the serial clock period of the first data bit of the serial word). Use the default of Early when targeting the evaluation board.

Output Delay

Sets register *014H bits 11:0. This parameter is used to offset the channel's output by the specified number of serial clocks to allow time multiplexing of channels onto a single serial output pair.

Phase Output

Sets bit 5 of register *013H to select either phase or dphi/dt to be available as "phase" at the output formatter. The dphi/dt output is useful for FM and FSK demodulation. *013H bit 7, required to output dphi/dt without recirculation through the filter compute engine, is always set by the software.

dp/dt Delay

Sets bits 2:0 of register *013H to set the delay, in samples, for the dphi/dt calculation. Allowable range is 1 to 8, inclusive.

Phase Gain

Sets bits 3 and 4 of register *013H to shift the phase up 0, 1, 2, or 3 bit positions (discarding bits shifted off the top) making the phase modulo 360, 180, 90 or 45 degrees, respectively.

Mag Gain

Sets bits 20 and 21 of register *014H to scale the magnitude output from the Cartesian-to-polar coordinate converter by 1, 2, 4 or 8.

Output 1 and 2

See datasheet description of registers *015H - *018H for serial output data settings.

Output 1 refers to the SD1x serial output and output 2 to the SD2x output, where x = A, B, C or D.

The evaluation board collects only the first 8, 16, 24, or 32 bits of data from each channel.

Type

Choose between zeros, I, Q, magnitude, phase (dphi/dt), I2, Q2, or AGC gain information for a given time slot.

Bits

Length of slot: disabled (outputs a single zero), 4, 6, 8, 10, 12, 16, 20, 24, or 32 bits fixed or 32 bit IEEE floating point. (IEEE 32 bit floating point mode available on output 1 only). When targeting the evaluation board, be sure to set "Bits captured per sample" (Data Collection & Display Settings) to the length of the first slot.

Sync

Y = output sync pulse generated on this slot, N = no sync pulse generated. (available on output 1 only)

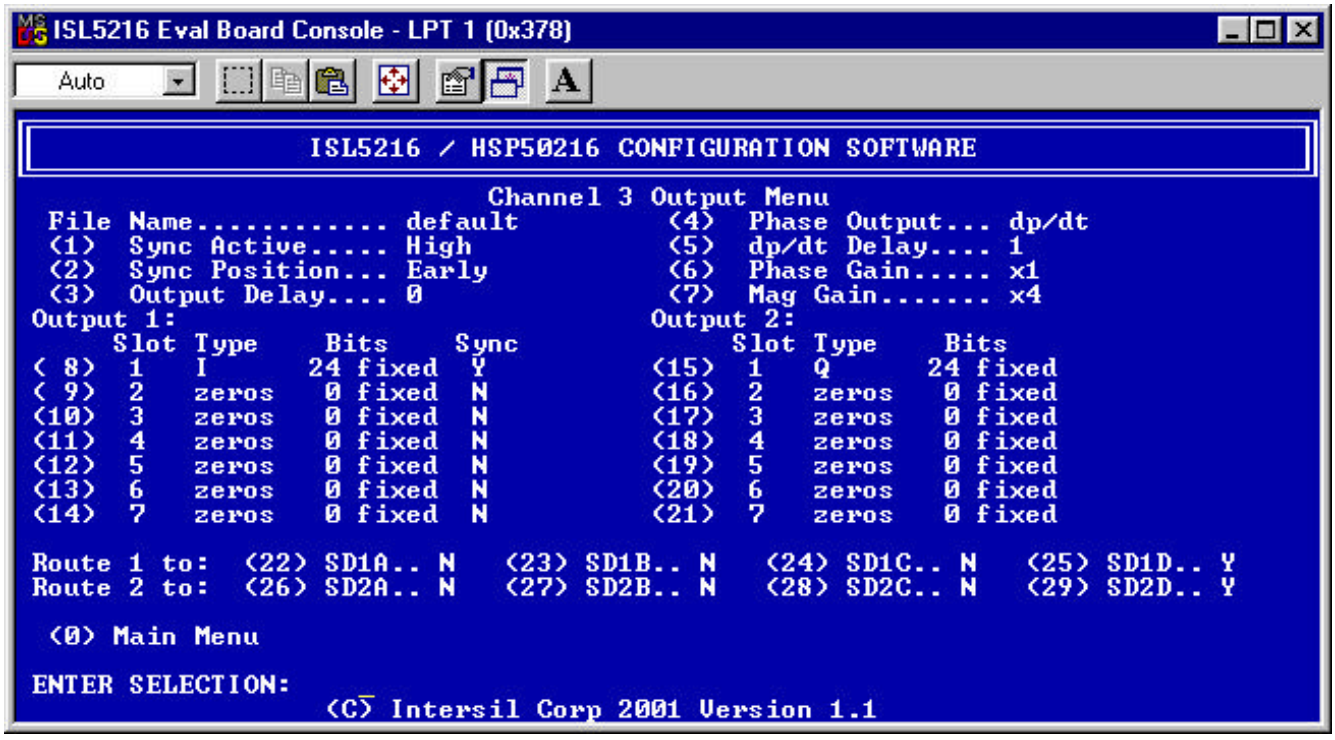
The evaluation board expects a sync to be present on the first slot.

Route 1 to:

Sets bits 19:16 of register *014H to enable the channel's output to serial pins SD1A, SD1B, SD1C and/or SD1D. Note that display and capture functions in the evaluation board software assume that channel 3's output is routed to output D, 2's to output C, 1's to output B and 0's to output A. When targeting the evaluation board this convention should be followed.

Route 2 to:

As above, but sets bits 15:12 of register *014H to enable the channel's output to serial pins SD2A, SD2B, SD2C and/or SD2D.



Sync Menu (Channel menu option # 4):

Load Carrier NCO Freq on SyncIn

Sets register F802H bit 29 (ch. 0), 21 (ch. 1), 13 (ch. 2) or 5 (ch. 0) and *004 bit 3. See datasheet for details.

Clear Carrier NCO Feedback on SyncIn

Sets register *004H bit 4 to clear the phase accumulator on loading the carrier NCO frequency register (not necessarily on SyncIn).

Reset CIC Filter on SyncIn

Sets register F802H bit 25 (ch. 0), 17 (ch. 1), 9 (ch. 2) or 1 (ch. 0) to reset the CIC decimation counter on SyncIn.

Reset FIR Filters on SyncIn

Sets register F802H bit 28 (ch. 0), 20 (ch. 1), 12 (ch. 2) or 4 (ch. 0) to reset the filter compute engine on SyncIn.

Load Timing NCO Frequency on SyncIn

Sets register F802H bit 26 (ch. 0), 18 (ch. 1), 10 (ch. 2) or 2 (ch. 0).

Clear Timing NCO Feedback on SyncIn

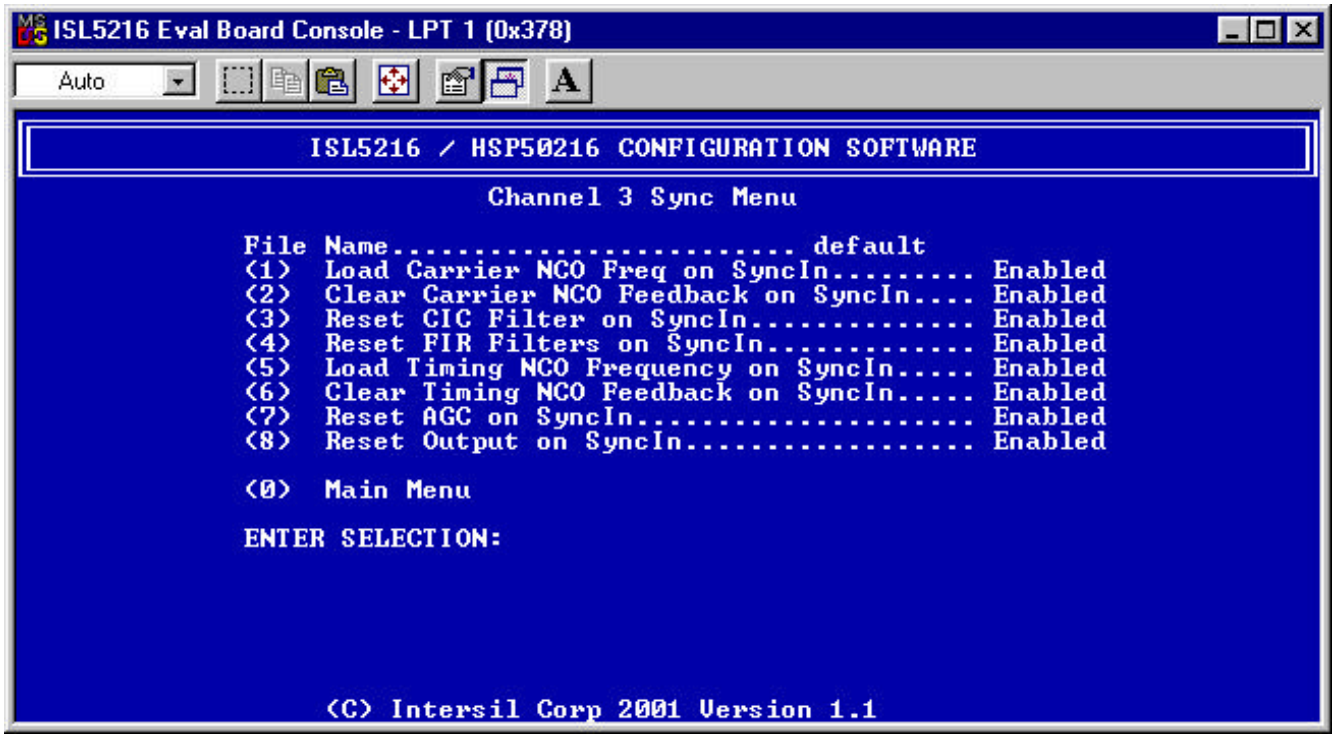
Not currently implemented. Register *00A bit 16 is unconditionally set by software to clear the resampler (timing) NCO phase accumulator on loading the timing NCO frequency register.

Reset AGC on SyncIn

Sets register F802H bit 27 (ch. 0), 19 (ch. 1), 11 (ch. 2) or 3 (ch. 0).

Reset Output on SyncIn

Sets register F802H bit 24 (ch. 0), 16 (ch. 1), 8 (ch. 2) or 0 (ch. 0) to reset the serial output block on SyncIn.



Data Collection & Display Settings Menu (Main menu option # 11):

Write Value to Input Reg and Capture Data / Capture Data

These options allow data to be captured from the serial outputs (first time slots only) and saved to a file. This file, data.imp, is ASCII text beginning with 7 lines of comments. Starting with the 8th line, the data are listed in 2 columns (SD1x and SD2x) and are signed 32 bit integers presented as decimal (base 10) numbers.

Prior to capturing data, set the "Bits captured per sample" to match the size of the 1st time slot of the output data. (See "Bits captured per sample" below).

Option (1) below ("Write Value to Input Reg and Capture Data") assumes that the microprocessor test register (register F807H) is being used as the input source for the mixer. You will be prompted for a value to load into that register before capture begins. The remaining parameters are the same as for option (2) ("Capture Data"). You will be prompted for the total number of samples to collect. The maximum number of samples available is determined by the

capture size - it is 262144 samples for 8 bit data, 131072 samples for 16 bit data, 87381 samples for 24 bit data and 65536 for 32 bit data.

The last item you will be prompted for is the output(s) to collect data from: D; D and C; D, C, and B or D, C, B and A. The latter 3 collection modes are useful for collecting data from certain polyphase filter structures. In the case of multiple channel data capture, the data are put in the file in the order shown starting with output D (i.e. D, then C, B, A, and then D again..). When capturing from multiple channels, the channel outputs must be synchronized. They should have the same FIR filter lengths, types and decimations so that their outputs are produced at the same time.

Channel D Frequency Sweep

This test uses the carrier NCO to sweep the filter to generate magnitude vs. frequency file sweep.imp.

The microprocessor test register (F807H) is selected as the input source. Since this is a DC source, the output of the mixer is simply the carrier NCO frequency. You will be prompted for the test register value (input signal magnitude) with "Enter uP Input Word (0x8000 to 0x7FFF)", where 0x8000 is negative full scale and 0x7FFF is positive full scale. All AGCs are automatically disabled by setting their upper and lower gain limits to zero.

When prompted by "Enter Sample Rate", enter the input sample rate to the chip (usually the clock rate) in Hz. Enter the sweep starting and ending frequencies in Hz. You will also be prompted for the step size. Smaller steps will provide a better resolution of the frequency response at the expense of a longer sweep time. A step of 1 KHz per MHz of sweep range provides good resolution at an acceptable run time. Dwell time in milliseconds is the last required parameter. This is the delay between carrier NCO update and the point of magnitude capture. Except for very long filters and slow output rates, a dwell time of 1 ms is usually sufficient.

The format of the sweep.imp output file is 7 lines of comments followed by two columns of numbers. The first column is frequency in Hz. The second column is the relative magnitude in dB.

Bits captured per sample

This setting is used by the evaluation board software in "Run and Display" and "Capture Data" modes. It specifies how many bits to capture from selected outputs when SYNCD goes active. Available options are 8, 16, 24, and 32 bits. If the 216's first output slot is not exactly one of these lengths, either choose the next smallest length (some LSB bits will be lost) or, if there are sufficient output clocks, set the second output slot to output enough zeros to pad to the selected capture length. Be sure not to pick capture length longer than the actual first time slot length unless the following time slot contains only zeros.

Polyphase mode

This parameter is used in the evaluation software's "Run and Display" mode to determine how outputs should be collected. Six polyphase modes are supported. They are:

channels 3 and 2 on outputs D and C

channels 3, 2 and 1 on outputs D, C and B

channels 3, 2, 1 and 0 on outputs D, C, B and A

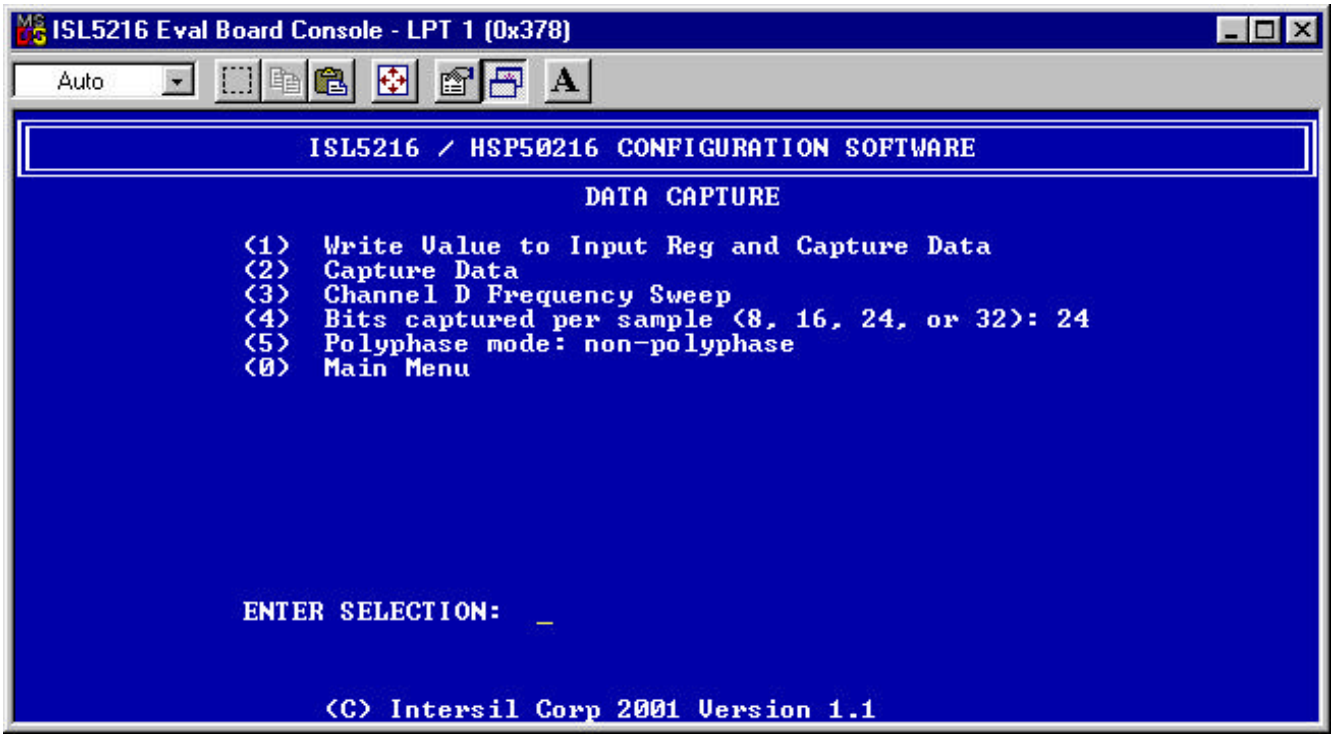
channels 3 and 2 mutiplexed on output D

channels 3, 2 and 1 mutiplexed on output D

channels 3, 2, 1 and 0 mutiplexed on output D

When multiplexing channels onto output D, each channel must be configured to produce a SYNC pulse on its first time slot. With four channels multiplexed onto output D, for example, four SYNC pulses should be seen per filter run.

When multiple output pairs are used, all outputs should be synchronized to channel D's SYNCD. For this to happen, all channels should have the same filter configuration (filter lengths, types and decimations) but the coefficients may vary. Outputs are collected in the order shown (D, C, B, then A), so channel 3's output (assumed routed to output D) should have the most negative offset (see Data Path menu section, option # 26).

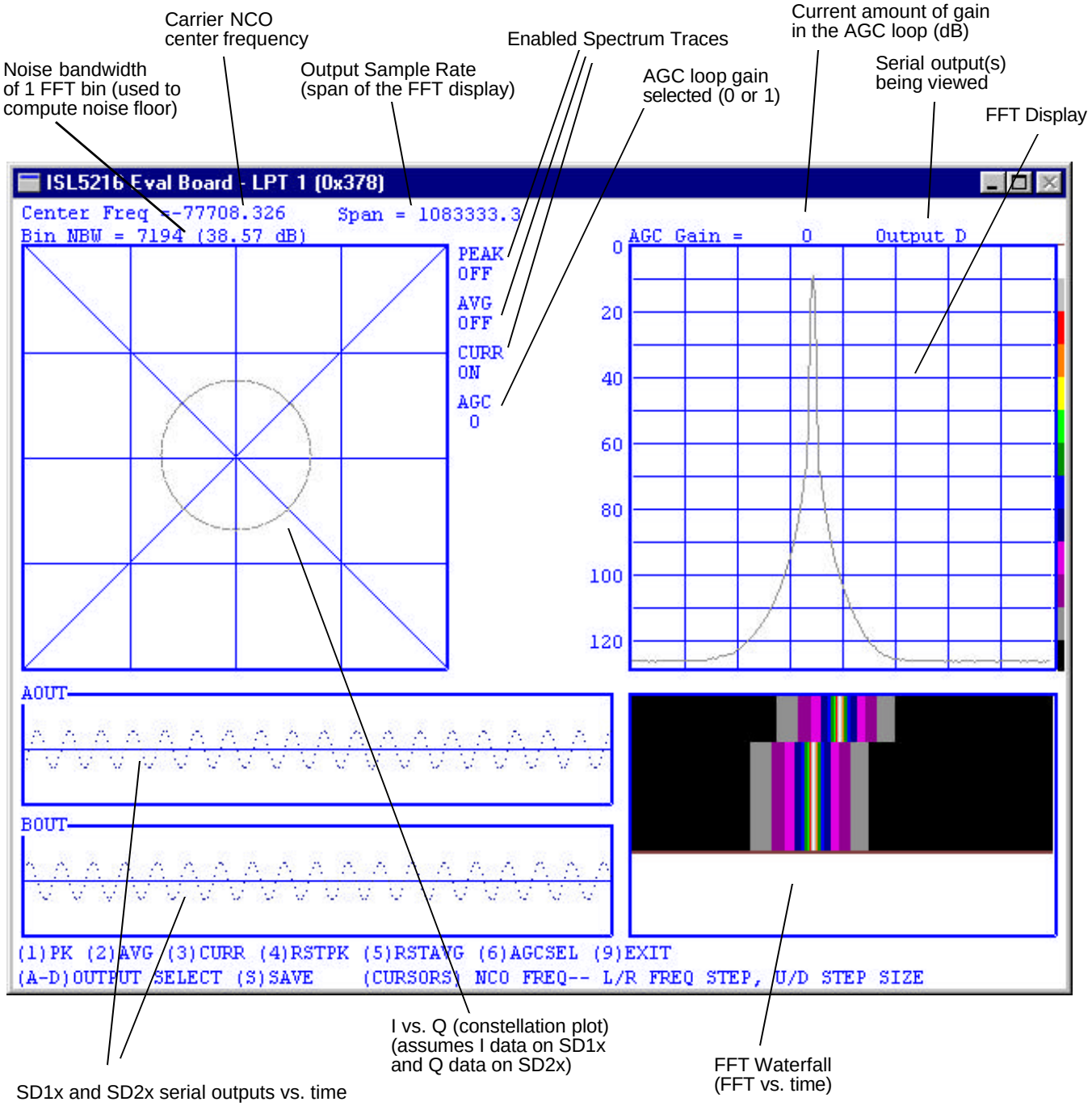


Run and Display (Main menu option # 13):

"Run and Display" mode provides the graphics window shown below to collect and display output samples in real time. While running, the evaluation board hardware captures 256 sample snapshots which are then transferred to the computer for Blackman-windowed FFT computation and display. The samples are captured on SYNCD (serial port D) pulses - if viewing an output other than D it must be synchronized to D (the channel should have the same configuration as the one driving output D). The table below lists the functions that are available in this mode (the text at the bottom of the graphics window also provides a brief listing). The text console is disabled in run and display mode. Press "9" to close the graphic window and return to the text console. For best performance in run and display mode, be sure the graphics window is selected as the active window (this is done by clicking anywhere on the window).

KEY	FUNCTION
1	toggles peak display (blue trace) on / off
2	toggles average display (green trace) on / off
3	toggles current (real-time) FFT display on / off
4	resets peak trace
5	resets average trace
6	toggles between AGC loop gains (slew rates) 0 and 1. (see register *010H description in datasheet). It is helpful to set loop gain 0 attack/decay as desired and loop gain 1 attack/decay to 0, making this key an "AGC on/off" control.
A - D	selects the serial output to monitor (if other than D, that channel must be synchronized to output D). Not used in polyphase mode.
$\leftarrow$ and $\rightarrow$	steps the carrier center frequency
$\uparrow$ and $\downarrow$	increases / decreases the step size (amount carrier frequency changes when left/right arrow keys are pressed). The step size range is 2^N FFT bins with N = 0 to 8.
S	Saves a snapshot of the SD1x and SD2x data to "output.dat" and a snapshot of the current, peak and average traces of the FFT windows to "spectrum.dat". These are human readable files which may be imported into other applications.

KEY	FUNCTION
9	Exits run and display mode (console window is re-enabled)



Test Menu (Main menu option # 15):

uP Interface R/W Test

Performs a quick test of the microprocessor interface to the chip. Writes A5A555AAH to the channel 0 carrier NCO register (0005H) and verifies it is read back correctly. This is then repeated with the values 00000001H, 00000002H, 00000004H, 00000008H, … , 80000000H (walking 1 test).

Instruction and Coefficient Memory Test

Performs an extensive test of the 216's filter compute engine instruction RAMs (*100H - *17FH), pointer RAMs (*180H - *1FCH), coefficient RAMs (*440H - *47FH and *480H - *4FFH), and coefficient ROMs (*400H - *428H, *430H - *43FH and *520H - *57FH) . In ISL5216 mode, the filter compute engine data RAMs are also tested. This may take several minutes to complete depending upon computer speed and evaluation board interface type.

Monitor Input Pins

Displays input busses A, B, C, D, reset (inverted with respect to input pin), ENIA, ENIB, ENIC, ENID, and SYNCI in real time. Input busses A, B, C and D are read via the input level detector while the remaining pins are obtained from the status register (direct address 3 - see Table of Microprocessor Direct Read/Write Addresses for details).

Marching 1 on Output Pins

In HSP50216 mode, this function marches a 1 through the following group of output pins: SERCLK (J6-3, 7, 11, 15), SYNCD (J6-4), SD1D (J6-5), SD2D (J6-6), SYNCC (J6-8), SD1C (J6-9), SD2C (J6-10), SYNCB (J6-12), SD1B (J6-13), SD2B (J6-14), SYNCA (J6-16), SD1A (J6-17), SD2A (J6-18), INTRPT (TP4-13), and SyncO (J10-1, 3, 5, 7).

In ISL5216 mode, a 1 is marched through all of the above output pins except SD2A, SD2B, SD2C and SD2D. These outputs are instead connected to the MSBs of the SIN outputs of the channel carrier NCOs (see GWA = F800H bits 7:4, bits 31:21 and bit 16).

Poke Data into HSP50216

Writes a 32 bit value directly to an HSP50216 / ISL5216 register.

Peek Data from HSP50216

Reads a 32 bits value from an HSP50216 / ISL5216 register.

Poke Data into Eval Board Register

Writes a 16 bit value to an evaluation board (FPGA) register.

Peek Data from Eval Board Register

Reads a 16 bit value from an evaluation board (FPGA) register.

HSP50216 HW Reset

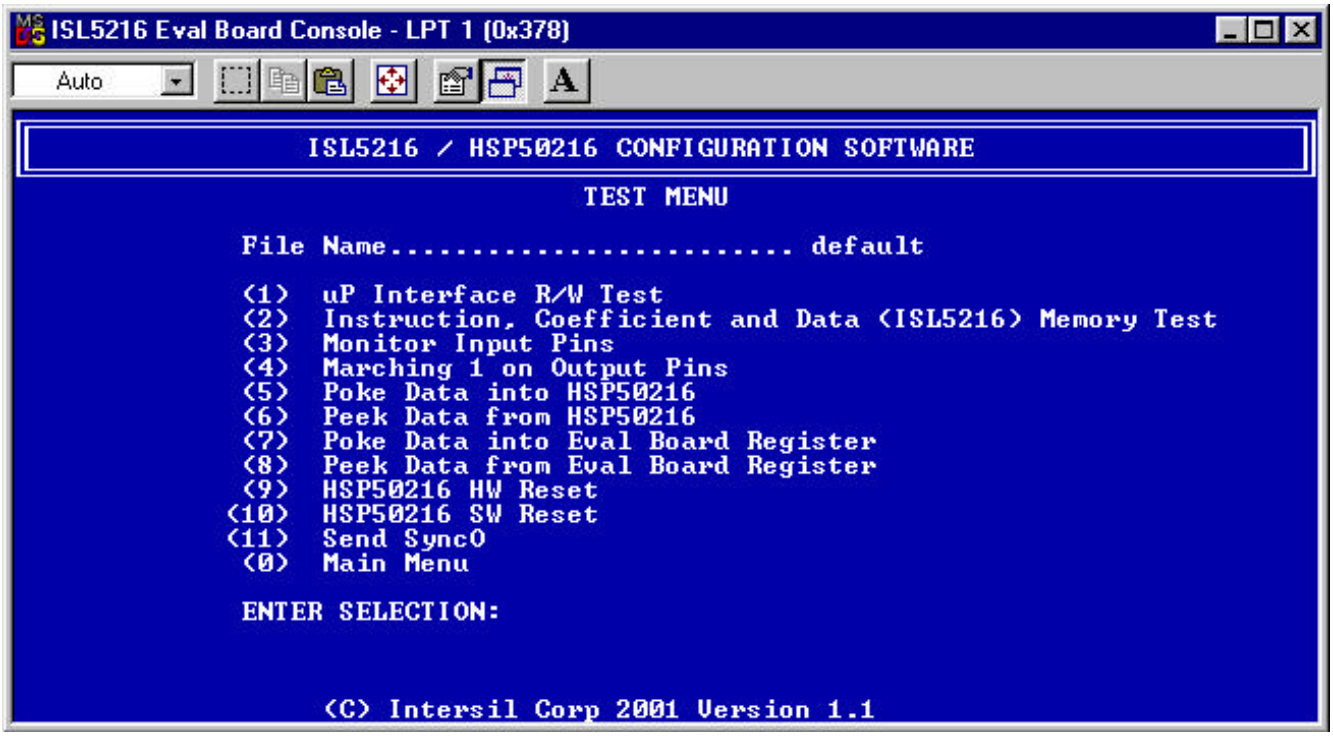
Performs a hardware reset of the HSP50216 / ISL5216 chip.

SP50216 SW Reset

Writes to register *019H of specified channel(s) to do a software reset of the channel.

Send SyncO

Writes to register F809H to generate a SyncO pulse.



File Descriptions and Formats:

Impulse response files (*.IMP files):

These are text files containing FIR filter coefficients. These coefficients must be less than 1.0 in magnitude. The first 7 lines of the file are reserved for comments and are ignored by the software. For complex coefficients, the first column represents the real numbers and second column the imaginary numbers. For real coefficients, use only a single column. All coefficients must be included in the .imp file, even if the filter is symmetric. The software will determine filter symmetry by examining the coefficients. Note that symmetric filters provide twice the computation speed of non-symmetric filters, and real coefficient filters run faster than complex coefficient filters. Maximal filter rate is therefore obtained with real, symmetric coefficient filters.

Imported filter files (*.I files)

An imported filter is simply a manually-created filter which is imported into the configuration rather than calculated from menu parameters. The first 3 lines of this file are reserved for comments and are ignored by the software. Starting with line 4, the format is similar to that of the .R# files - a 16 bit register number followed by a 32 bit value, both in hex. Any registers contained in this file will overwrite registers in the configuration the filter is imported into. Typically, an imported filter file will contain the following registers: *007H - *00DH (timing NCO and filter compute engine parameters), *100H - *17FH (filter compute engine instruction RAMs), and *440H - *4FFH (filter compute engine coefficient RAMs). Note that the high 4 bits of the register number are ignored (register number is ANDed with 0x0FFF) to remove reference to any particular channel. The imported filter file applies only to the channel it is imported into, as specified in the Data Path menu.

Register files (.R# and .RTP)

These files contain the actual register data downloaded to the HSP50216 / ISL5216. There are four .R# files - one for each channel. The # indicates which channel (0 - 3). .RTP contains the register information for the top level (global) functions (register F800H - F83FH). These files are created by main menu option 10 (compute register files) and are downloaded to the evaluation board using option 12. Option 14 creates a single batch file containing all the information found in the .R and .RTP files. It is described in the main menu section.

Statistics file (.STA)

The .STA file provides information on clock and memory usage. This is useful for determining if more taps can be added to a filter. It also shows all the intermediate data rates in a filter configuration. An excerpt from an STA file is provided below. "Peak Engine Run Rate" is the number of runs of the filter program per second. This is the filter compute engine input rate (CIC output rate) divided by the decimations of FIR1, FIR2 and FIR3. "Inputs / run" states the number of inputs a filter must receive before it can run - this is the product of its decimation and the decimation of the filter(s) that follow it. "Outputs / run" is "Inputs / run" divided by the filter's decimation. "Compute / output" is the number of clocks required to compute an output, not including clocks required for writing samples to the filter's input buffer. "Total / run" is "Compute / output" plus the clocks required for input writes (one clock per input sample). "Total clk/sec" is the "Total / run" multiplied by the filter run rate.

Note that the STA information is not available for channels using imported filters.

Channel 3 Processing and Resource Usage

```
CIC
 Input Sample Rate ..................................   65000000
 Decimation .........    30    CIC Output Rate ...... 2166666.67

FIRs
 Input Sample Rate ................................. 2166666.67
 FIR1
  Decimation ........     2    FIR1 Output Rate ..... 1083333.33
 FIR2
  Decimation ........bypass    FIR2 Output Rate ..... 1083333.33
 FIR3
  Decimation ........bypass    FIR3 Output Rate ..... 1083333.33
 RESAMPLER
  Decimation ........bypass    Resamp Output Rate ... 1083333.33
 INTERPOLATION HBF
  Interpolation .....bypass    IBHF Output Rate ..... 1083333.33


FIR Engine Usage
 Peak Engine Run Rate:     1.08333e+006

                                    Clocks       Total
 FIR      Inputs  Outputs  Compute   Total  Clk/sec
           /run    /run    /output   /run
 FIR1        2      1         7        9     9750000
 Overhead                              2     2166667

 TOTAL                                11    11916667
 UTILIZATION                                 18.3 %

 Memory Usage
    FIR      Data Memory     Coef Memory   Taps
             Start    Size      Start
   FIR1     0x0000      32      0x0018       23
                    _
     Total            32  (8.33% utilization)
```