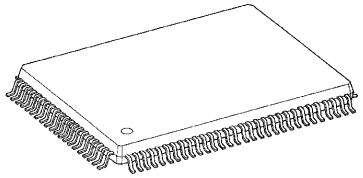
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC9432F

DIGITAL SERVO SINGLE CHIP PROCESSOR BUILT IN 1 BIT DA CONVERTER

The TC9432F is a single chip processor which incorporates the following function : synchronous separation protection and interpolation, EFM demodulation, Error correction, microcontroller interface, digital equalizer for use in servo LSI and servo control circuit.
In addition, the TC9432F incorporates a 1 bit DA converter. In combination with the head amplifier TA2109F for digital servo, the TC9432F allow simplified, adjustment-free structuring of CD player system.



QFP100-P-1420-0.65A

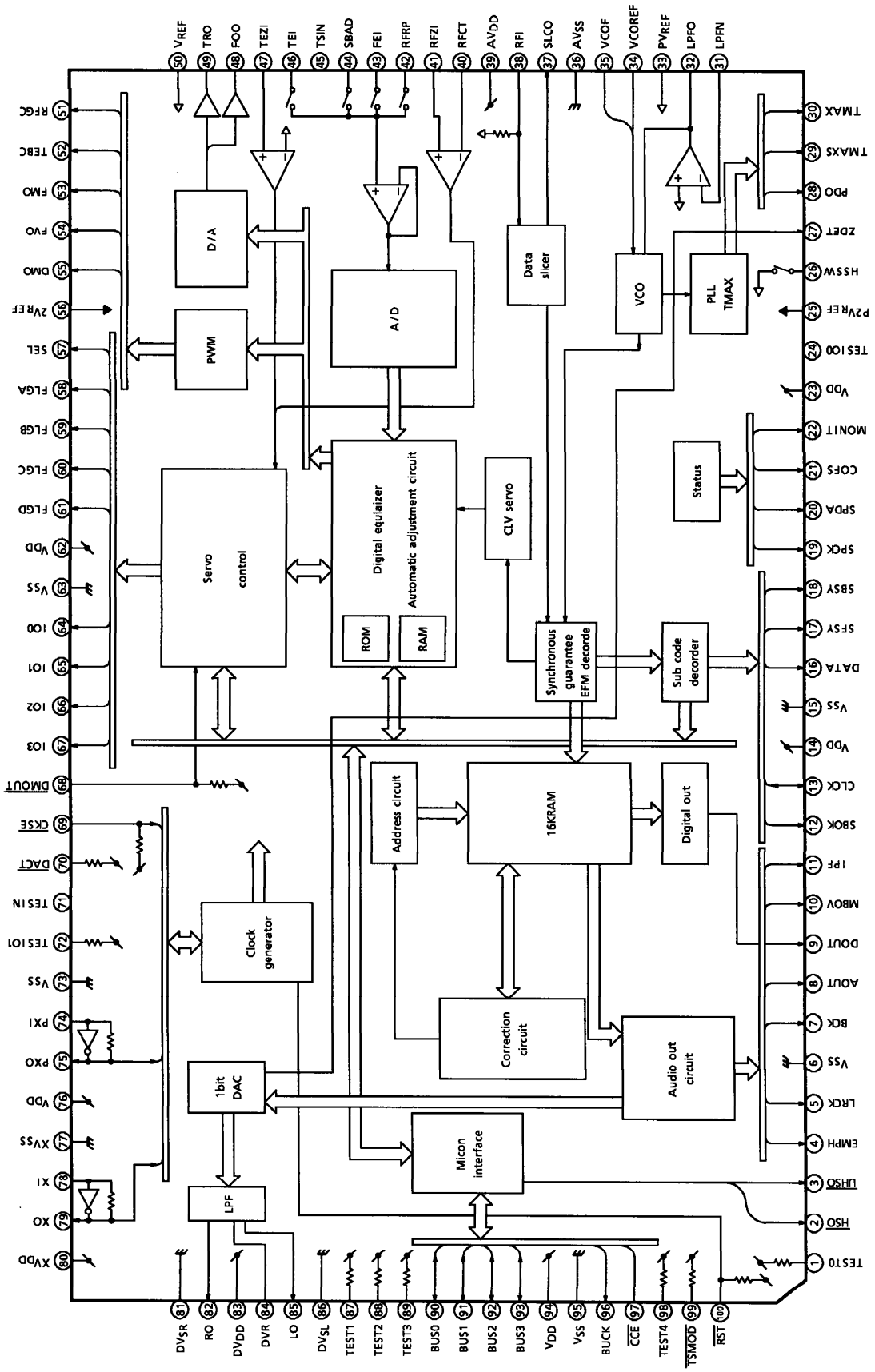
Weight : 1.6g (Typ.)

FEATURES

- Sync pattern detection, sync signal protection and synchronization can be made correctly.
- Built in EFM demodulation circuit, subcode demodulation circuit.
- Capable of correcting dual C1 correction and quadruple C2 correction using the CIRC correction theoretical format.
- The TC9432F respond to variable playback system.
- Jitter absorbing capacity of ±6 frames.
- Built in 16KRAM.
- Built in digital out circuit.
- Built in L/R independent digital attenuator.
- Audio output responds to bilingual function.
- Reed timing free subcode Q data and capable of synchronous output with audio data.

- Built in data slicer and analog PLL (free-adjustment VCO).
- Capable of automatic adjustment function of focus servo and tracking servo, for loop gain, offset and balance.
- Built in RF gain automatic adjustment circuit.
- Built in digital equalizer for phase compensation.
- Built in RAM for digital equalizer for coefficient, and capable of variable pickup.
- Built in focus, tracking servo control circuit.
- Search control corresponds to every mode and can realize high speed and stable search.
- Lens-kick are using speed controlled form.
- Built in AFC circuit and APC circuit for CLV servo of disc motor.
- Built in anti-defect and anti-shock circuit.
- Built in 8 times oversampling 1bit DA converter.
- Built in analog filter for 1bit DA converter.
- Built in zero data detect output circuit.
- The TC9432F capable of 4 times speed operation.
- Built in microcontroller interface circuit.
- CMOS silicon structure and high speed, low power consumption.
- 100 pin flat package.

BLOCK DIAGRAM (Top view)



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PIN FUNCTION

<table>
<tr><th>PIN No.</th><th>SYMBOL</th><th>I/O</th><th>FUNCTIONAL DESCRIPTION</th><th>REMARKS</th></tr>
<tr><td>1</td><td>TEST0</td><td>I</td><td>Test mode terminal. Normally, keep at open.</td><td>With pull-up resistor.</td></tr>
<tr><td>2</td><td>$\overline{HSO}$</td><td>O</td><td rowspan="2">Playback speed mode flag output terminal.
<table><tr><th>$\overline{UHSO}$</th><th>$\overline{HSO}$</th><th>PLAYBACK SPEED</th></tr><tr><td>H</td><td>H</td><td>Nomal</td></tr><tr><td>H</td><td>L</td><td>2 times</td></tr><tr><td>L</td><td>H</td><td>4 times</td></tr><tr><td>L</td><td>L</td><td>—</td></tr></table></td><td rowspan="2">—</td></tr>
<tr><td>3</td><td>$\overline{UHSO}$</td><td>O</td></tr>
<tr><td>4</td><td>EMPH</td><td>O</td><td>Subcode Q data emphasis flag output terminal. Emphasis ON at “H” level and OFF at “L” level. The output polarity can invert by command.</td><td>—</td></tr>
<tr><td>5</td><td>LRCK</td><td>O</td><td>Channel clock output terminal. (44.1kHz) L-ch at “L” level and R-ch at “H” level. The output polarity can invert by command.</td><td>—</td></tr>
<tr><td>6</td><td>V_{SS}</td><td>—</td><td>Digital GND terminal.</td><td>—</td></tr>
<tr><td>7</td><td>BCK</td><td>O</td><td>Bit clock output terminal. (1.4122MHz)</td><td>—</td></tr>
<tr><td>8</td><td>AOUT</td><td>O</td><td>Audio data output terminal.</td><td>—</td></tr>
<tr><td>9</td><td>DOUT</td><td>O</td><td>Digital data output terminal.</td><td>—</td></tr>
<tr><td>10</td><td>MBOV</td><td>O</td><td>Buffer memory over signal output terminal. Over at “H” level.</td><td>—</td></tr>
<tr><td>11</td><td>IPF</td><td>O</td><td>Correction flag output terminal. At “H” level, AOUT output is made to correction impossibility by C_2 correction processing.</td><td>—</td></tr>
<tr><td>12</td><td>SBOK</td><td>O</td><td>Subcode Q data CRCC check adjusting result output terminal. The adjusting result is OK at “H” level.</td><td>—</td></tr>
<tr><td>13</td><td>CLCK</td><td>I/O</td><td>Subcode P~W data readout clock input/output terminal. This terminal can select by command bit.</td><td>—</td></tr>
<tr><td>14</td><td>V_{DD}</td><td>—</td><td>Digital power supply voltage terminal.</td><td>—</td></tr>
<tr><td>15</td><td>V_{SS}</td><td>—</td><td>Digital GND terminal.</td><td>—</td></tr>
<tr><td>16</td><td>DATA</td><td>O</td><td>Subcode P~W data output terminal.</td><td>—</td></tr>
<tr><td>17</td><td>SFSY</td><td>O</td><td>Play-back frame sync signal output terminal.</td><td>—</td></tr>
<tr><td>18</td><td>SBSY</td><td>O</td><td>Subcode block sync signal output terminal.</td><td>—</td></tr>
<tr><td>19</td><td>SPCK</td><td>O</td><td>Processor status signal readout clock output terminal.</td><td>—</td></tr>
<tr><td>20</td><td>SPDA</td><td>O</td><td>Processor status signal output terminal.</td><td>—</td></tr>
<tr><td>21</td><td>COFS</td><td>O</td><td>Correction frame clock output terminal. (7.35kHz)</td><td>—</td></tr>
<tr><td>22</td><td>MONIT</td><td>O</td><td>Internal signal (DSP internal flag and PLL clock) output terminal. Selected by command.</td><td>—</td></tr>
<tr><td>23</td><td>V_{DD}</td><td>—</td><td>Digital power supply voltage terminal.</td><td>—</td></tr>
</table>

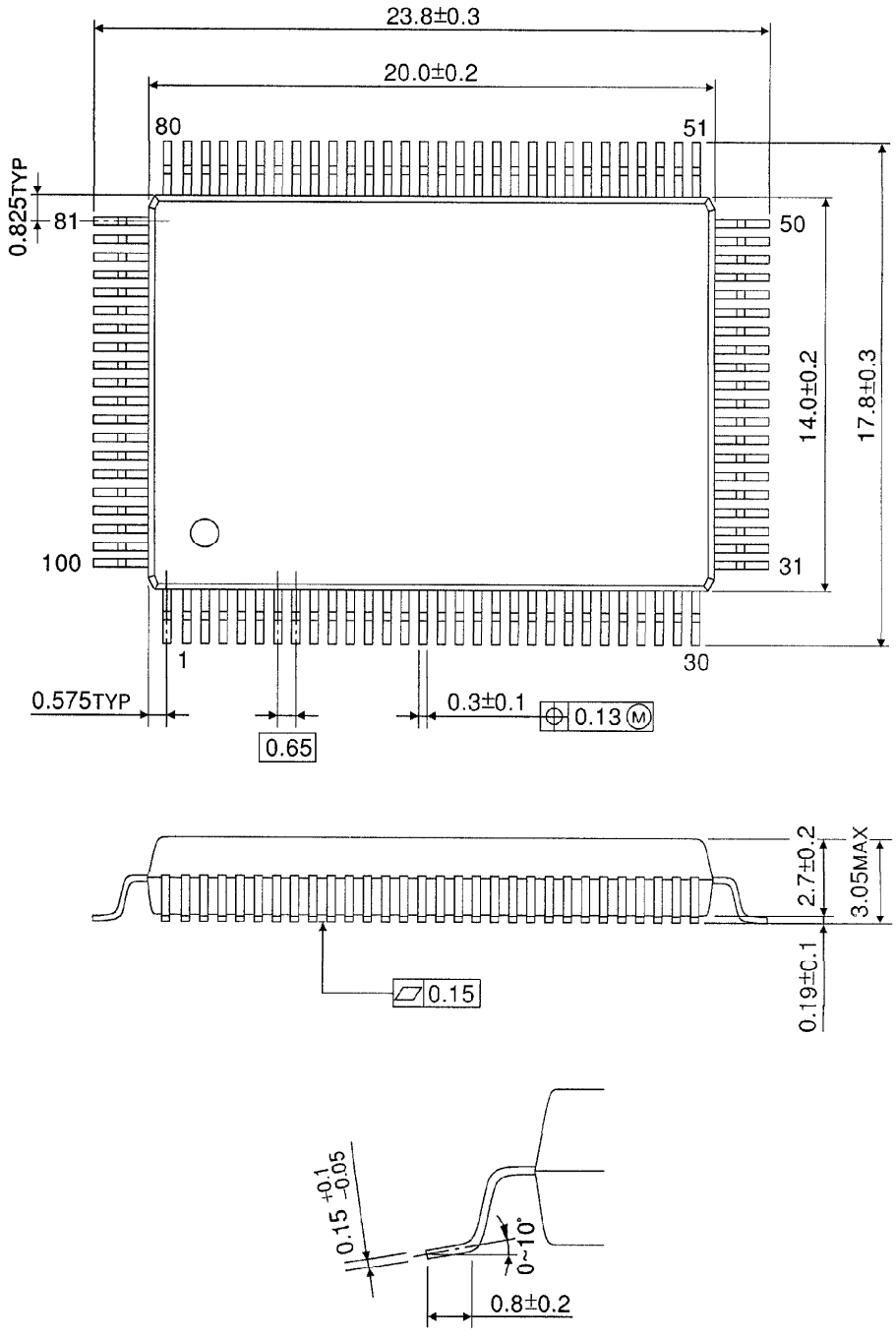
PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS
24	TESIO0	I	Test input/output terminal. Normally, keep at "L" level.	—
25	$P2V_{REF}$	—	PLL double reference voltage supply terminal.	—
26	HSSW	O	2/4 times speed at "V_{REF}" voltage.	2-state output. (PV_{REF}, HiZ)
27	ZDET	O	1bit DA converter zero detect flag output terminal.	—
28	PDO	O	Phase difference signal output terminal of EFM signal and PLCK signal.	3-state output. ($P2V_{REF}$, PV_{REF}, V_{SS})
29	TMAXS	O	TMAX detection result output terminal. Selected by command bit (TMPS).	3-state output. ($P2V_{REF}$, PV_{REF}, V_{SS})
30	TMAX	O	TMAX detection result output terminal. Selected by command bit (TMPS). DIFFERENCE RESULT / TMAX OUTPUT Longer than fixed freq. / "$P2V_{REF}$" Shorter than fixed freq. / "V_{SS}" Within the fixed freq. / "HiZ"	3-state output. ($P2V_{REF}$, HiZ, V_{SS})
31	LPFN	I	LPF amplifier inverting input terminal for PLL.	Analog input.
32	LPFO	O	LPF amplifier output terminal for PLL.	Analog output.
33	PV_{REF}	—	PLL reference voltage supply terminal.	—
34	VCOREF	I	VCO center frequency reference level terminal. Normally, keep at "PV_{REF}" level.	—
35	VCOF	O	VCO filter terminal.	Analog output.
36	AV_{SS}	—	Analog GND terminal.	—
37	SLCO	O	Data slice level output terminal.	Analog output.
38	RFI	I	RF signal input terminal.	Analog input. (Z_{in} : selected by command)
39	AV_{DD}	—	Analog power supply voltage terminal.	—
40	RFCT	I	RFRP signal center level input terminal.	Analog input. (Z_{in} : 50kΩ)
41	RFZI	I	RFRP zero cross input terminal.	Analog input.
42	RFRP	I	RF ripple signal input terminal.	Analog input.
43	FEI	I	Focus error signal input terminal.	Analog input.
44	SBAD	I	Sub-beam adder signal input terminal.	Analog input.
45	TSIN	I	Test input terminal. Normally, keep at "V_{REF}" level.	Analog input.
46	TEI	I	Tracking error signal input terminal. Take in at tracking servo on.	Analog input.
47	TEZI	I	Tracking error zero cross input terminal.	Analog input. (Z_{in} : 10kΩ)
48	FOO	O	Focus servo equalizer output terminal.	Analog output. ($2V_{REF}$~AV_{SS})
49	TRO	O	Tracking servo equalizer output terminal.	
50	V_{REF}	—	Analog reference voltage supply terminal.	—

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS
51	RFGC	O	RF amplitude adjustment control signal output terminal.	3-state PWM signal output. ($2V_{REF}$, V_{REF}, V_{SS}) (PWM carrier = 88.2kHz)
52	TEBC	O	Tracking balance control signal output terminal.	
53	TEBC	O	Feed equalizer output terminal.	
54	TEBC	O	Speed error signal or feed search equalizer output terminal.	
55	DMO	O	Disk equalizer output terminal. (PWM carrier = 88.2kHz for DSP, Synchronize to PXO)	3-state output. ($2V_{REF}$, V_{REF}, V_{SS})
56	$2V_{REF}$	—	Analog double reference voltage supply terminal.	—
57	SEL	O	APC circuit ON/OFF indication signal output terminal. At the laser on time, UHF = L at "Hi-Z" level and UHF = H at "H" level.	—
58	FLGA	O	Extemal flag output terminal for internal signal. Can select signal from TEZC, $\overline{FOON}$, $\overline{FOK}$ and RFZC by command.	—
59	FLGB	O	Extemal flag output terminal for internal signal. Can select signal from $\overline{DFCT}$, $\overline{FOON}$, $\overline{FMON}$ and RFZC by command.	—
60	FLGC	O	Extemal flag output terminal for internal signal. Can select signal from $\overline{TRON}$, $\overline{TRSR}$, $\overline{FOK}$ and $\overline{SRCH}$ by command.	—
61	FLGD	O	Extemal flag output terminal for internal signal. Can select signal from $\overline{TRON}$, $\overline{DMON}$, $\overline{HYS}$ and $\overline{SHC}$ by command.	—
62	V_{DD}	—	Digital power supply voltage terminal.	—
63	V_{SS}	—	Digital GND terminal.	—
64	IO0	I/O	General I/O terminal. Can change over input port or output port by command. At the input mode time can readout a state of terminal (H/L) by read command. At the output mode time can control a state of terminal (H/L/HiZ) by command.	—
65	IO1			
66	IO2			
67	IO3			
68	$\overline{DMOUT}$	I	This terminal controls IO0~IO3 terminal. At "L" level time, IO0, 1 out feed equalizer signal of 2-state PWM, IO2, 3 out disk equalizer signal of 2-state PWM.	With pull-up resistor.
69	$\overline{CKSE}$	I	Normally, keep at open.	With pull-up resistor.
70	$\overline{DACT}$	I	DAC test mode terminal. Normally, keep at open.	With pull-up resistor.
71	TESIN	I	Test input terminal. Normally, keep at "L" level.	Analog input.
72	TESIO1	I	Test input/output terminal. Normally, keep at "L" level.	Analog input.
73	V_{SS}	—	Digital GND terminal.	—

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS
74	PXI	I	Crystal oscillator connecting input terminal for DSP. Normally, keep at "L" level.	—
75	PXO	O	Crystal oscillator connecting output terminal for DSP.	
76	V_{DD}	—	Digital power supply voltage terminal.	—
77	XV_{SS}	—	Oscillator GND terminal for system clock.	—
78	XI	I	Crystal oscillator connecting input terminal for system clock.	—
79	XO	O	Crystal oscillator connecting output terminal for system clock.	—
80	XV_{DD}	—	Oscillator power supply voltage terminal for system clock.	—
81	DV_{SR}	—	Analog GND terminal for DA converter. (R-ch)	—
82	RO	O	R channel data forward output terminal.	—
83	DV_{DD}	—	Analog supply voltage terminal for DA converter.	—
84	DVR	—	Reference voltage terminal for DA converter.	—
85	LO	O	L channel data forward output terminal.	—
86	DV_{SL}	—	Analog GND terminal for DA converter. (L-ch)	—
87	TEST1	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
88	TEST2	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
89	TEST3	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
90	BUS0	I/O	Micon interface data input/output terminal.	Schmit input. With pull-up resistor.
91	BUS1	I/O		
92	BUS2	I/O		
93	BUS3	I/O		
94	V_{DD}	—	Digital power supply voltage terminal.	—
95	V_{SS}	—	Digital GND terminal.	—
96	BUCK	I	Micon interface clock input terminal.	Schmit input.
97	$\overline{CCE}$	I	Command and data sending/receiving chip enable signal input terminal. The bus line becomes active at "L" level.	Schmit input.
98	TEST4	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
99	$\overline{TSMOD}$	I	Local test mode selection terminal.	With pull-up resistor.
100	$\overline{RST}$	I	Reset signal input terminal. Reset at "L" level.	With pull-up resistor.

PACKAGE DIMENSIONS

QFP100-P-1420-0.65A Unit : mm



Weight : 1.6g (Typ.)

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